

Multilayer Ceramic Chip Capacitor

Part Number: 2211YA250332KSTSYX

2211 250Vac (Y2), 305Vac (X1), 50/60Hz / **Description:** 1000Vdc 3.3nF ±10% X7R (2R1) to AEC-

Q200

IEC/EN60384-14:2013+A1 Approval

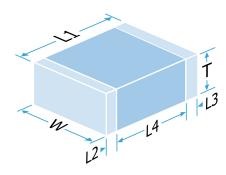
Specifications: UL60384-14, CAN/CSA E60384-14:14

TÜV R60156291 / ID11111239246 Certification:

UL/cUL E228790-20210208

IEC/EN 60384-14:2013+A1 Class Y2 / X1 Classification:

UL/cUL FOWX2, FOWX8



Component Marking and Certification Bodies:



Material Group I: CTI >= 600

Mechanical Specification

Size Code

Length (L1) in mm (") Width (W) in mm (")

Thickness (T) in mm (")

Minimum Termination Band (L2,L3) in mm (") Maximum Termination Band (L2,L3) in mm (")

Minimum Band Gap (L4) in mm (") (per IEC/EN 60384-14)

Termination Material

Solderability Packaging

2211

 $5.7 \pm 0.40 \ (0.225 \pm 0.016)$

 $2.79 \pm 0.30 (0.11 \pm 0.012)$

2.54 Max (0.1 Max)

0.50 (0.020)

0.80 (0.030)

4.0 (0.158)

FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder

(RoHS compliant) IEC-60068-2-58

7" Reel Horizontal Orientation, 750 per reel

General Electrical Specification

Rated Voltage

Humidity Grade

Maximum DC Working Voltage Nominal Capacitance Value Capacitance Tolerance

Tangent of Loss Angle (Tan δ)

Capacitance and Tan δ Test Conditions

Voltage Proof

(50mA max charging current for DC tests. 50% Max, RH)

Min Insulation Resistance (IR) Dielectric Classification Rated Temperature Range

Maximum Capacitance Change over Temperature Range

Climatic Category (IEC) Ageing Characteristic

Class Y2 (250Vac), Class X1 (305Vac), 50/60Hz, 5kV impulse

Grade IIIB (IEC/EN60384-14:2013 Annex I)

1000Vdc to Annex H / (2500Vdc outside scope of any specification)

3.3nF +10% ≤0.025

1.0Vrms @ 1kHz

100% test: 4000Vdc 1s min / 5s max

AQL test: 4000Vdc / 3000Vac 60s min / 5kV 1.2x50µs impulse

100.00GOhm @ 100Vdc X7R (2R1) to AEC-Q200

-55°C / +125°C

No DC Voltage +15% Rated DC Voltage -

55/125/56

<2% per decade (nominal capacitance is 1000 hour value)

This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data

for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

Knowles Precision Devices - Sales

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Data is correct to the best of our knowledge, errors and

omissions excepted.

Date: Sunday, February 23, 2025



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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

241 compliant

California Proposition 65

No exposure risk

Board Layout

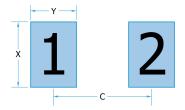
Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

Dimensions given are for guidance. It is ultimately the customers responsibility to confirm that the circuit layout is in accordance with their own product requirements.

IPC-7351 pad design

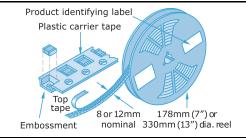
| | 2211 | |
|---|--------|--------|
| С | 6.00mm | 0.236" |
| Υ | 1.50mm | 0.059" |
| X | 3.10mm | 0.122" |



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

DLI

Temperature Preheat Time

Application notes with mounting and handling guidance are available on request.

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www.knowlescapacitors.com

Johanson MFG

Novacap

Syfer

Voltronics

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