SMARTsemi
Memory IC Datasheet

DDR4-2666 4Gb x16

June 22, 2022

Rev 1.0

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Part Number Decoder

K	T	D	M	4	G	4	B	6	2	6	B	G	x	E	A	T
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1-2	**IC Supplier** **KT:** SMARTsemi
3-4	**Product Family** **DM:** DRAM
5-6	**Density** **4G:** 4Gb
7	**Technology** **4:** DDR4
8	**Voltage** **B:** 1.2V
9	**Width** **6:** x16
10-11	**Speed** **26:** DDR4-2666
12-13	**Package** **BG:** Mono BGA
14	**Temperature** **C:** Commercial **I:** Industrial
15-16	**Internal Code** **EA**: For Internal Use
17	**Packaging** **T:** Tray

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Revision History

Date	Description
June 22, 2022	Initial release

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DDR4 SDRAM

128M x 16 Bit x 2 Banks DDR4 SDRAM

Features

- Power supply (JEDEC standard 1.2V)
  - VDD = 1.2V ± 5%
  - VPP = 2.375V to 2.75V
- 16 internal banks (x8)
  - 8 banks (4 banks x 2 bank groups) for x 16 product
- Interface: Pseudo Open Drain (POD)
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- CAS Latency (CL): 10,(11),12,(13),14,(15),16,(17),18,19,20,22,24
- CAS Write Latency (CWL): 9,10,11,12,14,16,18,20
- On-Die Termination (ODT): nom. values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  Average refresh period
  - 7.8μs at 0°C ≤ T_C ≤ +85°C or -40°C ≤ T_C ≤ +85°C
  - 3.9μs at +85°C < T_C ≤ +95°C
- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS_t and DQS_c) is transmitted/received with data for capturing data at the receiver
- Termination Data Strobe is supported (x8 only) (TDQS_t and TDQS_c)
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI)
  - Improve the power consumption and signal integrity
  - of the memory interface (x16 product only)
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- VREFDQ training
  - VREFDQ generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)
  - Each DRAM can be set a different mode register value individually and has individual adjustment.
- Fine granularity refresh
  - 2x, 4x mode for smaller tRFC
- Programmable Partial Array Self-Refresh (PASR)
- RESET_n pin for power-up sequence and reset function
- Operating case temperature range:
  - Commercial: T_C = 0°C to +95°C
  - Industrial: T_C = -40°C to +95°C

Ordering Information

Product ID	Max Freq.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Packing	Comments
KTDM4G4B626BGCEAT	1333MHz	1.2V	DDR4-2666 (19-19-19)	96 ball BGA	Commercial	Tray	Pb-free
KTDM4G4B626BGIEAT	1333MHz	1.2V	DDR4-2666 (19-19-19)	96 ball BGA	Industrial	Tray	Pb-free

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DDR4 SDRAM Addressing

Configuration		Device
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0 – BA1
Row Address		A0 – A14
Column Address		A0 – A9
Page size		2KB

Note:

1. Page size is per bank, calculated as follows:
   Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

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Pin Configuration – 96 balls BGA Package

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n/ DBIL_n	VSSQ	VSS
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD
K	VSS	CKE	ODT				CK_t	CK_c	VSS
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS
N	VSS	BA0	A4				A3	BA1	TEN
P	RESET_n	A6	A0				A1	A5	ALERT_n
R	VDD	A8	A2				A9	A7	VPP
T	VSS	A11	PAR				NC	A13	VDD

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Input / Output Functional Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered high. CS_n provides for external rank selection on systems with multiple memory ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	**Chip ID:** Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n, DBI_n, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5.
BG0 - BG1	Input	**Bank Group Inputs:** BG0 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0 - BA1	Input	**Bank Address Inputs:** BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	**Address Inputs:** Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16,CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	**Burst Chop:** A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

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Symbol	Type	Function
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input / Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1,A17-A0, and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and whenCS_n is low.
ALERT_n	Input/output	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** optional input on x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC	-	**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2 V +/- 0.06V
VSS	Supply	**Ground**
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference pin for ZQ calibration.**
Note: Input only pins (BG0, BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

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tREFI and tRFC parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e., tREFI1 = tREFI(base) (for Tcase≤ 85°C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in table of tREFI and tRFC parameters.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

tREFI and tRFC parameters

Refresh Mode	Parameter		4 Gb	Unit
	tREFI(base)		7.8	us
1X mode	tREFI1	0°C ≤ T_{CASE} ≤ 85°C	tREFI(base)	us
		-40°C ≤ T_{CASE} ≤ 85°C	tREFI(base)	us
		85°C < T_{CASE} ≤ 95°C	tREFI(base)/2	us
	tRFC1(min)		260	ns
2X mode	tREFI2	0°C ≤ T_{CASE} ≤ 85°C	tREFI(base)/2	us
		-40°C ≤ T_{CASE} ≤ 85°C	tREFI(base)/2	us
		85°C < T_{CASE} ≤ 95°C	tREFI(base)/4	us
	tRFC2(min)		160	ns
4X mode	tREFI4	0°C ≤ T_{CASE} ≤ 85°C	tREFI(base)/4	us
		-40°C ≤ T_{CASE} ≤ 85°C	tREFI(base)/4	us
		85°C < T_{CASE} ≤ 95°C	tREFI(base)/	us
	tRFC4(min)		110	ns

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Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Unit	Note
VDD	Voltage on VDD pin relative to VSS	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to VSS	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to VSS	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Recommended Operating Temperature Ranges

Parameter/Condition	Symbol	Min	Max-Normal	Max-Extended
Commercial Temperature	T_{OPER}	0°C	85°C	95°C
Industrial Temperature	T_{OPER}	-40°C	85°C	95°C

Note:

1. The operating temperature is the case surface temperature on the center-top side of the DDR4 device. For measurements conditions, refer to JESD51-2.
2. Max-Normal is the maximum limit when device is operating in the Normal Temperature Mode.
3. Max-Extended is the maximum limit when device is operating in the Extended Temperature Mode.

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AC & DC Logic input levels for single-ended signals

Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
$V_{IH.CA}$(DC65)	DC input logic high	V_{REFCA} + 0.065	V_{DD}	V	
$V_{IL.CA}$(DC65)	DC input logic low	V_{SS}	V_{REFCA} - 0.065	V	
$V_{IH.CA}$(AC90)	AC input logic high	V_{REF} + 0.09	Note 2	V	1
$V_{IL.CA}$(AC90)	AC input logic low	Note 2	V_{REF} - 0.09	V	1
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	V	2,3

Note:

1. See "Overshoot and Undershoot Specifications".
2. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA(DC)}$ by more than ± 1% V_{DD} (for reference : approx. ± 12mV).
3. For reference : approx. $V_{DD}/2$ ± 12mV.

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AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Illustration of $V_{REF(DC)}$ tolerance and V_{REF} AC-noise limits figure. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirement in Single-ended AC & DC input levels for Command and Address table. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% V_{DD}.

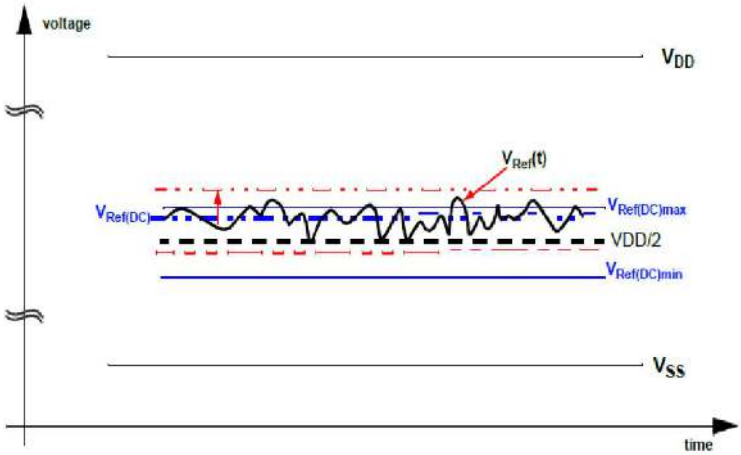

Illustration of $V_{REF(DC)}$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{REF}. "V_{REF}" shall be understood as $V_{REF(DC)}$, as defined in Illustration of $V_{REF(DC)}$ tolerance and V_{REF} AC-noise limits figure.
This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

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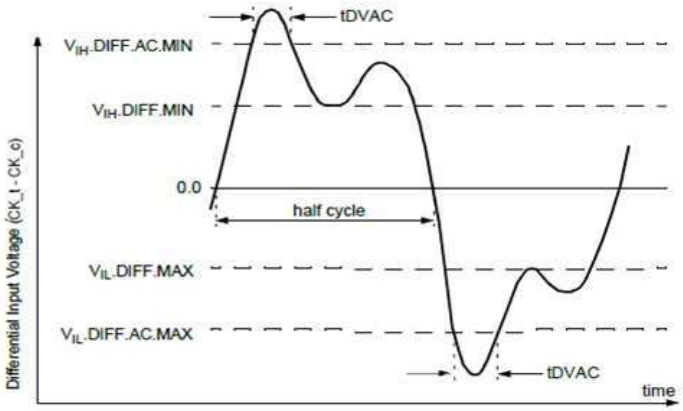
AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of differential ac-swing and "time above ac-level" tDVAC

Note:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

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Differential swing requirements for clock (CK_t - CK_c)

Differential AC and DC Input Levels

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
V_{IHdiff}	Differential input high	135	Note 3	mV	1
V_{ILdiff}	Differential input low	Note 3	-135	mV	1
V_{IHdiff}(AC)	Differential input high ac	2 x (V_{IH}(AC) - V_{REF})	Note 3	V	2
V_{ILdiff}(AC)	Differential input low ac	Note 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Note:

1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK_t - CK_c

Symbol	tDVAC [ps] @ |$V_{IH/Ldiff}$(AC)| = 200mV		tDVAC [ps] @ |$V_{IH/Ldiff}$(AC)| = TBDmV	
	Min.	Max.	Min.	Max.
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

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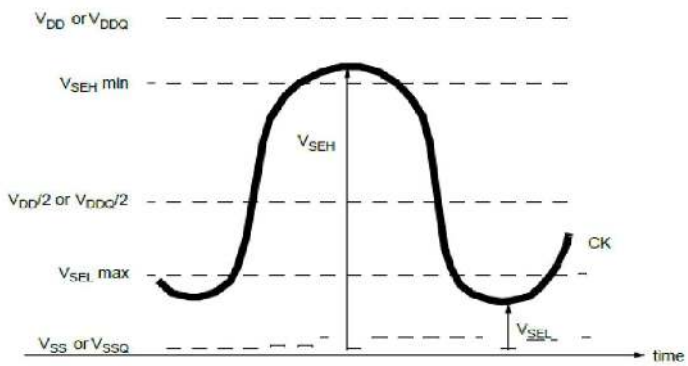
Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels ($V_{IH.CA}$(AC) / $V_{IL.CA}$(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than $V_{IH.CA}$(AC100)/ $V_{IL.CA}$(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c.



Single-ended requirement for differential signals

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2) + 0.095	Note3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	Note3	(VDD/2) - 0.095	V	1, 2

Note:

1. For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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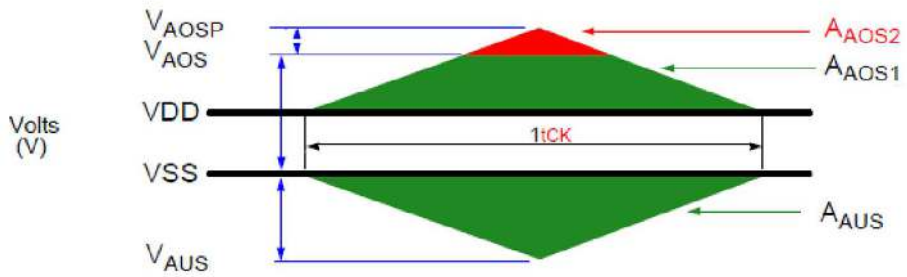
Address, Command and Control Overshoot and Undershoot specifications

AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	DDR4- 2666	Unit	Note
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06	V	
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	VDD + 0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30	V	
Maximum overshoot area per 1 tCK above V_{AOS}	A_{AOS2}	0.0055	V	
Maximum overshoot area per 1 tCK between VDD and V_{AOS}	A_{AOS1}	0.1699	V	
Maximum undershoot area per 1 tCK below VSS	A_{AUS}	0.1762	V	
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)				

Note: The value of V_{AOS} matches VDD absolute max as defined in Absolute Maximum DC Ratings table if VDD equals VDD max as defined in Recommended DC Operating Conditions table. If VDD is above the recommended operating conditions, V_{AOS} remains at VDD absolute max as defined in Absolute Maximum DC Ratings table.



Address, Command and Control Overshoot and Undershoot Definition

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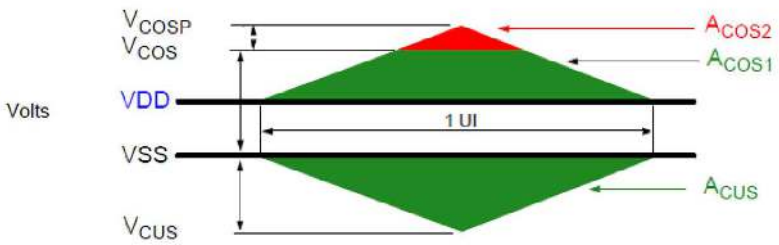
AC overshoot/undershoot specification for Clock

Parameter	Symbol	DDR4- 2666	Unit	Note
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06	V	
Upper boundary of overshoot area A_{DOS1}	V_{COS}	VDD + 0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30	V	
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0025	V-ns	
Maximum overshoot area per 1 UI between VDD and V_{DOS}	A_{COS1}	0.0750	V-ns	
Maximum undershoot area per 1 UI below VSS	A_{CUS}	0.0762	V-ns	
(CK_t, CK_c)				

Note: The value of V_{COS} matches VDD absolute max as defined in Absolute Maximum DC Ratings table if VDD equals VDD max as defined in Recommended DC Operating Conditions table. If VDD is above the recommended operating conditions, V_{COS} remains at VDD absolute max as defined in Absolute Maximum DC Ratings table.



Clock Overshoot and Undershoot Definition

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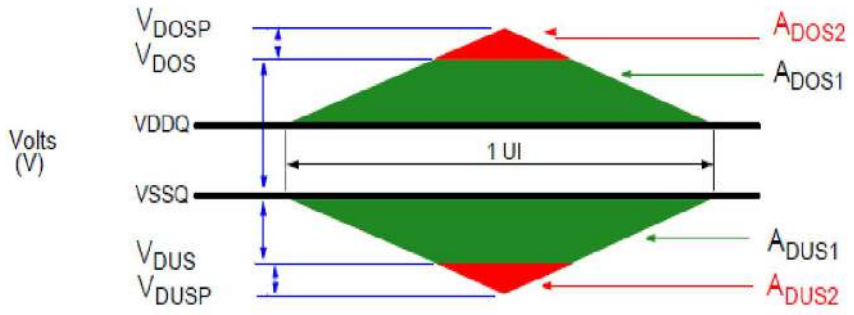
AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Symbol	DDR4- 2666	Unit	Note
Maximum peak amplitude above V_{DOS}	V_{DOSP}	0.16	V	
Upper boundary of overshoot area A_{DOS1}	V_{DOS}	V_{DDQ} + 0.24	V	1
Lower boundary of undershoot area A_{DUS1}	V_{DUS}	0.30	V	2
Maximum peak amplitude below V_{DUS}	V_{DUSP}	0.10	V	
Maximum overshoot area per 1 UI above V_{DOS}	A_{DOS2}	0.0100	V-ns	
Maximum overshoot area per 1 UI between V_{DDQ} and V_{DOS}	A_{DOS1}	0.0700	V-ns	
Maximum undershoot area per 1 UI between V_{SSQ} and V_{DUS1}	A_{DUS1}	0.0700	V-ns	
Maximum undershoot area per 1 UI below V_{DUS}	A_{DUS2}	0.0100	V-ns	
(DQ, DQS_t, DQS_c, DM_n, DBI_n)				

Note:

1. The value of V_{DOS} matches (V_{IN}, V_{OUT}) max as defined in Absolute Maximum DC Ratings table if V_{DDQ} equals V_{DDQ} max as defined in Recommended DC Operating Conditions table. If V_{DDQ} is above the recommended operating conditions, V_{DOS} remains at (V_{IN}, V_{OUT}) max as defined in Absolute Maximum DC Ratings table.
2. The value of V_{DUS} matches (V_{IN}, V_{OUT}) min as defined in Absolute Maximum DC Ratings table.



Data, Strobe and Mask Overshoot and Undershoot Definition

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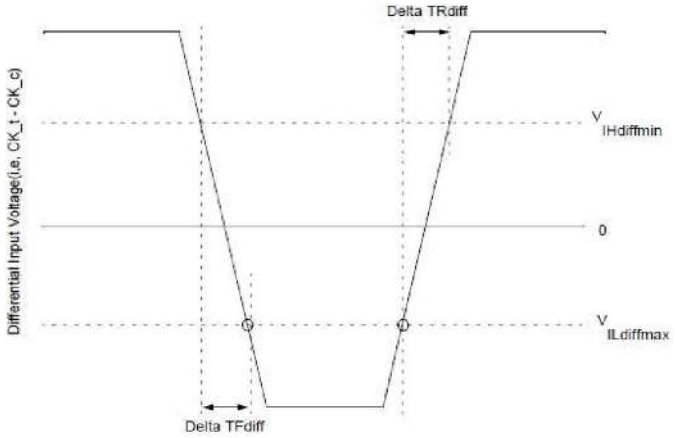
Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Differential Input Slew Rate Definition table and Differential Input Slew Rate Definition for CK_t, CK_c figure.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff

Note: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.



Differential Input Slew Rate Definition for CK_t, CK_c

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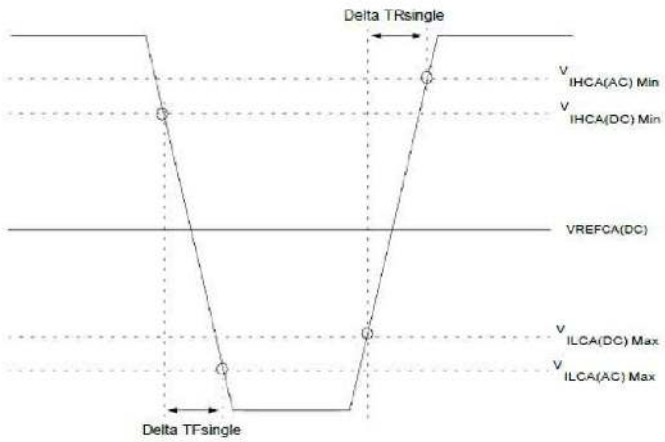
Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



Single-ended Input Slew Rate definition for CMD and ADD

Note:

1. Single-ended input slew rate for rising edge = { $V_{IHCA(AC)Min}$ - $V_{ILCA(DC)Max}$ } / Delta TR single.
2. Single-ended input slew rate for falling edge = { $V_{IHCA(DC)Min}$ - $V_{ILCA(AC)Max}$ } / Delta TF single.
3. Single-ended signal rising edge from $V_{ILCA(DC)Max}$ to $V_{IHCA(DC)Min}$ must be monotonic slope.
4. Single-ended signal falling edge from $V_{IHCA(DC)Min}$ to $V_{ILCA(DC)Max}$ must be monotonic slope.

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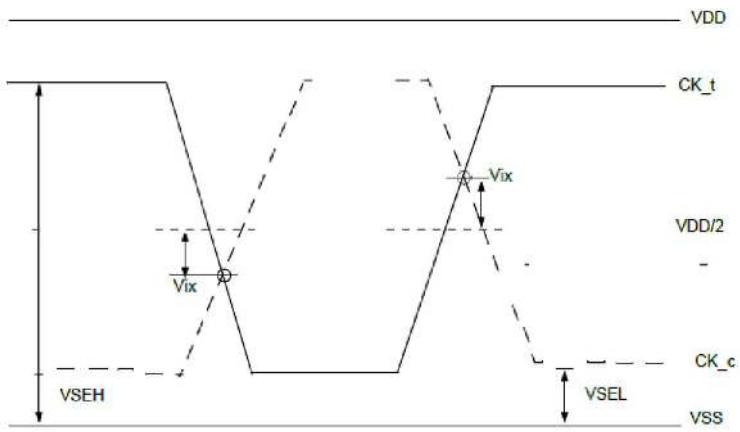
Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Cross point voltage for differential input signals (CK) table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.



Vix Definition (CK)

Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-2666			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145 mV	VDD/2 - 145 mV =< VSEL =< VDD/2 - 100 mV	VDD/2 + 100 mV =< VSEH =< VDD/2 + 145 mV	VDD/2 + 145 mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-110 mV	-(VDD/2 - VSEL) + 30 mV	(VSEH - VDD/2) - 30 mV	110 mV

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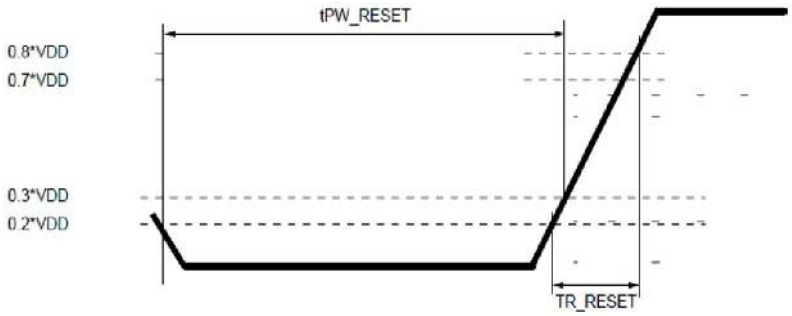
CMOS rail to rail Input Levels

CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

Note:

1. After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal (ringback) requirement during its level transition from Low to High.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.



RESET_n Input Slew Rate Definition

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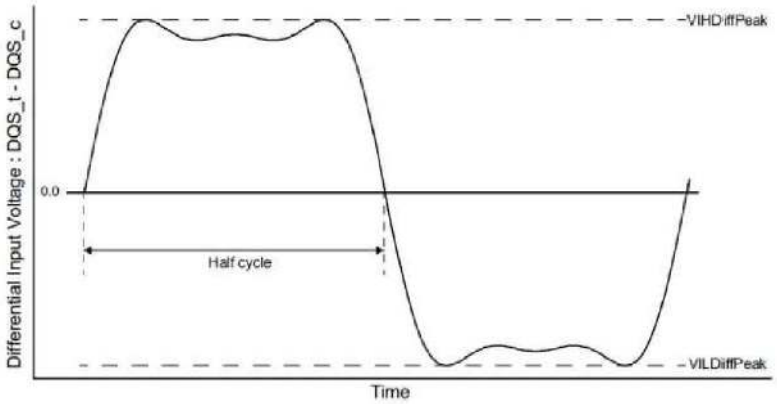
AC and DC Logic Input Levels for DQS Signals

Differential signal definition



Definition of differential DQS Signal AC-swing Level

Differential swing requirements for DQS (DQS_t - DQS_c)

Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-2666		Unit	Note
		Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	150	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-150	mV	1

Note:

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

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Peak voltage calculation method

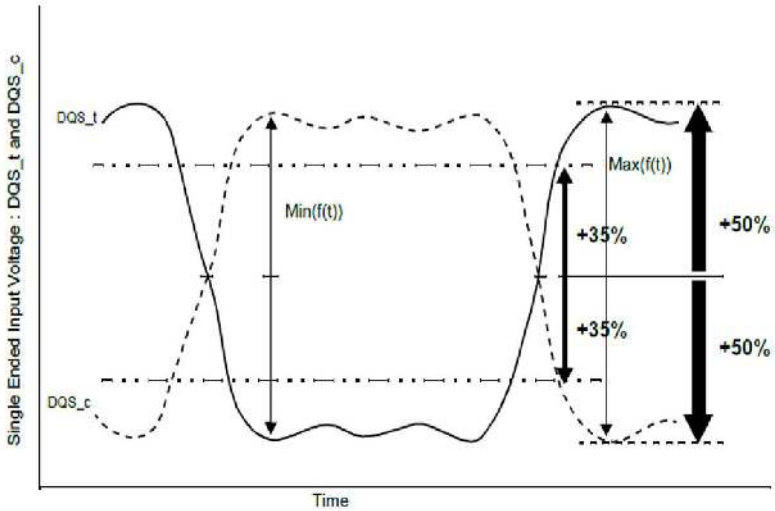
The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.



Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling

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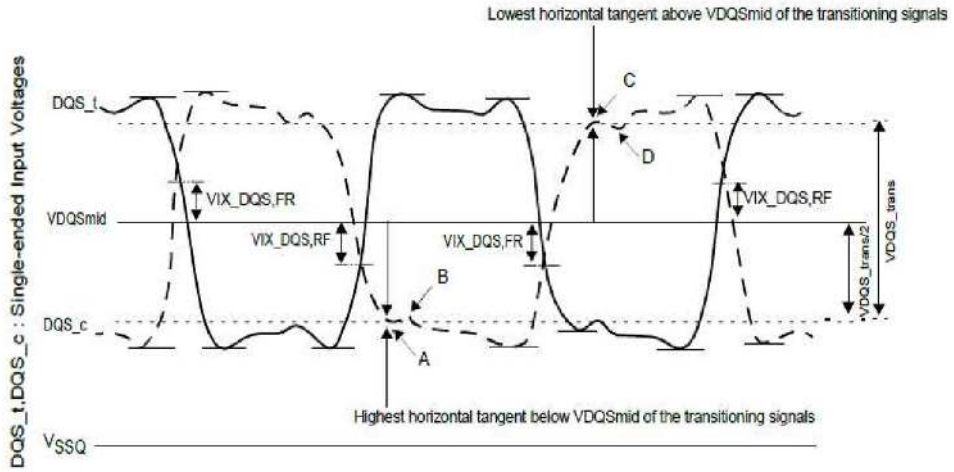
Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Cross point voltage for DQS differential input signals table. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling figure. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Vix Definition (DQS) figure) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Vix Definition (DQS) figure) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Vix Definition (DQS) figure) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Vix Definition (DQS) figure) is not a valid horizontal tangent.



Vix Definition (DQS)

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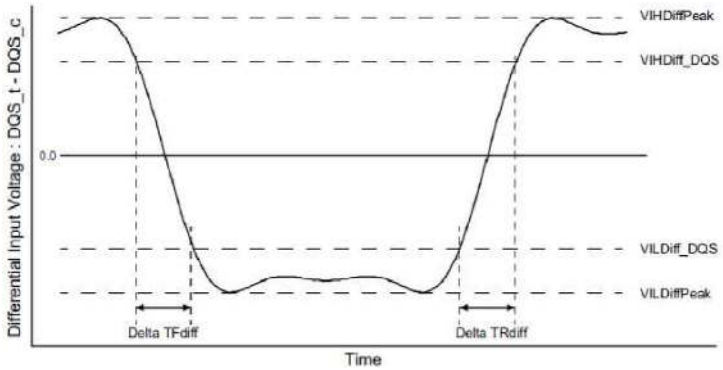
Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-2666		Unit	Note
		Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	%	1, 2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	Min (VIHdiff,50)	mV	3, 4, 5

Note:
1. Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Vix Definition (DQS) figure & Differential Input Slew Rate Definition for DQS_t, DQS_c figure.



Differential Input Slew Rate Definition for DQS_t, DQS_c

Note:
1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

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Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
VIHDiff_DQS	Differential Input High	130	-	mV	
VILDiff_DQS	Differential Input Low	-	-130	mV	

Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
SRIdiff	Differential Input Slew Rate	2.5	18	V/ns	

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AC and DC output Measurement levels

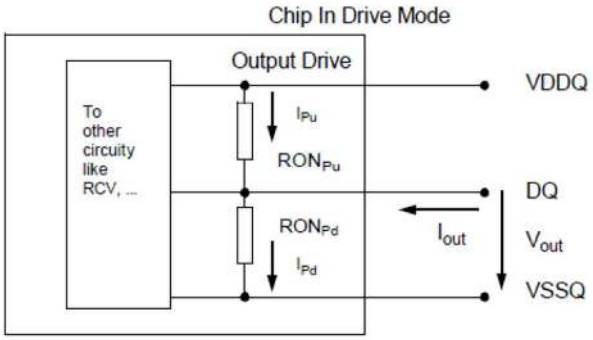
Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong (low Ron) and weak mode (high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|} \quad \text{under the condition that } RON_{Pd} \text{ is off}$$

$$RON_{Pd} = \frac{Vout}{|I\ out|} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$



Output driver

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Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	17	%	1,2,4,3
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5 * VDDQ and 1.1 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

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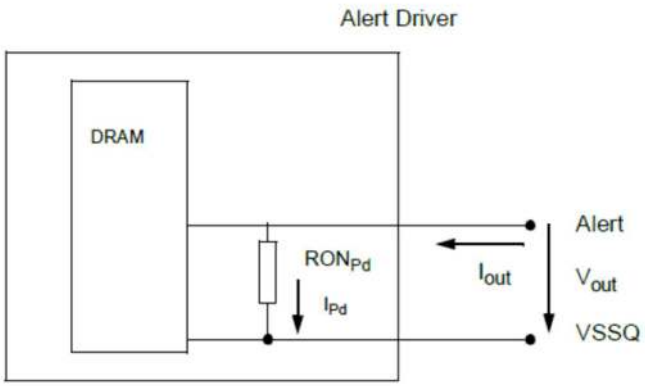
Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|Iout|} \quad \text{under the condition that RONPu is off}$$



Functional Representation of the Output Buffer

Output Driver Impedance

Resistor	Vout	Min	Max	Unit	Note
RON_{Pd}	V_{OLdc}= 0.1* VDDQ	0.3	1.2	34Ω	1
	V_{OMdc} = 0.8* VDDQ	0.4	1.2	34Ω	1
	V_{OHdc} = 1.1* VDDQ	0.4	1.4	34Ω	1

Note:

1. VDDQ voltage is at VDDQ DC. VDDQ DC definition is tbd.

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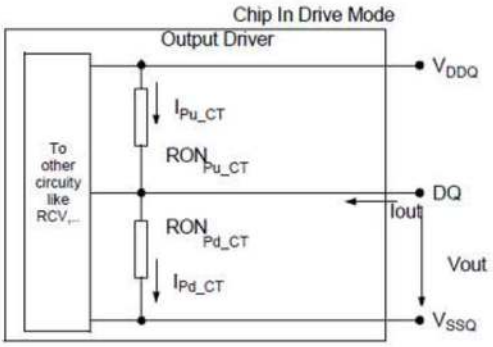
Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu_CT} = \frac{V_{DDQ} - V_{OUT}}{|\,Iout\,|}$$

$$RON_{Pd_CT} = \frac{V_{OUT}}{|\,Iout\,|}$$



Output Driver

RONPu_CT and RONPd_CT

RON_{NOM_CT}	Resistor	Vout	Max	Unit	Note
34Ω	RON_{Pd_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	2.5	34Ω	1
	RON_{Pu_CT}	$VOB_{dc} = 0.2 \times V_{DDQ}$	2.5	34Ω	1
		$VOL_{dc} = 0.5 \times V_{DDQ}$	2.2	34Ω	1
		$VOM_{dc} = 0.8 \times V_{DDQ}$	2.0	34Ω	1
		$VOH_{dc} = 1.1 \times V_{DDQ}$	1.9	34Ω	1

Note:

1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

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Single-ended AC & DC Output Levels

Single-ended AC & DC output levels

Symbol	Parameter	DDR4-2666	Unit	Note
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

Note:

1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

Differential AC & DC output levels

Symbol	Parameter	DDR4-2666	Unit	Note
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/ 7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

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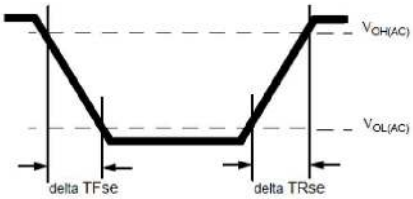
Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Single-ended output slew rate definition table and Single-ended Output Slew Rate Definition figure.

Single-ended output slew rate definition

Description	Measured		Defined by
	from	to	
Single ended output slew rate for rising edge	$V_{OL(}$AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate Definition

Single-ended output slew rate

Parameter	Symbol	DDR4-2666		Unit
		Min	Max	
Single ended output slew rate	SRQse	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

Note: 1 In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e., they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e., from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

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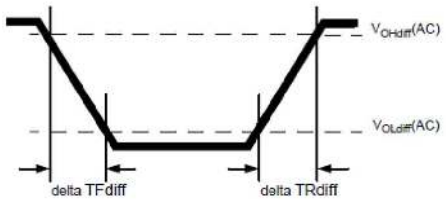
Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Differential output slew rate definition table and Differential Output Slew Rate Definition figure.

Differential output slew rate definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TFdiff

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential output slew rate

Parameter	Symbol	DDR4-2666		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query Output) diff: Differential Signals
For Ron = RZQ/7 setting

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Single-ended AC & DC Output Levels of Connectivity Test Mode

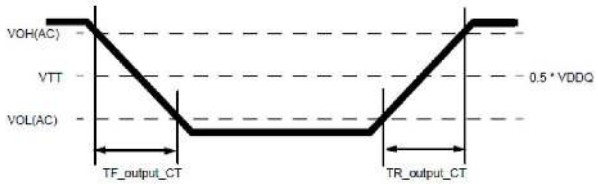
Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-2666	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

Note:

1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.



Output Slew Rate Definition of Connectivity Test Mode

Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-2666		Unit	Note
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

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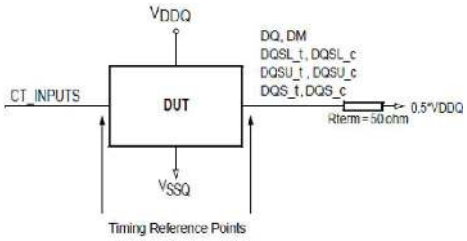
Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Connectivity Test Mode Timing Reference Load figure.



Connectivity Test Mode Timing Reference Load

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Speed Bin

DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	Note
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25 (13.75)[5,11]	18.00	ns	8
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	8
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,11]	-	ns	8
PRE command period			tRP	14.25 (13.75)[5,11]	-	ns	8
ACT to PRE command period			tRAS	32	9 x tREFI	ns	8
ACT to ACT or REF command period			tRC	46.25 (45.75)[5,11]	-	ns	8
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,6,7
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,6,7
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional)[5,11]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,6
				(Optional)[5,11]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,6
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,6
				(Optional)[5,11]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,6
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,6
				(Optional)[5,11]			
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,6
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	9
Supported CL Settings with read DBI				12,(13),14,(15),17,(18),19,(20),21,22,23		nCK	9

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Supported CWL Settings	9,10,11,12,14,16,18	nCK	

Speed Bin Table Notes

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

Note:

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e., 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. ‘Reserved’ settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Any combination of the ‘optional’ CL’s is supported. The associated ‘optional’ tAA, tRCD, tRP, and tRC values must be adjusted based upon the CL combination supported. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
8. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
9. CL number in parentheses, it means that these numbers are optional.
10. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min), tRCD(min), tRP(min), and tRC(min).
11. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

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IDD and IDDQ Specification Parameters and Test conditions

IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement figure. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

- For IDD, IPP and IDDQ measurements, the following definitions apply:
- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table .
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] table through IDD7 Measurement-Loop Pattern[1] table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM disabled in MR5

- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH} ; apply invert of BG/BA changes when directed above.

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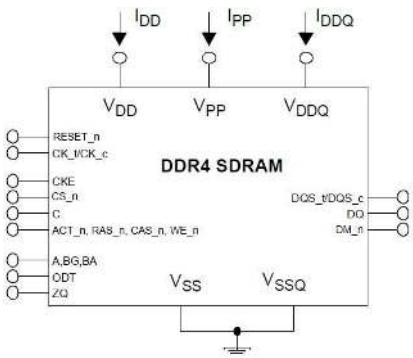
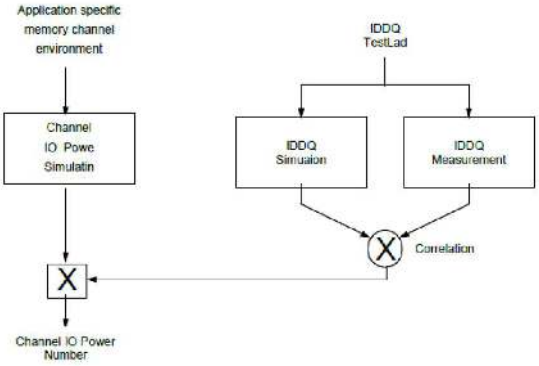


Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements



Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ

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Measurement Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol	DDR4-2666 (19-19-19)	Unit
tCK	0.75	ns
CL	19	nCK
CWL	18	nCK
nRCD	19	nCK
nRC	62	nCK
nRAS	43	nCK
nRP	19	nCK
nFAW (x16)	40	nCK
nRRDS (x16)	8	nCK
nRRDL (x16)	9	nCK
tCCD_S	4	nCK
tCCD_L	7	nCK
tWTR_S	4	nCK
tWTR_L	10	nCK
nRFC 4Gb	347	nCK

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Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to **IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] t**able; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] table.
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table
IDD2NA	**Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2NT Measurement-Loop Pattern[1] table; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to IDD2NT Measurement-Loop Pattern[1] table; **Pattern Details:** see IDD2NT Measurement-Loop Pattern[1] table
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]

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Symbol	Description
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see **Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd)** table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see **Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd)** table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD4R, IDDR4RA and IDD4RB Measurement-Loop Pattern[1] table; **Data IO:** seamless read data burst with different data between one burst and the next one according to IDD4R, IDDR4RA and IDD4RB Measurement-Loop Pattern[1] table; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD4R, IDDR4RA and IDD4RB Measurement-Loop Pattern[1] table); **Output Buffer and R_{TT}:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD4R, IDDR4RA and IDD4RB Measurement-Loop Pattern[1] table
IDD4RA	**Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table; **Data IO:** seamless write data burst with different data between one burst and the next one according to IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table

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Symbol	Description
IDD4WA	**Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled3, Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP** **Current Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD5B Measurement-Loop Pattern[1] table; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see IDD5B Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD5B Measurement-Loop Pattern[1] table
IPP5B	**Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2**
IDD5F4	**Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T_{CASE}* for devices:** -0 to 85°C or -40 to 85°C; **Low Power Auto Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) ***T_{CASE}* for devices:** 0 to 95°C **or** -40 to 95°C; **Low Power Auto Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** ***T_{CASE}* for CT devices:** 0 to 45°C or -40 to 45°C; **Low Power Auto Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**

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Symbol	Description
IDD6A	**Auto Self-Refresh Current** ***T_{CASE}* for CT devices:** 0 to 95°C or -40 to 95°C; **Low Power Auto Self Refresh (LP ASR)** : Auto[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD7 Measurement-Loop Pattern1 table; **Data IO:** read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern1 table; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD7 Measurement-Loop Pattern[1] table; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see DD7 Measurement-Loop Pattern[1] table
IPP7	**Operating Bank Interleave Read IPP** **Current Same condition with IDD7**
IDD8	**Maximum Power Down Current** **TBD**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

Note:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s
   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
   DLL disabled : set MR1 [A0 = 0]
   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s
   Read DBI enabled : set MR5 [A12 = 1]
   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10]: Extended Temperature range
   11]: Auto Self Refresh
5. IDD2NG should be measured after sync pulse (NOP) input.

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IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat nRC 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. DQ signals are VDDQ.

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IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD-AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			…	repeat pattern nRC + 1...4 until nRAS - 1, truncate if necessary																
			1*nRCD + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
			…	repeat pattern nRC + 1...4 until nRAS - 1, truncate if necessary																
			1*nRCD + nRAS	**PRE**	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	-
			…	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 2** instead																

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CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

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IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. DQ signals are VDDQ.

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IDD2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. DQ signals are VDDQ.

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IDD4R, IDDR4RA and IDD4RB Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2-3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
			5	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6-7	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Read Command.

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IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
			1	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2-3	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
			5	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6-7	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Write Command.

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IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF, D8=CRC
			1-2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3-4	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00, D8=CRC
			6-7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8-9	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	45-49	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Write Command.

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IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			5-8	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 1** instead																
			9-12	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 2** instead																
			13-16	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 3** instead																
			17-20	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 1** instead																
			21-24	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 2** instead																
			25-28	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 3** instead																
			29-32	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 0** instead																
			33-36	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 0** instead																
			37-40	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 1** instead																
			41-44	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 2** instead																
			45-48	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 3** instead																
			49-52	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 1** instead																
			53-56	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 2** instead																
			57-60	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 3** instead																
			61-64	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		2	65 … nRFC - 1	repeat Sub-Loop 0, truncate if necessary																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. DQ signals are VDDQ.

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IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	1	0	0	0	0		0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			…	repeat pattern 2 … 3 until nRRD – 1, if nRRD > 4, truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1		0	1	1	0	0	1	0	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
			…	repeat pattern 2 … 3 until 2*nRRD – 1, if nRRD > 4, truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 … 3 until nFAW – 1, if nFAW > 4*nRRD, truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																

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CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 … 3 until nRC– 1, if nRC > 4*nFAW, truncate if necessary																

Note:

1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

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IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

IDD and IDDQ Specification

Speed Grade Bin		Unit	Note
Symbol	DDR4-2666 (19-19-19		
IDD0	116	mA	
IDD0A	116	mA	
IDD1	158	mA	
IDD1A	160	mA	
IDD2N	93	mA	
IDD2NA	93	mA	
IDD2NT	135	mA	
IDD2NL	85	mA	
IDD2NG	90	mA	
IDD2ND	70	mA	
IDD2N_par	106	mA	
IDD2P	65	mA	
IDD2Q	98	mA	
IDD3N	115	mA	
IDD3NA	115	mA	
IDD3P	95	mA	
IDD4R	265	mA	
IDD4RA	280	mA	
IDD4RB	235	mA	
IDD4W	305	mA	
IDD4WA	319	mA	
IDD4WB	295	mA	
IDD4WC	280	mA	
IDD4W_par	335	mA	
IDD5B	200	mA	
IDD5F2	220	mA	
IDD5F4	180	mA	
IDD7	345	mA	
IDD8	35	mA	

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IPP Specification

Speed Grade Bin		Unit	Note
Symbol	DDR4-2666 (19-19-19)		
IPP0	9	mA	
IPP1	9	mA	
IPP2N	7	mA	
IPP2P	7	mA	
IPP3N	7	mA	
IPP3P	7	mA	
IPP4R	7	mA	
IPP4W	7	mA	
IPP5B	27	mA	
IPP5F2	29	mA	
IPP5F4	20	mA	
IPP7	40	mA	
IPP8	3	mA	

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IDD6 Specification

Symbol	Temperature Range	DDR4-2666 (19-19-19)	Unit	Note
IDD6N	0 to 85°C	40	mA	3,4
	-40 to 85°C	40		
IDD6E	0 to 95°C	45	mA	4,5,6
	-40 to 95°C	45		
IDD6R	0 to 45°C	35	mA	4,6,8
	-40 to 45°C	35		
IDD6A	0 to 85°C	40	mA	4,6,7
	-40 to 85°C	40		

IPP6 Specification

Symbol	Temperature Range	DDR4-2666 (19-19-19)	Unit	Note
IPP6N	0 to 85°C	6	mA	2,3
	-40 to 85°C			
IPP6E	0 to 95°C	8	mA	3,4,5
	-40 to 95°C			
IPP6R	0 to 45°C	4	mA	3,5,7
	-40 to 45°C			
IPP6A	0 to 85°C	6	mA	3,5,6
	-40 to 85°C			

Note:

1. Some IDD currents are higher for x16 organization due to larger page-size architecture.
2. Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6=0 and A7=0.
4. Supplier data sheets include a max value for IDD6.
5. Applicable for MR2 settings A6=0 and A7=1. IDD6E is only specified for devices which support the Extended Temperature Range feature.
6. Refer to the supplier data sheet for the value specification method (e.g., max, typical) for IDD6E and IDD6A.
7. Applicable for MR2 settings A6=1 and A7=0. IDD6A is only specified for devices which support the Auto Self Refresh feature.
8. Applicable for MR2 settings MR2 [A7:A6 = 01]: Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test

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Input/Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
C_{IO}	Input/output capacitance	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	pF	1,3,4
C_I	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	pF	1,3,7,8
$C_{DI_ADD_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	pF	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_t, DQS_c. Although the DM pins have different functions, the loading matches DQ and DQS.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value CK_t-CK_c.
5. Absolute value of CIO(DQS_t)-CIO(DQS_c).
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE.
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CK_t)+CI(CK_c)).
9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CK_t)+CI(CK_c)).
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_t)+CIO(DQS_c))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

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DRAM package electrical specifications

Symbol	Parameter	DDR4-2666		Unit	Note
		Min.	Max.		
Z_{IO}	Input/output Zpkg	45	85	Ω	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{IO}	Input/Output Lpkg	-	3.4	nH	1, 2
C_{IO}	Input/Output Cpkg	-	0.82	pF	1, 3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{IO\ DQS}$	DQS Lpkg	-	3.5	nH	1, 2
$C_{IO\ DQS}$	DQS Cpkg	-	0.82	pF	1, 3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	50	90	Ω	1
$T_{dI\ CTRL}$	Input CTRL pins Pkg Delay	14	42	ps	1
$L_{I\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1, 2
$C_{I\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1, 3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	Ω	1
$Td_{IADD\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{I\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1, 2
$C_{I\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1, 3
Z_{CK}	CK_t & CK_c Zpkg	50	90	Ω	1
Td_{CK}	CK_t & CK_c Pkg Delay	14	42	ps	1
$L_{I\ CLK}$	Input CK Lpkg	-	3.4	nH	1, 2
$C_{I\ CLK}$	Input CK Cpkg	-	0.7	pF	1, 3
DZ_{DCK}	Delta Zpkg CK_t & CK_c	-	10	Ω	-
D_{TdCK}	Delta Delay CK_t & CK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	-	100	Ω	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	-

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Note:

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

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Electrical Characteristics & AC Timing

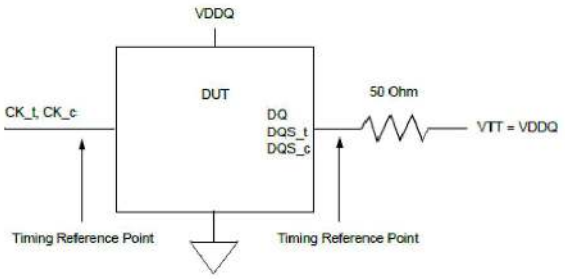
Reference Load for AC Timing and Output Slew Rate

Reference Load for AC Timing and Output Slew Rate figure represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,
The minimum DC Low level of Output signal = { 34 /(34 + 50) } *VDDQ = 0.4* VDDQ
The nominal reference level of an Output signal can be approximated by the following:
The center of maximum DC High and minimum DC Low = { (1 + 0.4) / 2 } * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

tREFI by device density

Parameter	Symbol		4Gb	Unit
Average periodic refresh interval	tREFI	0°C ≦ T_{CASE} ≦ 85°C	7.8	us
		-40°C ≦ T_{CASE} ≦ 85°C		
		85°C < T_{CASE} ≦ 95°C	3.9	us

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Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o production test.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\mathrm{tCK(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCK(avg)j}\right)/N \qquad N = 200$$

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$\mathrm{tCH(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCHj}\right)/\{N \times \mathrm{tCK(avg)}\} \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\mathrm{tCL(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCLj}\right)/\{N \times \mathrm{tCK(avg)}\} \qquad N = 200$$

Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

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Timing Parameters by Speed Grade

Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns	
Average Clock Period	tCK(avg)	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)m + tJIT(per)ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)	24
Clock Period Jitter - total	JIT(per)_tot	-38	38	ps	25
Clock Period Jitter - deterministic	JIT(per)_dj	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	60	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	ps	

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
Cumulative error across 13 cycles	tERR(13per)	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	((1 + 0.68ln(n)) * tJIT(per)_total min)	((1 + 0.68ln(n)) * tJIT(per)_total max)	ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	55	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	80	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	ps	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	max(4nCK, 6.4ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	max(28nCK, 30ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	ns	1,2,e,34

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-		34
WRITE recovery time	tWR	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR + max(5nCK, 3.75ns)	-	ns	1,28
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S + max(5nCK, 3.75ns)	-	ns	2, 29,34
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L + max(5nCK, 3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK	52
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	UI	46,47
CS_n to Command Address Latency					
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD + tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD + tCAL	-	nCK	
DRAM Data Timing					
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	tCK(avg)/2	13,18,39,49

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
DQ output hold time per group, per access from DQS_t, DQS_c	tQH	0.74	-	tCK(avg)/2	13,17,18,39, 49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	UI	17,18,39,49
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-310	170	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	170	ps	39
Data Strobe Timing					
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note 44	tCK	39,40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	1.8	Note 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note 45	tCK	39
DQS_t, DQS_c differential output high time	tQSH	0.4	-	tCK	21,39
DQS_t, DQS_c differential output low time	tQSL	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	tCK	
DQS_t, DQS_c low-impedance time Referenced from RL-1)	tLZ(DQS)	-310	170	ps	39
DQS_t, DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK	42

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	-0.50	0.50	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DLL On mode	tDQSCK(DLL On)	-170	170	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI(DLL On)	-	270	ps	37,38,39
MPSM Timing					
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-		
Calibration Timing					
Power-up and RESET calibration time	tZQinit	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min) + 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min) + 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min) + 10ns	-	nCK	

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min) + 1nCK + PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK, 10ns) + PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	nCK	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL + 2 + (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK	7

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	nCK	
PDA Timing					
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		nCK	
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.28	0.72	tCK(avg)	
Write Leveling Timing					
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	ns	
Write leveling output error	tWLOE	0	2	ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL + 6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	71	nCK	
Parity Latency	PL	5	-	nCK	
CRC Error Reporting					
CRC error to ALERT_n latency	tCRC_ALERT	3	13	ns	

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Speed		DDR4-2666		Unit	Note
Parameter	Symbol	Min	Max		
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	nCK	
Geardown Timing					
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	tXS	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD + 4nCK	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	tMOD	-		27
Geardown setup time	tGEAR_setup	2	-	nCK	
Geardown hold time	tGEAR_hold	2	-	nCK	
tREFI					
tRFC1 (min)	4Gb	260	-	ns	34
tRFC2 (min)	4Gb	160	-	ns	34
tRFC4 (min)	4Gb	110	-	ns	34

Note:

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on T_{OPER}.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power- down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

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22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RONNOM = 34 ohms.
40. 1tCK toggle mode with setting MR4:A11 to 0.
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.
42. 1tCK mode with setting MR4:A12 to 0.
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See --- “Clock to Data Strobe Relationship” figure. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in Section ----- “Read Preamble”.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship” figure.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.
51. Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. tRFC2 and tRFC4 needs to be set corresponding to each setting’s value (default / optional-1 / optional-2) accordingly. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
52. DALmin is required to refer to the rounding algorithm specified.

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Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

nCK = ceiling [(parameter_in_ns / application_tCK_in_ns) - 0.025]

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

  nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]

- Either algorithm yields identical results.In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect (SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm,

  nCK = ceiling (parameter_in_ns ÷ application_tCK_in_ns).

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Example 1, using REAL math to convert tAAmin from ns to nCK:

// This algorithm subtracts 2.5% correction factor and rounds up to next integer value real MTB, FTB, TaaMin, Correction, ClockPeriod, TempNck; int TaaInNck;

```
TaaMin = 15.0;                          // Calculate tAAmin in ns (FTB is negative offset)
Correction = 0.025;                     // 2.5%, per rounding algorithm
ClockPeriod = ApplicationTck;           // Frequency (clock period) is application dependent
TempNck = TaaMin / ClockPeriod          // Initial calculation of nCK
TempNck = TempNck - Correction;         // Subtract correction factor from nCK
TaaInNck = (int)ceiling(TempNck);       // Ceiling to next higher integer value//
```

DDR4-2666W Device Operating at Standard Application Data Rates (Full & Downbinned) Timing Parameter: t_{AA}min = 15.0ns						
Application Speed Grade	Device t_{AA}	Application t_{CK}	Device t_{AA} ÷ Application t_{CK}	2.5 Correction	t_{AA} / t_{CK} — Correction	Ceiling Result
	ns	ns	ratio (real)	(real)	ratio (real)	nCK (integer)
2666	15.000	0.750	20.0	0.025	19.975	20
2400	15.000	0.833	18.0072	0.025	17.9822	18
2133	15.000	0.937	16.00854	0.025	15.9835	16
1866	15.000	1.071	14.0056	0.025	13.9806	14
1600	15.000	1.250	12.0	0.025	11.975	12
Note that roundup values for bins 2400, 2133, and 1866 would have lost one clock of performance without the application of the rounding algorithm. For example, a DDR4-2666W device running at DDR4-2400 data rates would have been required to set tAA to 19 clocks without correction, but with correction tAA may be safely programmed to 18 clocks.						

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Example 2, using INT math to convert t_{AA}min from ns to nCK:

// This algorithm uses adds 97.4% of a clock and truncates down to the next lower integer value int MTB, FTB, TaaMin, ClockPeriod, TempNck, TaaInNck;

```
TaaMin = 15000;                                  // Calculate tAAmin in ns (FTB is negative offset)
ClockPeriod = ApplicationTckInPs;                // Clock period is application specific
TempNck = (TaaMin * 1000)/ ApplicationTckInPs;   // Preliminary nCK calculation, scaled by 1000
TempNck = TempNck + 974;                         // Apply inverse of 2.5% correction factor
TaaInNck = (int)(TempNck / 1000);                //Truncate to next lower integer
```

DDR4-2666W Device Operating at Standard Application Data Rates (Full & Downbinned) Timing Parameter: t_{AA}min = 15.0ns (15000ps)					
Application Speed Grade	Device t_{AA}	Application t_{CK}	(Device t_{AA}*1000) ÷ Application t_{CK}	Add Inverse Correction	Truncate Corrected nCK / 1000
	ps	ps	Scaled nCK	Scaled nCK	nCK (integer)
2666	15000	750	20000	220974	20
2400	15000	833	18007	18981	18
2133	15000	937	16008	16982	16
1866	15000	1071	14005	14979	14
1600	15000	1250	12000	12974	12

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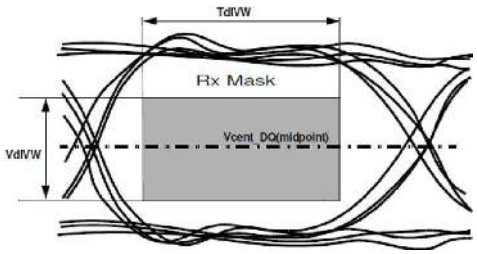
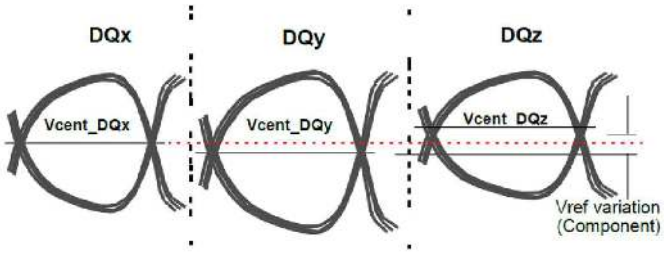
The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.



DQ Receiver(Rx) compliance mask



Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.
Vcent_DQ(midpoint) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Vcent_DQ Variation to Vcent_DQ(midpoint) figure. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

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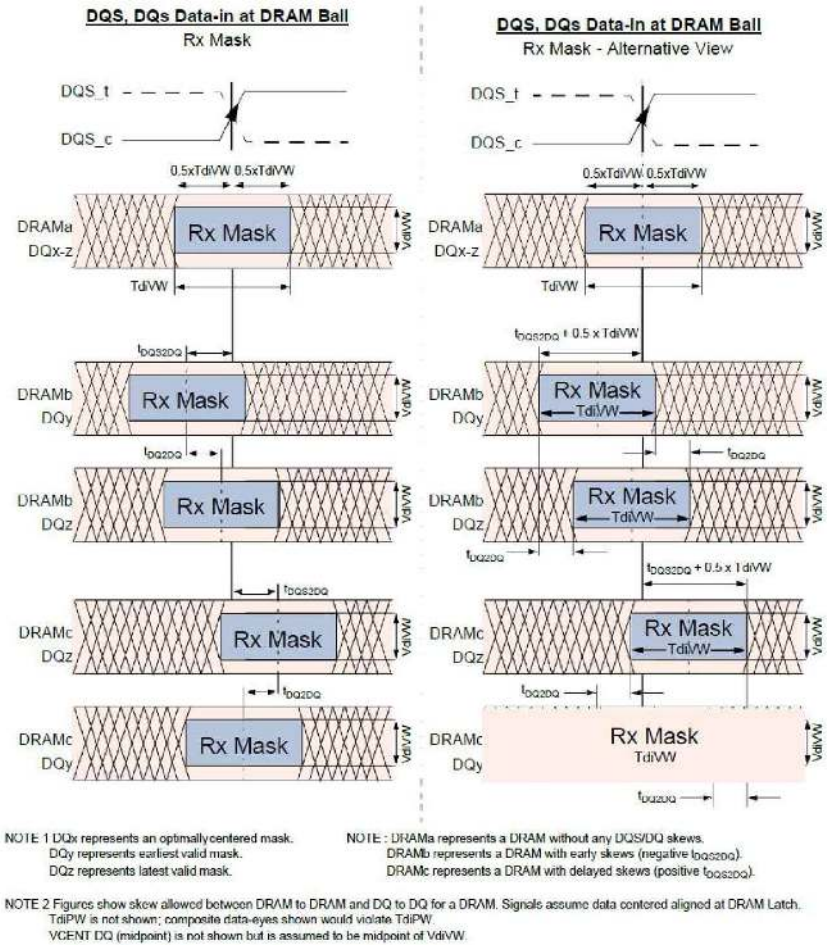

DQS to DQ and DQ to DQ Timings at DRAM Balls

All of the timing terms in DQS to DQ and DQ to DQ Timings at DRAM Balls figure are measured at the VdIVW voltage levels centered around Vcent_DQ(midpoint) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

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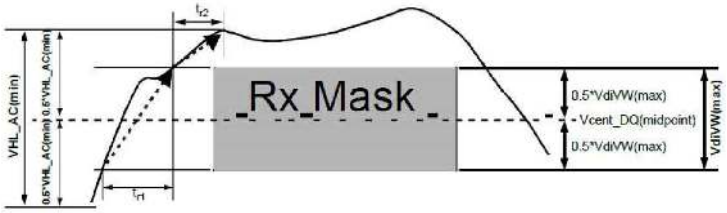
The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Slew Rate Conditions For Rising Transition figure below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1
srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

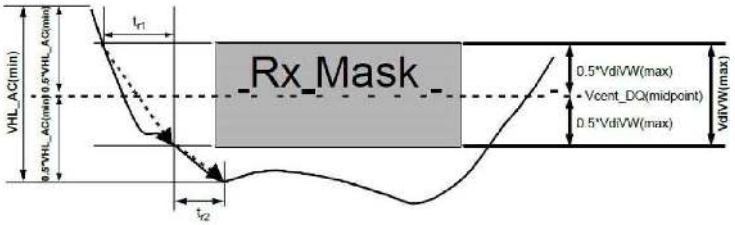


Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Slew Rate Conditions For Falling Transition figure below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1 srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)



Slew Rate Conditions For Falling Transition

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DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	DDR4-2666		Unit	Note
		min	max		
VdIVW	Rx Mask voltage - pk-pk	-	120	mV	1,2,10
TdIVW	Rx timing window	-	0.22	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	150	-	mV	6,10
TdIPW	DQ input pulse width	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.19	0.19	UI*	6,10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.105	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >= 0.937ns	1.0	9	V/ns	8,10
	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	V/ns	9,10

Note:

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
2. Defined over the DQ internal Vref range 1.
3. Overshoot and Undershoot Specifications see AC overshoot/undershoot specification for Data, Strobe and Mask figure.
4. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e., a valid TdiPW.
5. DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9. Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
10. All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

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Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/ VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/ VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

Command, Address, Control Setup and Hold Values

DDR4	2666	Unit	Reference
tIS(base, AC100)	-	ps	VIH/L(ac)
tIH(base, DC75)	-	ps	VIH/L(dc)
tIS(base, AC90)	55	ps	VIH/L(ac)
tIH(base, DC65)	80	ps	VIH/L(dc)
tIS/tIH @ VREF	145	ps	VIH/L(dc)

Note:

1. Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
2. Values listed are referenced only; applicable limits are defined elsewhere.

Command, Address, Control Input Voltage Values

DDR4	2666	Unit	Reference
VIH.CA(AC)min	90	mV	VIH/L(ac)
VIH.CA(DC)min	65	mV	VIH/L(dc)
VIL.CA(DC)max	-65	mV	VIH/L(ac)
VIL.CA(AC)max	-90	mV	VIH/L(dc)

Note:

1. Command, Address, Control input levels relative to VREFCA.
2. Values listed are referenced only; applicable limits are defined elsewhere.

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Derating values DDR4-2666 tIS/tIH - ac/dc based

△tIS, △tIH derating in [ps] AC/DC based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Note: 1. VIH/L(ac) = +/-tbd mV, VIH/L(dc) = +/- tbd mV; relative to VREFCA

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DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Function Matrix (By ORG. V:Supported, Blank: Not supported)

Functions	X16	Note
Write Leveling	V	
Temperature controlled Refresh	V	
Low Power Auto Self Refresh	V	
Fine Granularity Refresh	V	
Multi Purpose Register	V	
Data Mask	V	
Data Bus Inversion	V	
TDQS		
ZQ calibration —	V	
DQ Vref Training	V	
Per DRAM Addressability	V	
Mode Register Readout	V	
CAL	V	
WRITE CRC	V	
CA Parity	V	
Control Gear Down Mode	V	
Programmable Preamble	V	
Maximum Power Down Mode		
Boundary Scan Mode	V	
Additive Latency		
3DS		

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Function Matrix (By Speed. V:Supported, Blank: Not supported)

Functions	DLL Off mode	DLL On mode	Note
	equal or slower than 250Mbps	2666Mbps	
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Low Power Auto Self Refresh	V	V	
Fine Granularity Refresh	V	V	
Multi Purpose Register	V	V	
Data Mask	V	V	
Data Bus Inversion	V	V	
TDQS		V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability		V	
Mode Register Readout	V	V	
CAL		V	
WRITE CRC		V	
CA Parity		V	
Control Gear Down Mode		V	
Programmable Preamble (= 2tCK)		V	
Maximum Power Down Mode		V	
Boundary Scan Mode	V	V	
3DS	V	V	

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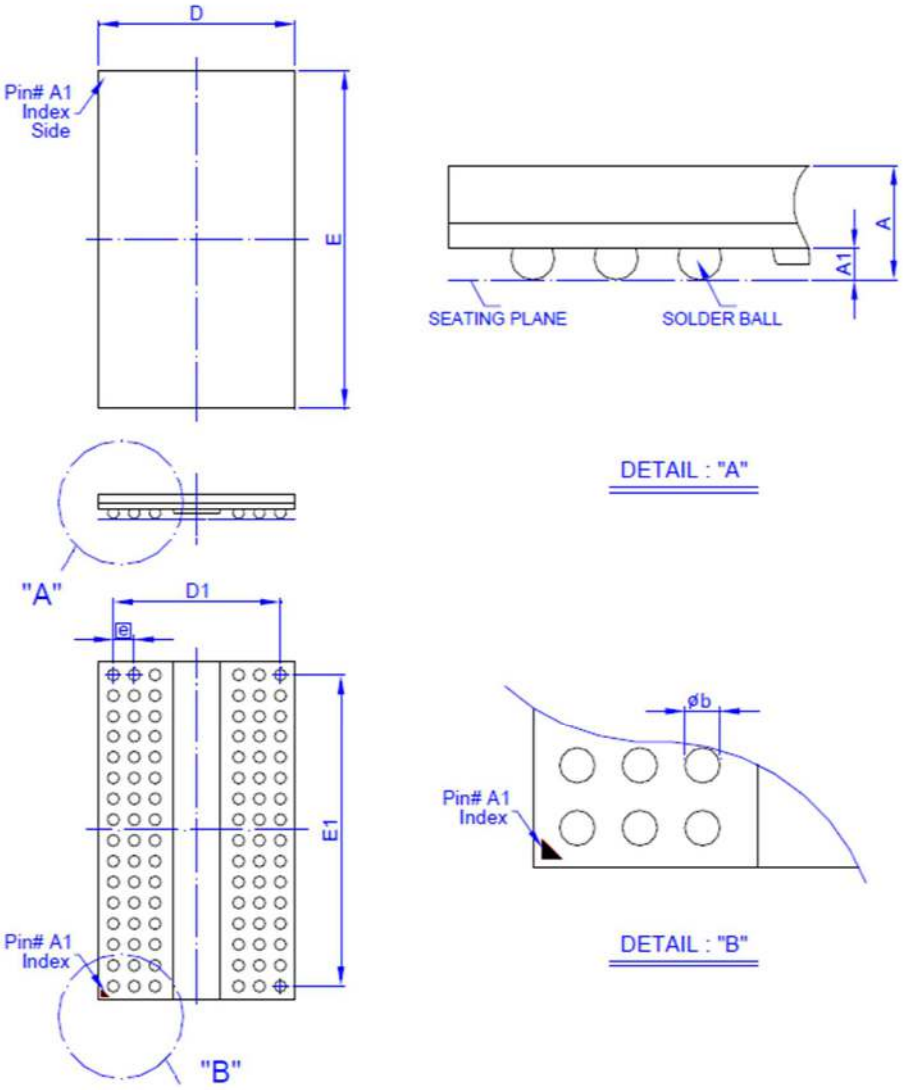
PACKAGING DIMENSIONS

96-BALL (7.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	---	---	1.00	---	---	0.039
A_1	0.30	0.35	0.40	0.012	0.014	0.016
Φ_b	0.40	0.45	0.50	0.016	0.018	0.020
D	7.40	7.50	7.60	0.291	0.295	0.299
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	6.40 BSC			0.252 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter

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