RA8T1 Group
Renesas Microcontrollers

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High-performance 480 MHz Arm® Cortex®-M85 core with Helium™, up to 2 MB code flash memory with Dual-bank, background and SWAP operation, 12 KB Data flash memory, and 1 MB SRAM with Parity/ECC. High-integration with Ethernet MAC controller, USB 2.0 Full-Speed, CANFD, SDHI, I3C and advanced analog. Integrated Renesas Secure IP with cryptography accelerators, key management support, tamper detection and power analysis resistance in concert with Arm® TrustZone for integrated secure element functionality.

Features

Arm® Cortex®-M85 core with Helium™

- Armv8.1-M architecture profile
- Armv8-M Security Extension
- Maximum operating frequency: 480 MHz
- Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by CPUCLK or MOCO divided by 8
- CoreSight™ ETM-M85

Memory

- Up to 2 MB code flash memory
- 12 KB data flash memory (100,000 program/erase (P/E) cycles)
- 1 MB SRAM including 128 KB of TCM

Connectivity

- Serial Communications Interface (SCI) × 6 , up to 60 Mbps
  - Asynchronous interfaces
  - 8 bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding (SCI0)
  - Simple LIN (SCI0, SCI1)
- I^2C bus interface (IIC) × 2
- I^3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2, up to 60 Mbps
- USB 2.0 Full-Speed Module (USBFS)
- CAN with Flexible Data-rate (CANFD) × 2
- Ethernet MAC/DMA Controller (ETHERC/EDMAC)
- SD/MMC Host Interface (SDHI) × 2

Analog

- 12-bit A/D Converter (ADC12) × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 2
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) × 8
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2
- Ultra-Low-Power Timer (ULPT) × 2

Security and Encryption

- Renesas Secure IP (RSIP-E51A)
  - Symmetric cryptography: AES
  - Asymmetric cryptography: RSA, ECC
  - Message digest computation: HASH
  - 128 bit unique ID
- Arm® TrustZone®
  - Up to two or four regions for the code flash, depending on the bank mode
  - Up to two regions for the data flash
  - Up to two regions for the SRAM
  - Individual Secure or Non-secure security attribution for each peripheral
- Privileged control
- Device lifecyle management
- Secure boot
- Pin function
  - Secure pin multiplexing

System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Programable Voltage Detection (PVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 48 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20/32/48 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL1/PLL2
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

Operating Voltage

- VCC: 1.68 to 3.6 V
- VCC2: 1.65 to 3.6 V

Operating Junction Temperature and Packages

- Tj = -40°C to +125°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
  - 224-pin BGA (13 mm × 13 mm, 0.8 mm pitch)

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1. Overview

The MCU integrates multiple series of software-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm® Cortex®-M85 core with Helium™running up to 480 MHz with the following features:

- Up to 2 MB code flash memory
- 1 MB SRAM (128 KB of TCM RAM, 896 KB of user SRAM)
- Ethernet MAC Controller (ETHERC), USBFS, SD/MMC Host Interface
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm® Cortex®-M85 core	• Maximum operating frequency: up to 480 MHz • Arm® Cortex®-M85 core – Revision: (r0p2-00rel0) – ARMv8.1-M architecture profile – Armv8-M Security Extension – Floating Point Unit (FPU) compliant with the ANSI/IEEE Std 754-2008 Scalar half, single, and double-precision floating-point operation – M-profile Vector Extension (MVE) Integer, half-precision, and single-precision floating-point MVE (MVE-F) – Helium™ technology is M-profile Vector Extension (MVE) • Arm® Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure instance (SysTick_S) and Non-secure instance (SysTick_NS) – Driven by CPUCLK or MOCO divided by 8 • CoreSight™ ETM-M85

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2 MB of code flash memory.
Data flash memory	12 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). SRAM0 is ECC. SRAM1 is Parity check.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode 1.
ROM	On-chip immutable ROM contains First Stage Bootloader (FSBL)

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Three operating modes: • Single-chip mode • JTAG boot mode • SCI/USB boot mode
Resets	This MCU provides 12 types of reset.

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Table 1.3 System (2 of 2)

Feature	Functional description
Programable Voltage Detection (PVD)	The Programable Voltage Detection (PVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The PVD module consists of three separate voltage level detectors (PVD0, PVD1, PVD2). PVD0, PVD1, and PVD2 measure the voltage level input to the VCC pin. PVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL1/PLL2 • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, power gating control, selecting operating power control modes in normal operation, and transitioning to low power modes and processor low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR_S and PRCR_NS).
Memory Protection Unit (MPU)	All bus masters have Memory Protection Units (MPUs).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External buses	• CS area (ECBI): Connected to the external devices (external memory interface) • SDRAM area (ECBI): Connected to the SDRAM (external memory interface)

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 8 channels and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

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Table 1.7 Timers (2 of 2)

Feature	Functional description
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Ultra-Low-Power Timer (ULPT)	The Ultra-Low-Power Timer (ULPT) is a 32-bit timer which can be used for outputting pulses or counting external events. This 32-bit timer consists of reload registers and a down-counter. The reload registers and the down-counter are allocated to the same address and can be accessed through the ULPTCNT register.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) has a 14-bit down-counter, which resets the MCU by a reset output when the down-counter underflows. Alternatively, generation of an interrupt request when the counter underflows can be selected. This enables detection of a program runaway taking the refresh interval into account. The IWDT has two start modes: auto start mode, in which counting automatically starts after release from the reset state, and register start mode, in which counting is started by refreshing (writing to a specific register).

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Simple LIN interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. All channels have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
I^2C Bus interface (IIC)	The I^2C Bus interface (IIC) has 2 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
I3C Bus Interface (I3C)	The I3C Bus Interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers per channel and 16 receive buffers per channel.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.

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Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
SD/MMC Host Interface (SDHI)	The Secure Digital (SD) Card and Multi Media Card (MMC) Host Interface provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes.
Ethernet Controller (ETHERC)	One-channel Ethernet Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D Converter is provided. Up to 25 analog input channels are selectable. Temperature sensor output, and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) can be used to compare an analog input voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the analog input voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output or internal reference voltage) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bits data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

Table 1.11 Security (1 of 2)

Feature	Functional description
Security function	• ARMv8-M TrustZone security • Privileged control • Device lifecycle management • Authentication Level (AL) • Key injection • Secure pin multiplexing • Secure boot • Secure factory programming

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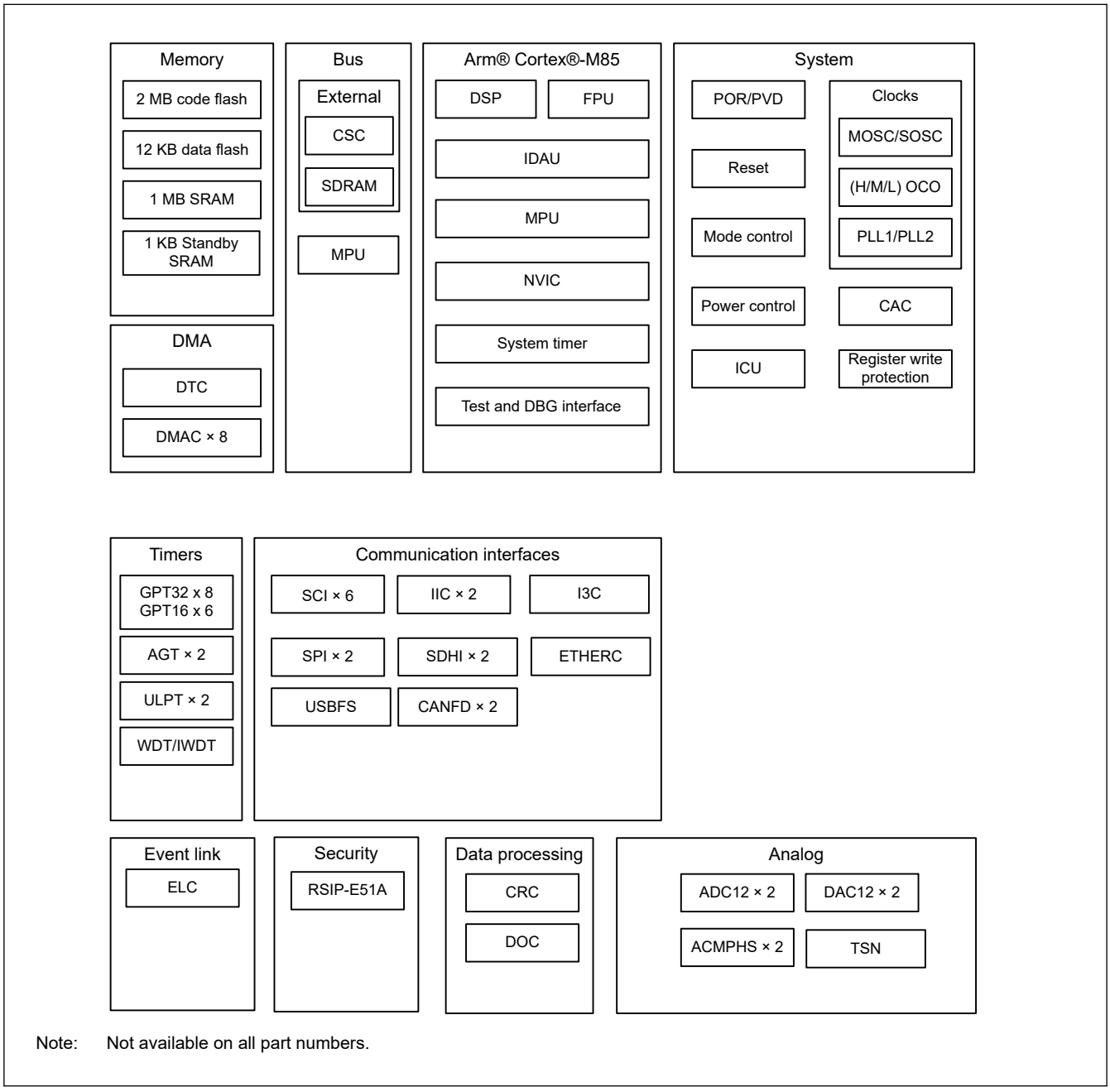
Table 1.11 Security (2 of 2)

Feature	Functional description
Renesas Secure IP (RSIP-E51A)	• Symmetric cryptography: AES • Asymmetric cryptography: RSA, ECC • Message digest computation: HASH • 128-bit true random number generation circuit • 256-bit Hardware Unique Key (HUK) • 128-bit unique ID • OEM boot loader version • SPA/DPA Protections

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1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.



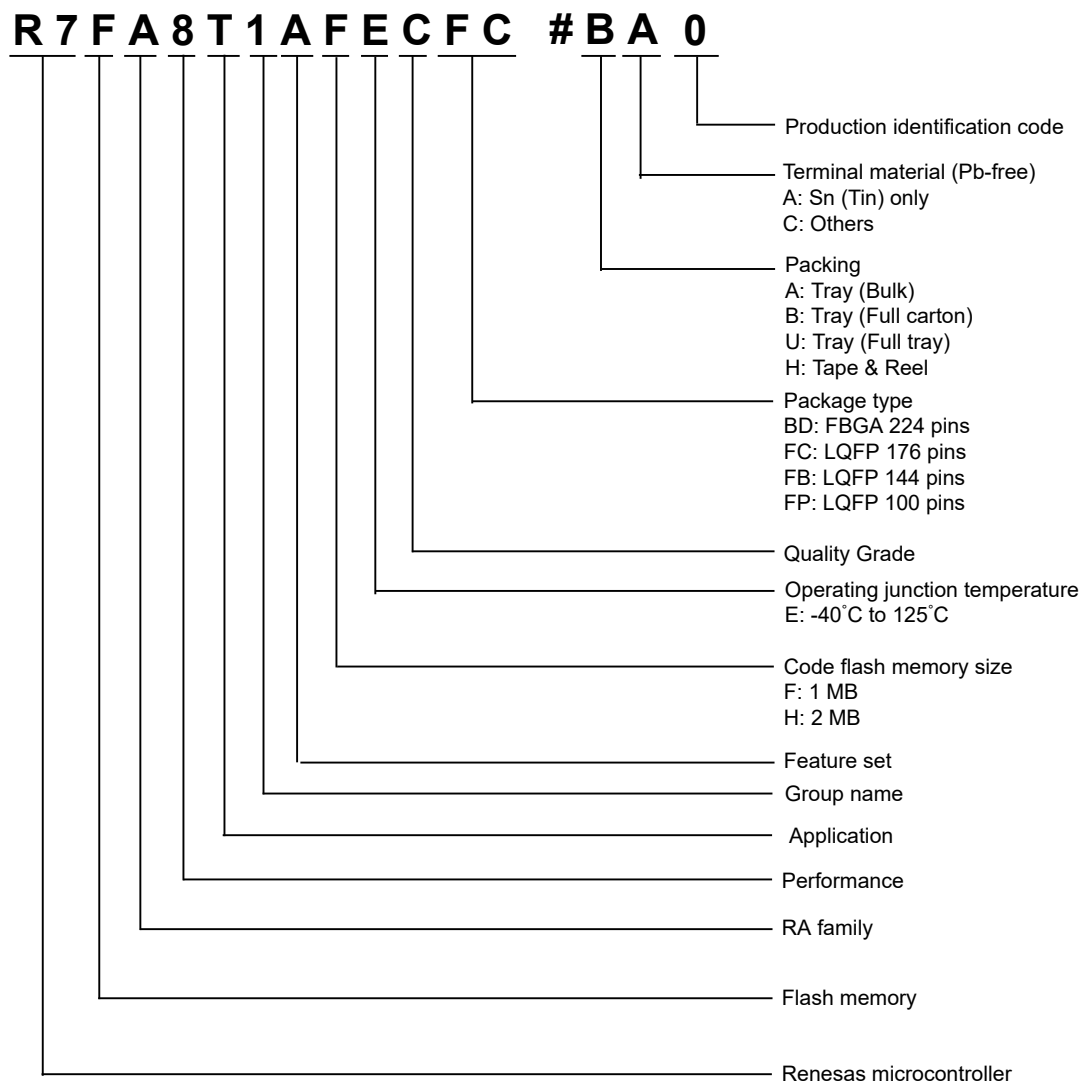
Note: Not available on all part numbers.

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

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Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating junction temperature
R7FA8T1AHECBD	PLBG0224GD-A	2 MB	12 KB	1MB	−40 to +125°C
R7FA8T1AHECFC	PLQP0176KJ-A				
R7FA8T1AHECFB	PLQP0144KA-B				
R7FA8T1AHECFP	PLQP0100KP-A				
R7FA8T1AFECBD	PLBG0224GD-A	1 MB			
R7FA8T1AFECFC	PLQP0176KJ-A				
R7FA8T1AFECFB	PLQP0144KA-B				
R7FA8T1AFECFP	PLQP0100KP-A				

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1.4 Function Comparison

Table 1.13 Function Comparison (1 of 2)

Parts number		R7FA8T1AxECBD	R7FA8T1AxECFC	R7FA8T1AxECFB	R7FA8T1AxECFP
Pin count		224	176	144	100
Package		BGA	LQFP		
I/O Port		174	128	106	70
Code flash memory		2 MB, 1 MB			
Data flash memory		12 KB			
TCM		128 KB			
I/D Caches		32 KB			
SRAM		896 KB			
	Parity	512 KB			
	ECC	384 KB			
Standby SRAM		1 KB			
DMA	DTC	Yes			
	DMAC	8			
BUS	External bus	32-bit bus	16-bit bus	No	
	SDRAM	32-bit bus	16-bit bus	No	
System	CPU clock	480 MHz (max.)	400 MHz (max.)		360 MHz (max.)
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, PLL1P			
	CAC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	6			
	IIC	2			
	I3C	Yes			
	SPI	2			
	CANFD	2			
	USBFS	Yes			
	SDHI/MMC	2			
	ETHERC	Yes			
Timers	GPT32[*1]	8			
	GPT16[*1]	6			
	AGT[*1]	2			
	ULPT[*1]	2			
Analog	ADC12	Unit 0: 12 Unit 1: 13 Shared channel pin: 4[*2]	Unit 0: 12 Unit 1: 12 Shared channel pin: 4[*2]	Unit 0: 11 Unit 1: 8 Shared channel pin: 3[*2]	Unit 0: 6 Unit 1: 5 Shared channel pin: 0[*2]
	DAC12	2			
	ACMPHS	2			
	TSN	Yes			
Data processing	CRC	Yes			
	DOC	Yes			
Event control	ELC	Yes			

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Table 1.13 Function Comparison (2 of 2)

Parts number	R7FA8T1AxECBD	R7FA8T1AxECFC	R7FA8T1AxECFB	R7FA8T1AxECFP
Security	RSIP-E51A, Secure Debug, Secure Boot, Immutable Storage, TrustZone, Secure Factory Programming, and Lifecycle management			

Note: The product name differs depending on the memory size. See section 1.3. Part Numbering.
Note 1. Available pins depend on the Pin count. For details, see section 1.7. Pin Lists.
Note 2. Some input channels of the ADC unit share the same port pins.

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1.5 Pin Functions

Table 1.14 Pin functions (1 of 6)

Function	Signal	I/O	Description
Power supply	VCC, VCC2	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCC_DCDC	Input	Switching regulator power supply pin.
	VLO	I/O	Switching regulator pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS, VSS_DCDC	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EXCIN	Input	External sub-clock input
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	Input	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode

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Table 1.14 Pin functions (2 of 6)

Function	Signal	I/O	Description
External bus interface	EBCLK	Output	Outputs the external bus clock for external devices
	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active-low.
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low.
	WRn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode, active-low.
	BCn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode, active-low.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low.
	CSn	Output	Select signals for CS areas, active-low
	A00 to A23	Output	Address bus
	D00 to D31	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus
SDRAM interface	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active low
	RAS	Output	SDRAM low address strobe signal, active low
	CAS	Output	SDRAM column address strobe signal, active low
	WE	Output	SDRAM write enable signal, active low
	DQMn	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00, DQ15 to DQ08, DQ23 to DQ16 or DQ31 to DQ24
	A00 to A16	Output	Address bus
	DQ00 to DQ31	I/O	Data bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)

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Table 1.14 Pin functions (3 of 6)

Function	Signal	I/O	Description
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
ULPT	ULPTEEn	Input	External count control input
	ULPTEVIn	Input	External event input
	ULPTOn	Output	Pulse output
	ULPTOAn	Output	Output compare match A output
	ULPTOBn	Output	Output compare match B output
	ULPTEEn-DS	Input	External count control input that can also be used in Deep Software Standby mode1
	ULPTEVIn-DS	Input	External event input that can also be used in Deep Software Standby mode1
	ULPTOn-DS	Output	Pulse output that can also be used in Deep Software Standby mode1
	ULPTOAn-DS	Output	Output compare match A output that can also be used in Deep Software Standby mode1
	ULPTOBn-DS	Output	Output compare match B output that can also be used in Deep Software Standby mode1
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	DEn	Output	Driver enable signal for RS-485
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
I3C	I3C_SCL0	I/O	Input/output pins for the clock
	I3C_SDA0	I/O	Input/output pins for data

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Table 1.14 Pin functions (4 of 6)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_OVRCURA-DS, USB_OVRCURB-DS	Input	Overcurrent pins for USBFS that can also be used in Deep Software Standby mode1. Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
SDHI/MMC	SDnCLK	Output	SD clock output pins
	SDnCMD	I/O	Command output pin and response input signal pins
	SDnDATA0 to SDnDATA7	I/O	SD and MMC data bus pins
	SDnCD	Input	SD card detection pins
	SDnWP	Input	SD write-protect signals

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Table 1.14 Pin functions (5 of 6)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXDn	Output	2-bit transmit data in RMII mode
	RMII0_RXDn	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXDn	Output	4 bits of MII transmit data
	ET0_ERXDn	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER	Output	Receive error pin. Functions as signal to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO
	ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to AVCC0 when not using the ADC12 (unit 1) and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to AVSS0 when not using the ADC12 (unit 1) and D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to AVCC0 when not using the ADC12 (unit 0).
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12 (unit 0).

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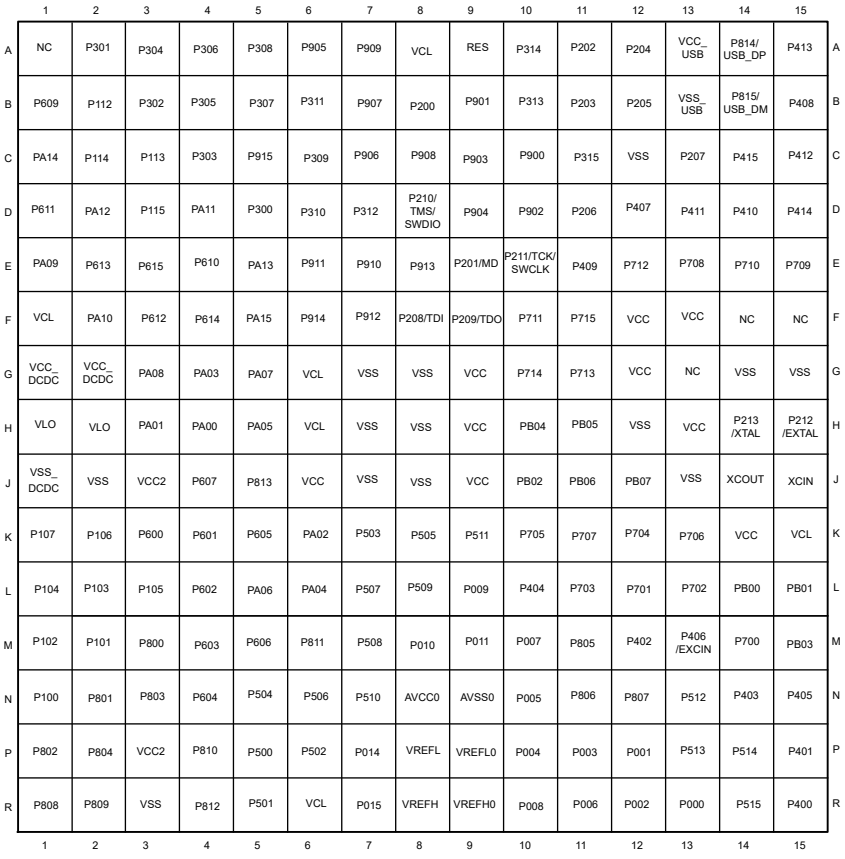
Table 1.14 Pin functions (6 of 6)

Function	Signal	I/O	Description
ADC12	ANmn	Input	Input pins for the analog signals to be processed by the A/D converter. (m: ADC unit number, n: pin number)
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

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1.6 Pin Assignments

The following figures show the pin assignments from the top view.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	P301	P304	P306	P308	P905	P909	VCL	RES	P314	P202	P204	VCC_USB	P814/USB_DP	P413	A
B	P609	P112	P302	P305	P307	P311	P907	P200	P901	P313	P203	P205	VSS_USB	P815/USB_DM	P408	B
C	PA14	P114	P113	P303	P915	P309	P906	P908	P903	P900	P315	VSS	P207	P415	P412	C
D	P611	PA12	P115	PA11	P300	P310	P312	P210/TMS/SWDIO	P904	P902	P206	P407	P411	P410	P414	D
E	PA09	P613	P615	P610	PA13	P911	P910	P913	P201/MD	P211/TCK/SWCLK	P409	P712	P708	P710	P709	E
F	VCL	PA10	P612	P614	PA15	P914	P912	P208/TDI	P209/TDO	P711	P715	VCC	VCC	NC	NC	F
G	VCC_DCDC	VCC_DCDC	PA08	PA03	PA07	VCL	VSS	VSS	VCC	P714	P713	VCC	NC	VSS	VSS	G
H	VLO	VLO	PA01	PA00	PA05	VCL	VSS	VSS	VCC	PB04	PB05	VSS	VCC	P213/XTAL	P212/EXTAL	H
J	VSS_DCDC	VSS	VCC2	P607	P813	VCC	VSS	VSS	VCC	PB02	PB06	PB07	VSS	XCOUT	XCIN	J
K	P107	P106	P600	P601	P605	PA02	P503	P505	P511	P705	P707	P704	P706	VCC	VCL	K
L	P104	P103	P105	P602	PA06	PA04	P507	P509	P009	P404	P703	P701	P702	PB00	PB01	L
M	P102	P101	P800	P603	P606	P811	P508	P010	P011	P007	P805	P402	P406/EXCIN	P700	PB03	M
N	P100	P801	P803	P604	P504	P506	P510	AVCC0	AVSS0	P005	P806	P807	P512	P403	P405	N
P	P802	P804	VCC2	P810	P500	P502	P014	VREFL	VREFL0	P004	P003	P001	P513	P514	P401	P
R	P808	P809	VSS	P812	P501	VCL	P015	VREFH	VREFH0	P008	P006	P002	P000	P515	P400	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.3 Pin assignment for BGA 224-pin

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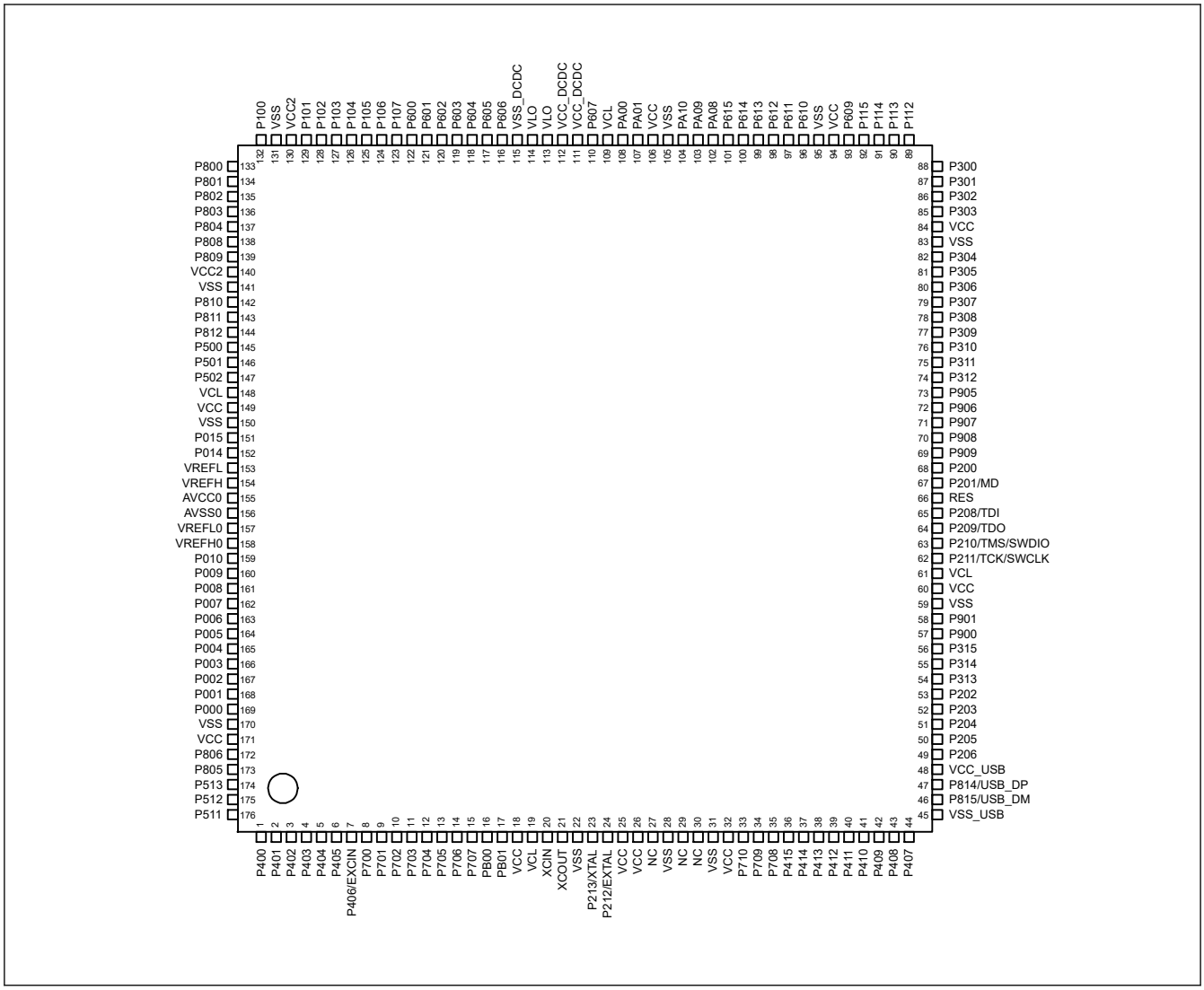


Figure 1.4 Pin assignment for LQFP 176-pin

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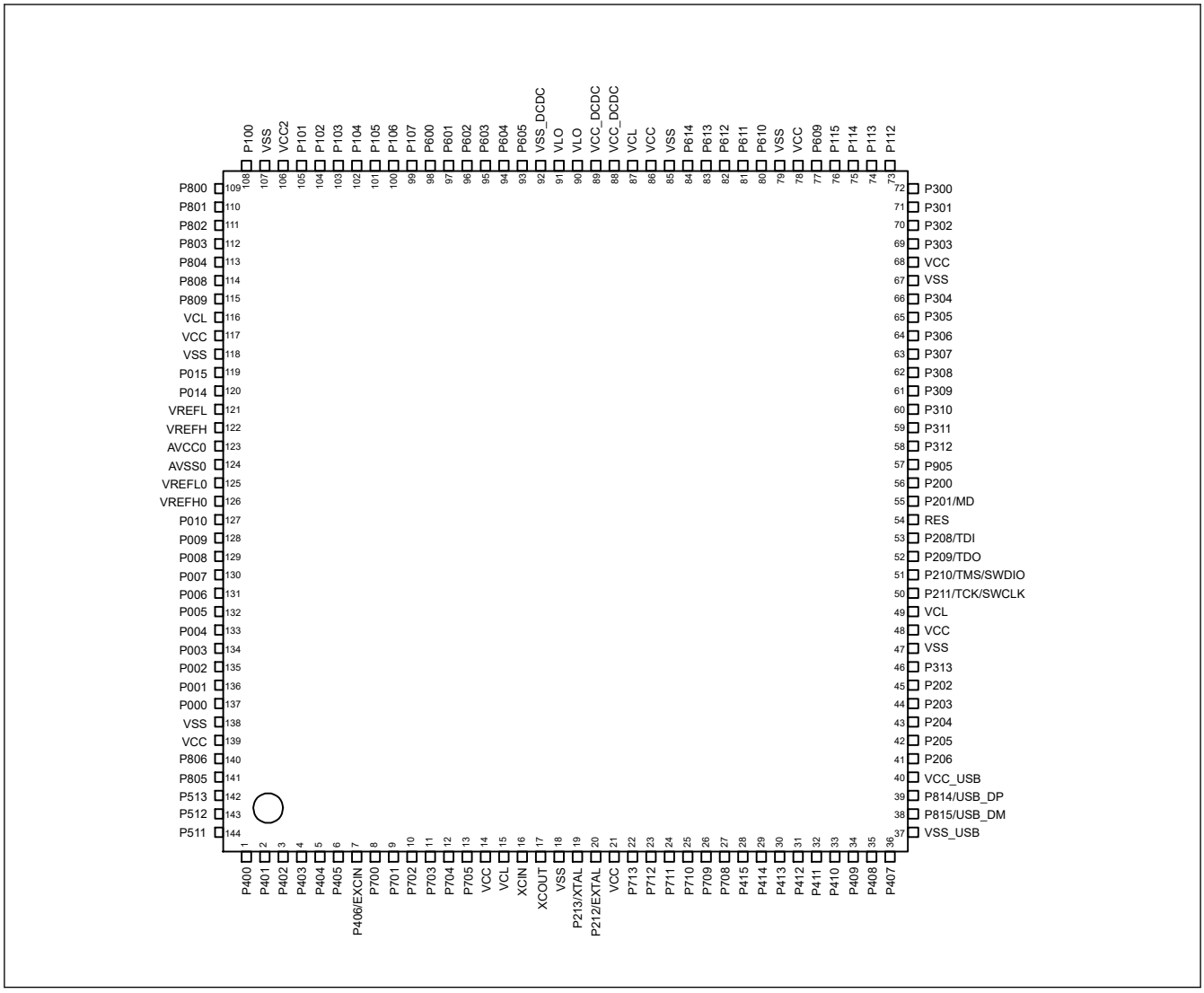


Figure 1.5 Pin assignment for LQFP 144-pin

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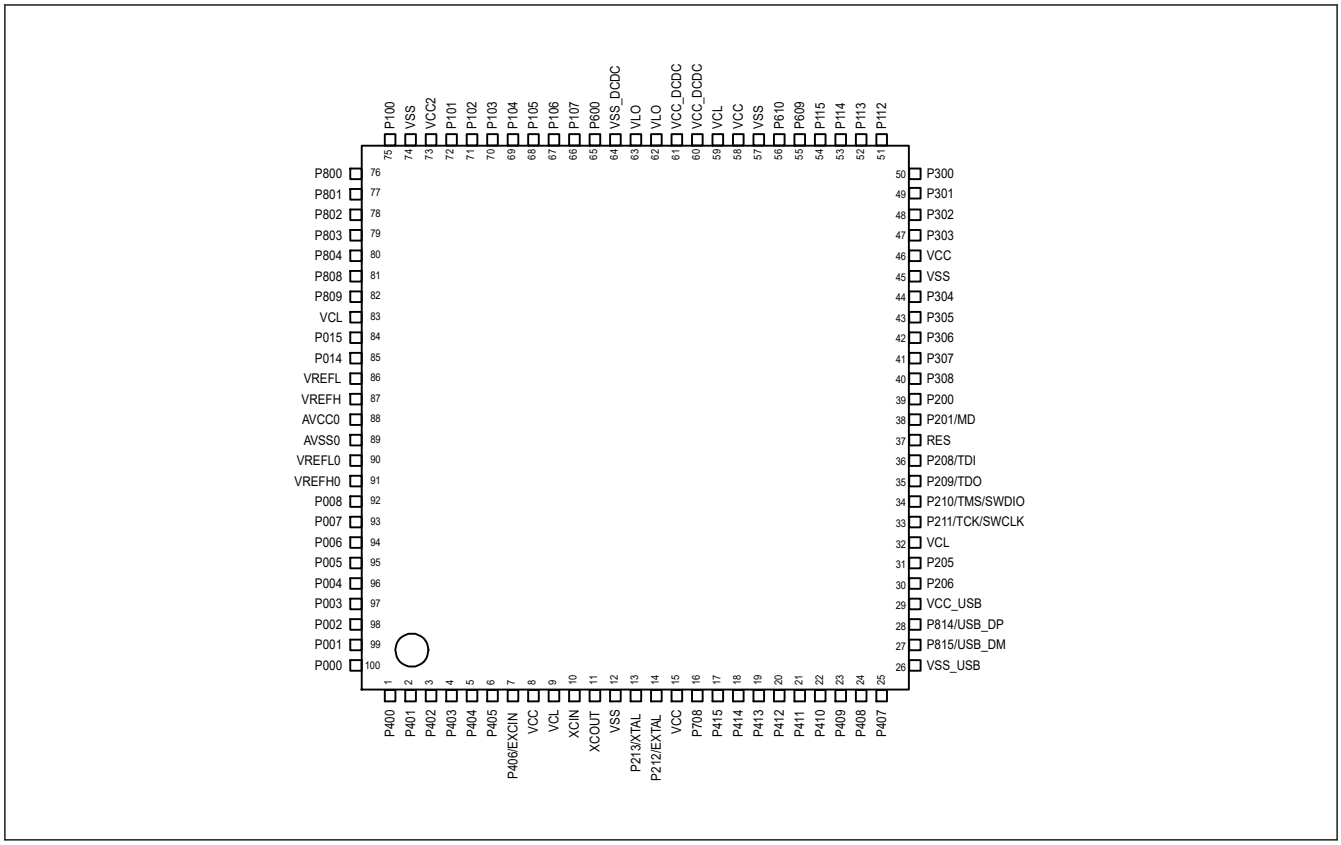


Figure 1.6 Pin assignment for LQFP 100-pin

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1.7 Pin Lists

Table 1.15 Pin list (1 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
R15	1	1	1	-	P400	-	IRQ0	TXD1_A/MOSI1_A/SDA1_A/I3C_SCL0/ SD1CLK_B/ET0_WOL/ET0_WOL	GTIOC6A/AGTIO1	ADTRG1
P15	2	2	2	-	P401	-	IRQ5-DS	RXD1_A/MISO1_A/SCL1_A/I3C_SDA0/ CTX0/SD1CMD_B/ET0_MDC/ET0_MDC	GTETRGA/GTIOC6B	-
M12	3	3	3	CACREF	P402	-	IRQ4-DS	SCK1_A/DE1/CRX0/SD1DAT0_B/ ET0_MDIO/ET0_MDIO	-	-
N14	4	4	4	-	P403	-	IRQ14-DS	CTS1_RTS1_A/SS4_A/DE1/SD1DAT1_B/ ET0_LINKSTA/ET0_LINKSTA	GTIOC3A	-
L10	5	5	5	-	P404	-	IRQ15-DS	CTS1_A/SD1DAT2_B/ET0_EXOUT/ ET0_EXOUT	GTIOC3B	-
N15	6	6	6	-	P405	-	-	SCK2_B/DE2/SD1DAT3_B/ET0_TX_EN/ RMII0_TXD_EN_B	GTIOC1A/AGTIO1	-
M13	7	7	7	EXCIN	P406	-	-	TXD2_B/MOSI2_B/SDA2_B/SSLA3_C/ SD1CD/ET0_RX_ER/RMII0_TXD1_B	GTIOC1B	-
M14	8	8	-	-	P700	-	-	RXD2_B/MISO2_B/SCL2_B/MISOA_C/ SD1WP/ET0_ETXD1/RMII0_TXD0_B	GTIOC5A	-
L12	9	9	-	-	P701	-	-	CTS2_RTS2_B/SS2_B/DE2/MOSIA_C/ SD1DAT4_B/ET0_ETXD0/REF50CK0_B	GTIOC5B/ULPTO1	-
L13	10	10	-	-	P702	-	-	CTS2_B/RSPCKA_C/SD1DAT5_B/ ET0_ERXD1/RMII0_RXD0_B	GTIOC6A/ULPTO0	-
L11	11	11	-	-	P703	-	-	SSLA0_C/SD1DAT6_B/ET0_ERXD0/ RMII0_RXD1_B	GTIOC6B/AGTO1	VCOUT
K12	12	12	-	-	P704	-	-	SSLA1_C/CTX0/SD1DAT7_B/ ET0_RX_CLK/RMII0_RX_ER_B	GTADSM0/AGTO0	-
K10	13	13	-	-	P705	-	-	CTS1_B/SSLA2_C/CRX0/ET0_CRS/ RMII0_CRS_DV_B	GTADSM1/AGTIO0	-
K13	14	-	-	-	P706	-	IRQ7	RXD1_B/MISO1_B/SCL1_B	AGTIO0	-
K11	15	-	-	-	P707	-	IRQ8	TXD1_B/MOSI1_B/SDA1_B	-	-
L14	16	-	-	-	PB00	-	-	SCK1_B/DE1	-	-
J10	-	-	-	-	PB02	-	-	-	-	-
M15	-	-	-	-	PB03	-	-	-	-	-
H10	-	-	-	-	PB04	-	-	-	-	-
L15	17	-	-	-	PB01	ALE	-	CTS1_RTS1_B/SS1_B/DE1	-	-
H11	-	-	-	-	PB05	-	-	-	-	-
J11	-	-	-	-	PB06	-	-	-	GTIOC9A	-
J12	-	-	-	-	PB07	-	-	-	GTIOC9B	-
K14	18	14	8	VCC	-	-	-	-	-	-
K15	19	15	9	VCL	-	-	-	-	-	-
J15	20	16	10	XCIN	-	-	-	-	-	-
J14	21	17	11	XCOUT	-	-	-	-	-	-
J13	22	18	12	VSS	-	-	-	-	-	-
H14	23	19	13	XTAL	P213	-	IRQ2	TXD1_C/MOSI1_C/SDA1_C	GTETRGC/GTIOC0A/ ULPTEE0	ADTRG1
H15	24	20	14	EXTAL	P212	-	IRQ3	RXD1_C/MISO1_C/SCL1_C	GTETRGD/GTIOC0B/ AGTEE1	-
G12	25	21	15	VCC	-	-	-	-	-	-
H13	26	-	-	VCC	-	-	-	-	-	-
G13	27	-	-	NC*1	-	-	-	-	-	-
G14	28	-	-	VSS	-	-	-	-	-	-
F15	29	-	-	NC*1	-	-	-	-	-	-
F14	30	-	-	NC*1	-	-	-	-	-	-
G15	31	-	-	VSS	-	-	-	-	-	-
F13	32	-	-	VCC	-	-	-	-	-	-
F11	-	-	-	-	P715	-	-	RXD4_C/MISO4_C/SCL4_C	-	-

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Table 1.15 Pin list (2 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
G10	-	-	-	-	P714	-	-	TXD4_C/MOSI4_C/SDA4_C	-	-
H12	-	-	-	VSS	-	-	-	-	-	-
G11	-	22	-	-	P713	-	-	-	GTIOC2A/AGTOA0	-
E12	-	23	-	-	P712	-	-	-	GTIOC2B/AGTOB0	-
F10	-	24	-	-	P711	-	-	-	AGTEE0	-
E14	33	25	-	-	P710	CS5	-	CTS4_B	-	-
E15	34	26	-	-	P709	CS4	IRQ10	CTS4_RTS4_B/SS4_B/DE4	-	-
E13	35	27	16	CACREF	P708	WR1/BC1	IRQ11	SCK4_B/DE4/SSLB3_B	-	-
C14	36	28	17	-	P415	WAIT	IRQ8	TXD4_B/MOSI4_B/SDA4_B/SSLB2_B/ CTX1/SD0CD	GTADSM0/GTIOC0A	-
D15	37	29	18	-	P414	A23	IRQ9	RXD4_B/MISO4_B/SCL4_B/SSLB1_B/ CRX1/SD0WP	GTADSM1/GTIOC0B	-
A15	38	30	19	-	P413	A22	-	SSLB0_B/SD0CLK_A	GTOUUP/ULPTEE1	-
C15	39	31	20	-	P412	A21	-	CTS3_A/RSPCKB_B/USB_EXICEN/ SD0CMD_A	GTOULO/AGTEE1	-
D13	40	32	21	-	P411	A20	IRQ4	CTS3_RTS3_A/SS3_A/DE3/MOSIB_B/ USB_ID/SD0DAT0_A	GTOVUP/GTIOC9A/ AGTOA1	-
D14	41	33	22	-	P410	A19	IRQ5	SCK3_A/DE3/SCL0_A/MISOB_B/ USB_OVRCURB-DS/SD0DAT1_A	GTOVLO/GTIOC9B/ AGTOB1	-
E11	42	34	23	-	P409	A18	IRQ6	TXD3_A/MOSI3_A/SDA3_A/SDA0_A/ USB_OVRCURA-DS	GTOWUP/ULPTOA0	-
G6	-	-	-	VCL	-	-	-	-	-	-
B15	43	35	24	-	P408	A17	IRQ7	CTS4_A/RXD3_A/MISO3_A/SCL3_A/ SCL0_B/USB_VBUSEN	GTOWLO/GTIOC10A/ ULPTOB0	-
D12	44	36	25	-	P407	CS6	-	CTS4_RTS4_A/SS4_A/DE4/SDA0_B/ SSLA3_A/USB_VBUS	GTIOC10B/AGTIO0	ADTRG0
B13	45	37	26	VSS_USB	-	-	-	-	-	-
B14	46	38	27	-	P815	-	-	CTX0/USB_DM	GTIOC8A	-
A14	47	39	28	-	P814	-	-	CRX0/USB_DP	GTIOC8B	-
A13	48	40	29	VCC_USB	-	-	-	-	-	-
C13	-	-	-	-	P207	-	-	-	-	-
D11	49	41	30	-	P206	CS7	IRQ0-DS	RXD4_A/MISO4_A/SCL4_A/SDA1_B/ SSLA2_A/USB_VBUSEN/SD0DAT2_A	GTIU	-
B12	50	42	31	CLKOUT	P205	-	IRQ1-DS	TXD4_A/MOSI4_A/SDA4_A/SCL1_B/ SSLA1_A/USB_OVRCURA/SD0DAT3_A	GTIV/GTIOC4A/AGTO1	-
A12	51	43	-	CACREF	P204	-	-	SCK4_A/DE4/SSLA0_A/USB_OVRCURB/ SD0DAT4_A	GTIW/GTIOC4B/AGTIO1	-
B11	52	44	-	-	P203	-	IRQ2-DS	RSPCKA_A/CTX0/SD0DAT5_A	GTIOC5A/ULPTOA1	-
A11	53	45	-	-	P202	-	IRQ3-DS	MOSIA_A/CRX0/SD0DAT6_A	GTIOC5B/ULPTOB1	-
B10	54	46	-	-	P313	-	-	CTS3_C/MISOA_A/SD0DAT7_A	-	-
A10	55	-	-	-	P314	-	-	CTS3_RTS3_C/SS3_C/DE3	-	ADTRG0
C11	56	-	-	-	P315	-	-	SCK3_C/DE3	-	-
C10	57	-	-	-	P900	-	-	TXD3_C/MOSI3_C/SDA3_C	-	-
B9	58	-	-	-	P901	-	-	RXD3_C/MISO3_C/SCL3_C	AGTIO1	-
D10	-	-	-	-	P902	-	-	-	-	-
C12	59	47	-	VSS	-	-	-	-	-	-
F12	60	48	-	VCC	-	-	-	-	-	-
C9	-	-	-	-	P903	-	-	-	GTIOC11A	-
D9	-	-	-	-	P904	-	-	-	GTIOC11B	-
A8	61	49	32	VCL	-	-	-	-	-	-
E10	62	50	33	TCK/SWCLK	P211	-	-	SCK9_B/DE9	GTOUUP/GTIOC0A	-
D8	63	51	34	TMS/SWDIO	P210	-	-	CTS9_RTS9_B/SS9_B/DE9	GTOULO/GTIOC0B	-
F9	64	52	35	TDO/SWO/CLKOUT	P209	-	-	TXD9_B/MOSI9_B/SDA9_B/CTX1	GTOVUP/GTIOC1A	-
F8	65	53	36	TDI	P208	-	IRQ3	RXD9_B/MISO9_B/SCL9_B/CRX1	GTOVLO/GTIOC1B	VCOUT

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Table 1.15 Pin list (3 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
E8	-	-	-	CLKOUT	P913	-	-	-	-	-
A9	66	54	37	RES	-	-	-	-	-	-
E9	67	55	38	MD	P201	-	-	-	-	-
B8	68	56	39	-	P200	-	NMI	-	-	-
F7	-	-	-	-	P912	-	-	-	GTIOC3A	-
E6	-	-	-	-	P911	-	-	-	GTIOC3B	-
E7	-	-	-	-	P910	-	-	-	-	-
A7	69	-	-	-	P909	CS3/CAS	-	-	GTIOC12A	-
C8	70	-	-	-	P908	CS2/RAS	IRQ11	-	GTIOC12B	-
B7	71	-	-	-	P907	A16/A16	IRQ10	USB_EXICEN	GTIOC13A	-
C7	72	-	-	-	P906	A15/A15	IRQ9	USB_ID	GTIOC13B	-
A6	73	57	-	-	P905	A14/A14	IRQ8	CTS3_B	-	-
D7	74	58	-	-	P312	A13/A13	-	CTS3_RTS3_B/SS3_B/DE3/CTX0/ ET0_TX_CLK	GTADSM0/AGTOA1	-
B6	75	59	-	-	P311	A12/A12	-	SCK3_B/DE3/CRX0/ET0_TX_ER	GTADSM1/AGTOB1	-
G8	-	-	-	VSS	-	-	-	-	-	-
D6	76	60	-	-	P310	A11/A11	-	TXD3_B/MOSI3_B/SDA3_B/ET0_ETXD2	AGTEE1	-
C6	77	61	-	-	P309	A10/A10	-	RXD3_B/MISO3_B/SCL3_B/ET0_ETXD3	-	-
A5	78	62	40	TCLK	P308	A9/A9	-	CTS9_B/SD0CLK_B/ET0_MDC/ET0_MDC	GTIU/ULPTOB1	-
B5	79	63	41	TDATA0	P307	A8/A8	-	SD0CMD_B/ET0_MDIO/ET0_MDIO	GTIV/ULPTOA1	-
A4	80	64	42	TDATA1	P306	A7/A7	-	SD0CD/ET0_TX_EN/RMII0_TXD_EN_A	GTIW/ULPTEVI1	-
B4	81	65	43	TDATA2	P305	A6/A6	IRQ8	SD0WP/ET0_RX_ER/RMII0_TXD1_A	GTOVUP/ULPTEE1	-
A3	82	66	44	TDATA3	P304	A5/A5	IRQ9	SD0DAT0_B/ET0_ETXD1/RMII0_TXD0_A	GTOVLO/GTIOC7A/ ULPTO1	-
G7	83	67	45	VSS	-	-	-	-	-	-
G9	84	68	46	VCC	-	-	-	-	-	-
C5	-	-	-	-	P915	-	-	-	GTIOC5A	-
F6	-	-	-	-	P914	-	-	-	GTIOC5B	-
C4	85	69	47	-	P303	A4/A4	-	SD0DAT1_B/ET0_ETXD0/REF50CK0_A	GTIOC7B	-
B3	86	70	48	-	P302	A3/A3	IRQ5	SD0DAT2_B/ET0_ERXD1/RMII0_RXD0_A	GTOUUP/GTIOC4A/ ULPTO0-DS	-
A2	87	71	49	-	P301	A2/A2	IRQ6	SD0DAT3_B/ET0_ERXD0/RMII0_RXD1_A	GTOULO/GTIOC4B/ AGTIO0/ULPTEE0-DS	-
D5	88	72	50	-	P300	A1/A1/DQM3	IRQ4	SCK0_A/DE0/SSLA3_B/ET0_RX_CLK/ RMII0_RX_ER_A	GTIOC3A/ULPTEVI0-DS	-
B2	89	73	51	-	P112	A0/BC0/A0/DQM1	-	TXD0_A/MOSI0_A/SDA0_A/SSLA2_B/ ET0_CRS/RMII0_CRS_DV_A	GTIOC3B/ULPTOB0-DS	-
C3	90	74	52	-	P113	CS1/CKE	-	RXD0_A/MISO0_A/SCL0_A/SSLA1_B/ ET0_EXOUT/ET0_EXOUT	GTIOC2A/ULPTOA0-DS	-
C2	91	75	53	-	P114	CS0/WE	-	CTS0_RTS0_A/SS0_A/DE0/SSLA0_B/ ET0_LINKSTA/ET0_LINKSTA	GTIOC2B	-
D3	92	76	54	-	P115	SDCS	-	CTS0_A/MOSIA_B/ET0_WOL/ET0_WOL	GTIOC5A	-
B1	93	77	55	-	P609	D8[A8/D8]/DQ8	-	TXD0_C/MOSI0_C/SDA0_C/MISOA_B/ CTX1/ET0_RX_DV	GTIOC5B/ULPTOA1-DS	-
D4	-	-	-	-	PA11	WR2/BC2/DQM2	-	-	GTIOC6A	-
D2	-	-	-	-	PA12	D16/DQ16	-	-	GTIOC6B	-
E5	-	-	-	-	PA13	D17/DQ17	-	-	-	-
C1	-	-	-	-	PA14	D18/DQ18	-	TXD9_C/MOSI9_C/SDA9_C	-	-
-	94	78	-	VCC	-	-	-	-	-	-
H7	95	79	-	VSS	-	-	-	-	-	-
E4	96	80	56	-	P610	D9[A9/D9]/DQ9	-	RXD0_C/MISO0_C/SCL0_C/RSPCKA_B/ CRX1/ET0_COL	GTIOC4A/ULPTOB1-DS	-
D1	97	81	-	CLKOUT/CACREF	P611	D10[A10/D10]/DQ10	-	SCK0_C/DE0/MOSIA_B/ET0_ERXD2	GTIOC4B	-

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Table 1.15 Pin list (4 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
F3	98	82	-	-	P612	D11[A11/D11]/DQ11	-	CTS0_RTS0_C/SS0_C/DE0/SSLA0_B/ ET0_ERXD3	-	-
E2	99	83	-	-	P613	D12[A12/D12]/DQ12	-	CTS0_C	GTETRGA/AGTO1	-
F4	100	84	-	-	P614	D13[A13/D13]/DQ13	-	-	GTETRGB/AGTO0	-
E3	101	-	-	-	P615	D14[A14/D14]/DQ14	IRQ7	USB_VBUSEN	GTETRGC	-
G3	102	-	-	-	PA08	D15[A15/D15]/DQ15	IRQ6	-	GTETRGD	-
E1	103	-	-	-	PA09	EBCLK/SDCLK	IRQ5	-	-	-
F2	104	-	-	-	PA10	WR/WR0/DQM0	IRQ4	-	-	-
F5	-	-	-	-	PA15	D19/DQ19	-	RXD9_C/MISO9_C/SCL9_C	-	-
J5	-	-	-	-	P813	D20/DQ20	-	-	-	-
G5	-	-	-	-	PA07	D21/DQ21	-	-	GTIOC7A	-
L5	-	-	-	-	PA06	D22/DQ22	-	CTS2_C	GTIOC7B	-
H5	-	-	-	-	PA05	D23/DQ23	-	CTS2_RTS2_C/SS2_C/DE2	-	-
L6	-	-	-	-	PA04	D24/DQ24	-	SCK2_C/DE2	-	-
G4	-	-	-	-	PA03	D25/DQ25	-	TXD2_C/MOSI2_C/SDA2_C	-	-
K6	-	-	-	-	PA02	D26/DQ26	-	RXD2_C/MISO2_C/SCL2_C	-	-
J7	105	85	57	VSS	-	-	-	-	-	-
J6	106	86	58	VCC	-	-	-	-	-	-
H3	107	-	-	-	PA01	RD	-	-	-	-
H4	108	-	-	-	PA00	D7[A7/D7]/DQ7	-	-	-	-
F1	109	87	59	VCL	-	-	-	-	-	-
J4	110	-	-	-	P607	D6[A6/D6]/DQ6	-	-	-	-
G1	111	88	60	VCC_DCDC	-	-	-	-	-	-
G2	112	89	61	VCC_DCDC	-	-	-	-	-	-
H1	113	90	62	VLO	-	-	-	-	-	-
H2	114	91	63	VLO	-	-	-	-	-	-
J1	115	92	64	VSS_DCDC	-	-	-	-	-	-
M5	116	-	-	-	P606	D5[A5/D5]/DQ5	-	-	-	-
K5	117	93	-	-	P605	D4[A4/D4]/DQ4	-	CTS0_B	GTIOC8A	-
N4	118	94	-	-	P604	D3[A3/D3]/DQ3	-	CTS0_RTS0_B/SS0_B/DE0	GTIOC8B	-
M4	119	95	-	-	P603	D2[A2/D2]/DQ2	-	TXD0_B/MOSI0_B/SDA0_B	GTIOC7A/ULPTO0	-
L4	120	96	-	-	P602	D1[A1/D1]/DQ1	-	RXD0_B/MISO0_B/SCL0_B	GTIOC7B/ULPTEE0	-
K4	121	97	-	-	P601	D0[A0/D0]/DQ0	-	SCK0_B/DE0	GTIOC6A/ULPTEVI0	-
K3	122	98	65	CACREF	P600	-	-	-	GTIOC6B/ULPTEVI1-DS	-
K1	123	99	66	-	P107	-	-	-	GTOWUP/GTIOC8A/ AGTOA0	-
K2	124	100	67	-	P106	-	-	SSLB3_A	GTOWLO/GTIOC8B/ AGTOB0/ULPTEE1-DS	-
L3	125	101	68	-	P105	-	IRQ0	SSLB2_A	GTIOC1A/ULPTO1-DS	-
L1	126	102	69	-	P104	-	IRQ1	CTS9_A/SSLB1_A	GTETRGB/GTIOC1B	-
L2	127	103	70	-	P103	-	-	CTS9_RTS9_A/SS9_A/DE9/SSLB0_A/ CTX0	GTOWUP/GTIOC2A	-
M1	128	104	71	-	P102	-	-	TXD9_A/MOSI9_A/SDA9_A/RSPCKB_A/ CRX0	GTOWLO/GTIOC2B/ AGTO0	ADTRG0
M2	129	105	72	-	P101	-	IRQ1	RXD9_A/MISO9_A/SCL9_A/MOSIB_A	GTETRGB/GTIOC8A/ AGTEE0	-
J3	130	106	73	VCC2	-	-	-	-	-	-
J2	131	107	74	VSS	-	-	-	-	-	-
N1	132	108	75	-	P100	-	IRQ2	SCK9_A/DE9/MISOB_A	GTETRGA/GTIOC8B/ AGTIO0	-
M3	133	109	76	-	P800	-	IRQ11	CTS2_A	GTIU/GTIOC11A/ AGTOA0	-

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Table 1.15 Pin list (5 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
N2	134	110	77	-	P801	-	IRQ12	TXD2_A/MOSI2_A/SDA2_A	GTIV/GTIOC11B/ AGTOB0	-
P1	135	111	78	-	P802	-	-	RXD2_A/MISO2_A/SCL2_A	GTIW/GTIOC12A	-
N3	136	112	79	-	P803	-	-	SCK2_A/DE2	GTETRGC/GTIOC12B	-
P2	137	113	80	-	P804	-	IRQ14	CTS2_RTS2_A/SS2_A/DE2	GTETRGD/GTIOC13A	-
R1	138	114	81	-	P808	-	IRQ15	-	GTIOC13B	-
R2	139	115	82	-	P809	-	-	-	-	-
P3	140	-	-	VCC2	-	-	-	-	-	-
R3	141	-	-	VSS	-	-	-	-	-	-
P4	142	-	-	-	P810	-	-	SD1CLK_A	ULPTOA0	-
M6	143	-	-	-	P811	-	-	USB_ID/SD1CMD_A	ULPTOB0	-
R4	144	-	-	-	P812	-	-	USB_EXICEN/SD1DAT0_A	-	AN122
P5	145	-	-	CACREF	P500	-	-	USB_VBUSEN/SD1DAT1_A	-	AN121
R5	146	-	-	-	P501	-	-	USB_OVRCURA/SD1DAT2_A	-	AN120
P6	147	-	-	-	P502	-	-	USB_OVRCURB/SD1DAT3_A	-	AN019/AN119
K7	-	-	-	-	P503	-	-	SD1CD	-	-
N5	-	-	-	-	P504	-	-	SD1WP	-	-
K8	-	-	-	-	P505	D27/DQ27	-	SD1DAT4_A	-	-
N6	-	-	-	-	P506	D28/DQ28	-	SD1DAT5_A	-	-
L7	-	-	-	-	P507	D29/DQ29	-	SD1DAT6_A	-	-
M7	-	-	-	-	P508	D30/DQ30	IRQ1	SD1DAT7_A	-	-
L8	-	-	-	-	P509	D31/DQ31	IRQ2	-	ULPTEVI1	-
N7	-	-	-	-	P510	WR3/BC3	IRQ3	-	ULPTEVI0	-
R6	148	116	83	VCL	-	-	-	-	-	-
J9	149	117	-	VCC	-	-	-	-	-	-
J8	150	118	-	VSS	-	-	-	-	-	-
R7	151	119	84	-	P015	-	IRQ13	-	-	AN105/DA1
P7	152	120	85	-	P014	-	-	-	-	AN007/DA0
P8	153	121	86	VREFL	-	-	-	-	-	-
R8	154	122	87	VREFH	-	-	-	-	-	-
N8	155	123	88	AVCC0	-	-	-	-	-	-
N9	156	124	89	AVSS0	-	-	-	-	-	-
P9	157	125	90	VREFL0	-	-	-	-	-	-
R9	158	126	91	VREFH0	-	-	-	-	-	-
M9	-	-	-	-	P011	-	-	-	-	AN106
M8	159	127	-	-	P010	-	IRQ14	-	-	AN005/IVCMP0
L9	160	128	-	-	P009	-	IRQ13-DS	-	-	AN006
R10	161	129	92	-	P008	-	IRQ12-DS	-	-	AN008
M10	162	130	93	-	P007	-	-	-	-	AN004
R11	163	131	94	-	P006	-	IRQ11-DS	-	-	AN002/IVCMP3
N10	164	132	95	-	P005	-	IRQ10-DS	-	-	AN001
P10	165	133	96	-	P004	-	IRQ9-DS	-	-	AN000/IVCMP2
P11	166	134	97	-	P003	-	-	-	-	AN104/IVREF1
R12	167	135	98	-	P002	-	IRQ8-DS	-	-	AN102/IVCMP3
P12	168	136	99	-	P001	-	IRQ7-DS	-	-	AN101/IVREF0
R13	169	137	100	-	P000	-	IRQ6-DS	-	-	AN100/IVCMP2
H6	-	-	-	VCL	-	-	-	-	-	-
H8	170	138	-	VSS	-	-	-	-	-	-
H9	171	139	-	VCC	-	-	-	-	-	-
N11	172	140	-	-	P806	-	IRQ0	-	-	AN018/AN118

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Table 1.15 Pin list (6 of 6)

BGA224	LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ SDHI/MMC/EHTERC(MII,RMII)	GPT/AGT/ULPT	ADC12/DAC12/ ACMPHS
M11	173	141	-	-	P805	-	-	-	-	AN017/AN117
N12	-	-	-	-	P807	-	-	-	-	-
P13	174	142	-	-	P513	-	-	-	-	AN016/AN116/ IVCMP0
R14	-	-	-	-	P515	-	-	-	-	-
N13	175	143	-	-	P512	-	IRQ14	SCL1_A/CTX1	GTIOC0A	-
P14	-	-	-	-	P514	-	-	-	-	-
K9	176	144	-	-	P511	-	IRQ15	SDA1_A/CRX1	GTIOC0B	-

Note: Several pin names have the added suffix of _A, _B, and _C. These suffixes have special conditions for electrical characteristics. See section 2, Electrical Characteristics for detail.

Note 1. NC but the ball exists.

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2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = VCC_DCDC = VCC_USB = 1.68 to 3.6 V
- VCC2 = 1.65 to 3.6 V
- AVCC0 = 1.65 to 3.6 V
- VREFH0 = 2.7 V to AVCC0
- VREFH = 1.65 V to AVCC0
- VSS = VSS_DCDC = AVSS0 = VREFL0 /VREFL = VSS_USB = 0 V
- VCC voltage is lower than 2.7 V : LVOCR.LVO0E = 1, otherwise LVOCR.LVO0E = 0
- VCC2 voltage is lower than 2.7 V : LVOCR.LVO1E = 1, otherwise LVOCR.LVO1E = 0
- $T_j = T_{opj}$
- When not specified otherwise, typical values are measured at room temperature of 25 °C and VCC = VCC_DCDC = VCC_USB = AVCC0 = VREFH0 = VREFH = 3.3V

Figure 2.1 shows the timing conditions.

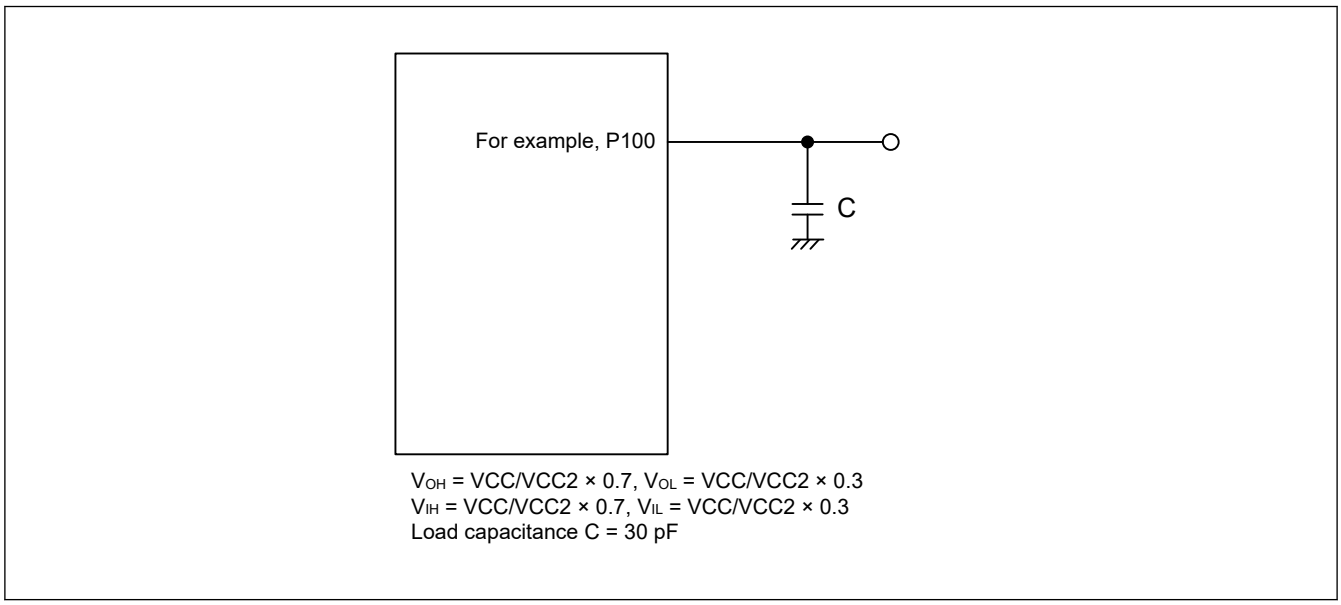


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC2, VCC_DCDC, VCC_USB*2	–0.3 to +4.0	V
External power supply voltage	VCL	–0.3 to +1.6	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3 or –0.3 to VCC2 + 0.3	V

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Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage	AVCC0	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating junction temperature*3 *4	T_{opj}	–40 to +125	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715 and PB01 are 5 V tolerant.
Note 2. Connect VCC_DCDC and VCC_USB to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Tj = +105°C to +125°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC, VCC_DCDC	Other than the following	1.68	—	3.60	V
		When ETHERC/IIC Fast-mode+ is used	2.70	—	3.60	V
		When USB/SDRAM is used	3.00	—	3.60	V
	VCC2		1.65	—	3.60	V
	VCL	When external VDD is used*2	1.20	—	1.25	V
		When DCDC is used (High-speed mode)	—	1.21	—	V
		When DCDC is used (Low-speed mode or Software Standby mode)	—	1.18	—	V
	VSS, VSS_DCDC		—	0	—	V
USB power supply voltages	VCC_USB		—	VCC	—	V
	VSS_USB		—	0	—	V
Analog power supply voltages	AVCC0*1	When ADC is not used	1.65	—	3.60	V
		When ADC is used	2.70	—	3.60	V
	AVSS0		—	0	—	V

Note 1. When the A/D converter, the D/A converter and the High-Speed Analog Comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.
Note 2. VCL voltage must never be higher than VCC voltage.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible operating junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode

Note: Make sure that $T_j = T_a + \theta_{ja} \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + (I_{CC}max + I_{CC_DCDC}max) \times VCC$.
Note: Minimum Ambient Temperature(Ta) is -40℃

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2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} except for Schmitt trigger input pins

Parameter		VCC/VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit
Peripheral function pins	EXTAL (external clock input), WAIT, SPI*1 (except RSPCK)	1.68 V or above	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
	SPI*2 (except RSPCKB_A)	1.65 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
	SD*3	2.70 V or above	V_{IH}	VCC × 0.625	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.25	
		1.70 V ~ 1.95 V	V_{IH}	1.27	—	2	
			V_{IL}	VSS − 0.3	—	0.58	
	SD*4	2.70 V or above	V_{IH}	VCC2 × 0.625	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.25	
		1.70 V ~ 1.95 V	V_{IH}	1.27	—	2	
			V_{IL}	VSS − 0.3	—	0.58	
	MMC*5	2.70 V or above	V_{IH}	VCC × 0.625	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.25	
		1.70 V ~ 1.95 V	V_{IH}	VCC × 0.65	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.35	
	MMC*6	2.70 V or above	V_{IH}	VCC2 × 0.625	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.25	
		1.70 V ~ 1.95 V	V_{IH}	VCC2 × 0.65	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.35	
	D00 to D31, TMS, TDI, TCK, SWDIO, SWCLK	1.68 V or above	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
	DQ00 to DQ31	3.00 V or above	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
	ETHERC	2.70 V or above	V_{IH}	2.3	—	—	
			V_{IL}	—	—	VCC × 0.2	
	IIC (SMBus)	2.70 V or above	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
	EXCIN	1.68 V or above	V_{IH}	0.9	—	3.9	
			V_{IL}	—	—	0.3	

Note 1. SPI0_A, SPI0_B, SPI0_C and SPI1_B
Note 2. SPI1_A
Note 3. SD_A ch0, SD_B ch1 and SD_B ch1
Note 4. SD_A ch1
Note 5. MMC_A ch0, MMC_A ch1 and MMC_B ch1
Note 6. MMC_A ch1 (Up to 4-bit bus width)

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Table 2.5 I/O V_{IH}, V_{IL} of Schmitt trigger input pins

Parameter		VCC/VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit
Peripheral function pins	IIC (except for SMBus)	1.68 V or above	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
	I3C	1.68 V or above	V_{IH}	VCC × 0.7	—	VCC + 0.3	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.1	—	—	
	5 V-tolerant ports*1*5	1.68 V or above	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Other VCC input pins*2	1.68 V or above	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Other VCC2 input pins*2	1.65 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
			ΔV_T	VCC2 × 0.05	—	—	
	Other AVCC0 input pins*2	1.65 V or above	V_{IH}	AVCC0 × 0.8	—	—	
			V_{IL}	—	—	AVCC0 × 0.2	
			ΔV_T	AVCC0 × 0.05	—	—	
Ports	5 V-tolerant port*3*5	1.68 V or above	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
	Other VCC input pins*4	1.68 V or above	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
	Other VCC2 input pins*4	1.65 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
	Other AVCC0 input pins*4	1.65 V or above	V_{IH}	AVCC0 × 0.8	—	—	
			V_{IL}	—	—	AVCC0 × 0.2	

Note 1. RES and peripheral function pins associated with P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715, PB01 (total 26 pins).
Note 2. All input pins except for the peripheral function pins already described in the table. There is an item for each power supply voltage for each port. Refer to the IO chapter for the power supply of the port.
Note 3. P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715, PB01 (total 25 pins).
Note 4. All input pins except for the ports already described in the table. There is an item for each power supply voltage for each port. Refer to the IO chapter for the power supply of the port.
Note 5. When VCC is less than 1.68 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

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2.2.3 I/O I_{OH}, I_{OL}

Table 2.6 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			VCC/ VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P011, P014, P015, P201	—	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
	Ports P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715, PA09, PB01 (total 26 pins)	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
	Ports P100 to P103, P304 to P308, P800 to P804, P808 to P810, PA09 (total 18 pins)	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−16	mA
				I_{OL}	—	—	16.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
	Port PA09	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
	Other output pins*5	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−16	mA
				I_{OL}	—	—	16.0	mA

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Table 2.6 I/O I_{OH}, I_{OL} (2 of 2)

Parameter			VCC/ VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit
Permissible output current (max value per pin)	Ports P000 to P011, P014, P015, P201	—	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
	Ports P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715, PA09, PB01 (total 26 pins)	Low drive*1	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		Middle drive*2	—	I_{OH}	—	—	−8.0	mA
				I_{OL}	—	—	8.0	mA
		High drive*3	—	I_{OH}	—	—	−40	mA
				I_{OL}	—	—	40.0	mA
	Ports P100 to P103, P304 to P308, P800 to P804, P808 to P810, PA09 (total 18 pins)	Low drive*1	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		Middle drive*2	—	I_{OH}	—	—	−8.0	mA
				I_{OL}	—	—	8.0	mA
		High drive*3	—	I_{OH}	—	—	−32	mA
				I_{OL}	—	—	32.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−40	mA
				I_{OL}	—	—	40.0	mA
	Other output pins*5	Low drive*1	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		Middle drive*2	—	I_{OH}	—	—	−8.0	mA
				I_{OL}	—	—	8.0	mA
		High drive*3	—	I_{OH}	—	—	−32	mA
				I_{OL}	—	—	32.0	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins	VCC I/O	1.68 V or above	$\Sigma I_{OH\ (max)}$	—	—	−80	mA
		VCC2 I/O	1.65 V or above		—	—	−80	
		AVCC0 I/O	1.65 V or above		—	—	−33	
		VCC and VCC2 I/O	1.65 V or above	$\Sigma I_{OL\ (max)}$	—	—	80	mA
		AVCC0 I/O	1.65 V or above		—	—	33	

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for 400 and P401 is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for 400 and P401 is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for 400 and P401 is retained in Deep Software Standby mode.
Note 4. This is the value when high-speed high driving ability is selected in the Port Drive Capability in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. Except for P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

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2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (1 of 3)

Parameter		VCC/VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC	2.70 V or above	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
		1.68 V or above	V_{OL}	—	—	VCC × 0.2		I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	IIC*1	2.70 V or above	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	I3C	2.70 V or above	V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 1)
			V_{OH}	VCC − 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
		1.68 V or above	V_{OL}	—	—	VCC × 0.2		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	VCC × 0.2		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 1)
			V_{OH}	VCC − 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
	ETHERC	2.70 V or above	V_{OH}	VCC − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.4		I_{OL} = 1.0 mA
	SD	2.70 V or above	V_{OH}	VCC × 0.75	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	VCC × 0.125		I_{OL} = 3.0 mA
			V_{OH}	VCC2 × 0.75	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	VCC2 × 0.125		I_{OL} = 3.0 mA
		1.70 V to 1.95 V	V_{OH}	1.4	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	0.45		I_{OL} = 2.0 mA

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Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (2 of 3)

Parameter		VCC/VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	MMC	2.70 V or above	V_{OH}	VCC × 0.75	—	—	V	I_{OH} = −0.1 mA (VCC = 2.7V)
			V_{OL}	—	—	VCC × 0.125		I_{OL} = 0.1 mA (VCC = 2.7V)
			V_{OH}	VCC2 × 0.75	—	—		I_{OH} = −0.1mA (VCC2 = 2.7V)
			V_{OL}	—	—	VCC2 × 0.125		I_{OL} = 0.1 mA (VCC2 = 2.7V)
		1.70 V to 1.95 V	V_{OH}	VCC − 0.45	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	0.45		I_{OL} = 2.0 mA
			V_{OH}	VCC2 − 0.45	—	—		I_{OH} = −2.0 mA
	Ports P205, P206, P402 to P404, P406 to P415, P511, P512, P709 to P715, PA09, PB01 (total 26 pins)*2	—	V_{OH}	VCC − 1.0	—	—		I_{OH} = −20 mA VCC = 3.3 V
		—	V_{OL}	—	—	1		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	1.68 V or above	V_{OH}	VCC − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
		1.65V or above	V_{OH}	VCC2 − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
			V_{OH}	AVCC0 − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	1.68 V or above	$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200	1.68 V or above		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	1.68 V or above	$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P200)	1.68 V or above		—	—	1.0		V_{in} = 0 V V_{in} = VCC
		1.65 V or above		—	—	1.0		V_{in} = 0 V V_{in} = VCC2, AVCC0
Input pull-up MOS current	Ports P0 to PB	2.70 V or above	I_p	−300	—	−10	µA	VCC, VCC2, AVCC0 = 2.7 to 3.6 V V_{in} = 0 V
		1.68 V or above		−300	—	−5	µA	VCC = 1.68 to 3.6 V V_{in} = 0 V
		1.65 V or above		−300	—	−5	µA	VCC2, AVCC0 = 1.65 to 3.6 V V_{in} = 0 V

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Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (3 of 3)

Parameter		VCC/VCC2/ AVCC0	Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up current serving as the SCL current source	I3C*3	3.0 V to 3.6 V	I_{cs}	3	—	12	mA	VCC = 3.0 to 3.6 V V_{in} = 0.3 × VCC to 0.7 × VCC
		1.68 V to 1.95 V						VCC = 1.68 to 1.95 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P014, P015	—	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Ports P814/ USB_DP, P815/ USB_DM	—		—	—	12		
	Ports P400, P401, P409, P410, P511, P512	—		—	—	10		
	Other input pins	—		—	—	8		

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. I3C_SCL0 (1 pin). This is the value when IIC high speed mode is selected.

2.2.5 Operating and Standby Current

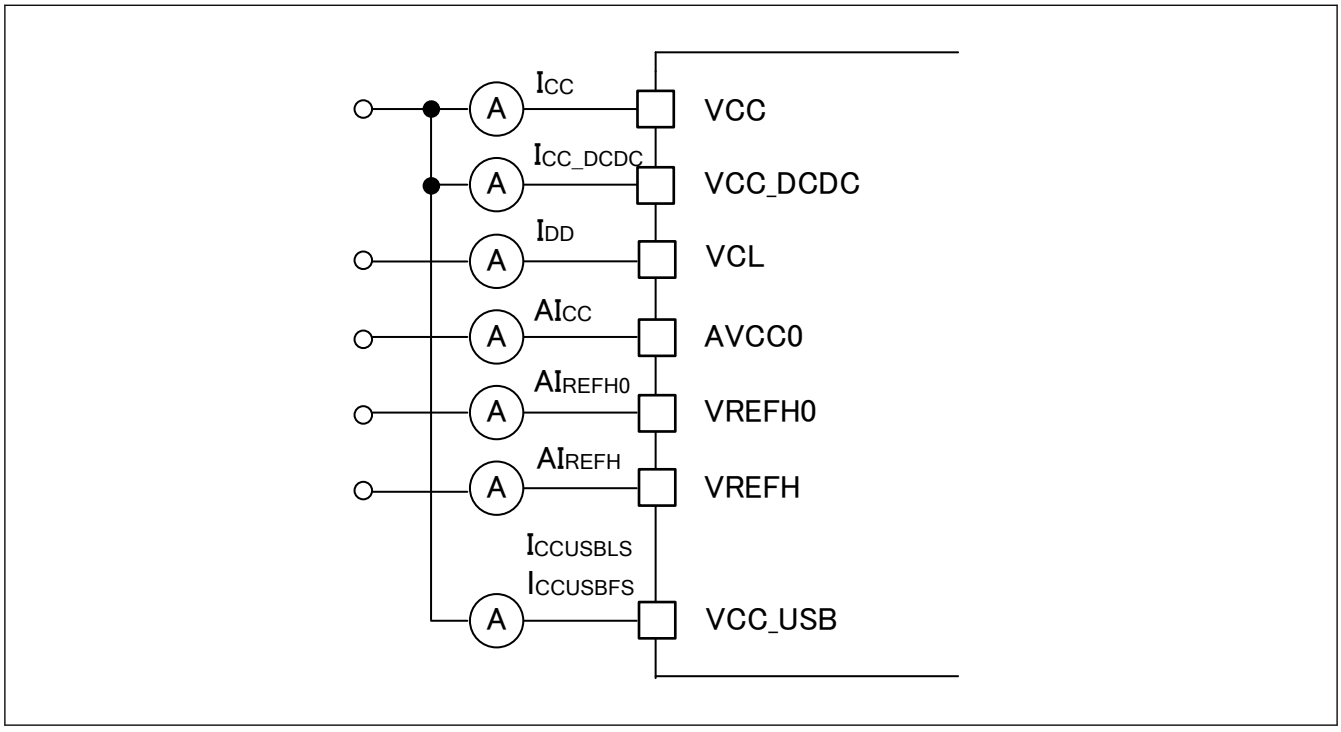


Figure 2.2 Consumption current measurement diagram

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Table 2.8 Current of high-speed mode, maximum condition (MVE and peripheral operation) (DCDC mode)

Parameter			Symbol	Typ	Max		Unit	Test conditions
					105℃	125℃		
Supply current *1*2	—		I_{CC}	2.8	7.05	7.19	mA	
	CPUCLK = 480 MHz	VCC_DCDC ≧ 2.5 V	I_{CC_DCDC}*5	159	289	—	mA	VCC_DCDC = 3.3 V CPUCLK = 480 MHz, ICLK = 240 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 240 MHz, FCLK = 60 MHz, BCLK = 120 MHz
			I_{DD}*3	374	595	—		
		VCC_DCDC < 2.5 V	I_{CC_DCDC}*5	292	320	—		VCC_DCDC = 1.8 V
			I_{DD}	374	400*4	—		
	CPUCLK = 400 MHz	VCC_DCDC ≧ 2.5 V	I_{CC_DCDC}*5	133	255	295	mA	VCC_DCDC = 3.3 V CPUCLK = 400 MHz, ICLK = 200 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 50 MHz, PCLKD = 100 MHz, PCLKE = 100 MHz, FCLK = 50 MHz, BCLK = 100 MHz
			I_{DD}*3	312	526	607		
		VCC_DCDC < 2.5 V	I_{CC_DCDC}*5	244	320	320		VCC_DCDC = 1.8 V
			I_{DD}	312	400*4	400*4		
	CPUCLK = 360 MHz	VCC_DCDC ≧ 2.5 V	I_{CC_DCDC}*5	122	243	283	mA	VCC_DCDC = 3.3 V CPUCLK = 360 MHz, ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 120 MHz, FCLK = 60 MHz, BCLK = 120 MHz
			I_{DD}*3	287	501	583		
		VCC_DCDC < 2.5 V	I_{CC_DCDC}*5	224	320	320		VCC_DCDC = 1.8 V
			I_{DD}	287	400*4	400*4		
	CPUCLK = 240 MHz	VCC_DCDC ≧ 2.5 V	I_{CC_DCDC}*5	95	210	249	mA	VCC_DCDC = 3.3 V CPUCLK = 240 MHz, ICLK = 240 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 120 MHz, FCLK = 60 MHz, BCLK = 120 MHz
			I_{DD}*3	224	432	514		
		VCC_DCDC < 2.5 V	I_{CC_DCDC}*5	175	320	320		VCC_DCDC = 1.8 V
			I_{DD}	224	400*4	400*4		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.68× f CPUCLK + 0.41 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.68 × f CPUCLK + 0.41 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 4. Do not actual consumption current during operation exceed the current value described here in VCC_DCDC < 2.5V.
Note 5. Typical DCDC efficiency is applied.

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Table 2.9 Current of high-speed mode, maximum condition (MVE and peripheral operation) (External VDD mode)

Parameter	CPUCLK Frequency	Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1 *2	—	I_{CC}	2.8	7.05	7.19	mA	
	CPUCLK = 480 MHz	I_{DD}*3	374	595	—	mA	CPUCLK = 480 MHz, ICLK = 240 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 240 MHz, FCLK = 60 MHz, BCLK = 120 MHz
	CPUCLK = 400 MHz	I_{DD}*3	312	526	607	mA	CPUCLK = 400 MHz, ICLK = 200 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 50 MHz, PCLKD = 100 MHz, PCLKE = 100 MHz, FCLK = 50 MHz, BCLK = 100 MHz
	CPUCLK = 360 MHz	I_{DD}*3	287	501	583	mA	CPUCLK = 360 MHz, ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 120 MHz, FCLK = 60 MHz, BCLK = 120 MHz
	CPUCLK = 240 MHz	I_{DD}*3	224	432	514	mA	CPUCLK = 240 MHz, ICLK = 240 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 120 MHz, PCLKE = 120 MHz, FCLK = 60 MHz, BCLK = 120 MHz

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.68 × f CPUCLK + 0.41 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.68 × f CPUCLK + 0.41 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)

Table 2.10 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock ON (DCDC mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*2	CPUCLK = 480 MHz	I_{CC_DCDC}*4	154	271	—	mA	VCC_DCDC = 3.3 V *5
		I_{DD}*3	362	559	—		
	CPUCLK = 400 MHz	I_{CC_DCDC}*4	130	242	282		
		I_{DD}*3	305	497	580		
	CPUCLK = 360 MHz	I_{CC_DCDC}*4	119	228	268		
		I_{DD}*3	279	469	552		
	CPUCLK = 240 MHz	I_{CC_DCDC}*4	92	194	234		
		I_{DD}*3	215	399	483		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.67 × f CPUCLK + 0.29 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.67 × f CPUCLK + 0.29 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 4. Typical DCDC efficiency is applied.
Note 5. Same frequency condition is applied as in the maximum condition.

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Table 2.11 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock ON (External VDD mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*2	CPUCLK = 480 MHz	I_{DD}*3	362	559	—	mA	*4
	CPUCLK = 400 MHz	I_{DD}*3	305	497	580		
	CPUCLK = 360 MHz	I_{DD}*3	279	469	552		
	CPUCLK = 240 MHz	I_{DD}*3	215	399	483		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.67 × f CPUCLK + 0.29 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.67 × f CPUCLK + 0.29 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

Table 2.12 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (DCDC mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*2	CPUCLK = 480 MHz	I_{CC_DCDC}*4	146	260	—	mA	VCC_DCDC = 3.3 V *5
		I_{DD}*3	342	536	—		
	CPUCLK = 400 MHz	I_{CC_DCDC}*4	123	232	272		
		I_{DD}*3	289	478	560		
	CPUCLK = 360 MHz	I_{CC_DCDC}*4	111	216	256		
		I_{DD}*3	261	445	528		
	CPUCLK = 240 MHz	I_{CC_DCDC}*4	83	181	222		
		I_{DD}*3	194	373	457		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.68 × f CPUCLK + 0.17 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.68 × f CPUCLK + 0.17 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 4. Typical DCDC efficiency is applied.
Note 5. Same frequency condition is applied as in the maximum condition.

Table 2.13 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (External VDD mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*2	CPUCLK = 480 MHz	I_{DD}*3	342	536	—	mA	*4
	CPUCLK = 400 MHz	I_{DD}*3	289	478	560		
	CPUCLK = 360 MHz	I_{DD}*3	261	445	528		
	CPUCLK = 240 MHz	I_{DD}*3	194	373	457		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Max. (105℃) = 0.68 × f CPUCLK + 0.17 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.68 × f CPUCLK + 0.17 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

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Table 2.14 Current of high-speed mode, CPU Sleep mode (DCDC mode and External VDD mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*3*4	CPUCLK = 240 MHz	I_{DD}*2	29	216	310	mA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (CPUCLK and ICLK) as follows.
I_{DD} Typ. (25℃) = 0.063 × fCPUCLK + 0.13 × fICLK + 17.6 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (105℃) = 0.063 × fCPUCLK + 0.13 × fICLK + 175 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.063 × fCPUCLK + 0.13 × fICLK + 253 (unit : mA, fCPUCLK and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. ICLK, FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD and PCLKE are set to divided by 64.

Table 2.15 Current of high-speed mode, CPU Deep Sleep mode (DCDC mode and External VDD mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1*3*4	CPUCLK = 240 MHz	I_{DD}*2	12	85	112	mA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (ICLK) as follows.
I_{DD} Typ. (25℃) = 0.13 × fICLK + 5 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (105℃) = 0.13 × fICLK + 69 (unit : mA, fCPUCLK and fICLK are MHz)
I_{DD} Max. (125℃) = 0.13 × fICLK + 97 (unit : mA, fCPUCLK and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. ICLK, FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD and PCLKE are set to divided by 64.

Table 2.16 Increase during BGO operation (DCDC mode and External VDD mode)

Parameter		Symbol	Typ	Max		Unit	Test conditions
				105℃	125℃		
Supply current*1	Data flash P/E	I_{CC}	6	—	—	mA	—
	Code flash P/E		8	—	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Table 2.17 Current of Low-speed mode (DCDC mode)

Parameter	Symbol	Typ	Max		Unit	Test conditions
			105℃	125℃		
Supply current*1*2*3	I_{DD}	14.5	—	—	mA	CPUCLK = ICLK = 1MHz

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD and PCLKE are set to divided by 64 (15.6 kHz).

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Table 2.18 Standby current (DCDC mode)

Parameter				Symbol	Typ	Max 125℃	Unit	Test conditions
Supply current*1	Software Standby mode*2			I_{CC}	0.02	0.94	mA	—
	Data of SRAM and TCM is retained			I_{CC_DCDC}	0.88	28.29		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 6) PDRAMSCR1.RKEEP0 = 1
	Data of SRAM and TCM is not retained			I_{CC_DCDC}	0.83	26.64		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 6) PDRAMSCR1.RKEEP0 = 0
	Deep Software Standby mode 1			I_{CC}	5.21	148	µA	—
				I_{CC_DCDC}	0.57	5.50		
		Increase when the function is activated	Data of Standby SRAM is retained	I_{CC}	0.12	2.60		—
			PVD0, PVD1,PVD2		See Table 2.20			—
			When the LOCO is in use		3.10	—		—
			Crystal oscillator		See Table 2.21			—
			IWDT and ULPT(all units) are operating		0.07	—		—
	Deep Software Standby mode 2			I_{CC}	1.68	43.99		—
				I_{CC_DCDC}	0.57	5.50		
		Increase when the function is activated	PVD0, PVD1,PVD2	I_{CC}	See Table 2.20			—
			Crystal oscillator		See Table 2.21			—
	Deep Software Standby mode 3			I_{CC}	0.99	42.90		—
				I_{CC_DCDC}	0.57	5.50		
		Increase when the function is activated	Crystal oscillator	I_{CC}	See Table 2.21			—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. When an external clock is used, EXTAL pin is pull-up or pull-down. In case clock is toggled, software standby mode current consumption is increased by 130µA at 48MHz under typical conditions.

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Table 2.19 Coremark and normal mode current (DCDC and External power supply mode)

Parameter			Symbol	Typ	Max	Unit	Test conditions
Supply current*1*2	Coremark	Cache on	I_{DD}	318	—	µA/MHz	CPUCLK = 480 MHz ICLK = 240 MHz PCLKA = 7.5 MHz PCLKB = 7.5 MHz PCLKC = 7.5 MHz PCLKD = 7.5 MHz PCLKE = 7.5 MHz FCLK = 7.5 MHz BCLK = 7.5 MHz
		Cache off, executing from ITCM		281	—		
		Cache off, executing from SRAM		178	—		
		Cache off, executing from flash		169	—		
	Normal mode	All peripheral disabled, Cache on, while (1) code		223	—		
		All peripheral disabled, Cache off, while (1) code executing from flash		138	—		
	Coremark	Cache off, executing from flash		165	—	µA/MHz	CPUCLK = 360 MHz ICLK = 120 MHz PCLKA = 30 MHz PCLKB = 30 MHz PCLKC = 30 MHz PCLKD = 30 MHz PCLKE = 30 MHz FCLK = 30 MHz BCLK = 30 MHz
	Normal mode	All peripheral disabled, Cache off, while (1) code executing from flash		137	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Table 2.20 Increase when the PVD0, PVD1, or PVD2 is enabled in Deep Software Standby mode 1 and 2.

Parameter		Symbol	Typ	Max 125℃	Unit	Test conditions
Supply current	Common circuit when enabling PVDn (n = 0 to 2) in Deep Software Standby mode 1	I_{CC}	4.51	—	µA	—
	Common circuit when enabling PVDn (n = 0 to 2) in Deep Software Standby mode 2		4.97	—		—
	PVD0 enabled with OFS1(_SEC).PVDLPSEL = 1		2.16	—		—
	PVD1 enabled		2.16	—		—
	PVD2 enabled		2.16	—		—

Table 2.21 Increase when the sub-clock oscillator is enabled in Deep Software Standby mode 1, 2 and 3.

Parameter			Symbol	Typ	Max 125℃	Unit	Test conditions
Supply current	When a crystal oscillator is in use	Low Power mode 3	I_{CC}	0.22	—	µA	—
		Low Power mode 2		0.27	—		—
		Low Power mode 1		0.34	—		—
		Standard mode		0.67	—		—

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Table 2.22 Inrush current

Parameter				Symbol	Typ	Max 125℃	Unit	Test conditions
Supply current	Inrush current on returning from deep software standby mode	Inrush current of VCC_DCDC*1	DPSBYCR.DCSSMODE = 0	I_{RUSH}	—	630	mA	—
			DPSBYCR.DCSSMODE = 1		—	1020		—

Note 1. Reference value

Table 2.23 Operating current (Analog)

Parameter				Symbol	Typ	Max 125 ℃	Unit	Test conditions
Supply current*1	Oscillator	Main clock oscillator		I_{CC}	0.48	—	mA	MOMCR.MODRV0[2:0] = 000b
					0.58	—	mA	MOMCR.MODRV0[2:0] = 011b
					0.90	—	mA	MOMCR.MODRV0[2:0] = 101b
	Analog power supply current	During 12-bit A/D conversion		AI_{CC}	0.8	1.1	mA	—
		During 12-bit A/D conversion with S/H amp			2.3	3.3	mA	—
		ACMPHS(1unit)			100	150	μA	—
		Temperature sensor			0.1	0.2	mA	—
		During D/A conversion(per unit)	Without AMP output		0.1	0.2	mA	—
			With AMP output		0.8	1.6	mA	—
		Waiting for A/D, D/A conversion (all units)			0.9	1.6	mA	—
		ADC12, DAC12 in standby modes (all units)*2			2	8	μA	—
	Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)		AI_{REFH0}	70	120	μA	—
		Waiting for 12-bit A/D conversion (unit 0)			0.07	0.5	μA	—
		ADC12 in standby modes (unit 0)			0.07	0.5	μA	—
	Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)		AI_{REFH}	70	120	μA	—
		During D/A conversion(per unit)	Without AMP output		0.1	0.4	mA	—
			With AMP output		0.1	0.4	mA	—
		Waiting for 12-bit A/D (unit 1), D/A (all units) conversion			0.07	0.8	μA	—
		ADC12 in standby modes (unit 1)			0.07	0.8	μA	—
	USB operating current	Low speed	USBFS	$I_{CCUSBLS}$	3.5	6.5	μA	VCC_USB
		Full speed	USBFS	$I_{CCUSBFS}$	4.0	10.0	mA	VCC_USB

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D converter 1 module stop bit) are in the module-stop state.

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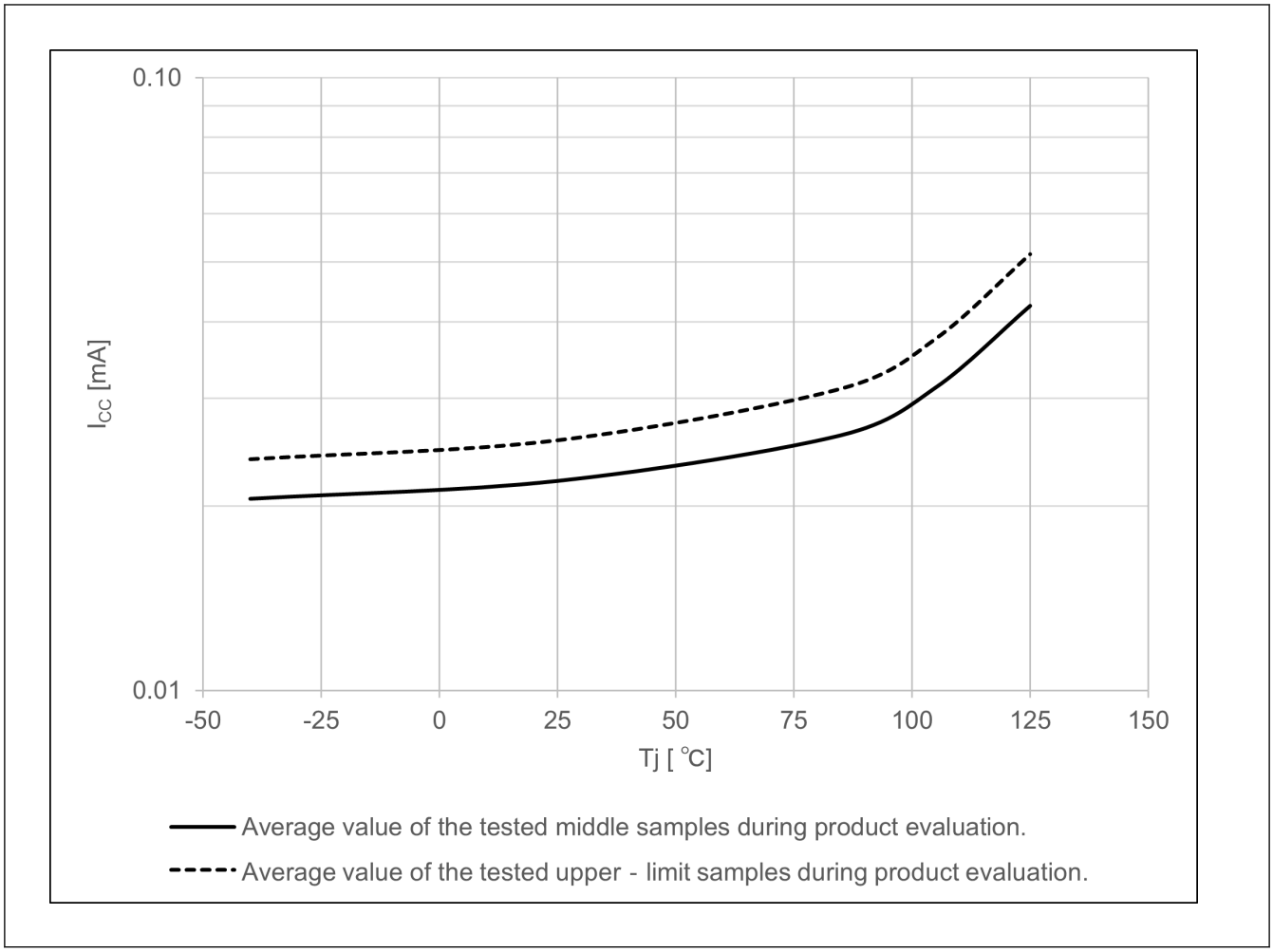


Figure 2.3 Temperature dependency in Software Standby mode (I_{CC}) (reference data)

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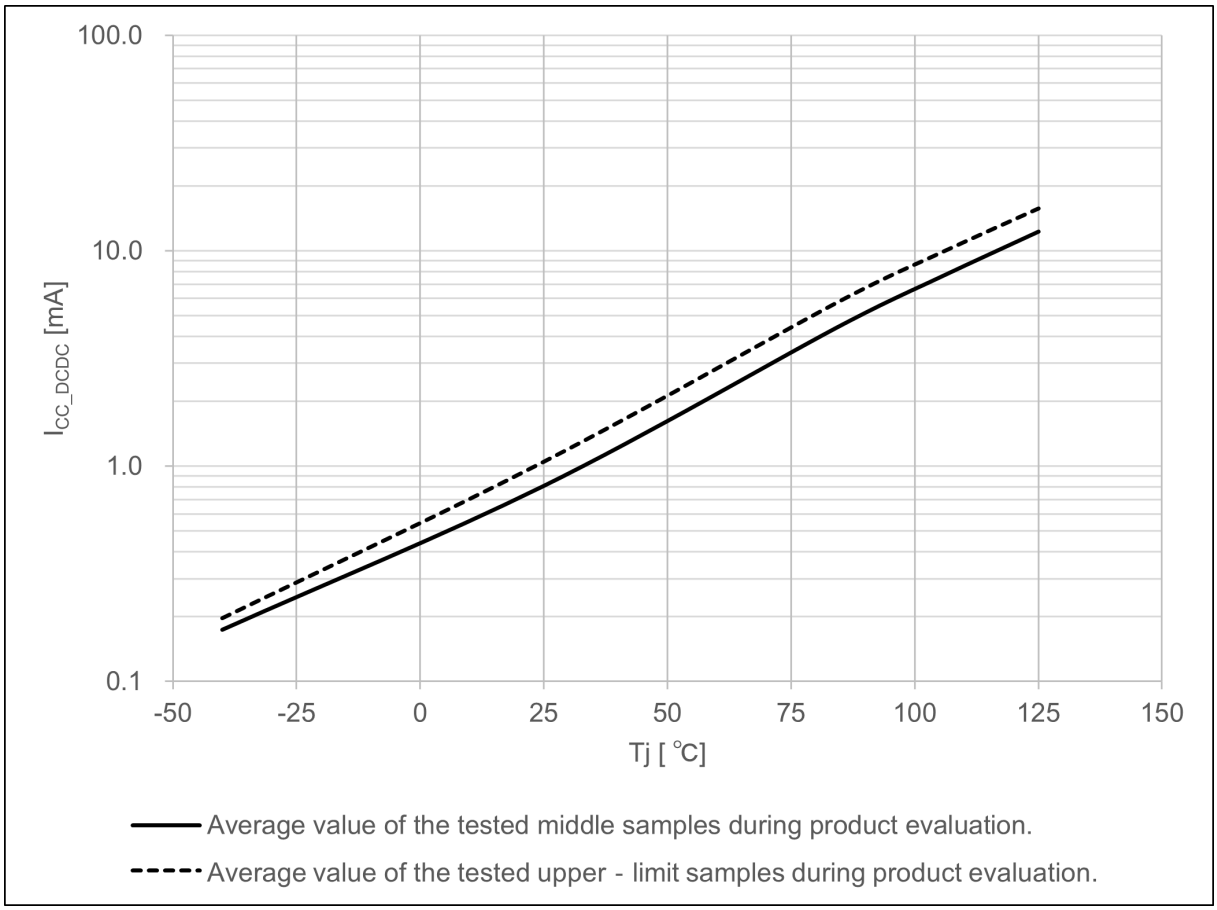


Figure 2.4 Temperature dependency in Software Standby mode (I_{CC_DCDC}) (reference data)

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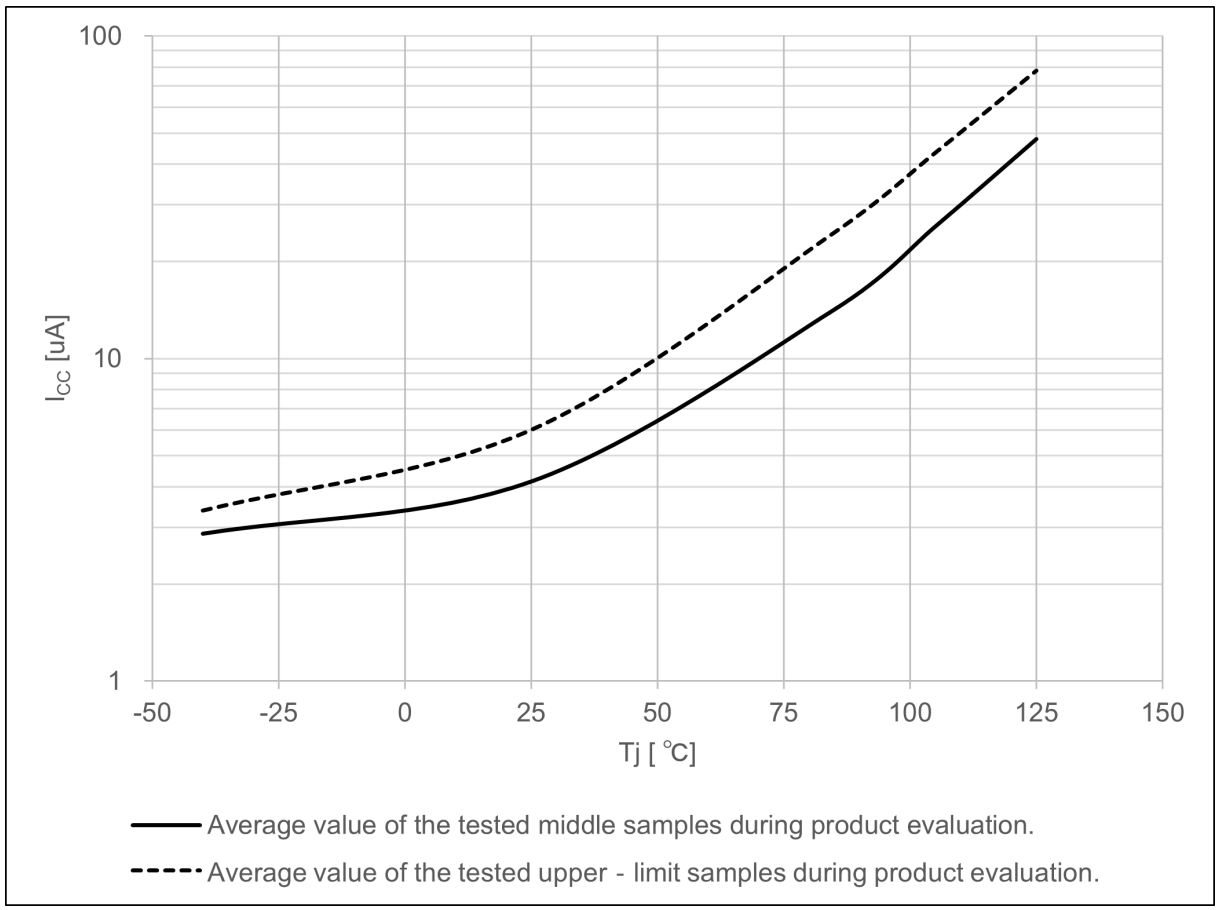


Figure 2.5 Temperature dependency in Deep Software Standby mode 1 (reference data)

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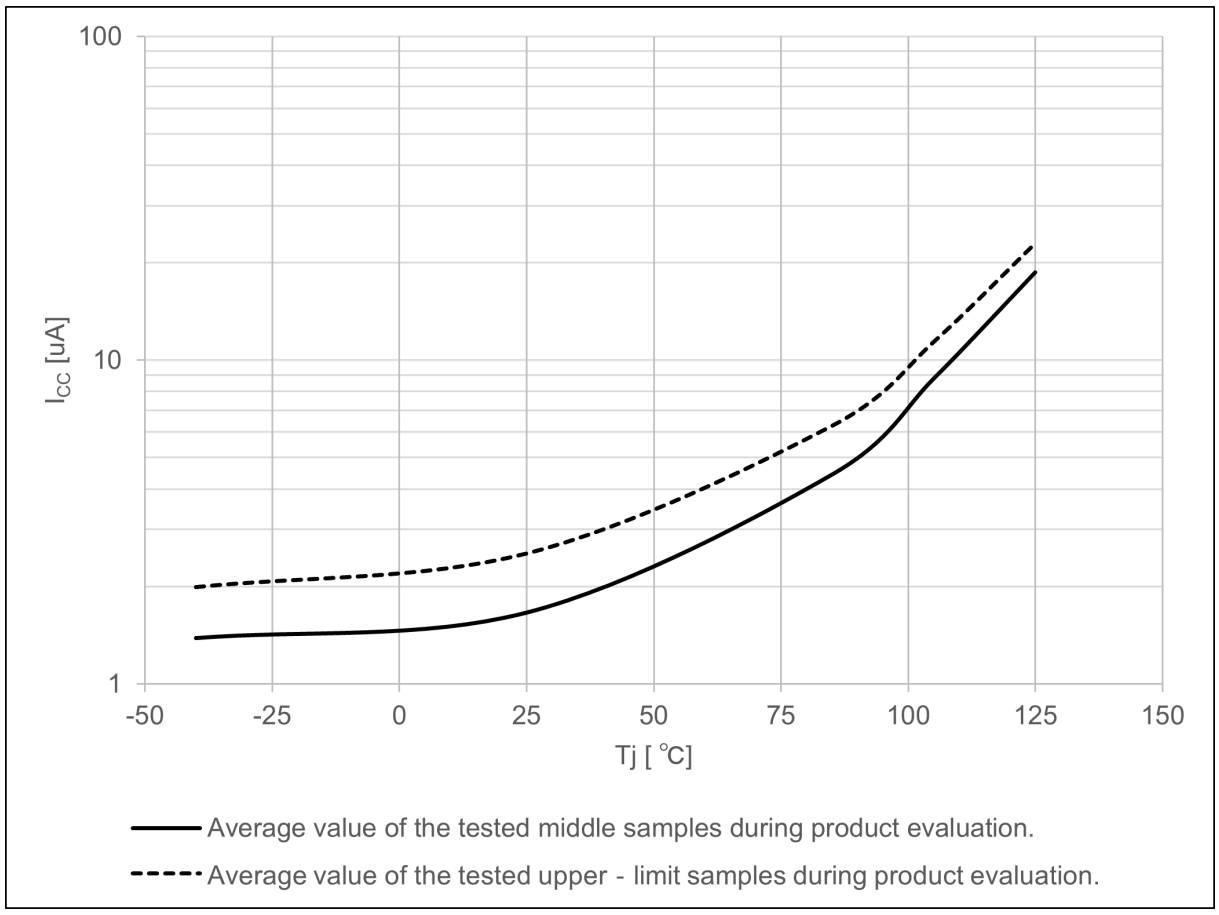


Figure 2.6 Temperature dependency in Deep Software Standby mode 2 (reference data)

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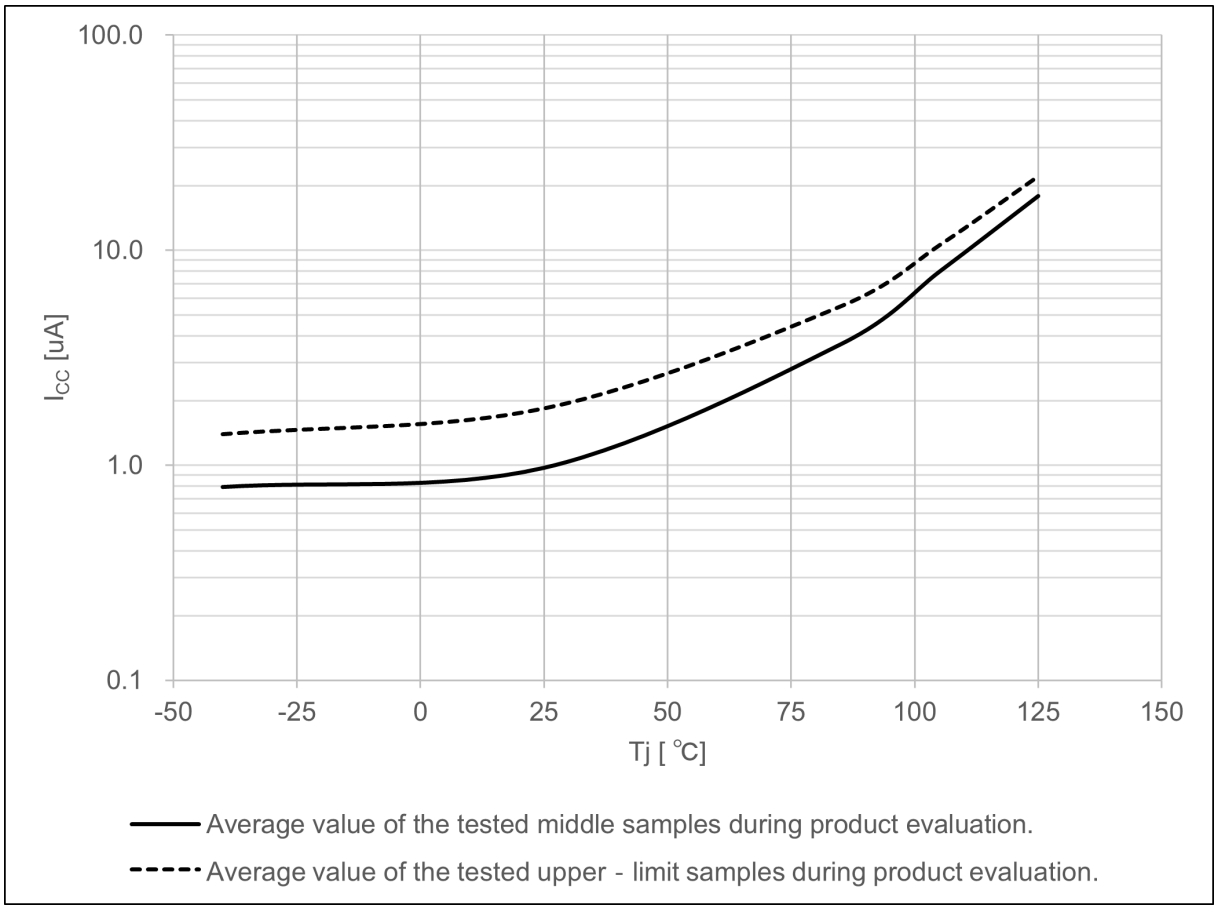


Figure 2.7 Temperature dependency in Deep Software Standby mode 3 (reference data)

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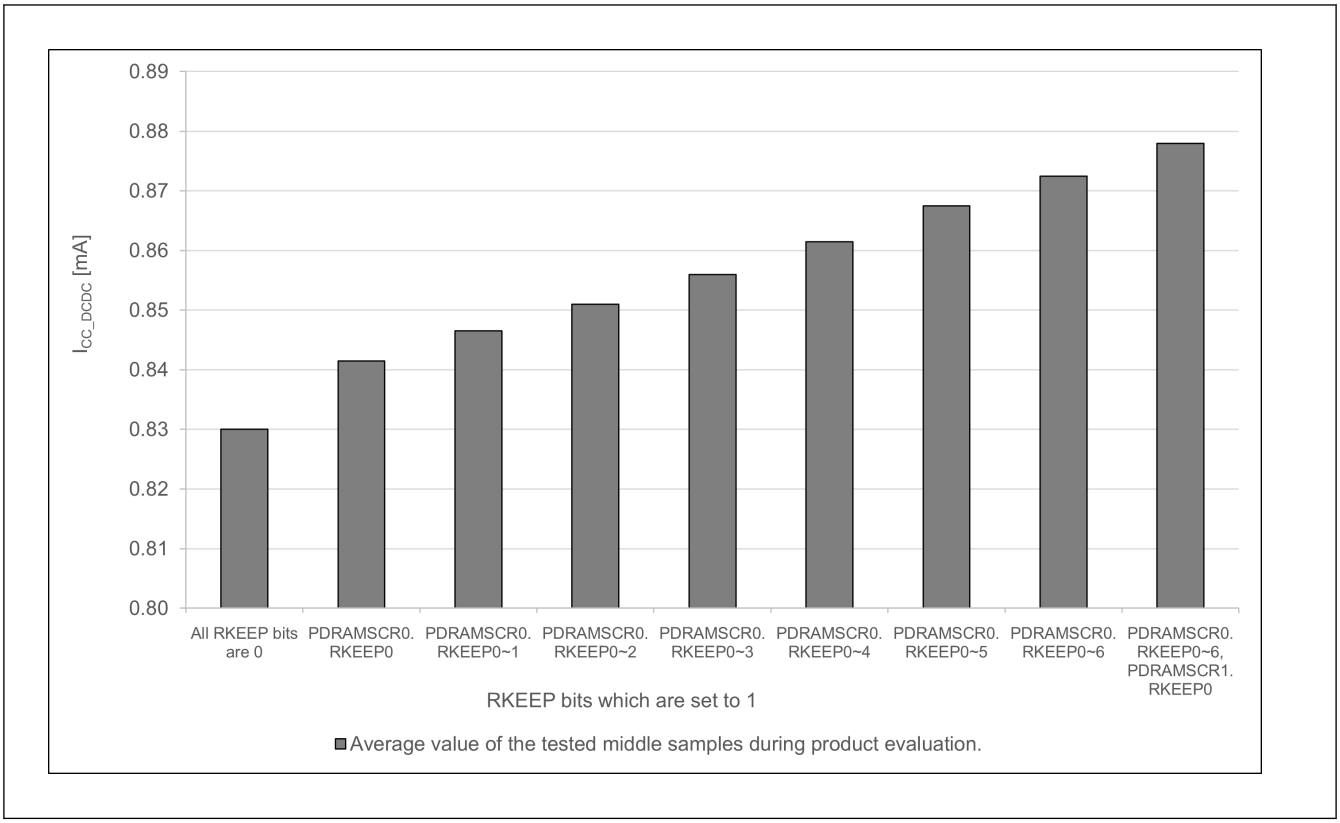


Figure 2.8 Software Standby current per SRAM state (reference data)

The more practical I_{CC_DCDC} value can be obtained with the following formula.

$I_{CC_DCDC} = I_{DD} \times (VCL \div VCC) \div efficiency$

Where: VCL and VCC are the voltage of VCL pin and VCC pin respectively, and efficiency is shown in the following figures.

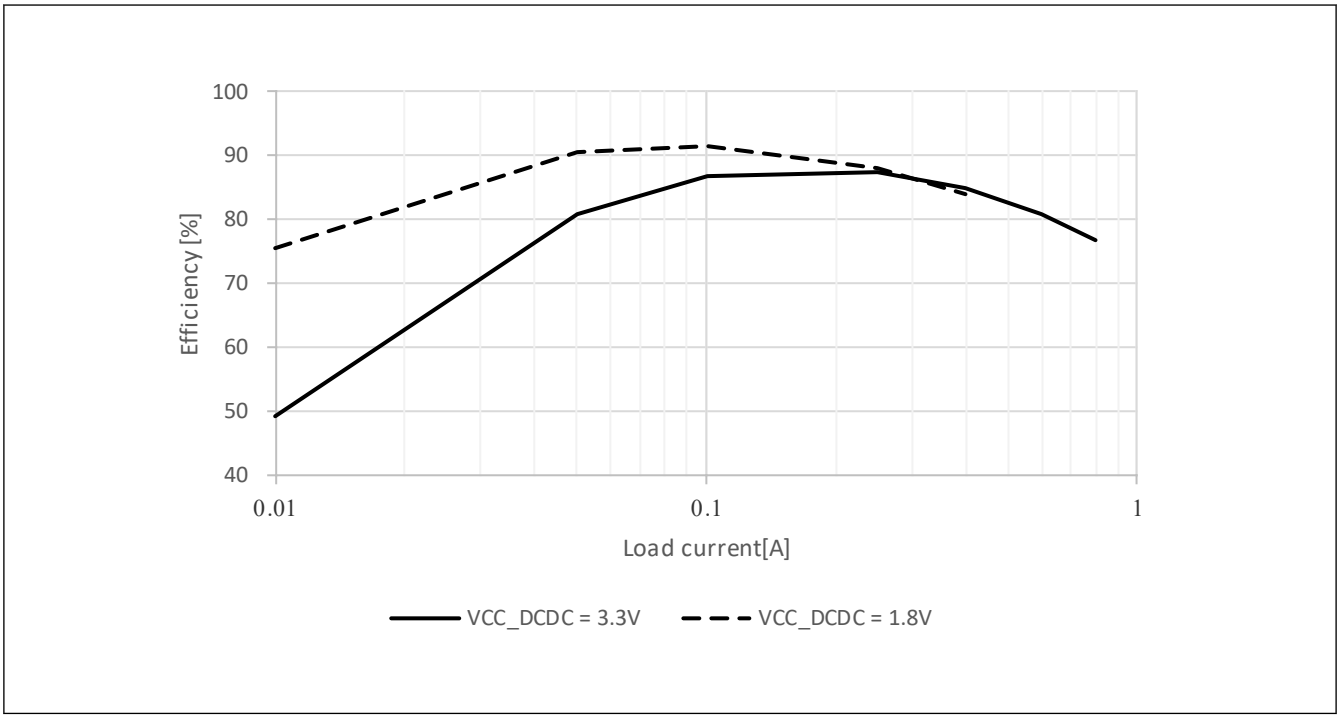


Figure 2.9 Typical DCDC efficiency (%) vs load current (A) in High-speed mode , Tj = 25°C

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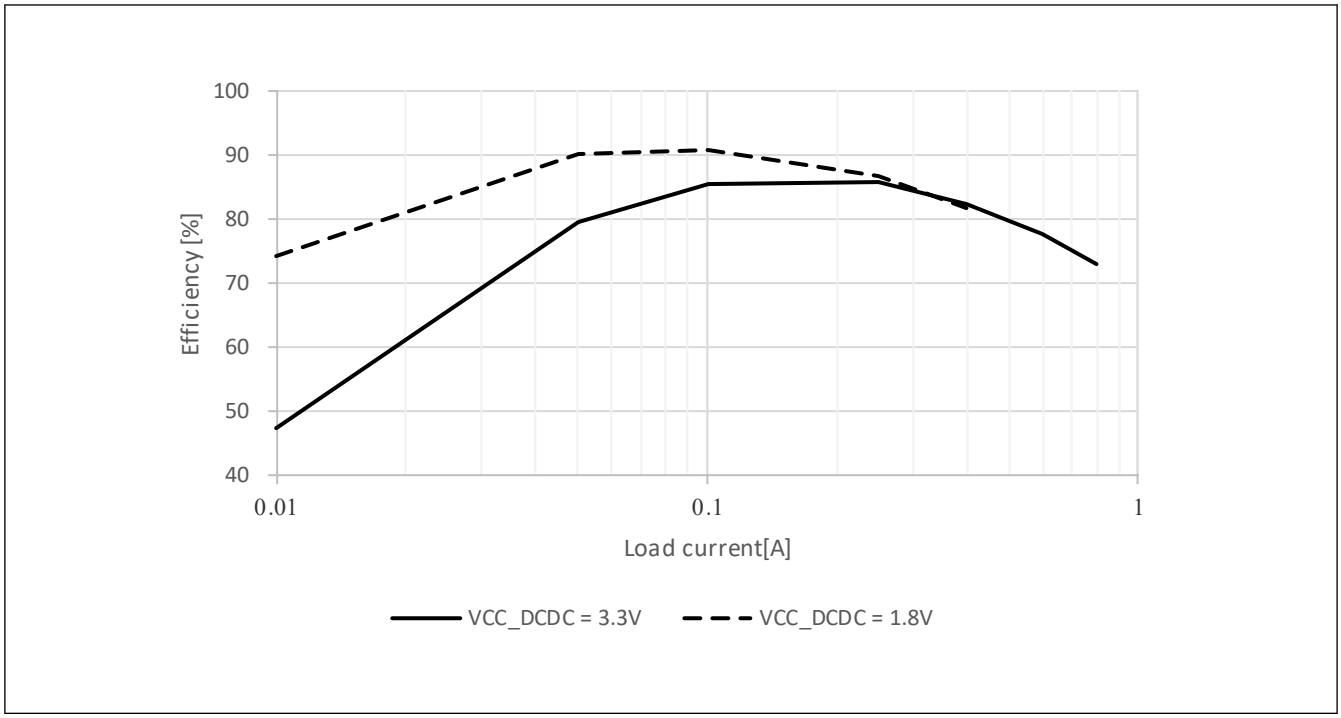


Figure 2.10 Typical DCDC efficiency (%) vs load current (A) in High-speed mode , Tj = 125℃

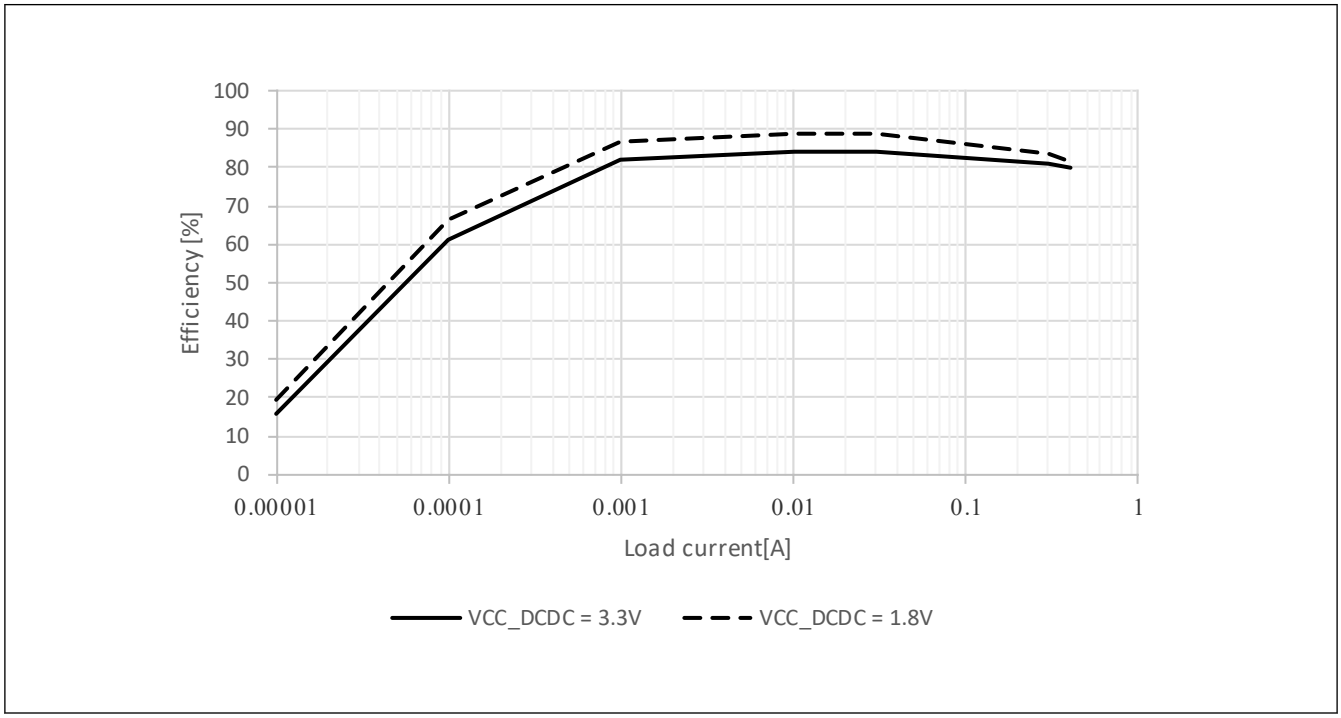


Figure 2.11 Typical DCDC efficiency (%) vs load current (A) in Low-speed mode and Software Standby mode, Tj = 25℃

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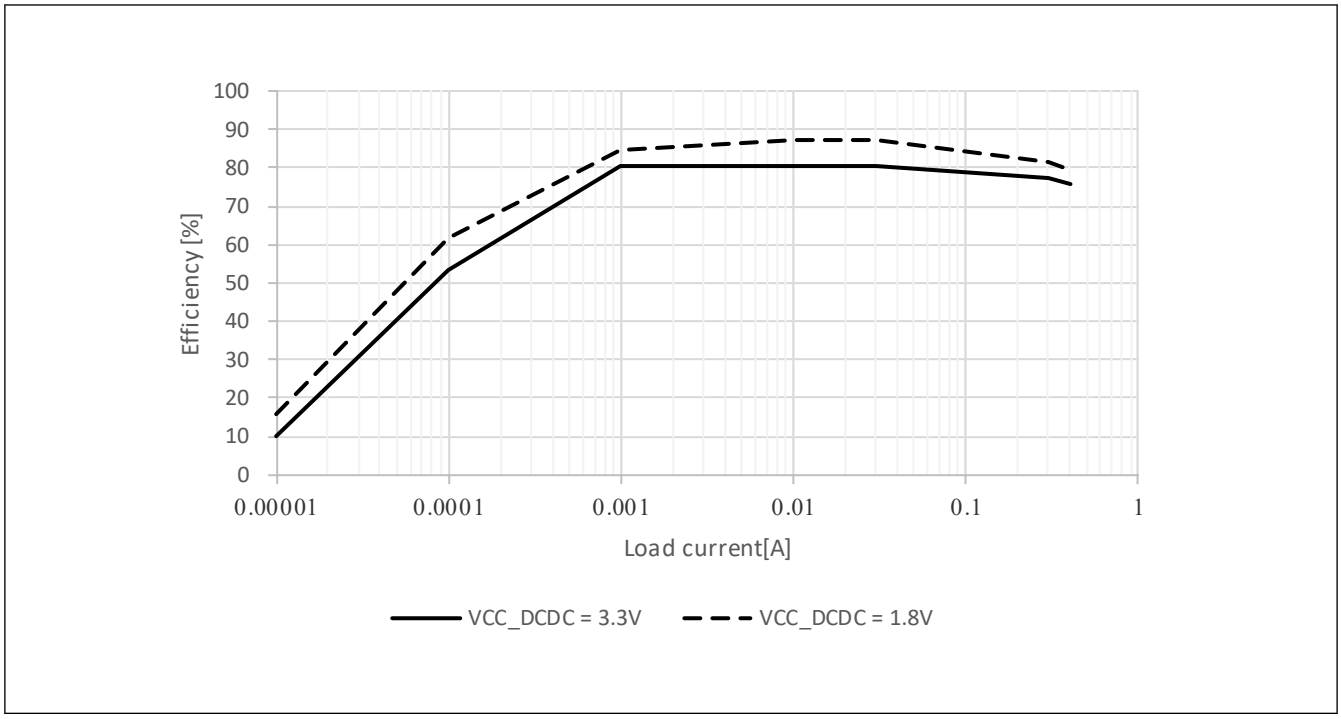


Figure 2.12 Typical DCDC efficiency (%) vs load current (A) in Low-speed mode and Software Standby mode, Tj = 125°C

Note: DCDC efficiency is obtained based on the VCC_DCDC current.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.24 VCC rise and fall gradient characteristics at power on/off

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient at power on*1	SrVCC	0.0084	—	20	ms/V	—
VCC falling gradient at power off*1	SfVCC1	0.0084	—	—	ms/V	—

Note 1. In case the VCC voltage crosses V_{POR1}.

Table 2.25 VCC ripple frequency and gradient characteristics during operation

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.68 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10.0	kHz	Figure 2.13 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1.0	MHz	Figure 2.13 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10.0	MHz	Figure 2.13 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC*1	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

Note 1. In case the VCC voltage does not cross V_{POR1}.

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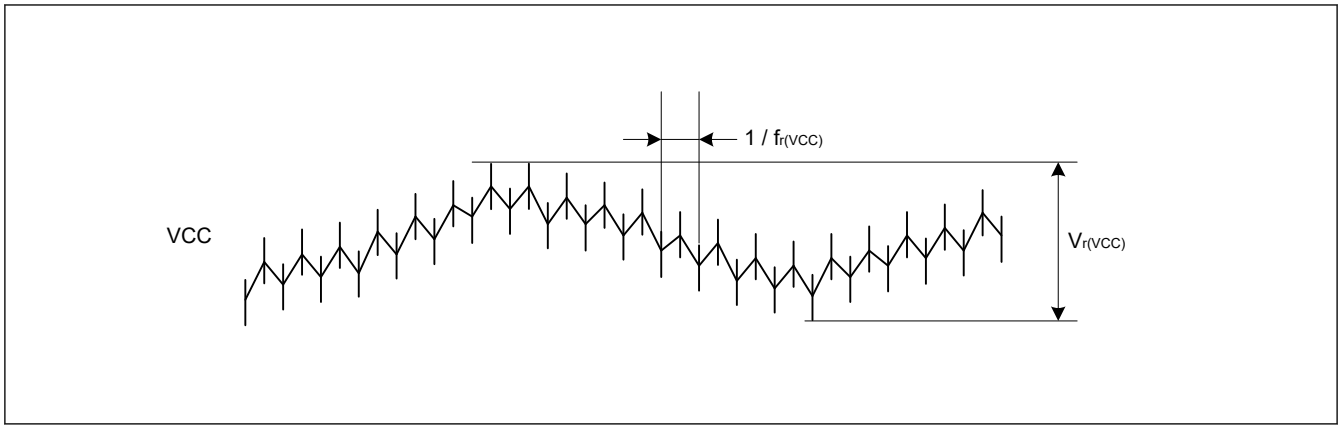


Figure 2.13 Ripple waveform

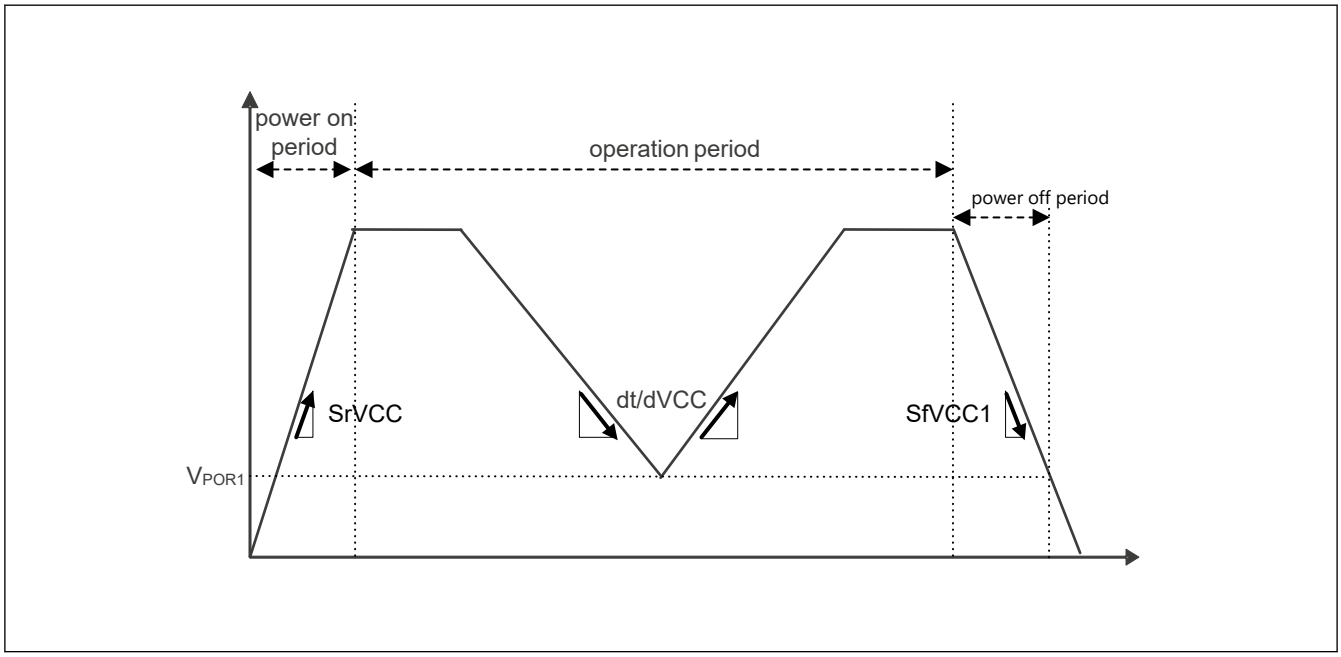


Figure 2.14 VCC rising and falling waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of “Junction”-to-“Ambient” (°C/W)
  - Ψjt : Thermal Resistance of “Junction”-to-“Top Center Case” (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance

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– C_{load}: Output capacitance

Regarding θja and Ψjt, see Table 2.26.

Table 2.26 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	100-pin LQFP (PLQP0100KP-A)	θja	32.9	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		31.7		
	176-pin LQFP (PLQP0176KJ-A)		32.0		
	224-pin BGA (PLBG0224GD-A)		21.5		JESD 51-2 and 51-9 compliant
	100-pin LQFP (PLQP0100KP-A)	Ψjt	0.42	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		0.40		
	176-pin LQFP (PLQP0176KJ-A)		0.42		
	224-pin BGA (PLBG0224GD-A)		0.24		JESD 51-2 and 51-9 compliant

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.2.7.1 Calculation guide of maximum current

Table 2.27 Power consumption of each unit (1 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]	Condition
Leakage current	Analog	Regulator and Leak*1	Tj = 95°C	I_{CC}	—	—	0.54	—
			Tj = 105°C		—	—	0.64	
			Tj = 115°C		—	—	0.75	
			Tj = 125°C		—	—	0.85	
			Tj = 95°C	I_{CC_DCDC}	—	—	62	VCC_DCDC = 3.3V, High speed mode
			Tj = 105°C		—	—	75	
			Tj = 115°C		—	—	91	
			Tj = 125°C		—	—	108	
			Tj = 95°C		—	—	112	VCC_DCDC = 1.8V, High speed mode
			Tj = 105°C		—	—	134	
			Tj = 115°C		—	—	164	
			Tj = 125°C		—	—	193	
			Tj = 95°C	I_{DD}	—	—	146	—
			Tj = 105°C		—	—	175	
			Tj = 115°C		—	—	214	
			Tj = 125°C		—	—	253	

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Table 2.27 Power consumption of each unit (2 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]	Condition
Dynamic current	CPU	Operation with Cache	CoreMark	I_{DD}	480	307	147	CPUCLK = 480MHz
	Peripheral Unit	Timer	GPT16 (6ch)*2		120	16.988	2.039	—
			GPT32 (8ch)*2		120	20.279	2.433	
			POEG (4 Groups)*2		60	1.363	0.082	
			AGT (2ch)*2		60	2.233	0.134	
			ULPT (2ch)*2		60	0.350	0.021	
			WDT		60	0.775	0.047	
			IWDT		60	0.100	0.006	
Dynamic current	Peripheral Unit	Communication interfaces	ETHERC	I_{DD}	120	8.149	0.978	—
			USBFS		60	8.713	0.523	
			SCI (6ch)*2		120	22.717	2.726	
			IIC (2ch)*2		60	2.867	0.172	
			I3C		120	15.274	1.833	
			CANFD (2ch)*2		120	9.050	1.086	
			SPI (2ch)*2		120	7.950	0.954	
			SDHI (2ch)*2		60	16.742	1.005	
		Analog	ADC (2Units)*2		120	3.961	0.475	—
			DAC12 (2ch)*2		120	1.079	0.129	
			TSN		60	0.092	0.005	
			ACMPHS (2ch)*2		60	0.083	0.005	
		Event link	ELC		60	1.670	0.100	—
		Security	RSIP-E51A		120	311.301	37.4	—
		Data processing	CRC		120	4.372	0.525	—
			DOC		120	0.427	0.051	
		System	CAC		60	0.738	0.044	—
		DMA	DMAC (per 1ch)		240	9.012	2.163	—
			DTC		240	11.175	2.682	
	FSBL operation				240	—	93.4	—
					120	—	72.9	—

Note 1. Regulator and Leak are Internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Tj.
Note 2. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.28 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode.
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
ULPT	ULPT is operating with LOCO.

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Table 2.28 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
ETHERC	Operation modes is set to full-duplex mode. ETHERC is operating using Reduced Media Independent Interface (RMII).
USBFS	Transfer types is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps).
SCI	SCI is transmitting data in clock synchronous mode.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
I3C	Communication format is set to I3C SDR format. I3C is transmitting data in master mode (12.5MHz).
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 32-bit width data.
SDHI	Transfer bus mode is set to 8-bit wide bus mode. SDHI is issuing CMD24 (single-block write).
ADC	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
TSN	TSN is operating.
ACMPHS	ACMPHS is operating.
ELC	Only clear module stop bit.
RSIP-E51A	RSIP is doing self-test operation.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data comparison mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.2.7.2 Example of Tj calculation

Assumption :

- Package 224-pin BGA : θja = 21.5 °C/W
- Ta = 80 °C
- $I_{CC} + I_{CC_DCDC}$ = 240 mA
- VCC = 3.5 V (VCC = VCC2 = AVCC0 = VCC_USB)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 32 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 32 pins, Output frequency = 10 MHz

Static current of IO = Σ (VOL × IOL) / Voltage + Σ ((VCC - VOH) × IOH) / Voltage

= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V

= 45.7 mA + 1.71 mA + 1.71 mA

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= 49.1 mA

Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V

= 42.6 mA

Total power consumption = Voltage × (Static current + Dynamic current)

= (240 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V

= 1161 mW (1.161 W)

Tj = Ta + θja × Total power consumption

= 80 °C + 21.5 °C/W × 1.161W

= 105.0 °C

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2.3 AC Characteristics

2.3.1 Frequency

Table 2.29 Operation frequency value in high-speed mode

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	CPU clock (CPUCLK)	DCDC, BGA package, Tj ≤ 105℃*3	f	—	—	480	MHz
		DCDC, BGA package, Tj ≤ 125℃*3		—	—	400	
		External VDD, BGA package, Tj ≤ 105℃		—	—	480	
		External VDD, BGA package, Tj ≤ 125℃		—	—	400	
		DCDC, 176-pin and 144-pin LQFP package, Tj ≤ 125℃*3		—	—	400	
		External VDD, 176-pin and 144-pin LQFP package, Tj ≤ 125℃		—	—	400	
		DCDC, 100-pin LQFP package, Tj ≤ 105℃*3		—	—	360	
		DCDC, 100-pin LQFP package, Tj ≤ 125℃*3		—	—	240	
		External VDD, 100-pin LQFP package, Tj ≤ 105℃		—	—	360	
		External VDD, 100-pin LQFP package, Tj ≤ 125℃		—	—	240	
	System clock (ICLK)			—	—	240	
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—*2	—	60	
	Peripheral module clock (PCLKD)			—	—	120	
	Peripheral module clock (PCLKE)			—	—	240	
	Flash interface clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	VCC ≥ 2.7 V		—	—	120	
		VCC ≥ 1.68 V		—	—	60	
	EBCLK pin output	VCC ≥ 2.7 V		—	—	60	
		VCC ≥ 1.68 V		—	—	30	
	SDCLK pin output	VCC ≥ 3.0 V		—	—	120	
	SCI clock (SCICLK)			—	—	120	
	SPI clock (SPICLK)			—	—	120	
	CANFD core clock (CANFDCLK)			—	—	80	
	USB clock (USBCLK)			—	—	48	
	I3C clock (I3CCLK)			—	—	200	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.
Note 3. When DCDC is used with VCC_DCDC < 2.5V, I_{DD} current must be less than the value specified in operating current. Please see Table 2.8.

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Table 2.30 Operation frequency value in low-speed mode

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	CPU clock (CPUCLK)		f	—	—	1	MHz
	System clock (ICLK)			—	—	1	
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)			—*2	—	1	
	Peripheral module clock (PCLKD)			—	—	1	
	Peripheral module clock (PCLKE)			—	—	1	
	Flash interface clock (FCLK)			—*1	—	1	
	External bus clock (BCLK)			—	—	1	
	EBCLK pin output			—	—	1	
	SDCLK pin output	VCC ≥ 3.0 V		—	—	1	
	SCI clock (SCICLK)			—	—	1	
	SPI clock (SPICLK)			—	—	1	
	CANFD core clock (CANFDCLK)			—	—	1	
	USB clock (USBCLK)			—	—	1	
	I3C clock (I3CCLK)			—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

2.3.2 Clock Timing

Table 2.31 Clock timing except for sub-clock oscillator (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	VCC = 2.70 V or above	t_{Bcyc}	16.6	—	—	ns	Figure 2.15
	VCC = 1.68 V or above		33.3	—	—		
EBCLK pin output high pulse width	VCC = 2.70 V or above	t_{CH}	3.3	—	—	ns	
	VCC = 1.68 V or above		9.6	—	—		
EBCLK pin output low pulse width	VCC = 2.70 V or above	t_{CL}	3.3	—	—	ns	
	VCC = 1.68 V or above		9.6	—	—		
EBCLK pin output rise time	VCC = 2.70 V or above	t_{Cr}	—	—	5.0	ns	
	VCC = 1.68 V or above		—	—	7.0		
EBCLK pin output fall time	VCC = 2.70 V or above	t_{Cf}	—	—	5.0	ns	
	VCC = 1.68 V or above		—	—	7.0		
SDCLK pin output cycle time		t_{SDcyc}	8.33	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	1.0	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	1.0	—	—	ns	
SDCLK pin output rise time		t_{Cr}	—	—	3.0	ns	
SDCLK pin output fall time		t_{Cf}	—	—	3.0	ns	

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Table 2.31 Clock timing except for sub-clock oscillator (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	20.80	—	—	ns	Figure 2.16
EXTAL external clock input high pulse width		t_{EXH}	5.30	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	5.30	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	3.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	3.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	48	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.17
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	µs	Figure 2.18
MOCO clock oscillation frequency		f_{MOCO}	6.8	8.0	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16.00	16.22	MHz	–20 ≤ Tj ≤ 125 °C
		f_{HOCO18}	17.75	18.00	18.25		
		f_{HOCO20}	19.72	20.00	20.28		
		f_{HOCO32}	31.55	32.00	32.45		
		f_{HOCO48}	47.33	48.00	48.67		
		f_{HOCO16}	15.71	16.00	16.29		–40 ≤ Tj ≤ –20 °C
		f_{HOCO18}	17.68	18.00	18.32		
		f_{HOCO20}	19.64	20.00	20.36		
		f_{HOCO32}	31.42	32.00	32.58		
		f_{HOCO48}	47.14	48.00	48.86		
	With FLL	f_{HOCO16}	15.960	16.000	16.040		–40 ≤ Tj ≤ 125 °C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18.000	18.045		
		f_{HOCO20}	19.950	20.000	20.050		
		f_{HOCO32}	31.920	32.000	32.080		
		f_{HOCO48}	47.880	48.000	48.120		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO stop width time		$t_{HOCOSTP}$	1	—	—	µs	Figure 2.21
HOCO period jitter		Jitter	-3	—	3	%	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL1/PLL2 VCO frequency		f_{VCO}	640	—	1440.0	MHz	—
PLL1/PLL2 Output frequency for output clock P		t_{PLL}	40	—	480	MHz	—
PLL1/PLL2 Output frequency for output clock Q, R		t_{PLL}	71	—	480	MHz	—
PLL1/PLL2 clock oscillation stabilization wait time		t_{PLLWT}	—	—	40	µs	Figure 2.19
PLL1/PLL2 period jitter		—	—	—	±70	—	ps	—
PLL1/PLL2 long term jitter		—	—	—	±300	—	ps	Term: 1 µs, 10 µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

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Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.32 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.20

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

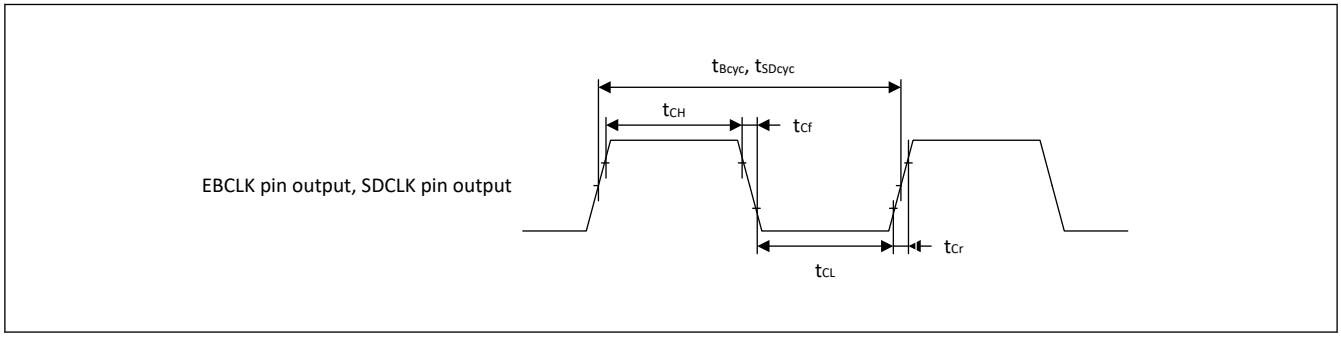


Figure 2.15 EBCLK and SDCLK output timing

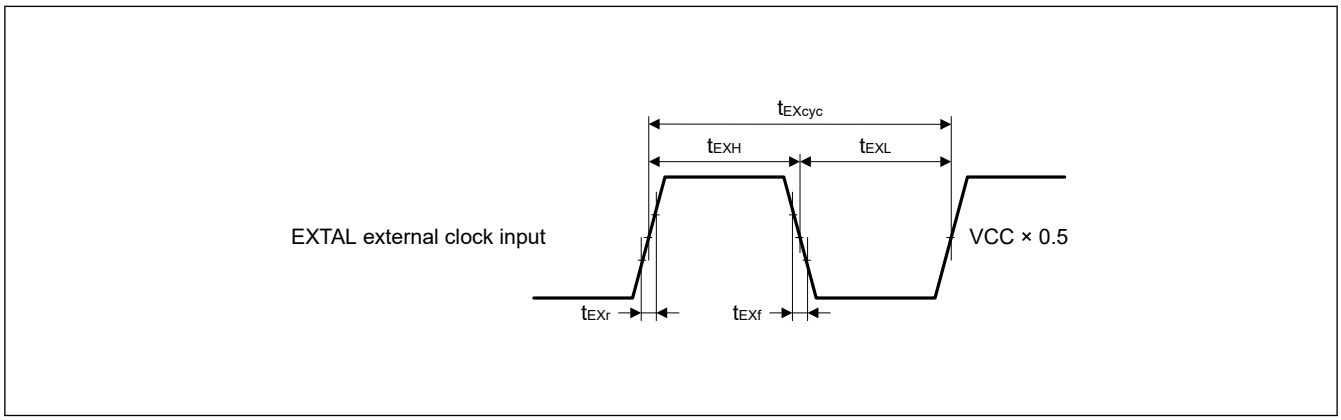


Figure 2.16 EXTAL external clock input timing

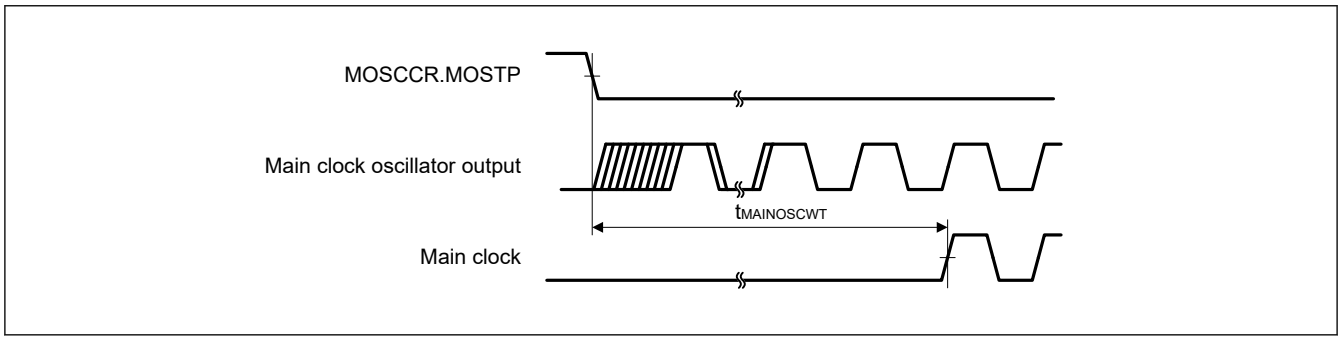


Figure 2.17 Main clock oscillation start timing

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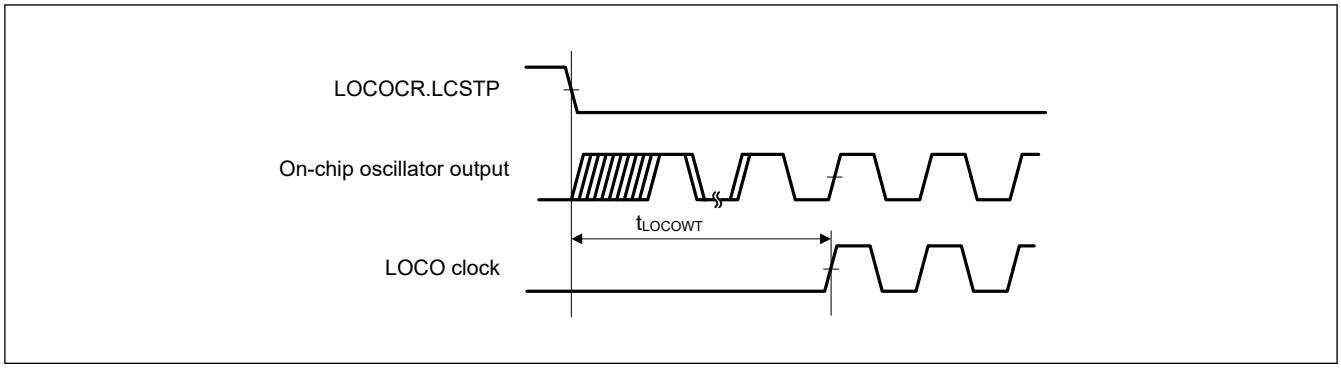
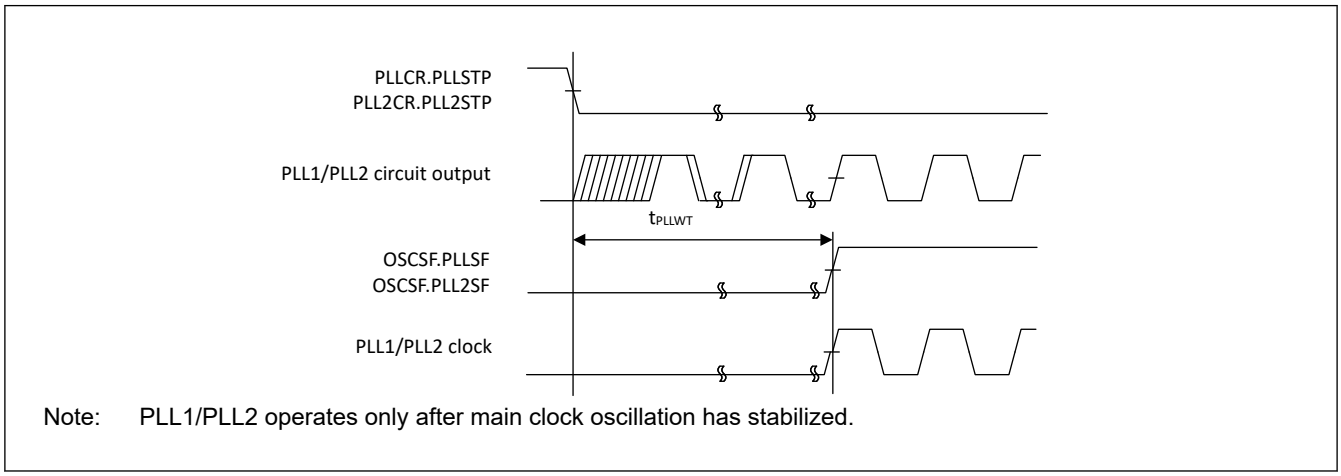


Figure 2.18 LOCO clock oscillation start timing



Note: PLL1/PLL2 operates only after main clock oscillation has stabilized.

Figure 2.19 PLL1/PLL2 clock oscillation start timing

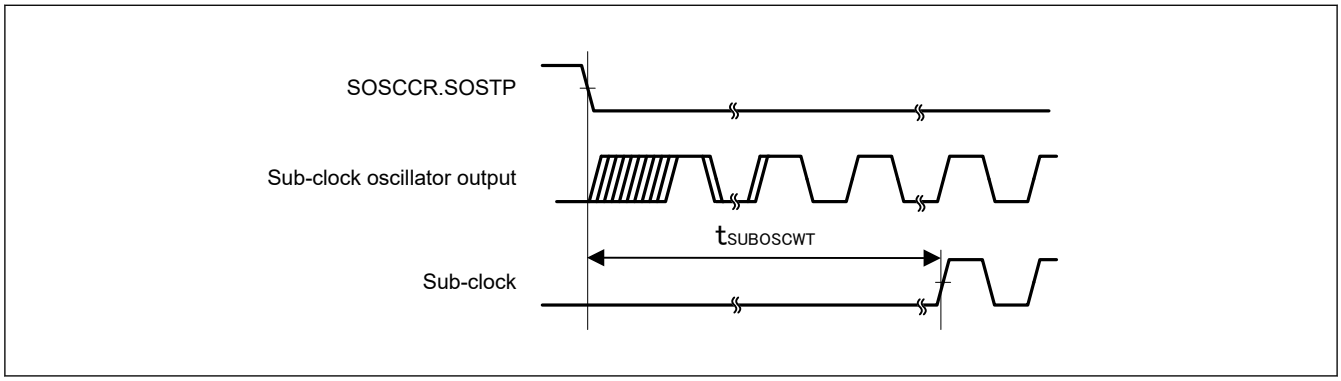


Figure 2.20 Sub-clock oscillation start timing

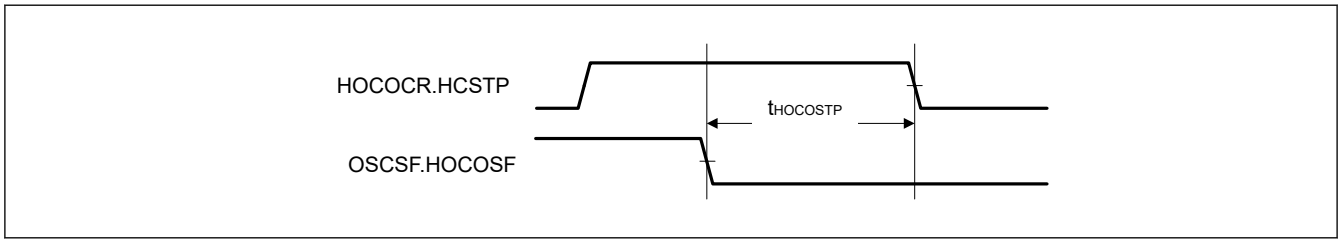


Figure 2.21 HOCO stop width time

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2.3.3 Reset Timing

Table 2.33 Reset timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on		t_{RESWP}	4.2	—	—	ms	Figure 2.22
	Deep Software Standby mode 1	DPSBYCR.DCSSMODE = 0	t_{RESWD}	1.30	—	—	ms	Figure 2.23
		DPSBYCR.DCSSMODE = 1		0.71	—	—		
	Deep Software Standby mode 2	DPSBYCR.DCSSMODE = 0		2.00	—	—		
		DPSBYCR.DCSSMODE = 1		1.50	—	—		
	Deep Software Standby mode 3	DPSBYCR.DCSSMODE = 0		3.50	—	—		
		DPSBYCR.DCSSMODE = 1		2.90	—	—		
	Software Standby mode		t_{RESWS}	0.66	—	—	ms	
	Low-speed Mode		t_{RESWLS}	0.46	—	—	ms	
	CPU Deep Sleep mode (SOSC operation)		$t_{RESWSODS}$	0.36	—	—	ms	
	CPU Deep Sleep mode (Other than SOSC operation)		t_{RESWDS}	0.24	—	—	ms	
	SOSC operation		t_{RESWSO}	0.19	—	—	ms	
	Other than above		t_{RESW}	62.0	—	—	µs	
Wait time after RES cancellation			t_{RESWT}	—	54.9	64.6	µs	Figure 2.22
Wait time after internal reset cancellation (IWDT reset, WDT reset, CPU Lockup reset, Bus Error reset, Common Memory Error reset, Software reset)			t_{RESW2}	—	54.9	64.6	µs	—

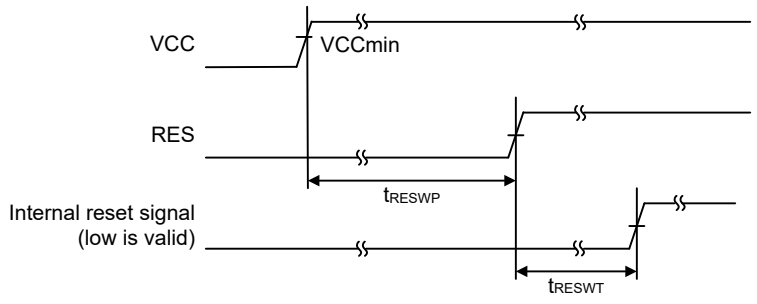


Figure 2.22 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

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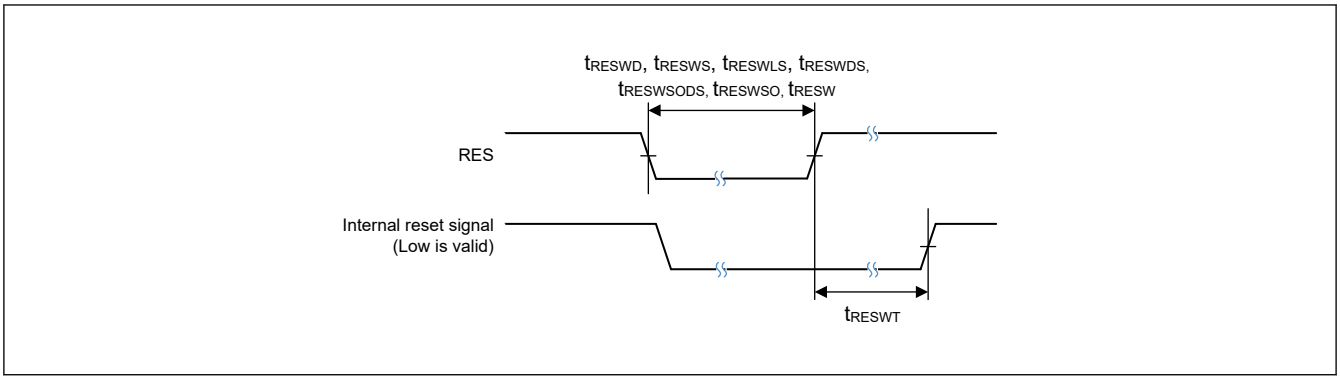


Figure 2.23 Reset input timing

2.3.4 Wakeup Timing

Table 2.34 Timing of recovery from low power modes (1 of 2)

Parameter			Fast return function	Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from CPU Deep Sleep mode			—	t_{DSLP}*10	—	182	214	µs	—
Recovery time from Software Standby mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*1 MOSCSCR.MOSCSOKP = 0	Enabled	t_{SBYMC}*9	—	2.33	2.43	ms	Figure 2.24 The division ratio of all oscillators is 1.
		System clock source is main clock oscillator*1 MOSCSCR.MOSCSOKP = 1	Enabled		—	310	385	µs	
		System clock source is PLL1P with main clock oscillator*2 MOSCSCR.MOSCSOKP = 0	Enabled	t_{SBYPC}*9	—	2.47	2.59	ms	
		System clock source is PLL1P with main clock oscillator*2 MOSCSCR.MOSCSOKP = 1	Enabled		—	388	511	µs	
	External clock input to main clock oscillator	System clock source is main clock oscillator*3	Enabled	t_{SBYEX}*9	—	310	385	µs	
		System clock source is PLL1P with main clock oscillator*4	Enabled	t_{SBYPE}*9	—	388	511		
	System clock source is sub-clock oscillator*5		Enabled	t_{SBYSC}*9	—	0.81	0.87	ms	
	System clock source is HOCO clock oscillator*6		Enabled	t_{SBYHO}*9	—	310	385	µs	
	System clock source is PLL1P with HOCO*7		Enabled	t_{SBYPH}*9	—	398	522	µs	
	System clock source is MOCO clock oscillator*8		Enabled	t_{SBYMO}*9	—	312	387	µs	

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Table 2.34 Timing of recovery from low power modes (2 of 2)

Parameter			Fast return function	Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	Deep Software Standby mode 1	Any of PVD0(OFS1(_SEC).PVDLPSEL=1), PVD1, or PVD2 is enabled	Standard	t_{DSBY}	—	0.68	1.20	ms	Figure 2.25
			Fast		—	0.29	0.62	ms	
		All of PVD0(OFS1(_SEC).PVDLPSEL=1), PVD1, and PVD2 are disabled	Standard			0.73	1.30		
			Fast			0.33	0.71		
	Deep Software Standby mode 2	DPSWCR.WSTS = 0x0B	Standard		—	0.73	1.10	ms	
			Fast		—	0.33	0.50	ms	
		DPSWCR.WSTS = 0x9A	Standard		—	1.60	2.00	ms	
			Fast		—	1.20	1.50	ms	
	Deep Software Standby mode 3		Standard		—	2.10	3.50	ms	
			Fast		—	1.70	2.90	ms	
Wait time after cancellation of Deep Software Standby mode			—	t_{DSBYWT}	47.7	—	64.6	µs	

Note 1. When the frequency of the crystal is 48 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 2. When the frequency of PLL1P is 480 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 8.
Note 3. When the frequency of the external clock is 48 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 4. When the frequency of PLL1P is 480 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 8.
Note 5. The Sub-clock oscillator frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 6. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 7. The PLL frequency is 480 MHz and the greatest value of the internal clock division setting is 8.
Note 8. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The recovery time can be calculated with the equation of t_{Common} + max(t_{OSCSTB}, t_{PG1}, t_{PGCK}) + max(t_{PG2}, t_{LPW}). And they can be determined with the following values and equations. For n, the greatest value is selected from among the internal clock(CPUCLK, ICLK, PCLKm, FCLK, BCLK and EBCLK) division settings (m = A to E).
t_{OSCSTB} in the table below means the time when each oscillator is active. When multiple oscillators are active, t_{OSCSTB} is determined by the longest t_{OSCSTB} among the active oscillators.
Note 10. The ICLK frequency is 240 MHz. This recovery time corresponds to t_{PG2}.

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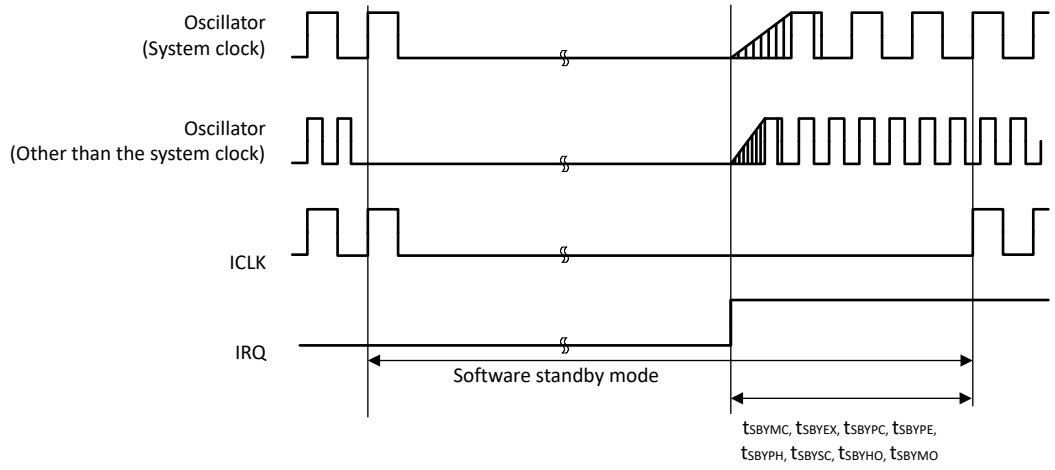
Table 2.35 Each element of recovery time

Wakeup time	Oscillation keep	Fast return function	Typ						Max						Unit
			t_{Common}	t_{OSCSTB} *1	t_{PG1}	t_{PGCK}	t_{PG2}	t_{LPW}	t_{Common}	t_{OSCSTB} *1	t_{PG1}	t_{PGCK}	t_{PG2}	t_{LPW}	
t_{SBYMC}	MOSC disabled	Enabled	52.667 + 4/ fICLK	$t_{MAINOSCWT}$	75.5	2.1 + 10.5/ fMOCO + 2.5n/ fMOCO + 2.5/ fSRCCLK + 2/ fICLK	1449/ fMOCO + 10/ fICLK	10 + 2/ fICLK + 2n/ fMAIN	82.369 + 4/ fICLK	$t_{MAINOSCWT}$ + 11/0.236	88.8	2.5 + 10.5/ fMOCO + 2.5n/ fMOCO + 2.5/ fSRCCLK + 2/ fICLK	1449/ fMOCO+ 10/ fICLK	10 + 2/ fICLK + 2n/ fMAIN	µs
	MOSC enabled	Enabled	52.667 + 4/ fICLK	3/0.262				10 + 2/ fICLK + 2n/ fMAIN	82.369 + 4/ fICLK	14/0.236				10 + 2/ fICLK + 2n/ fMAIN	µs
t_{SBYPC}	MOSC disabled	Enabled	52.667 + 4/ fICLK	24.125 +$t_{MAINOSCWT}$ + 31/0.262 *2				10 + 2/ fICLK + 2n/ fPLL	82.369 + 4/ fICLK	24.05 + $t_{MAINOSCWT}$ + 42/0.236 *3				10 + 2/ fICLK + 2n/ fPLL	µs
	MOSC enabled	Enabled	52.667 + 4/ fICLK	24.125 + 34/0.262 *2				10 + 2/ fICLK + 2n/ fPLL	82.369 + 4/ fICLK	24.05 + 45/0.236 *3				10 + 2/ fICLK + 2n/ fPLL	µs
t_{SBYEX}	—	Enabled	52.667 + 4/ fICLK	3/0.262				10 + 2/ fICLK + 2n/ fEXMAIN	82.369 + 4/ fICLK	14/0.236				10 + 2/ fICLK + 2n/ fEXMAIN	µs
t_{SBYPE}	—	Enabled	52.667 + 4/ fICLK	24.125 + 34/0.262 *2				10 + 2/ fICLK + 2n/ fPLL	82.369 + 4/ fICLK	24.05 +45/0.236*3				10 + 2/ fICLK + 2n/ fPLL	µs
t_{SBYSC}	—	Enabled	52.667 + 4/ fICLK	0				10 + 2/ fICLK + 2n/ fSOSC	82.369 + 4/ fICLK	0				10 + 2/ fICLK + 2n/ fSOSC	µs
t_{SBYHO}	—	Enabled	52.667 + 4/ fICLK	23.375				10 + 2/ fICLK + 2n/ fHOCO	82.369 + 4/ fICLK	70.234				10 + 2/ fICLK + 2n/ fHOCO	µs
t_{SBYPH}	—	Enabled	52.667 + 4/ fICLK	24.125 + 140*2				10 + 2/ fICLK + 2n/ fPLL	82.369 + 4/ fICLK	24.05 +202*3				10 + 2/ fICLK + 2n/ fPLL	µs
t_{SBYMO}	—	Enabled	52.667 + 4/ fICLK	0				10 + 2/ fICLK + 2n/ fMOCO	82.369 + 4/ fICLK	0				10 + 2/ fICLK + 2n/ fMOCO	µs

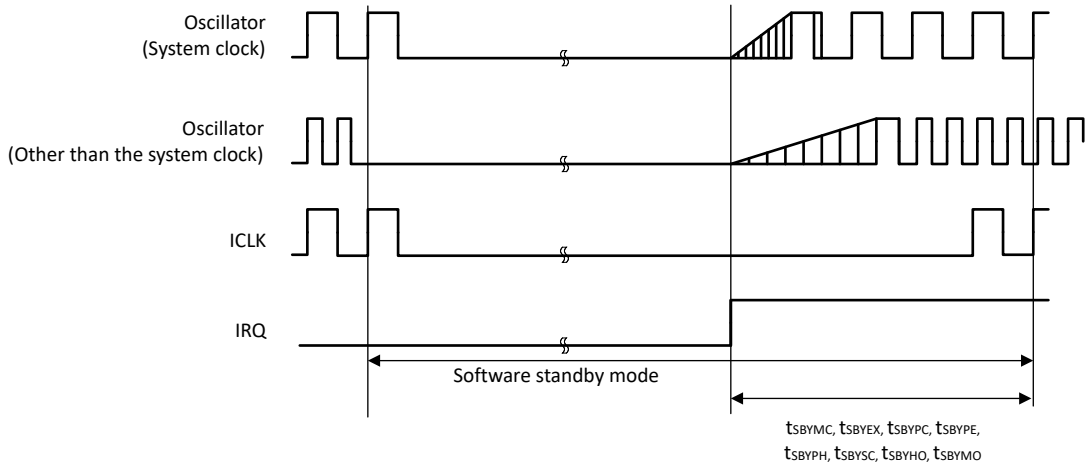
Note: The unit of frequency is MHz.
Note 1. If more than one oscillator is operating, the largest value of the operating oscillator in this column is applied.
Note 2. "24.125" can be reduced when both PLL1LDOCR.SKEEP and PLL2LDOCR.SKEEP are 1.

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Note 3. "24.05" can be reduced when both PLL1LDOCR.SKEEP and PLL2LDOCR.SKEEP are 1.



When stabilization of the system clock oscillator is slower



When stabilization of an oscillator other than the system clock is slower

Figure 2.24 Software Standby mode cancellation timing

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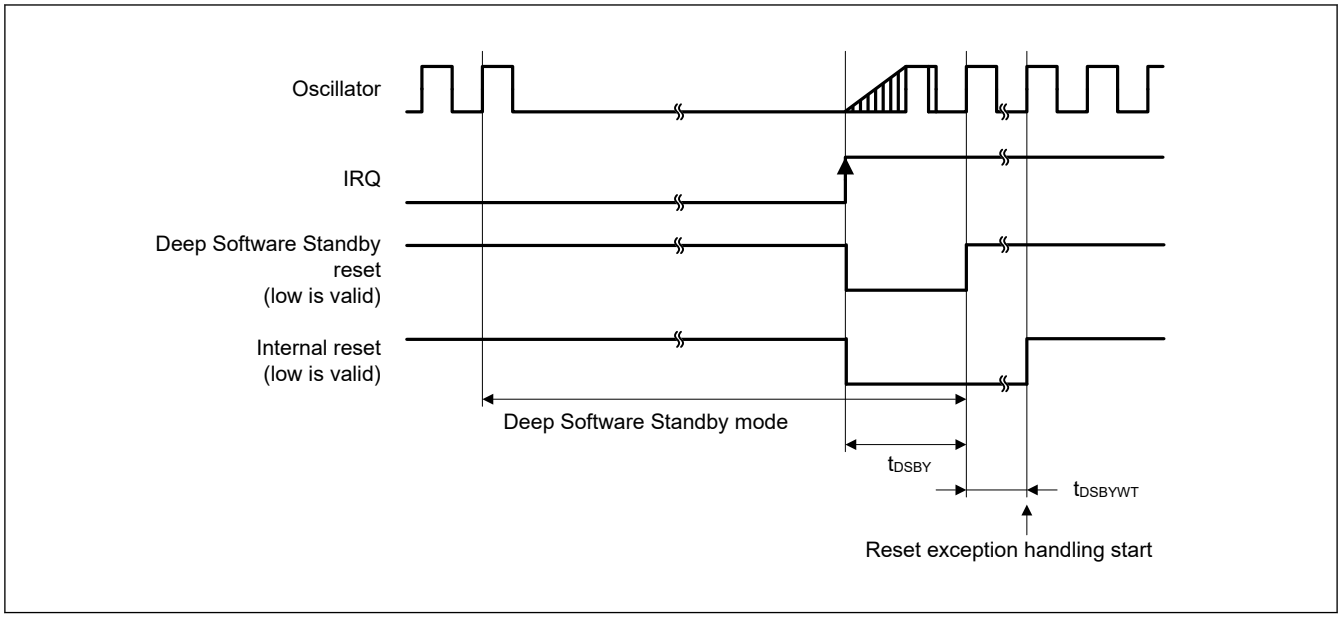


Figure 2.25 Deep Software Standby mode cancellation timing

2.3.5 NMI and IRQ Noise Filter

Table 2.36 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the system clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

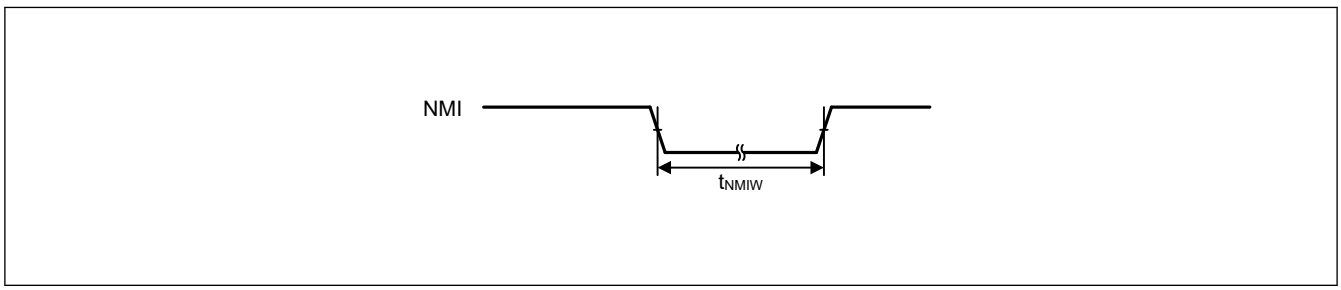


Figure 2.26 NMI interrupt input timing

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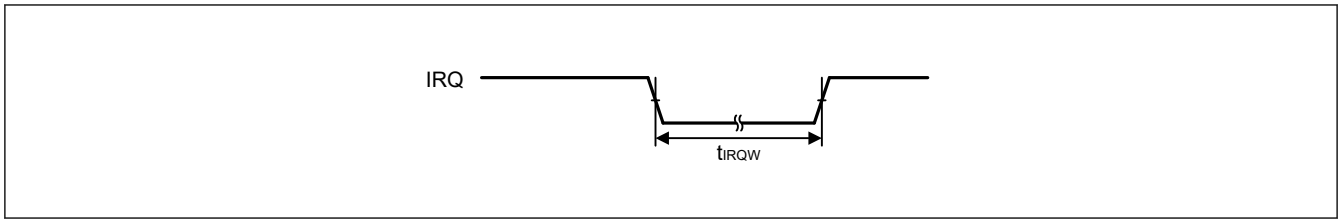


Figure 2.27 IRQ interrupt input timing

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2.3.6 Bus Timing

Table 2.37 Bus timing (1 of 2)

Condition 1: When using the CS area controller (CSC).
VCC = VCC_DCDC = VCC_USB = 1.68 V to 3.6 V, VCC2 = 1.65 V to 3.6 V
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz (When VCC = VCC_USB = 2.70 to 3.6 V)
BCLK = 8 to 60 MHz, EBCLK = 8 to 30 MHz (When VCC = VCC_USB = 1.68 to 3.6 V)
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = VCC2 = VCC_DCDC = VCC_USB = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
SDCLK: High-speed high drive output is selected in the port drive capability bit in the PmnPFS register.
Others: High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = VCC2 = VCC_DCDC = VCC_USB = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
EBCLK/SDCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Address delay	2.70V or above	t_{AD}	1.0	12.5	ns	Figure 2.28 to Figure 2.34
	1.68V or above		1.0	12.5	ns	
Byte control delay	2.70V or above	t_{BCD}	1.0	12.5	ns	
	1.68V or above		1.0	12.5	ns	
CS delay	2.70V or above	t_{CSD}	1.0	12.5	ns	
	1.68V or above		1.0	12.5	ns	
ALE delay time	2.70V or above	t_{ALED}	1.0	12.5	ns	
	1.68V or above		1.0	12.5	ns	
RD delay	2.70V or above	t_{RSD}	1.0	12.5	ns	
	1.68V or above		1.0	12.5	ns	
Read data setup time	2.70V or above	t_{RDS}	12.5	—	ns	
	1.68V or above		20.5	—	ns	
Read data hold time	2.70V or above	t_{RDH}	0	—	ns	
	1.68V or above		0	—	ns	
WR/WRn delay	2.70V or above	t_{WRD}	1.0	12.5	ns	
	1.68V or above		1.0	12.5	ns	
Write data delay	2.70V or above	t_{WDD}	—	12.5	ns	
	1.68V or above		—	12.5	ns	
Write data hold time	2.70V or above	t_{WDH}	1.0	—	ns	
	1.68V or above		1.0	—	ns	
WAIT setup time	2.70V or above	t_{WTS}	12.5	—	ns	
	1.68V or above		20.5	—	ns	
WAIT hold time	2.70V or above	t_{WTH}	0	—	ns	
	1.68V or above		0	—	ns	

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Table 2.37 Bus timing (2 of 2)

Condition 1: When using the CS area controller (CSC).
VCC = VCC_DCDC = VCC_USB = 1.68 V to 3.6 V, VCC2 = 1.65 V to 3.6 V
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz (When VCC = VCC_USB = 2.70 to 3.6 V)
BCLK = 8 to 60 MHz, EBCLK = 8 to 30 MHz (When VCC = VCC_USB = 1.68 to 3.6 V)
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = VCC2 = VCC_DCDC = VCC_USB = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
SDCLK: High-speed high drive output is selected in the port drive capability bit in the PmnPFS register.
Others: High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = VCC2 = VCC_DCDC = VCC_USB = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
EBCLK/SDCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	Condition 2	t_{AD2}	0.8	6.8	ns	Figure 2.35 to Figure 2.41
	Condition 3		0.8	10.8		
CS delay 2 (SDRAM)	Condition 2	t_{CSD2}	0.8	6.8	ns	
	Condition 3		0.8	10.8		
DQM delay (SDRAM)	Condition 2	t_{DQMD}	0.8	6.8	ns	
	Condition 3		0.8	10.8		
CKE delay (SDRAM)	Condition 2	t_{CKED}	0.8	6.8	ns	
	Condition 3		0.8	10.8		
Read data setup time 2 (SDRAM)	Condition 2	t_{RDS2}	2.9	—	ns	
	Condition 3		6.9	—		
Read data hold time 2 (SDRAM)	Condition 2	t_{RDH2}	1.5	—	ns	
	Condition 3		1.5	—		
Write data delay 2 (SDRAM)	Condition 2	t_{WDD2}	—	6.8	ns	
	Condition 3		—	10.8		
Write data hold time 2 (SDRAM)	Condition 2	t_{WDH2}	0.8	—	ns	
	Condition 3		0.8	—		
WE delay (SDRAM)	Condition 2	t_{WED}	0.8	6.8	ns	
	Condition 3		0.8	10.8		
RAS delay (SDRAM)	Condition 2	t_{RASD}	0.8	6.8	ns	
	Condition 3		0.8	10.8		
CAS delay (SDRAM)	Condition 2	t_{CASD}	0.8	6.8	ns	
	Condition 3		0.8	10.8		

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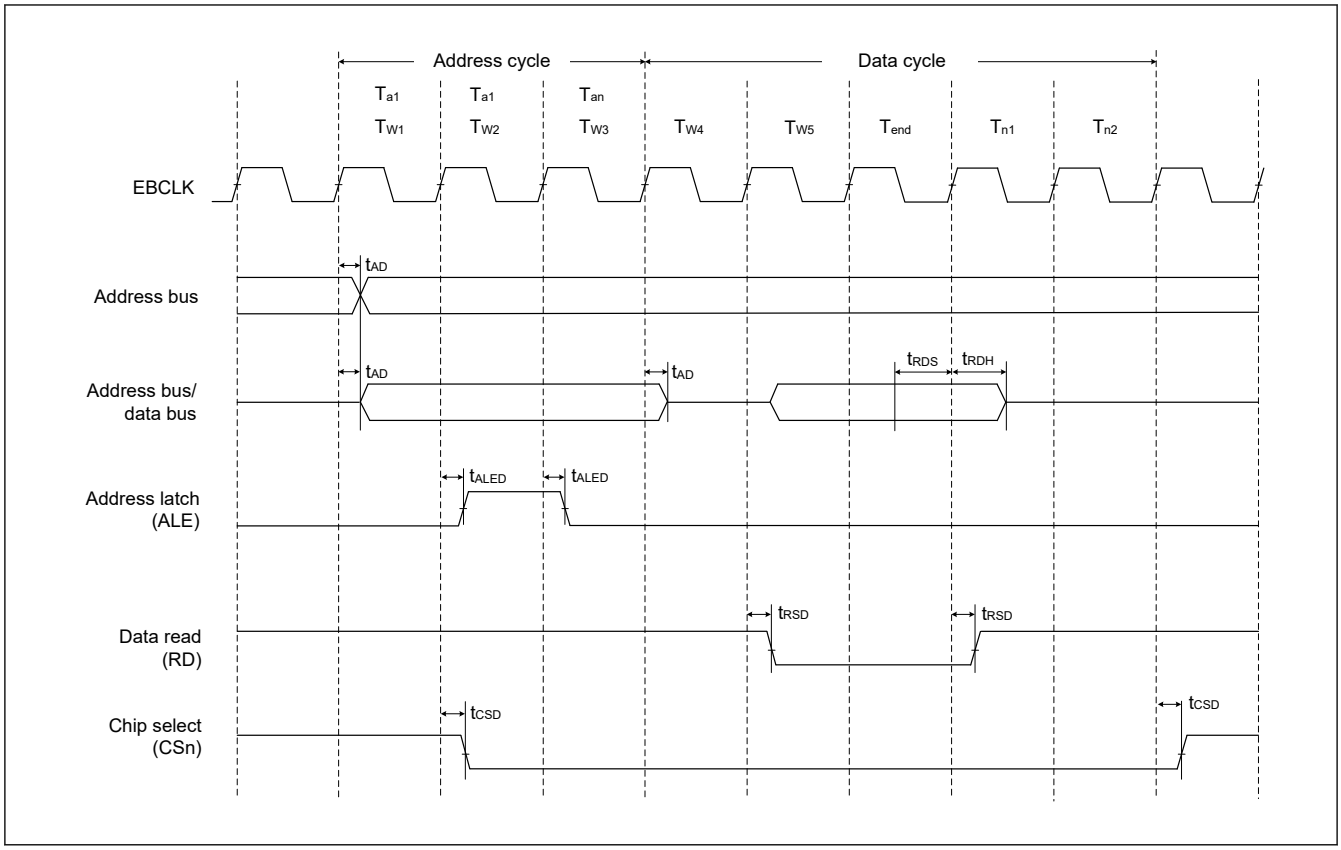


Figure 2.28 Address/data multiplexed bus read access timing

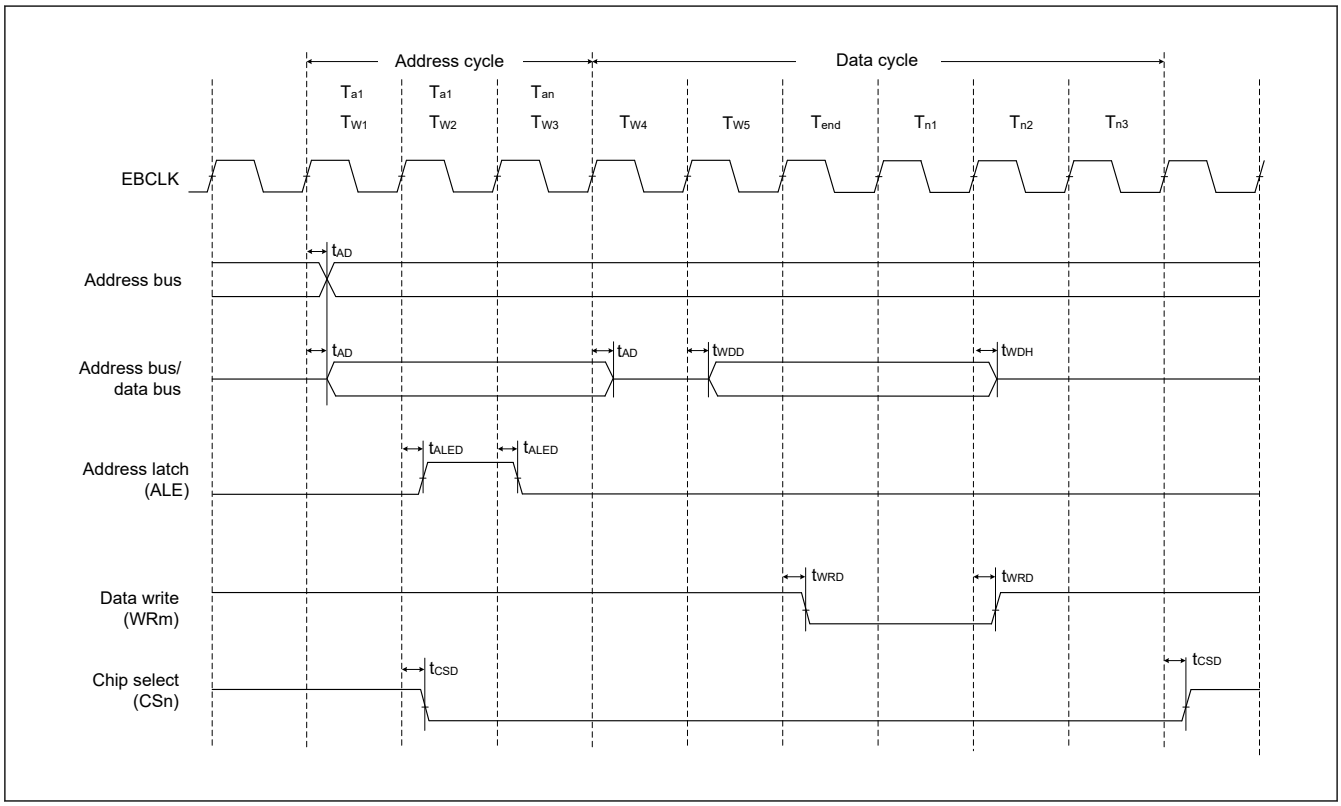


Figure 2.29 Address/data multiplexed bus write access timing

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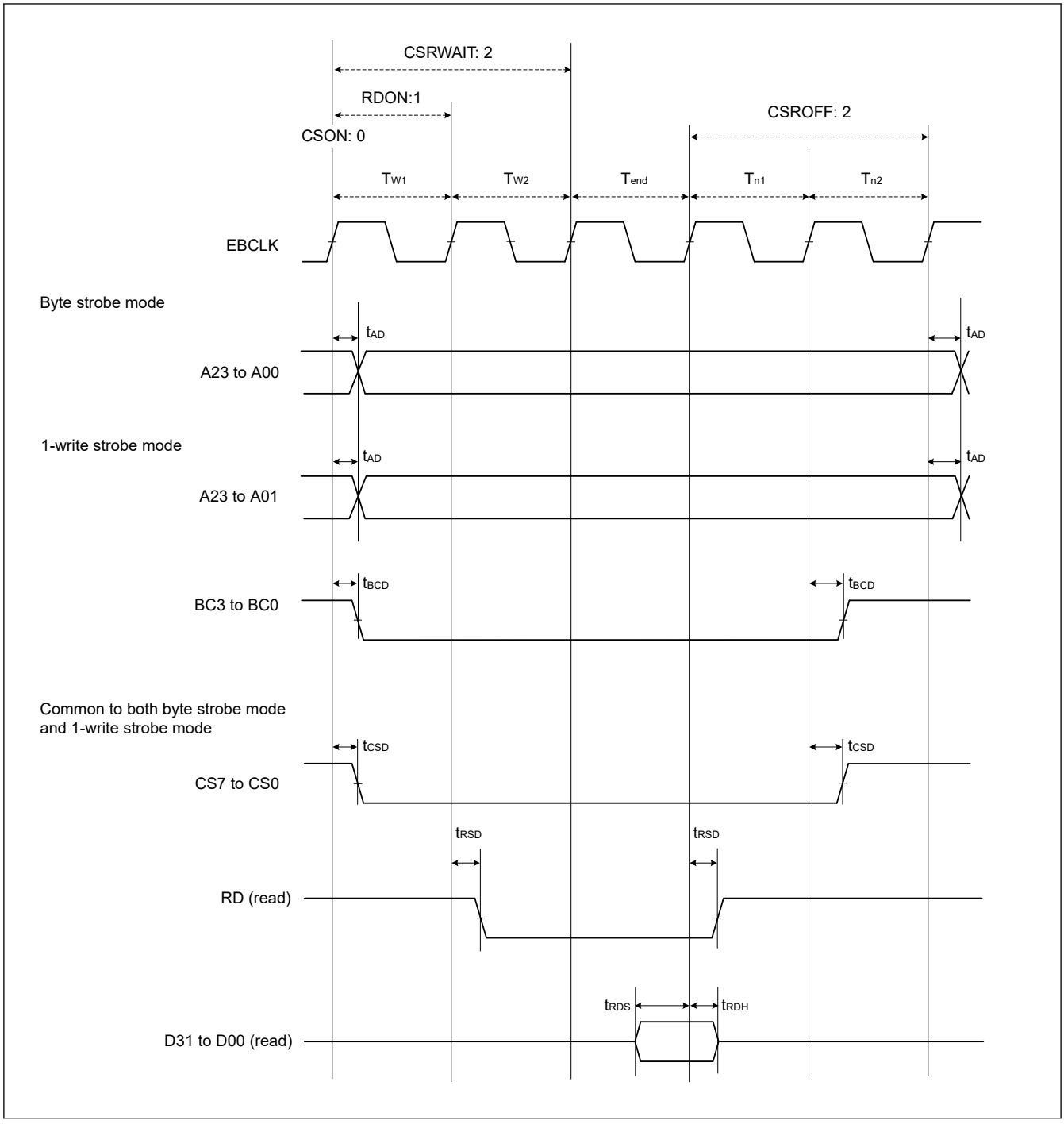
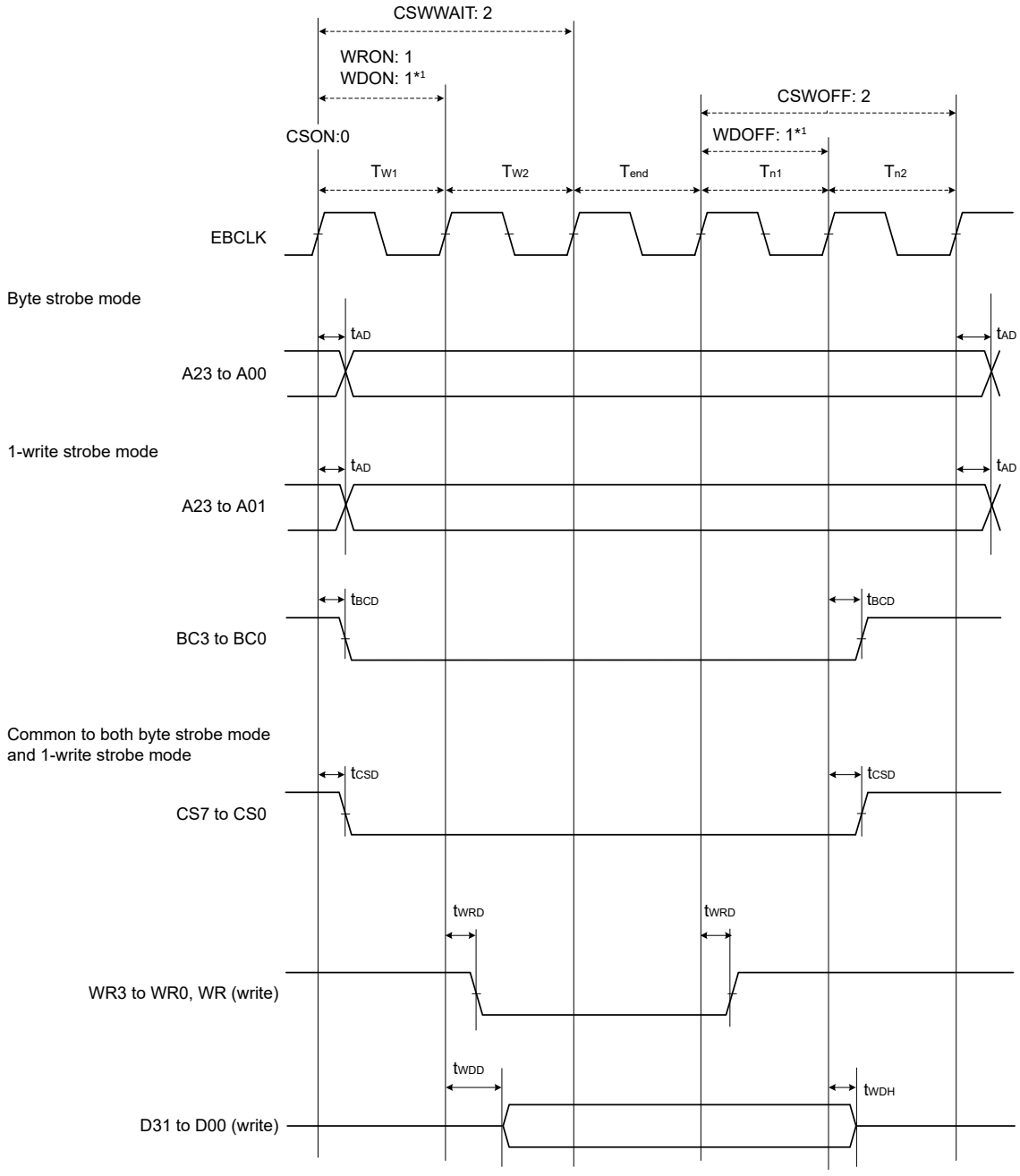


Figure 2.30 External bus timing for normal read cycle with bus clock synchronized

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Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.31 External bus timing for normal write cycle with bus clock synchronized

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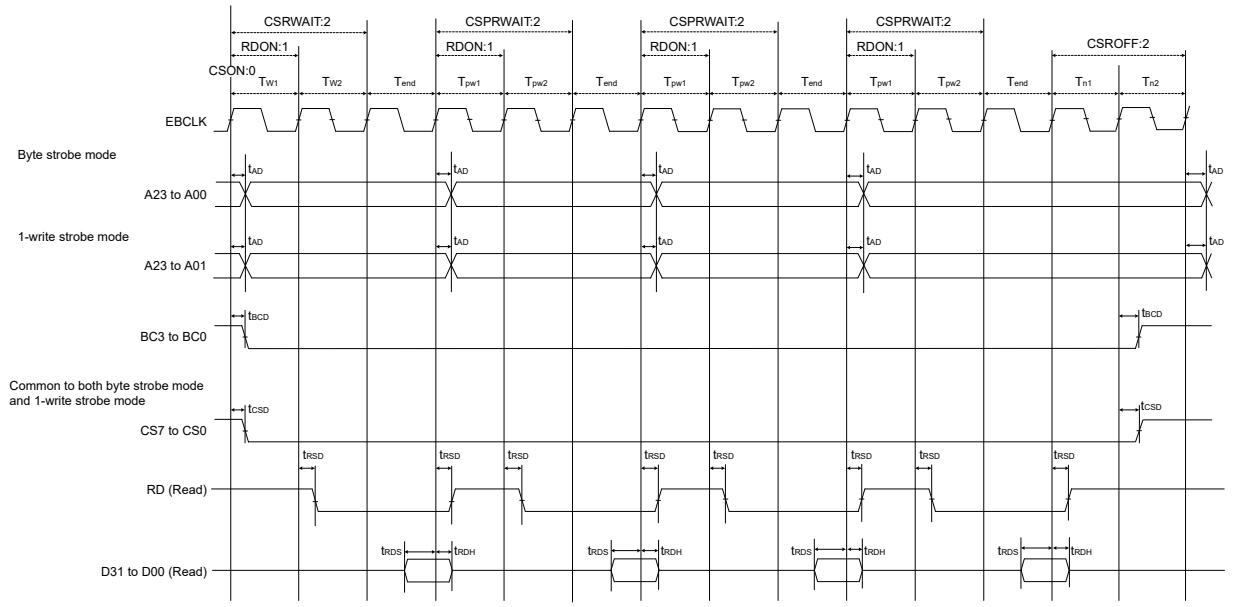
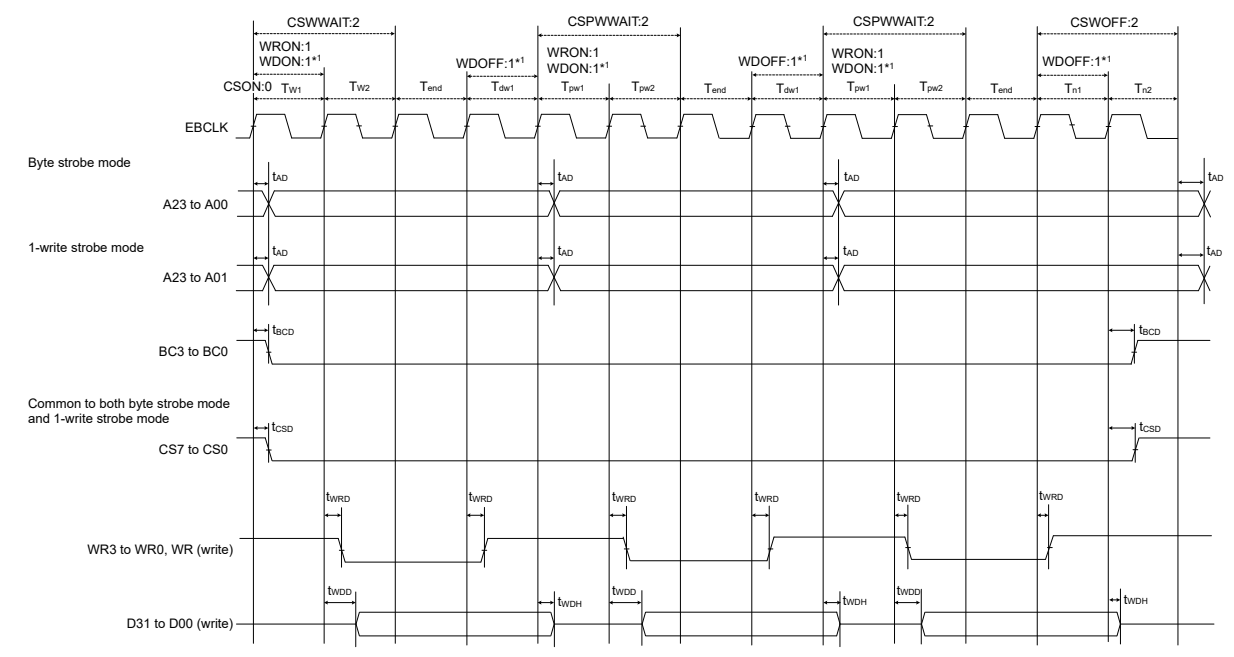


Figure 2.32 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.33 External bus timing for page write cycle with bus clock synchronized

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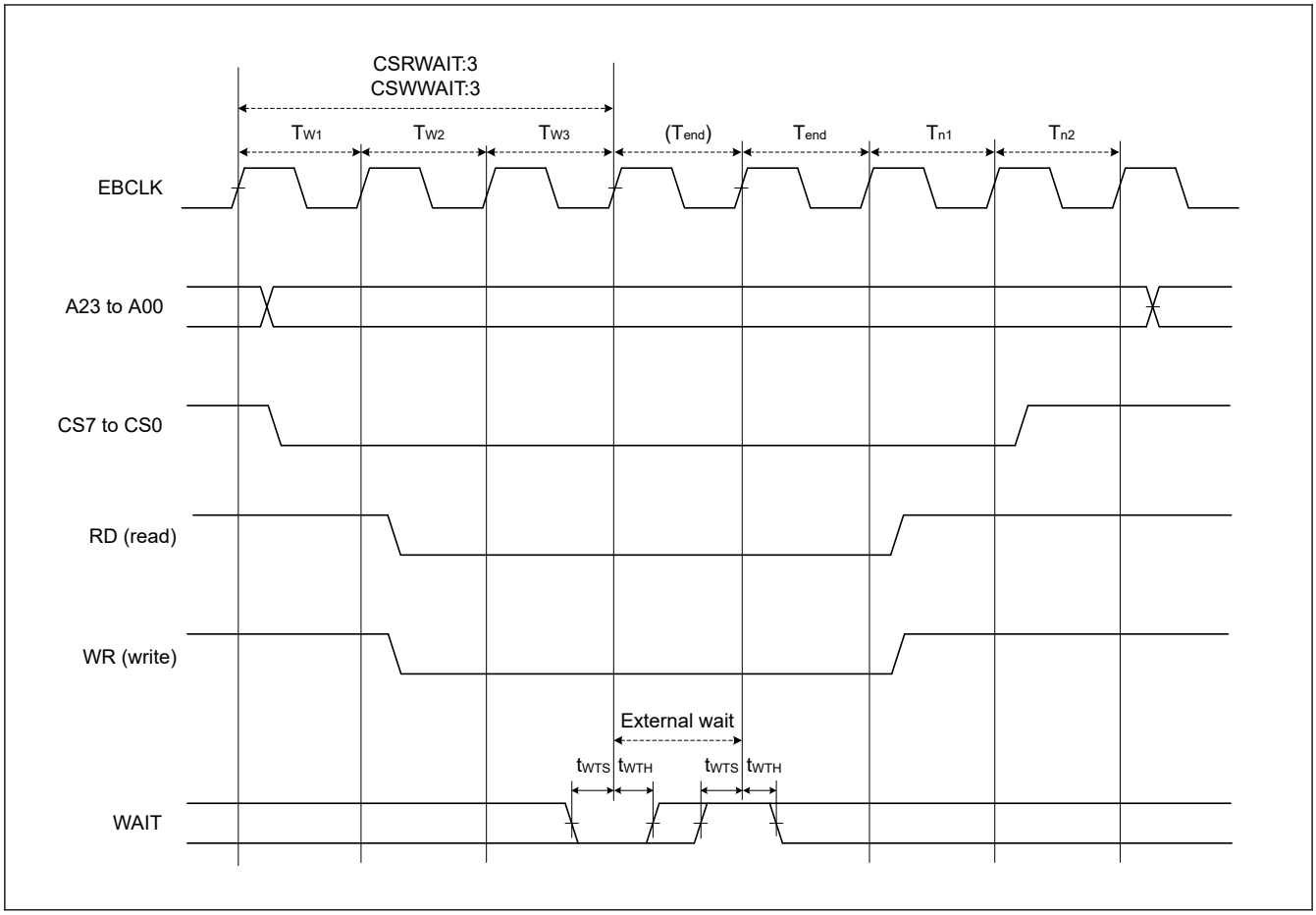
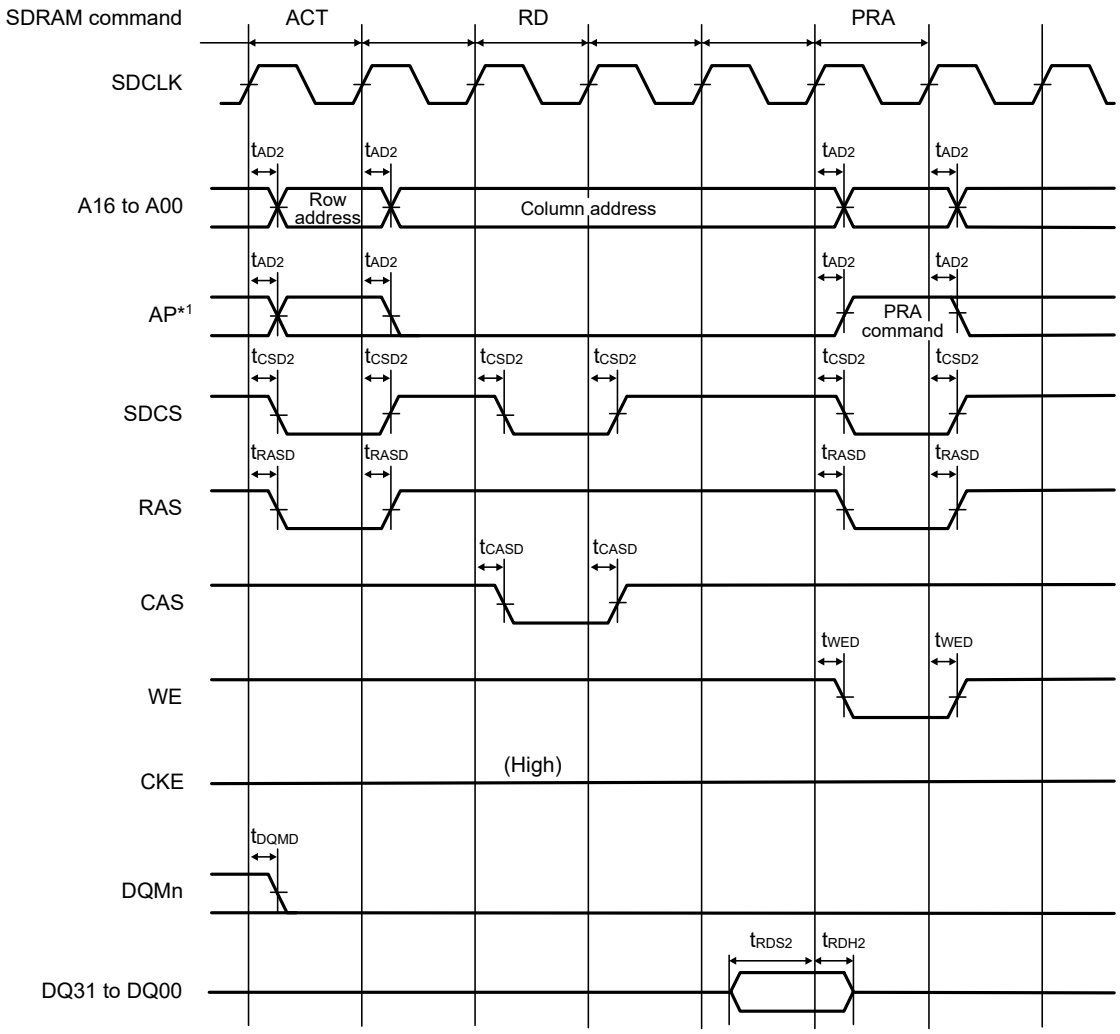


Figure 2.34 External bus timing for external wait control

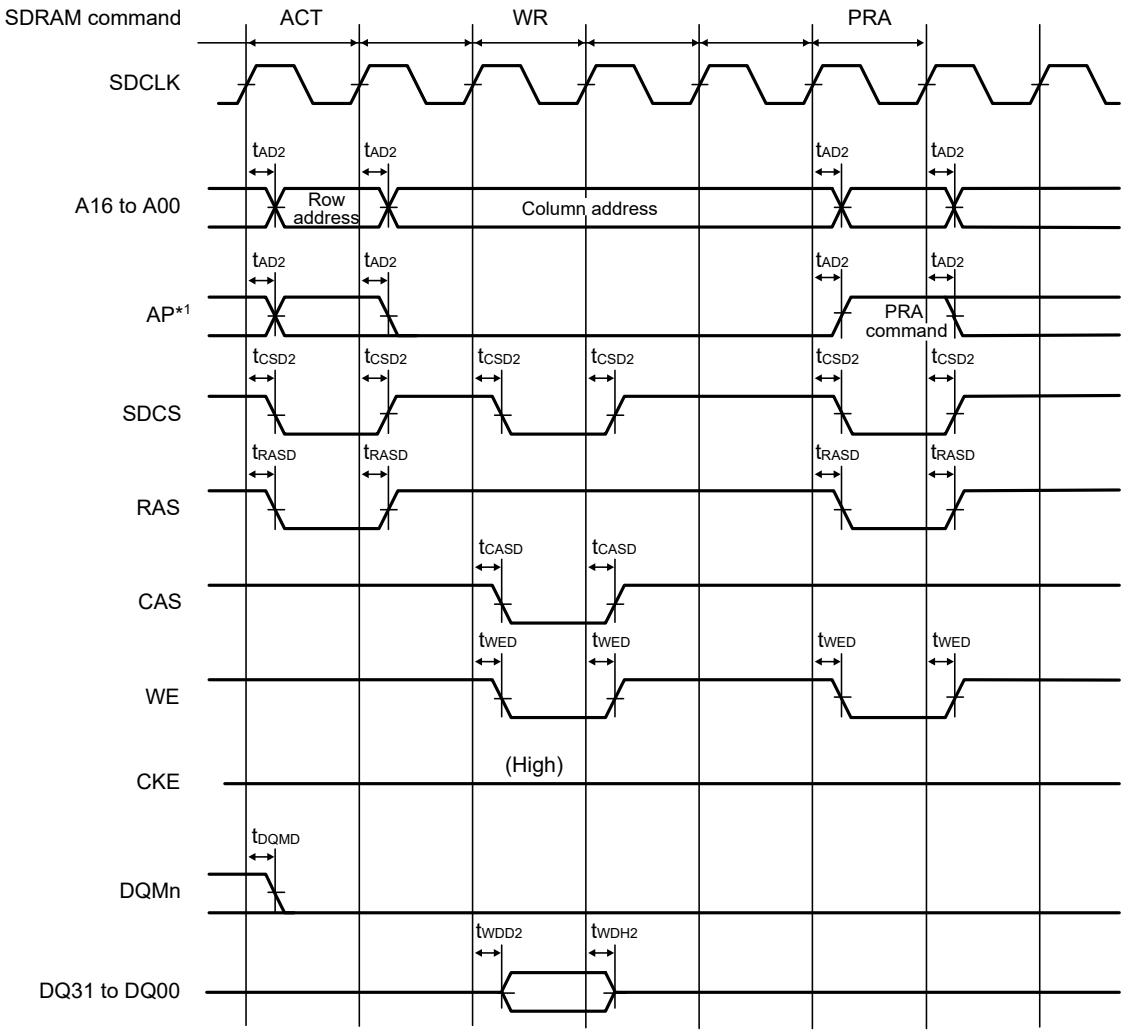
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.35 SDRAM single read timing

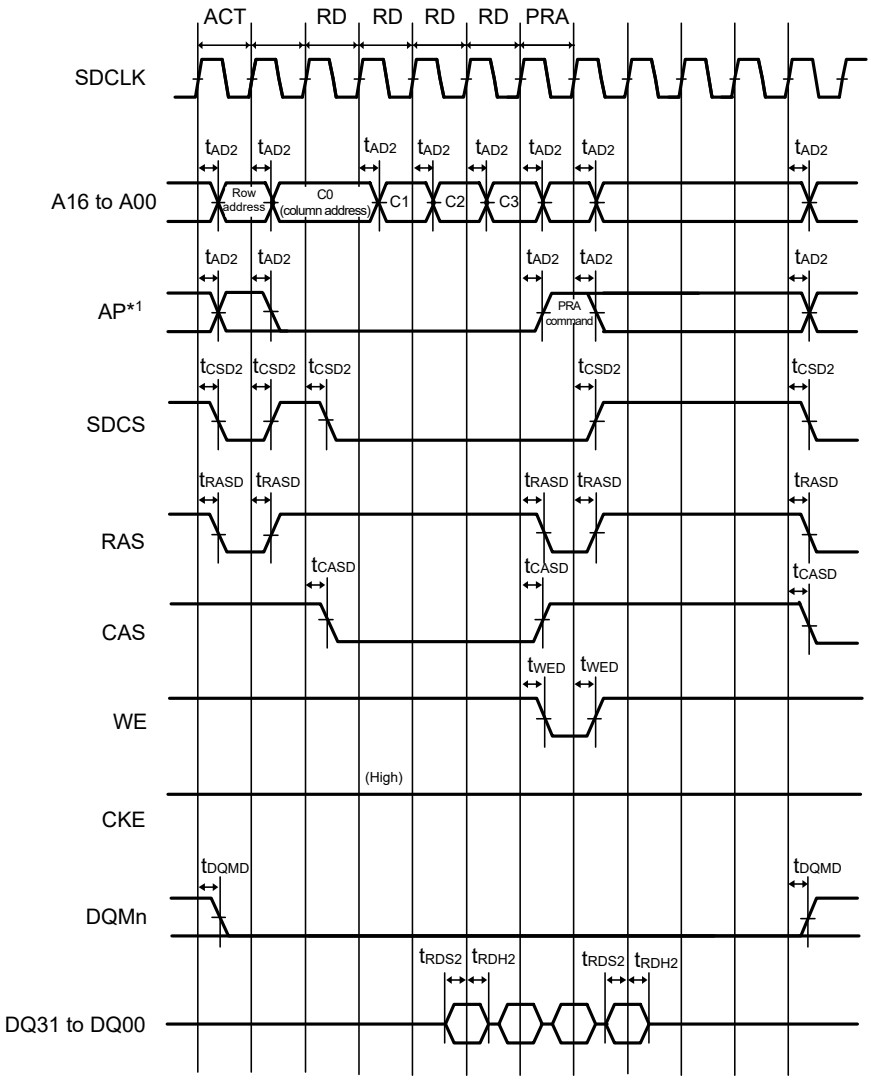
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM

Figure 2.36 SDRAM single write timing

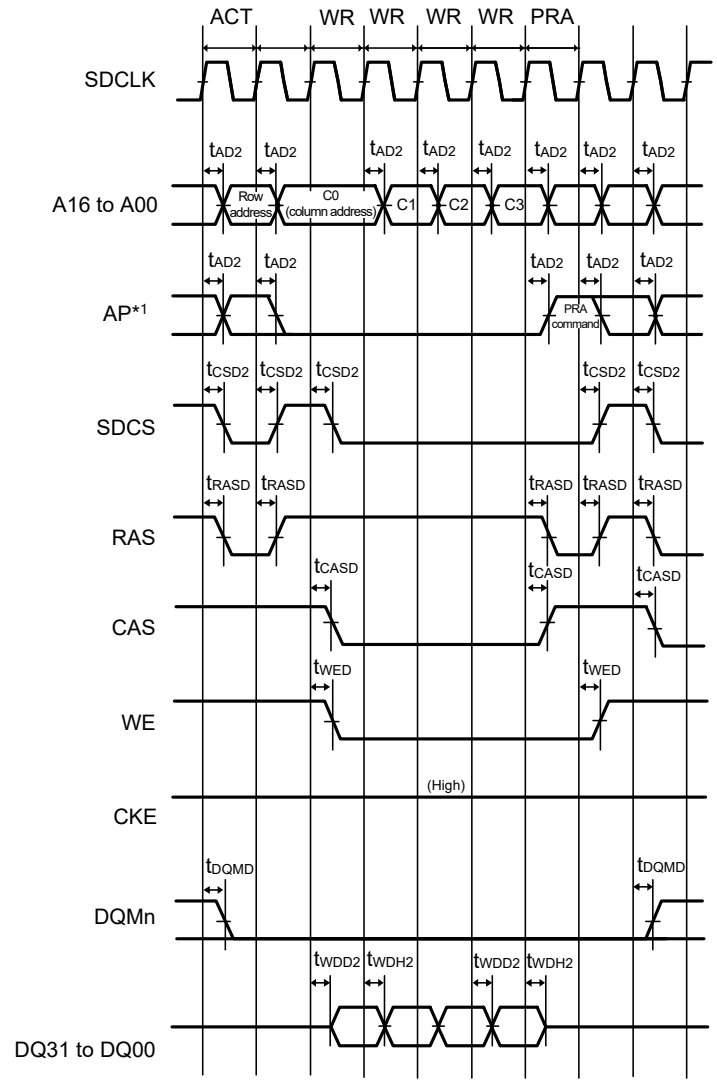
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.37 SDRAM multiple read timing

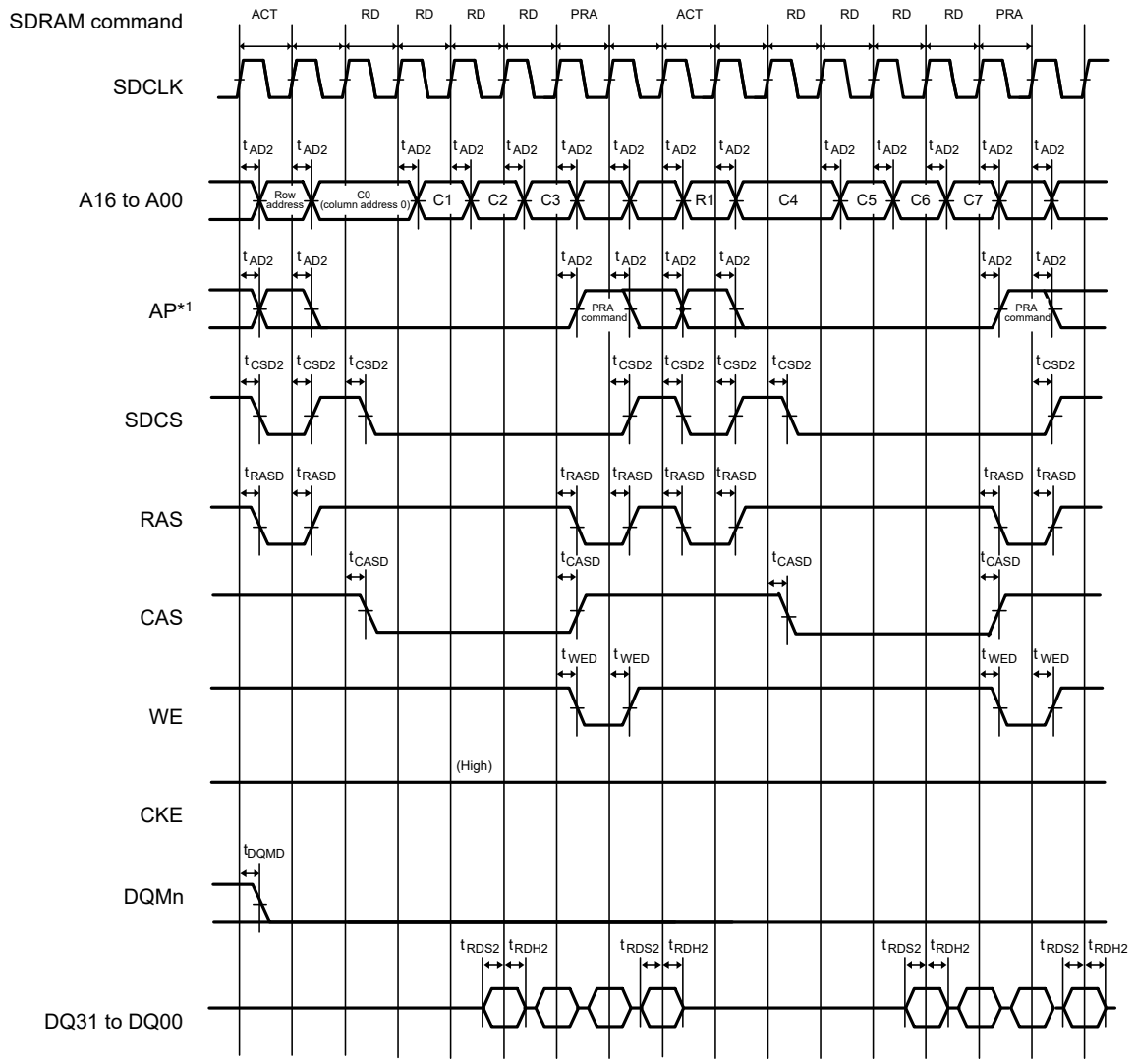
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.38 SDRAM multiple write timing

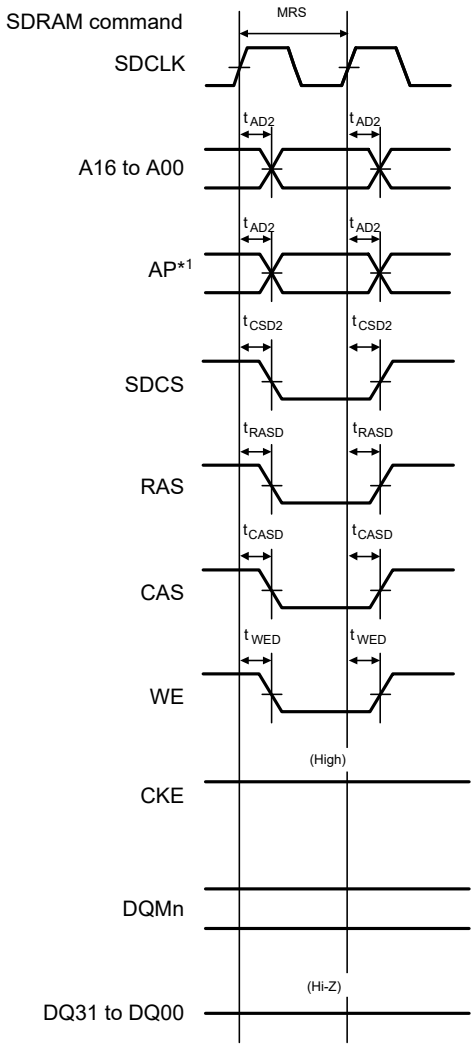
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.39 SDRAM multiple read line stride timing

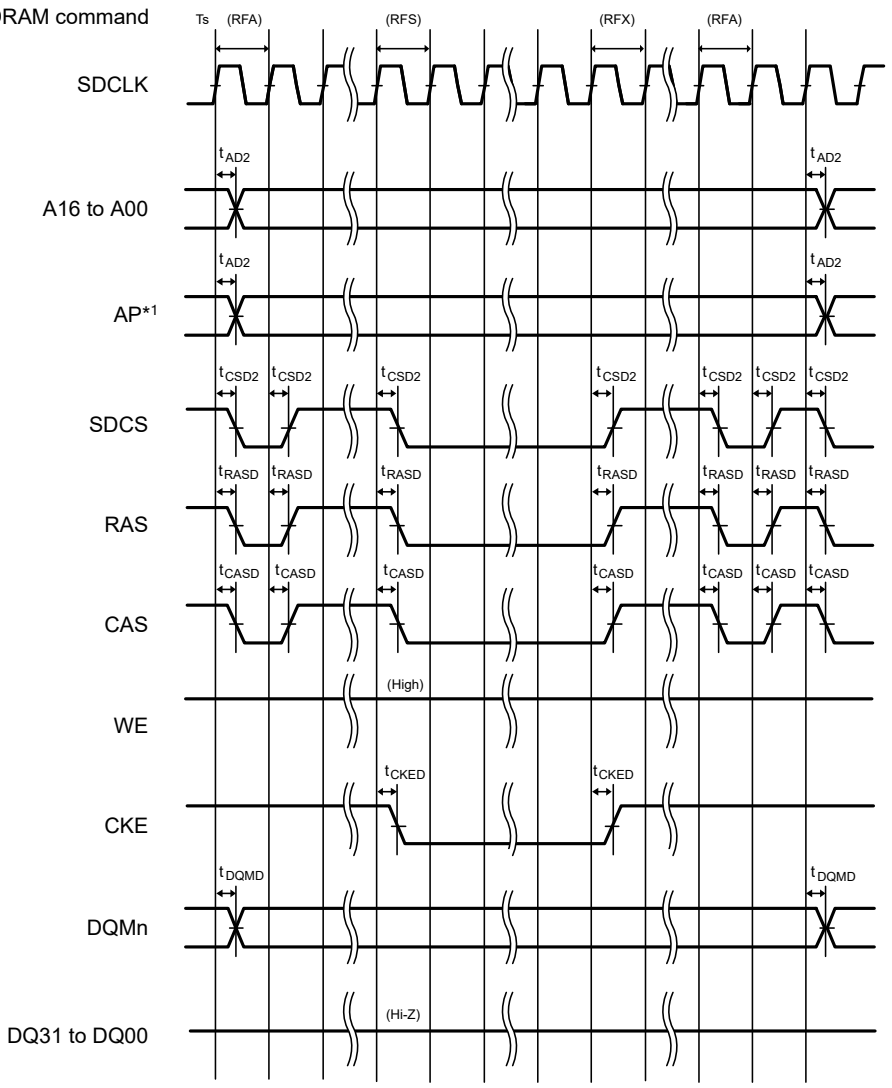
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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.40 SDRAM mode register set timing

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Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.41 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT, AGT, ULPT and ADC12 Trigger Timing

Table 2.38 I/O ports, POEG, GPT, AGT, ULPT and ADC12 trigger timing (1 of 3)

GPT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	5.5	—	t_{Icyc}	Figure 2.42
	EXCIN input frequency	t_{EXCIN}	—	36	kHz	
POEG	POEG input trigger pulse width	t_{POEW}	3	—	t_{Pcyc}	Figure 2.43

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Table 2.38 I/O ports, POEG, GPT, AGT, ULPT and ADC12 trigger timing (2 of 3)

GPT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
GPT	Input capture pulse width (Cycle)	Single edge	t_{GTICW}*1	1.5	—	t_{PDcyc}	Figure 2.44
		Dual edge		2.5	—		
	Input capture pulse width (Time)	2.70V or above	t_{GTICW}*1	12.5	—	ns	
		1.68V or above (VCC) 1.65V or above (VCC2)		25.0	—		
	GTIOCxY output skew (x = 0 to 7, Y = A or B)	2.70V or above	t_{GTISK}	—	4	ns	Figure 2.45
		1.68V or above (VCC) 1.65V or above (VCC2)		—	5		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	2.70V or above		—	4		
		1.68V or above (VCC) 1.65V or above (VCC2)		—	5		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	2.70V or above		—	6		
		1.68V or above (VCC) 1.65V or above (VCC2)		—	7		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO	2.70V or above	t_{GTOSK}	—	5	ns	Figure 2.46
		1.68V or above (VCC) 1.65V or above (VCC2)		—	6		
AGT	AGTIO, AGTEE input cycle	2.70V or above	t_{ACYC}*2	100	—	ns	Figure 2.47
		1.68V or above (VCC) 1.65V or above (VCC2)		100	—		
	AGTIO, AGTEE input high width, low width	2.70V or above	t_{ACKWH}, t_{ACKWL}	40	—	ns	
		1.68V or above (VCC) 1.65V or above (VCC2)		40	—		
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.70V or above	t_{ACYC2}	62.5	—	ns	
		1.68V or above (VCC) 1.65V or above (VCC2)		62.5	—		

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Table 2.38 I/O ports, POEG, GPT, AGT, ULPT and ADC12 trigger timing (3 of 3)

GPT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
ULPT	ULPTEE, ULPTEVI input cycle	2.70V or above	t_{ULCYC}*3	32	-	μs	Figure 2.48
		1.68V or above (VCC) 1.65V or above (VCC2)		32	-		
	ULPTEE, ULPTVI input high width, low width	2.70V or above	t_{ULCKWH}, t_{ULCKWL}	12	-	μs	
		1.68V or above (VCC) 1.65V or above (VCC2)		12	-		
	ULPTO, ULPTOA, ULPTOB output cycle	2.70V or above	t_{ULCYC2}	64	-	μs	
		1.68V or above (VCC) 1.65V or above (VCC2)		64	-		
ADC12	ADC12 trigger input pulse width	2.70V or above	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.49
		1.68V or above (VCC) 1.65V or above (VCC2)		3.0	—		

Note: t_{Icyc}: ICLK cycle, t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle, $t_{ULPTLCLK}$: ULPTLCLK cycle..
Note 1. For Cycle and Time, the longer time characteristics is applied.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.
Note 3. Constraints on input cycle:
ULPTEVI : $t_{Pcyc} \times 2 < t_{ULCYC}$ should be satisfied.
ULPTEE: $t_{ULPTLCLK} \times 2 < t_{ULCYC}$ should be satisfied.

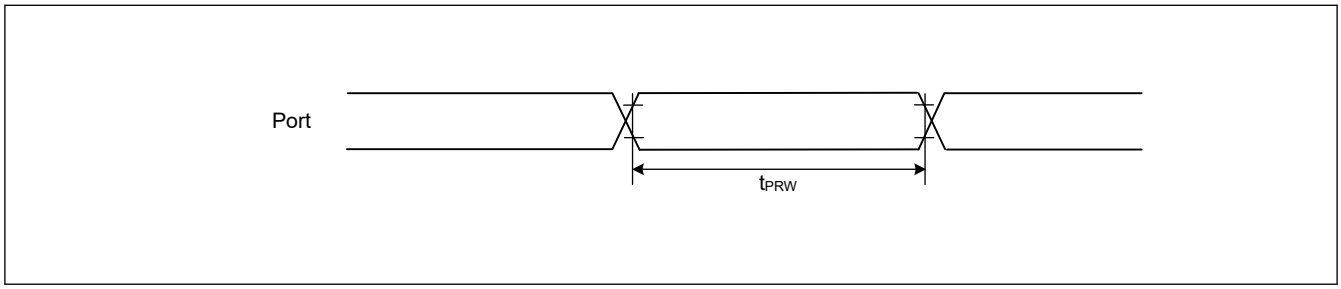


Figure 2.42 I/O ports input timing

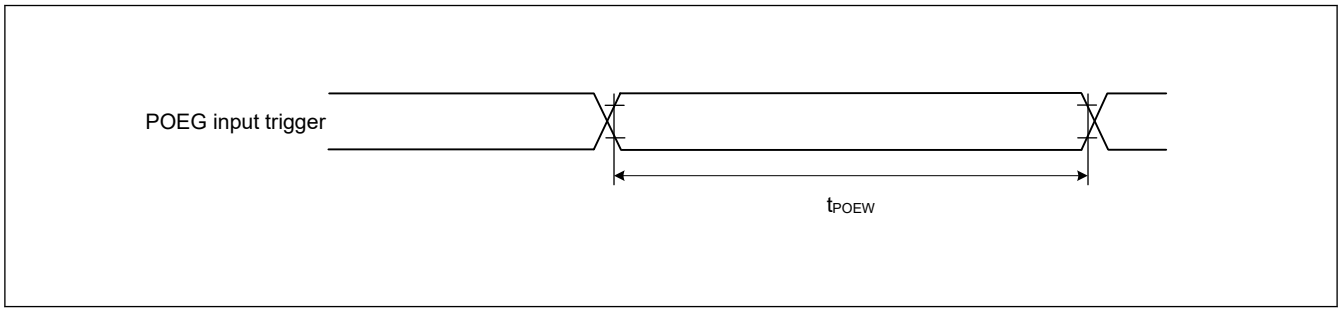


Figure 2.43 POEG input trigger timing

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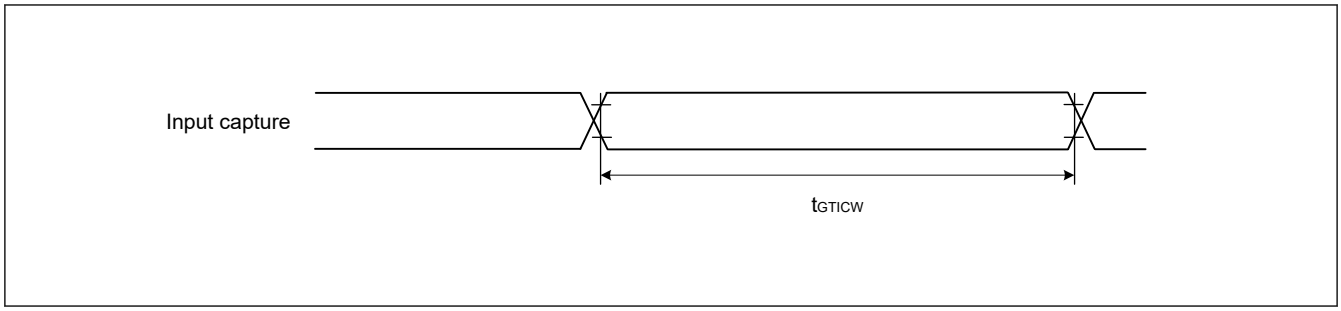


Figure 2.44 GPT input capture timing

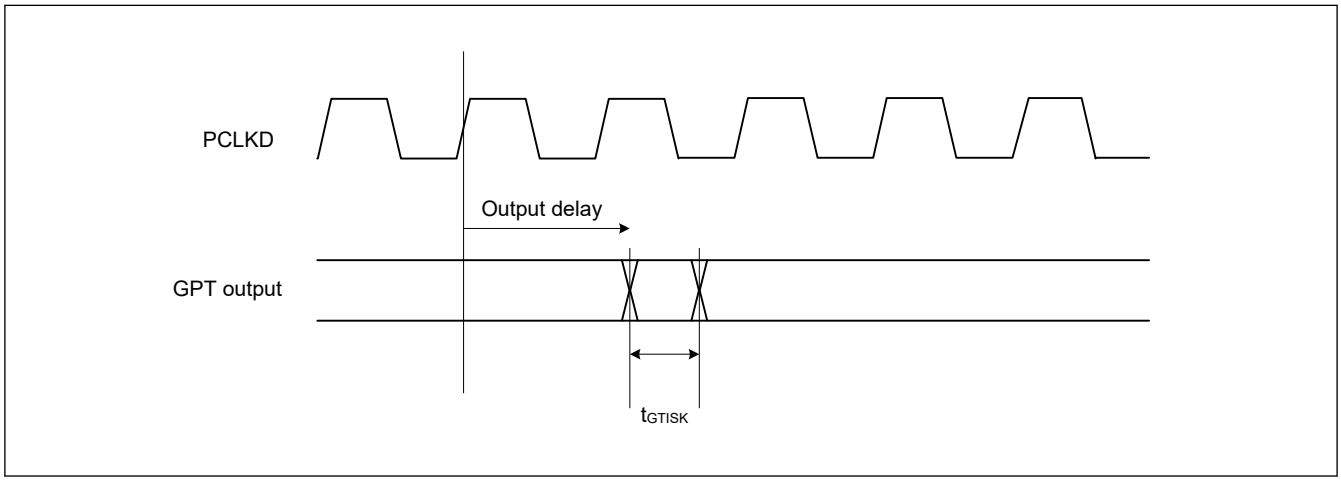


Figure 2.45 GPT output delay skew

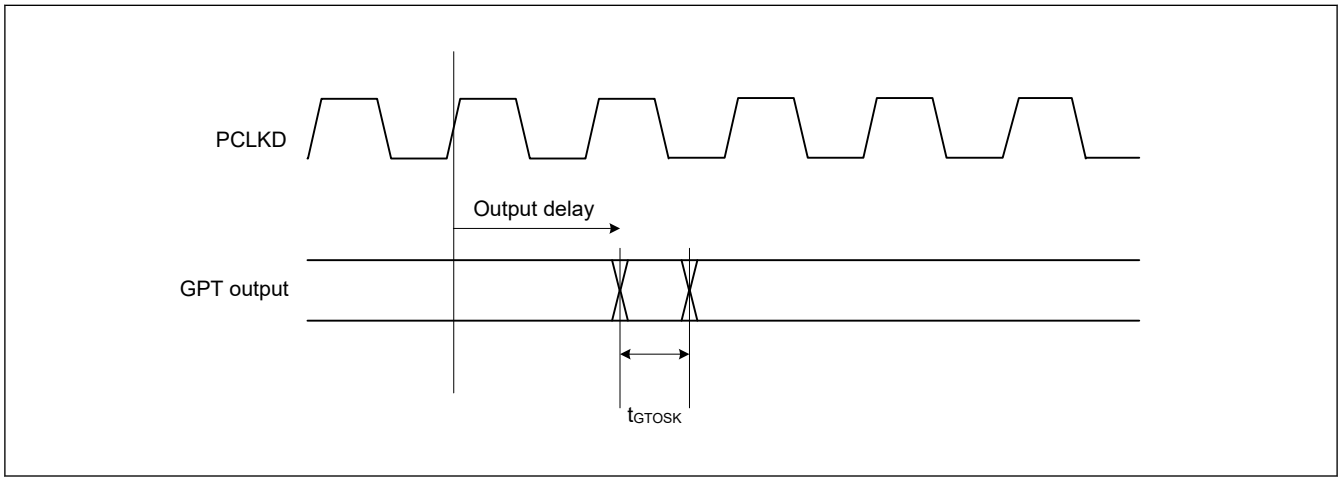


Figure 2.46 GPT output delay skew for OPS

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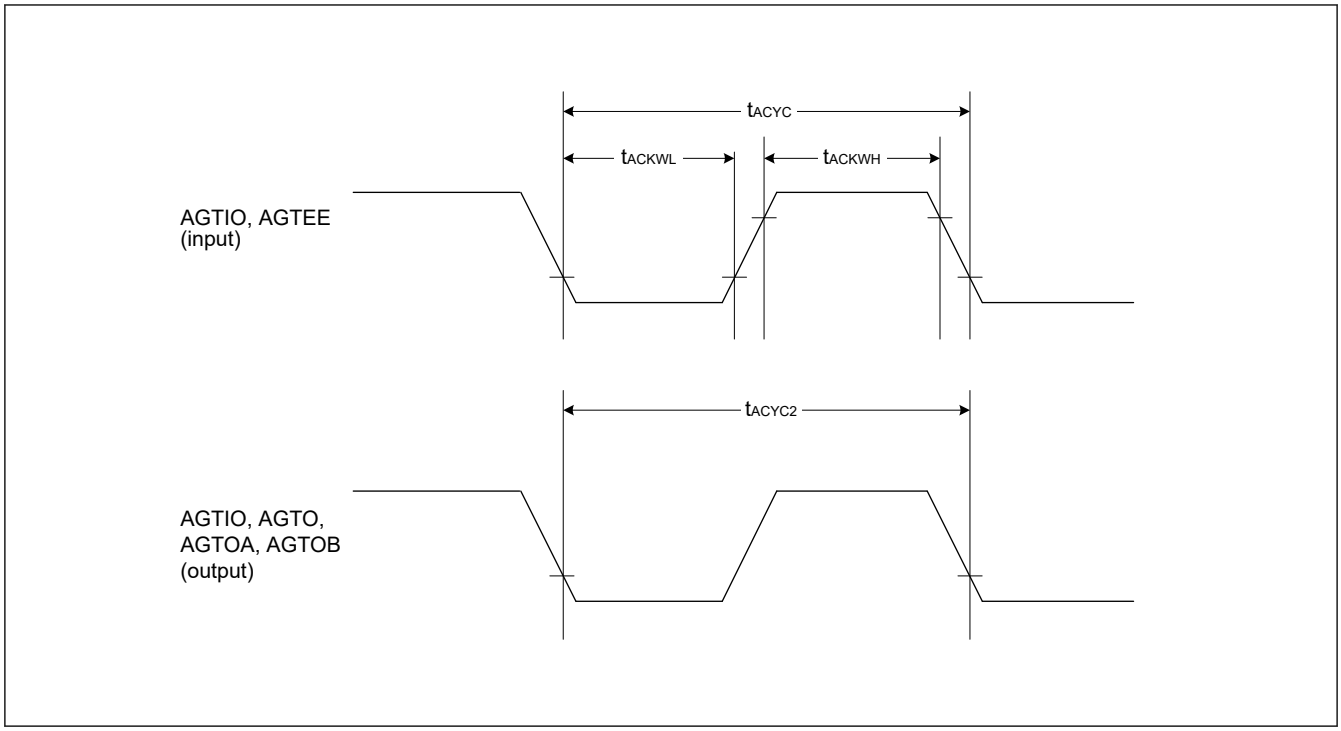


Figure 2.47 AGT input/output timing

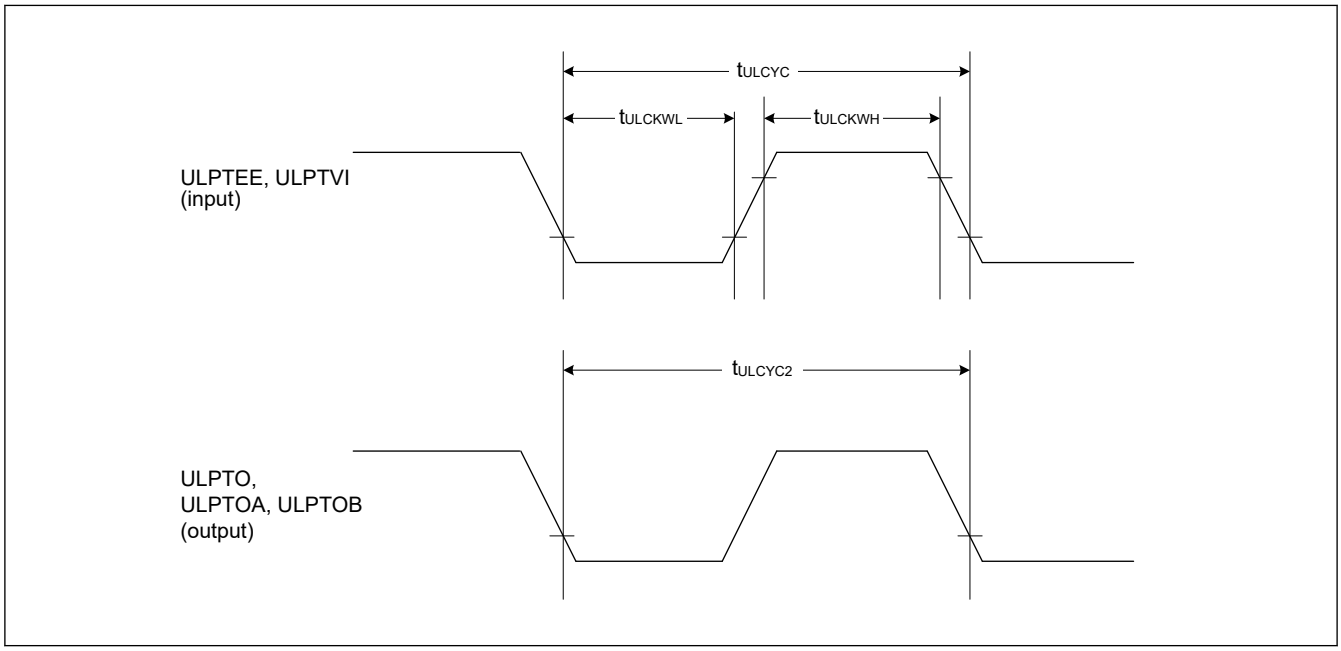


Figure 2.48 ULPT input/output timing

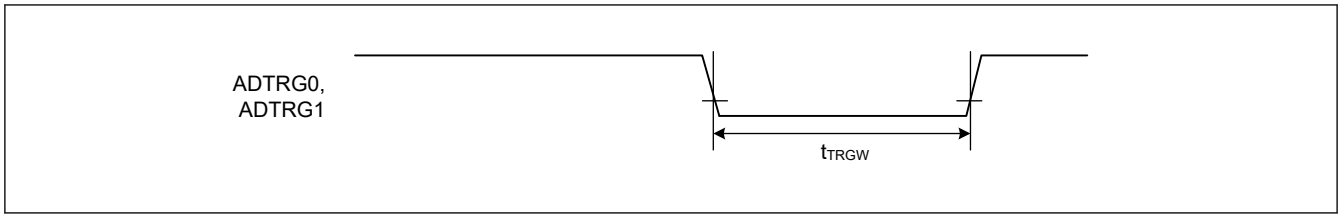


Figure 2.49 ADC12 trigger input timing

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2.3.8 CAC Timing

Table 2.39 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

2.3.9 SCI Timing

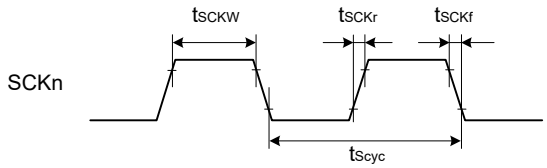
Table 2.40 SCI timing (Asynchronous mode)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter	VCC/VCC2	Symbol	Min	Max	Unit	Note
Input clock cycle	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{Scyc}	4.0	—	t_{Tcyc}	Figure 2.50
Input clock pulse width	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SCKW}	0.4	—	t_{Scyc}	
Input clock rise time	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SCKr}	—	0.1*1	t_{Scyc}	
Input clock fall time	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SCKf}	—	0.1*1	t_{Scyc}	
Output clock cycle	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{Scyc}	6.0	—	t_{Tcyc}	
Output clock pulse width	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SCKW}	0.4	—	t_{Scyc}	
Output clock rise time	2.70 V or above	t_{SCKr}	—	3.3	ns	
	1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		
Output clock fall time	2.70 V or above	t_{SCKf}	—	3.3	ns	
	1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		

Note: t_{Tcyc}: TCLK cycle.
Note 1. 1 µs at the longest

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Note: n = 0 to 4, 9

Figure 2.50 SCK clock input/output timing

Table 2.41 SCI timing (Simple SPI) (1 of 3)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master	—	2.70 V or above	t_{SPcyc}	2.0	65536	t_{Tcyc}	Figure 2.51
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	65536		
SCK clock cycle input	Slave	—	2.70 V or above		2.0	65536		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	65536		
SCK clock high pulse width	Master	—	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SPCKWH}	0.4	—	t_{SPcyc}	
	Slave	—						
SCK clock low pulse width	Master	—	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SPCKWL}	0.4	—	t_{SPcyc}	
	Slave	—						
SCK clock rise and fall time	Output	—	2.70 V or above	t_{SPCKr}, t_{SPCKf}	—	3.3	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		
	Input	—	2.70 V or above		—	0.1*3	t_{SPcyc}	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	0.1*3		
Data input setup time	Master	High Speed*1	2.70 V or above	t_{SU}	14.9 - (AST[2:0] settings)	—	ns	Figure 2.52, Figure 2.53
			1.68 V or above (VCC) 1.65 V or above (VCC2)		23.1 - (AST[2:0] settings)	—		
		Default*2	2.70 V or above		16.2 - (AST[2:0] settings)	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		23.8 - (AST[2:0] settings)	—		
	Slave	Default*2	2.70 V or above		2.5	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.5	—		

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Table 2.41 SCI timing (Simple SPI) (2 of 3)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Data input hold time	Master	High Speed*1	2.70 V or above	t_H	-3.2 + (AST[2:0] settings)	—	ns	Figure 2.52, Figure 2.53
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-3.2 + (AST[2:0] settings)	—		
		Default*2	2.70 V or above		-3.2 + (AST[2:0] settings)	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-3.2 + (AST[2:0] settings)	—		
	Slave	Default*2	2.70 V or above		2.5	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.5	—		
Data output delay	Master	High Speed*1	2.70 V or above	t_{OD}	—	3.0	ns	Figure 2.52, Figure 2.53
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	4.5		
		Default*2	2.70 V or above		—	3.5		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	5.5		
	Slave	High Speed*1	2.70 V or above		—	15.0		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	23.0		
		Default*2	2.70 V or above		—	21.0		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	29.0		
Data output hold time	Master	High Speed*1	2.70 V or above	t_{OH}	-3.0	—	ns	Figure 2.52, Figure 2.53
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-4.5	—		
		Default*2	2.70 V or above		-3.5	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-5.5	—		
	Slave	Default*2	2.70 V or above		0.0	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		0.0	—		
Data rise and fall time	Output	—	2.70 V or above	t_{Dr}, t_{Df}	—	3.3	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		
	Input	—	2.70 V or above		—	1.0	µs	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	1.0		
SS input setup time		—	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{LEAD}	1.0	—	t_{SPcyc}	Figure 2.54, Figure 2.55
SS input hold time		—	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{LAG}	1.0	—	t_{SPcyc}	
SS input rise and fall time		—	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SSLr}, t_{SSLf}	—	1.0	µs	—

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Table 2.41 SCI timing (Simple SPI) (3 of 3)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter	High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Slave access time	—	2.70 V or above	t_{SA}	—	3 × t_{Tcyc} + 25	ns	Figure 2.54, Figure 2.55
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	3 × t_{Tcyc} + 32		
Slave output release time	—	2.70 V or above	t_{REL}	—	3 × t_{Tcyc} + 25	ns	
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	3 × t_{Tcyc} + 32		

Note: t_{Tcyc}: TCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0, SCI1, SCI2, SCI3 and SCI9 are instance _A, SCI4 is instance _B.
Note 2. All pins of group membership can be used.
Note 3. 1 µs at the longest

Table 2.42 SCI timing (Clock synchronous mode) (1 of 4)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master	—	2.70 V or above	t_{Scyc}	2.0	—	t_{Tcyc}	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	—		
SCK clock cycle input	Slave	—	2.70 V or above		2.0	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	—		
SCK clock high pulse width	Master	—	2.70 V or above	t_{SCKWH}	0.4	—	t_{Scyc}	
	Slave		1.68 V or above (VCC) 1.65 V or above (VCC2)					
SCK clock low pulse width	Master	—	2.70 V or above	t_{SCKWL}	0.4	—	t_{Scyc}	
	Slave		1.68 V or above (VCC) 1.65 V or above (VCC2)					

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Table 2.42 SCI timing (Clock synchronous mode) (2 of 4)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock rise and fall time	Output	—	2.70 V or above	t_{SCKr}, $_{SCKf}$	—	3.3	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		
	Input	—	1.68 V or above (VCC) 1.65 V or above (VCC2)		—	0.1*3	t_{Scyc}	
Data input setup time	Master	High Speed*1	2.70 V or above	t_{SU}	15.1 - (AST[2:0] settings)	—	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		23.2 - (AST[2:0] settings)	—		
		Default*2	2.70 V or above		16.5 - (AST[2:0] settings)	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		24.2 - (AST[2:0] settings)	—		
	Slave	Default*2	2.70 V or above		3.3	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		5.3	—		
Data input hold time	Master	High Speed*1	2.70 V or above	t_H	-3.3 + (AST[2:0] settings)	—	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-3.3 + (AST[2:0] settings)	—		
		Default*2	2.70 V or above		-3.2 + (AST[2:0] settings)	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-3.2 + (AST[2:0] settings)	—		
	Slave	Default*2	2.70 V or above		3.0	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		5.0	—		

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Table 2.42 SCI timing (Clock synchronous mode) (3 of 4)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Data output delay	Master	High Speed*1	2.70 V or above	t_{OD}	—	5.0	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	5.0		
		Default*2	2.70 V or above		—	7.3		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	7.3		
	Slave	High Speed*1	2.70 V or above		—	15.0		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	23.0		
		Default*2	2.70 V or above		—	21.0		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		—	29.0		
Data output hold time	Master	High Speed*1	2.70 V or above	t_{OH}	-5.0	—	ns	
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-5.0	—		
		Default*2	2.70 V or above		-7.3	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		-7.3	—		
	Slave	High Speed*1	2.70 V or above		0	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		0	—		
		Default*2	2.70 V or above		0	—		
			1.68 V or above (VCC) 1.65 V or above (VCC2)		0	—		

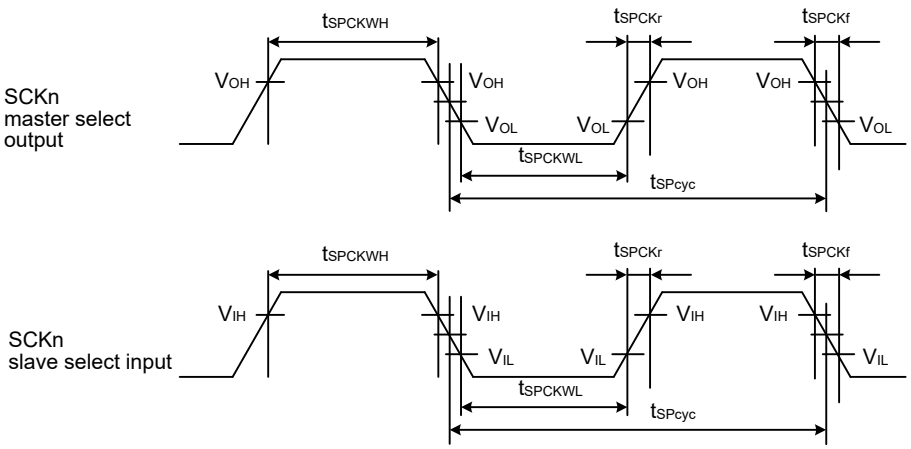
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Table 2.42 SCI timing (Clock synchronous mode) (4 of 4)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Data rise and fall time	Output	—	2.70 V or above	t_{Dr}, t_{Df}	—	3.3	ns	
		—	1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.6		
	Input	—	1.68 V or above (VCC) 1.65 V or above (VCC2)		—	1.0	µs	

Note: t_{Tcyc}: TCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0, SCI1, SCI2, SCI3 and SCI9 are instance _A, SCI4 is instance _B.
Note 2. All pins of group membership can be used.
Note 3. 1 µs at the longest



V_{OH} = 0.7 × VCC or 0.7 × VCC2, V_{OL} = 0.3 × VCC or 0.3 × VCC2,
V_{IH} = 0.7 × VCC or 0.7 × VCC2, V_{IL} = 0.3 × VCC or 0.3 × VCC2

Note: n = 0 to 4, 9

Figure 2.51 SCI simple SPI mode clock timing

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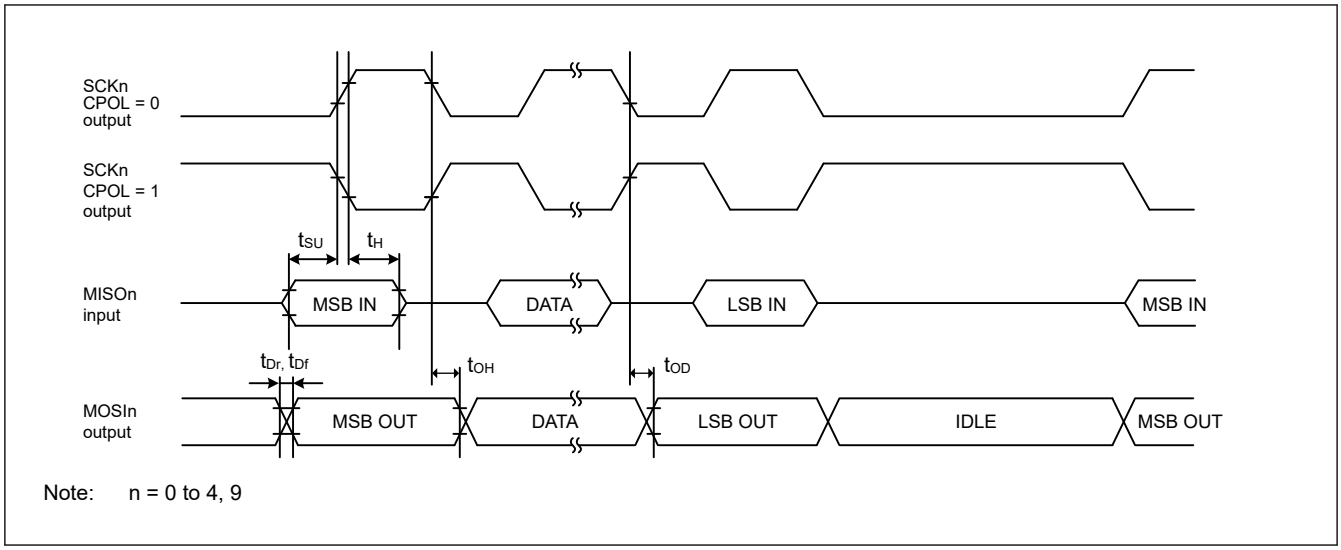


Figure 2.52 SCI simple SPI mode timing for master when CPHA = 0

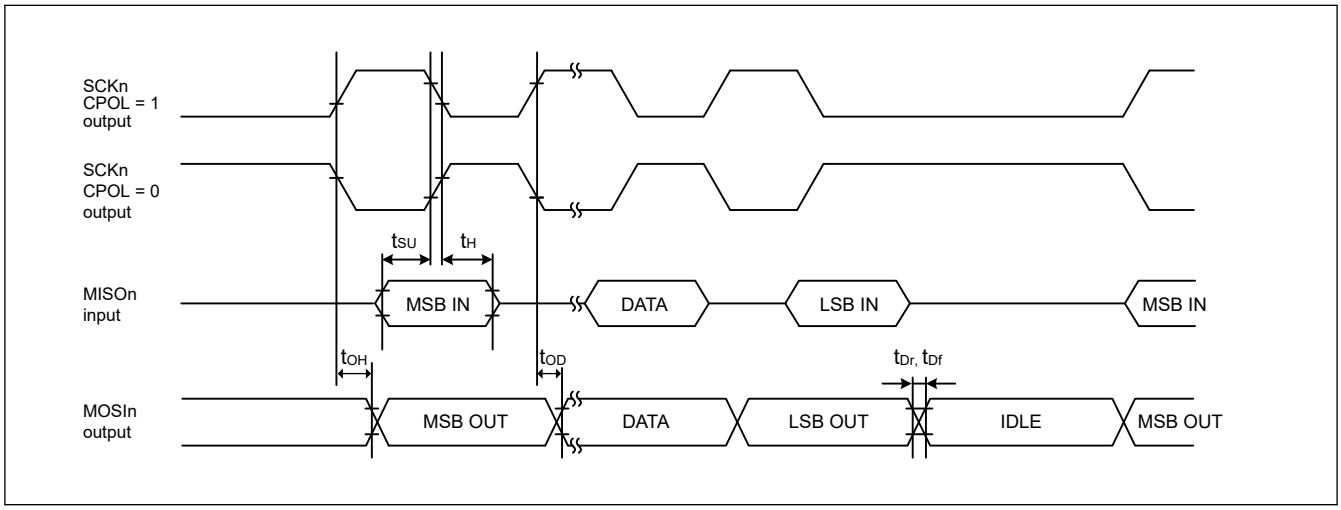


Figure 2.53 SCI simple SPI mode timing for master when CPHA = 1

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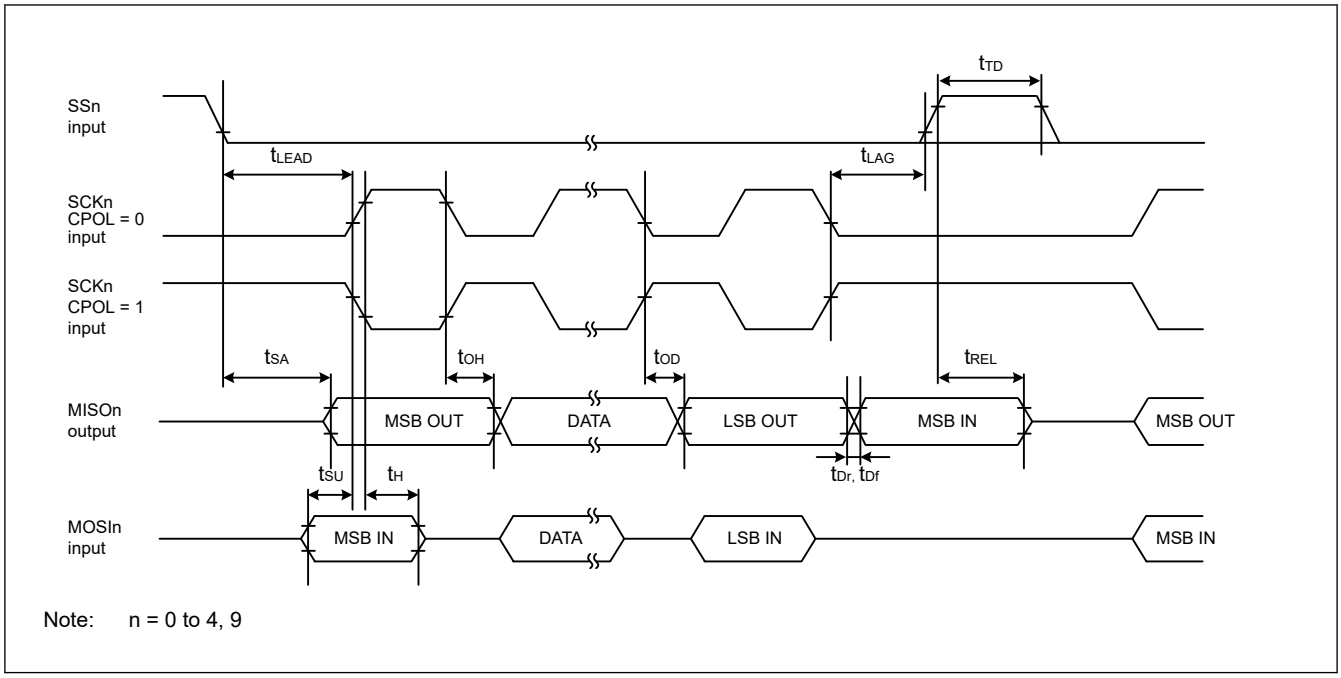


Figure 2.54 SCI simple SPI mode timing for slave when CPHA = 0

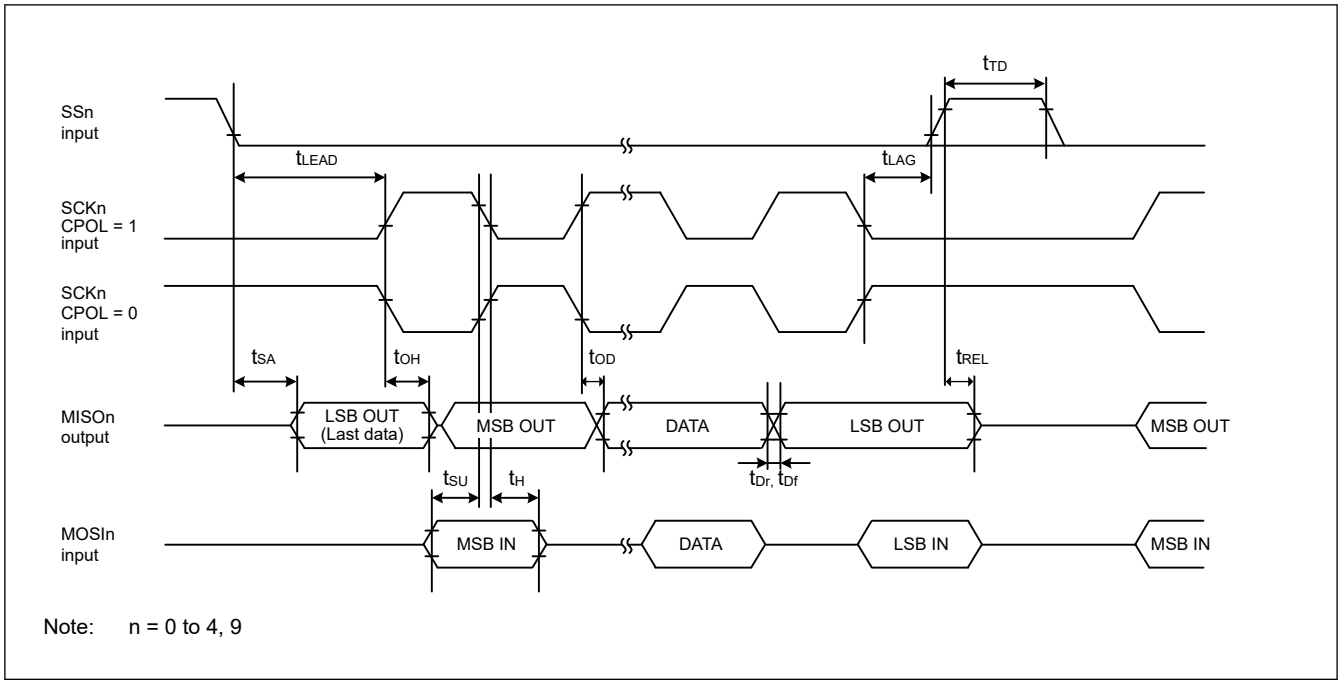


Figure 2.55 SCI simple SPI mode timing for slave when CPHA = 1

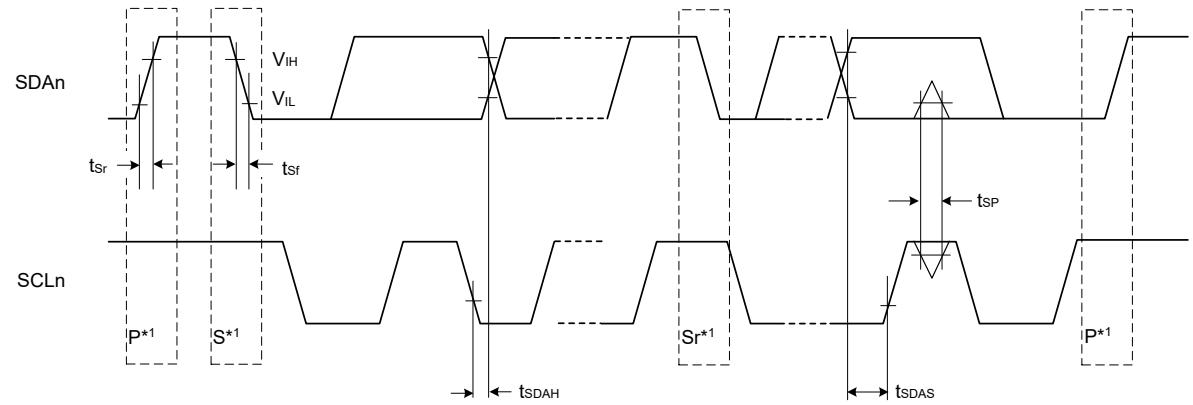
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Table 2.43 SCI timing (Simple IIC mode)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
VCC: 1.68V or above, VCC2: 1.65V or above
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		Symbol	Min	Max	Unit	Note
Simple IIC (Standard mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	

Note: t_{Tcyc}: TCLK cycle.
Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7 or VCC2 × 0.7
V_{IL} = VCC × 0.3 or VCC2 × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 4, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.56 SCI simple IIC mode timing

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2.3.10 SPI Timing

Table 2.44 SPI timing (1 of 4)

Conditions:

1. High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		VCC/VCC2	Symbol	Min	Max	Unit	Note
RSPCK clock cycle	Master	3.00 V or above	t_{SPcyc}	2.0	4096	t_{Tcyc}	Figure 2.57
		2.70 V or above		2.0	4096		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	4096		
	Slave	3.00 V or above		2.0	—		
		2.70 V or above		2.0	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	—		
RSPCK clock high pulse width	Master	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
	Slave	1.68 V or above (VCC) 1.65 V or above (VCC2)		0.4	—	t_{SPcyc}	
RSPCK clock low pulse width	Master	1.68 V or above (VCC) 1.65 V or above (VCC2)	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
	Slave	1.68 V or above (VCC) 1.65 V or above (VCC2)		0.4	—	t_{SPcyc}	
RSPCK clock rise and fall time	Output	3.00 V or above	t_{SPCKr}, t_{SPCKf}	—	1.66	ns	
		2.70 V or above		—	3.30		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.60		
	Input	3.00 V or above		—	0.1*1	t_{SPcyc}	
		2.70 V or above		—	0.1*1		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	0.1*1		

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Table 2.44 SPI timing (2 of 4)

Conditions:

1. High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance “_A” or “_B” to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		VCC/VCC2	Symbol	Min	Max	Unit	Note
Data input setup time	Master	3.00 V or above	t_{SU}	-2.5	—	ns	Figure 2.58, Figure 2.59
		2.70 V or above		0.0	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		0.0	—		
	Slave	3.00 V or above		2.5	—		
		2.70 V or above		2.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		2.5	—		
Data input hold time	Master	3.00 V or above	t_{H}	7.5	—	ns	
		2.70 V or above		7.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		9.5	—		
	Slave	3.00 V or above		2.5	—		
		2.70 V or above		2.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		5.5	—		
SSL setup time	Master	3.00 V or above	t_{LEAD}	1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10	ns	
		2.70 V or above		1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10		
	Slave	3.00 V or above		4.0	—	t_{Tcyc}	
		2.70 V or above		4.0	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	—		
SSL hold time	Master	3.00 V or above	t_{LAG}	1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10	ns	
		2.70 V or above		1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		1 × t_{SPcyc} - 10	8 × t_{SPcyc} + 10		
	Slave	3.00 V or above		4.0	—	t_{Tcyc}	
		2.70 V or above		4.0	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		4.0	—		

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Table 2.44 SPI timing (3 of 4)

Conditions:

1. High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		VCC/VCC2	Symbol	Min	Max	Unit	Note
TI SSP SS input setup time	Slave	3.00 V or above	t_{TISS}	2.5	—	ns	Figure 2.63
		2.70 V or above		2.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		2.5	—		
TI SSP SS input hold time	Slave	3.00 V or above	t_{TISH}	2.5	—	ns	
		2.70 V or above		2.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		5.5	—		
TI SSP next-access time	Slave	3.00 V or above	t_{TIND}	$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—	ns	
		2.70 V or above		$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—		
TI SSP master SS output delay	Master	3.00 V or above	t_{TISSOD}	—	4.0	ns	Figure 2.60
		2.70 V or above		—	8.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	8.0		
Data output delay time	Master	3.00 V or above	t_{OD1}	—	2.0	ns	Figure 2.58, Figure 2.59
		2.70 V or above		—	3.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.0		
		3.00 V or above	t_{OD2}	—	2.5		
		2.70 V or above		—	2.5		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	4.5		
	Slave	3.00 V or above	t_{OD}	—	12.5		
		2.70 V or above		—	16.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	24.0		
Data output hold time	Master	3.00 V or above	t_{OH}	-2.5	—	ns	Figure 2.58, Figure 2.59
		2.70 V or above		-2.5	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		-4.5	—		
	Slave	3.00 V or above		0.0	—		
		2.70 V or above		0.0	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		0.0	—		

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Table 2.44 SPI timing (4 of 4)

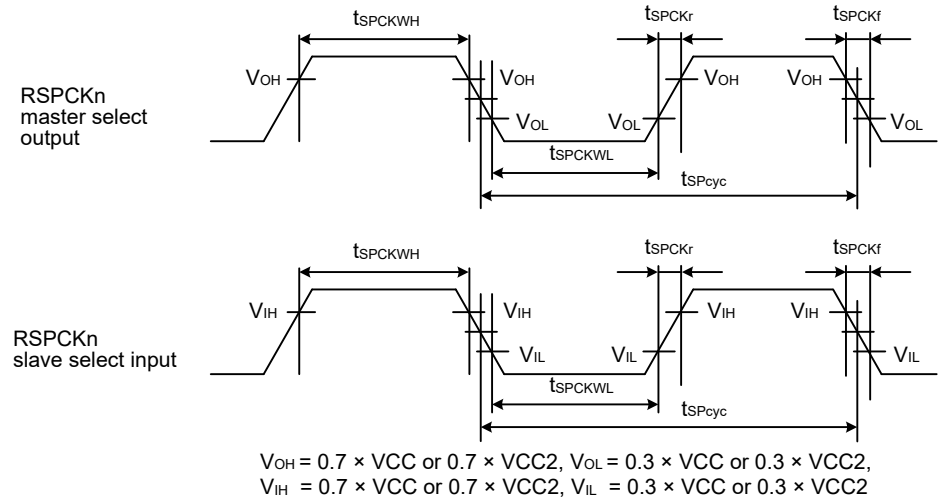
Conditions:

1. High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance “_A” or “_B” to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		VCC/VCC2	Symbol	Min	Max	Unit	Note
Successive transmission delay time	Master	3.00 V or above	t_{TD}	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Tcyc}$	ns	Figure 2.58, Figure 2.59
		2.70 V or above		$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Tcyc}$		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Tcyc}$		
	Slave	3.00 V or above		t_{Tcyc}	—	ns	
		2.70 V or above		t_{Tcyc}	—		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		t_{Tcyc}	—		
MOSI and MISO rise and fall time	Output	3.00 V or above	t_{Dr}, t_{Df}	—	1.66	ns	Figure 2.58, Figure 2.59
		2.70 V or above		—	3.30		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.60		
	Input	3.00 V or above		—	1.0	µs	
		2.70 V or above		—	1.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	1.0		
SSL rise and fall time	Output	3.00- V or above	t_{SSLr}, t_{SSLf}	—	1.66	ns	Figure 2.58, Figure 2.59
		2.70 V or above		—	3.30		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	6.60		
	Input	3.00 V or above		—	1.0	µs	
		2.70 V or above		—	1.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	1.0		
Slave access time	Slave	3.00 V or above	t_{SA}	—	20.0	ns	Figure 2.61, Figure 2.62
		2.70 V or above		—	20.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	25.0		
Slave output release time	Slave	3.00 V or above	t_{REL}	—	20.0	ns	
		2.70 V or above		—	20.0		
		1.68 V or above (VCC) 1.65 V or above (VCC2)		—	25.0		

Note: t_{Tcyc}: TCLK cycle.
Note 1. 1 µs at the longest

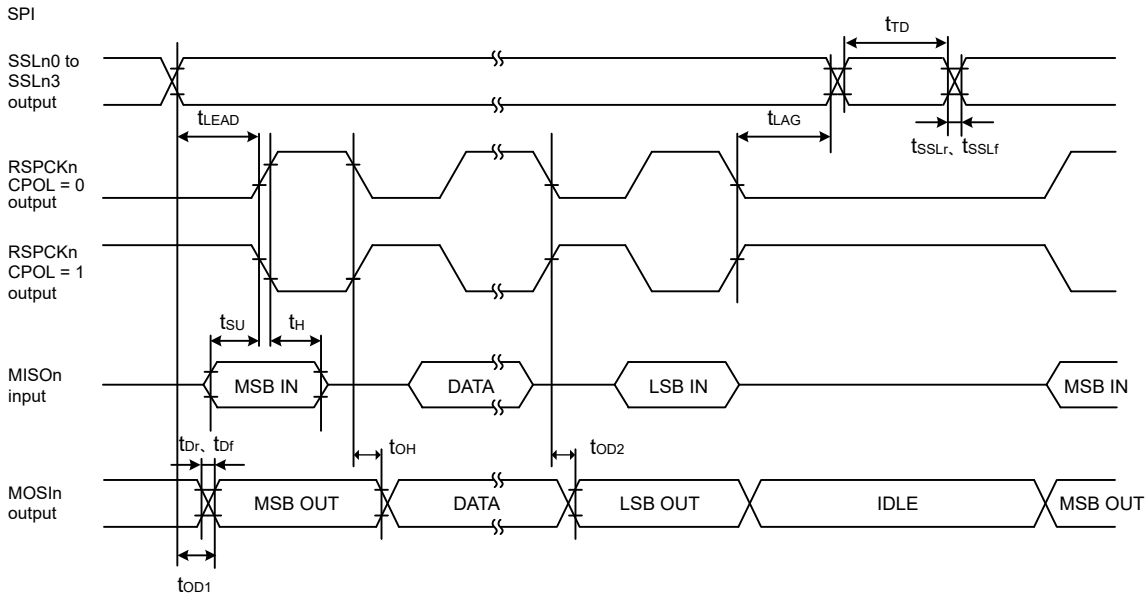
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V_{OH} = 0.7 × VCC or 0.7 × VCC2, V_{OL} = 0.3 × VCC or 0.3 × VCC2,
V_{IH} = 0.7 × VCC or 0.7 × VCC2, V_{IL} = 0.3 × VCC or 0.3 × VCC2

Note: n = A or B

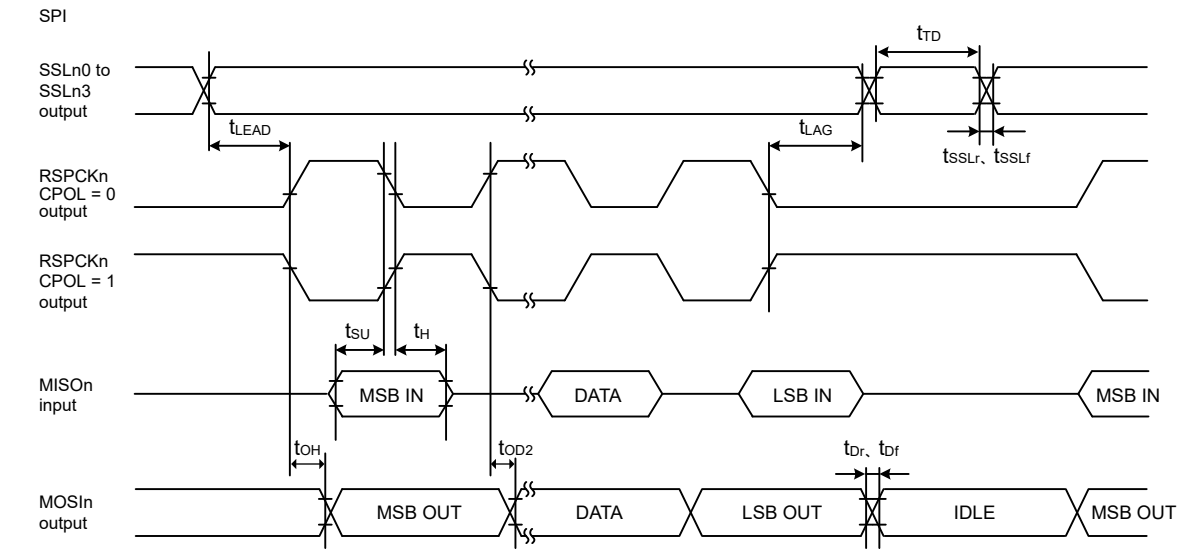
Figure 2.57 SPI clock timing



Note: n = A or B

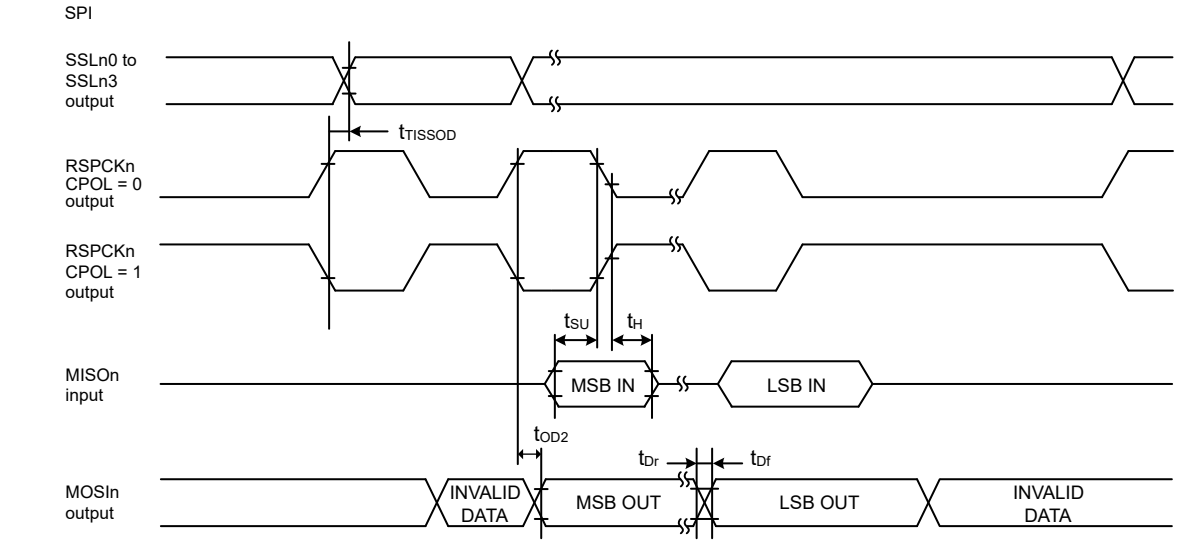
Figure 2.58 SPI timing for Motorola SPI master when CPHA = 0

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Note: n = A or B

Figure 2.59 SPI timing for Motorola SPI master when CPHA = 1



Note: n = A or B

Figure 2.60 SPI timing for TI SSP master

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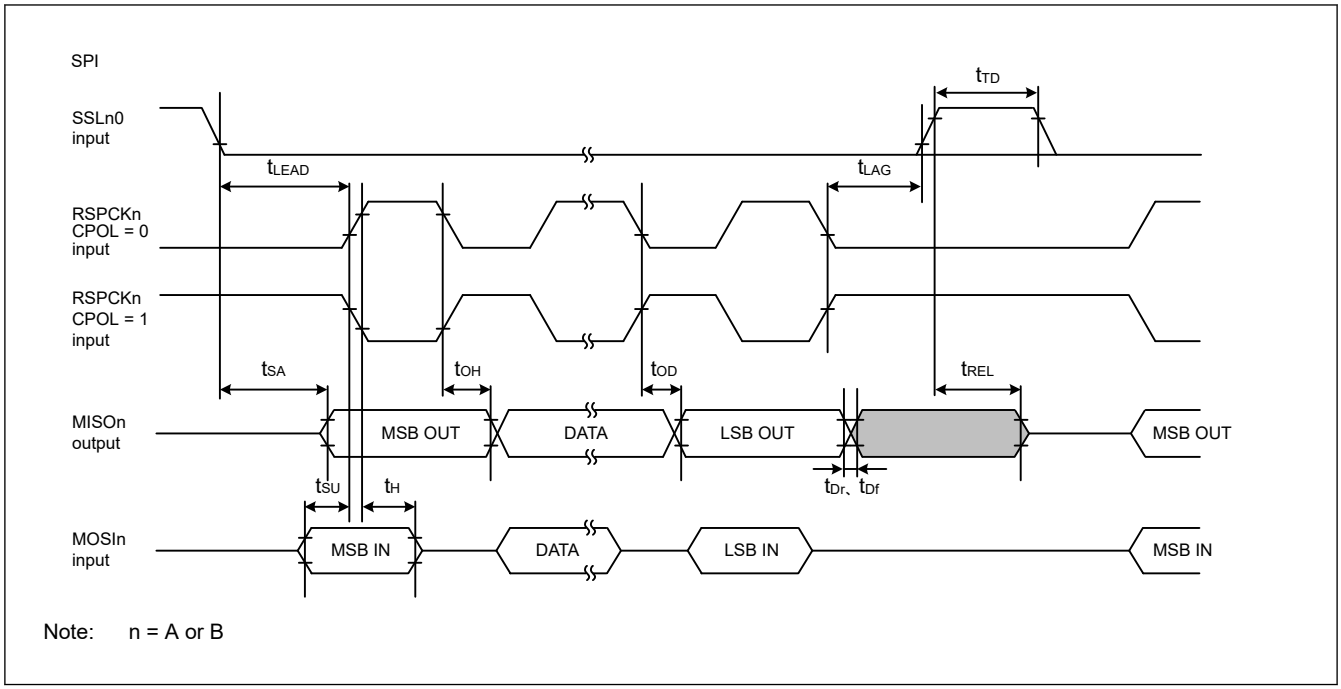


Figure 2.61 SPI timing for Motorola SPI slave when CPHA = 0

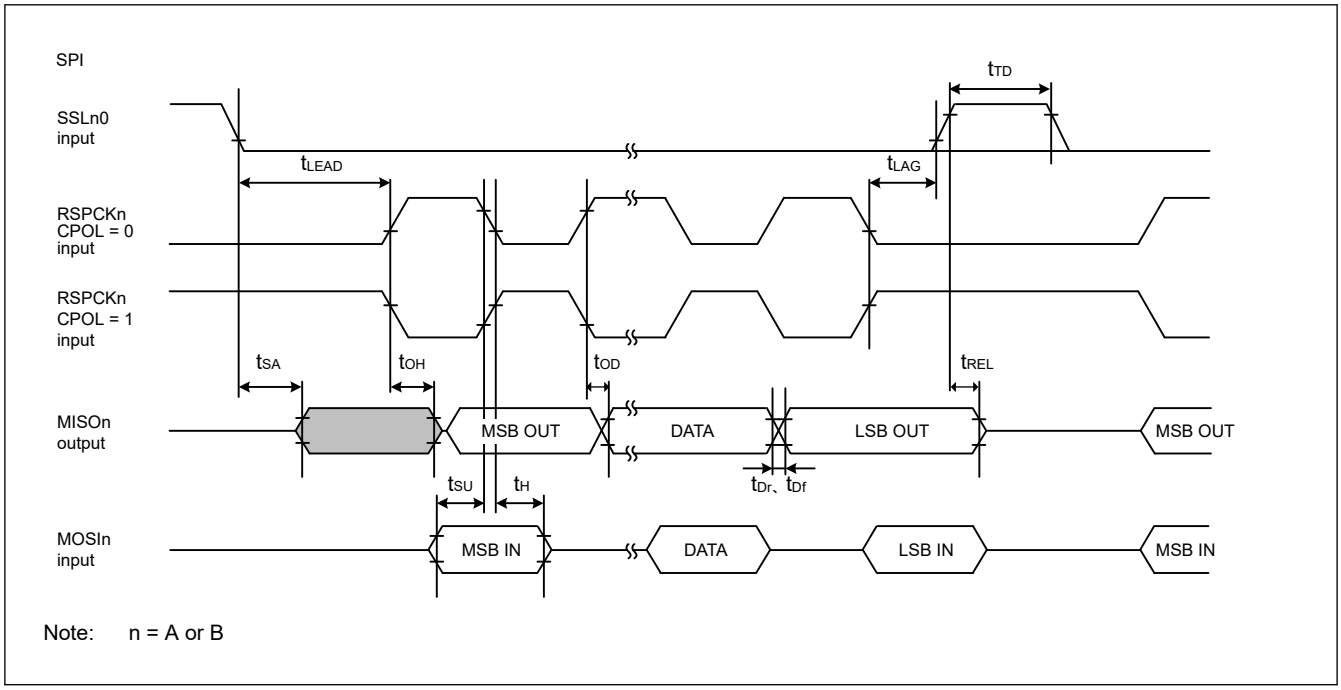


Figure 2.62 SPI timing for Motorola SPI slave when CPHA = 1

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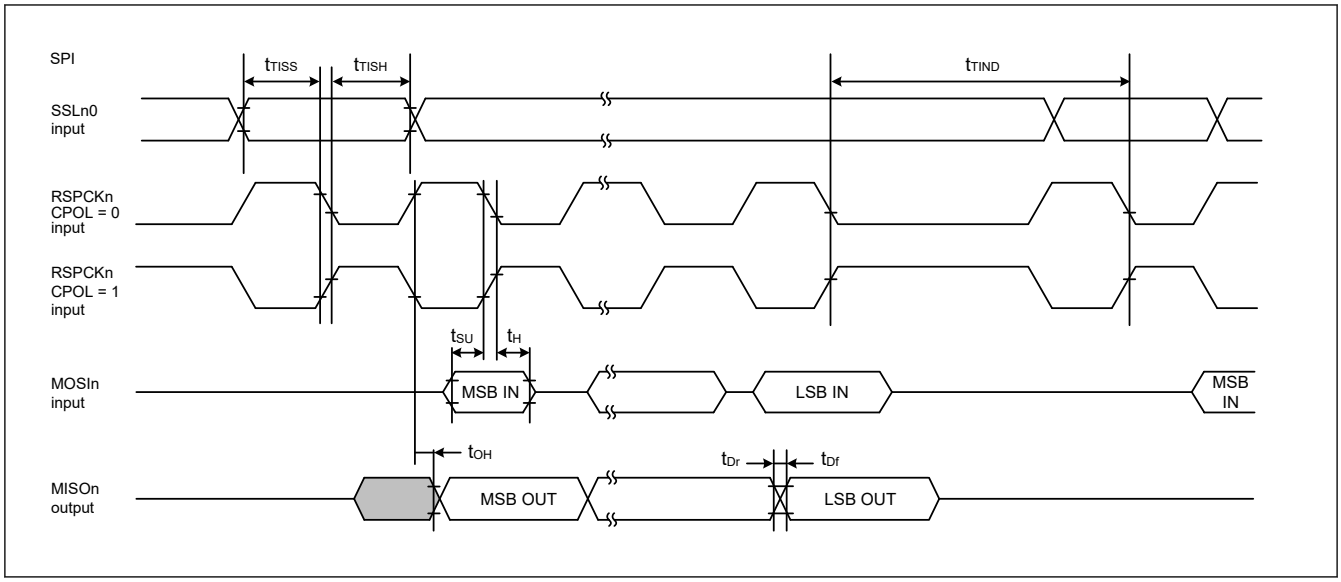


Figure 2.63 SPI timing for TI SSP slave when transmit with delay between frames

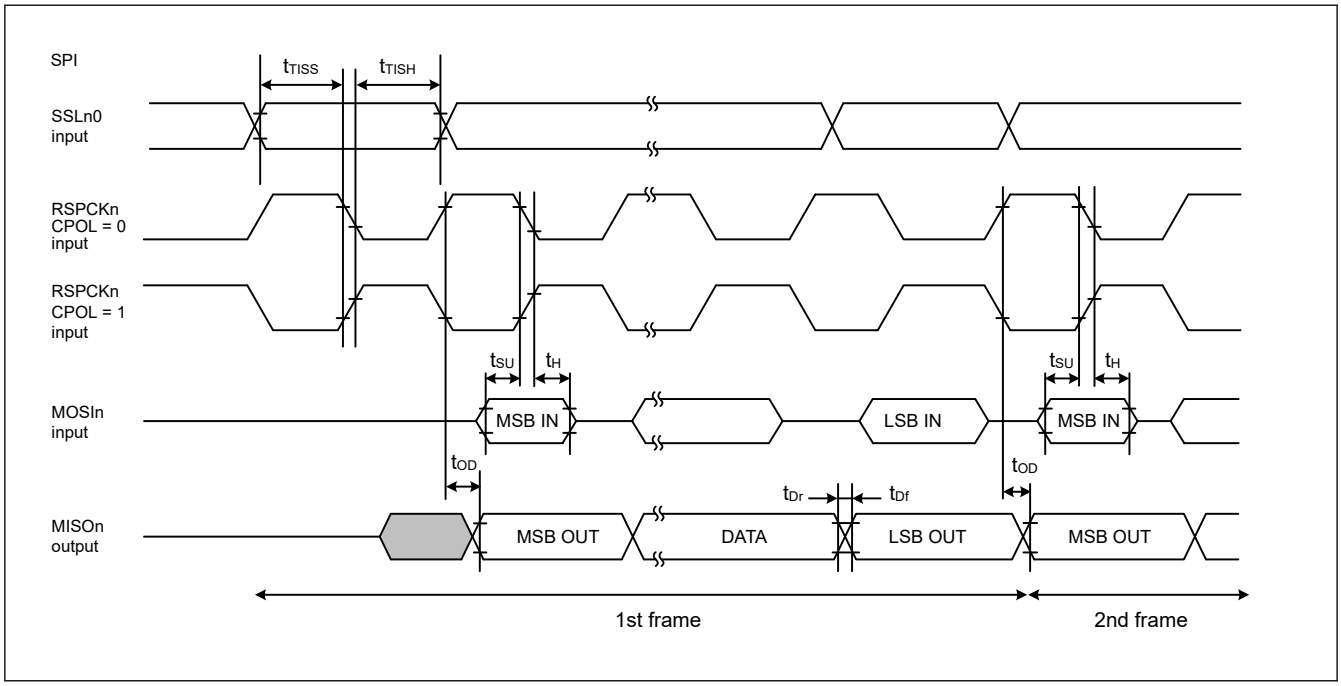


Figure 2.64 SPI timing for TI SSP slave when transmit with no delay between frames

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2.3.11 IIC Timing

Table 2.45 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected when VCC is 2.70 V or above, High drive output is selected when VCC is 1.68 to 1.95 V in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B
(2) The following pins do not require setting: SCL0_A, SDA0_A. SCL1_A, SDA1_A
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership.
For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Standard mode, SMBus) ICFER.FMPE = 0 when VCC is 2.70 V or above, ICFER.FMPE = 1 when VCC is 1.68 to 1.95 V	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.65
			1.68 to 1.95 V				
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SCL, SDA rise time	t_{Sr}	2.70 V or above	—	1000	ns	
			1.68 to 1.95 V				
	SCL, SDA fall time	t_{Sf}	2.70 V or above	—	300	ns	
			1.68 to 1.95 V				
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
			1.68 to 1.95 V				
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
			1.68 to 1.95 V				
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
			1.68 to 1.95 V				
	Repeated START condition input setup time	t_{STAS}	2.70 V or above	1000	—	ns	
			1.68 to 1.95 V				
	STOP condition input setup time	t_{STOS}	2.70 V or above	1000	—	ns	
			1.68 to 1.95 V				
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 50	—	ns	
			1.68 to 1.95 V				
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
			1.68 to 1.95 V				
	SCL, SDA capacitive load	C_b	2.70 V or above	—	400	pF	
			1.68 to 1.95 V				

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Table 2.45 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected when VCC is 2.70 V or above, High drive output is selected when VCC is 1.68 to 1.95 V in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B
(2) The following pins do not require setting: SCL0_A, SDA0_A. SCL1_A, SDA1_A
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership.
For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Fast mode) ICFER.FMPE = 0 when VCC is 2.70 V or above, ICFER.FMPE = 1 when VCC is 1.68 to 1.95 V	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.65
			1.68 to 1.95 V				
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SCL, SDA rise time	t_{Sr}	2.70 V or above	20	300	ns	
			1.68 to 1.95 V				
	SCL, SDA fall time	t_{Sf}	2.70 V or above	20 × (external pullup voltage/5.5 V)*1	300	ns	
			1.68 to 1.95 V				
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
			1.68 to 1.95 V				
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
			1.68 to 1.95 V				
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 300	—	ns	
			1.68 to 1.95 V				
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
			1.68 to 1.95 V				
	Repeated START condition input setup time	t_{STAS}	2.70 V or above	300	—	ns	
			1.68 to 1.95 V				
	STOP condition input setup time	t_{STOS}	2.70 V or above	300	—	ns	
			1.68 to 1.95 V				
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 50	—	ns	
			1.68 to 1.95 V				
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
			1.68 to 1.95 V				
	SCL, SDA capacitive load	C_b	2.70 V or above	—	400	pF	
			1.68 to 1.95 V				

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, and SDA1_A.

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Table 2.46 IIC timing (2)

Setting of the SCL0_A, SDA0_A, SCL1_A, SDA1_A pins are not required with the port drive capability bit in the PmnPFS register.

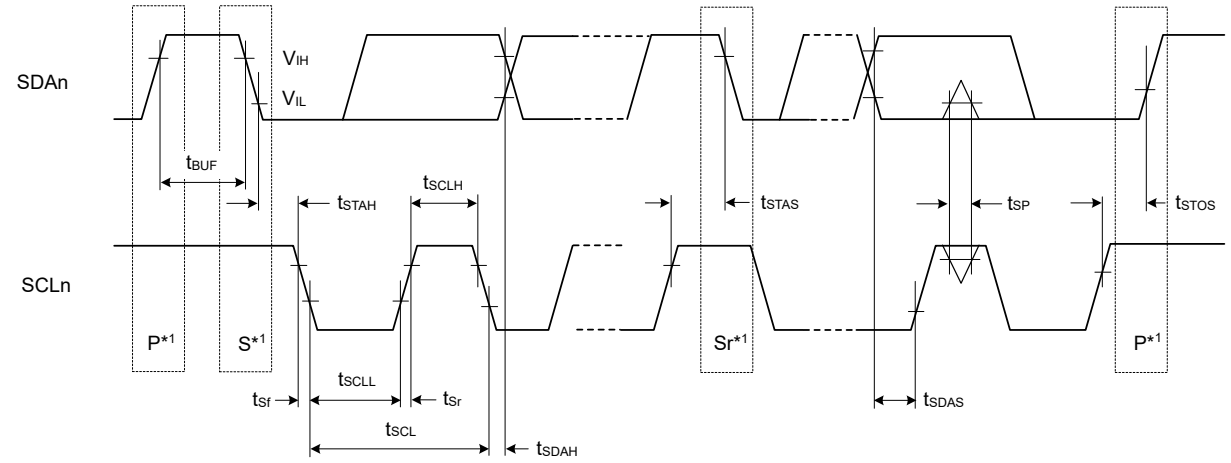
Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 240	—	ns	Figure 2.65
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	2.70 V or above	—	120	ns	
	SCL, SDA fall time	t_{Sf}	2.70 V or above	20 × (external pullup voltage/ 5.5V)	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 120	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	2.70 V or above	120	—	ns	
	Stop condition input setup time	t_{STOS}	2.70 V or above	120	—	ns	
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
	SCL, SDA capacitive load	C_b*1	2.70 V or above	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, tPcyc: PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 1. Cb indicates the total capacity of the bus line.

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Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.65 I^2C bus interface input/output timing

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2.3.12 I3C Timing

Table 2.47 IIC timing(1)-1

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	2.70 V or above, 1.68 to 1.95 V	10 (18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above, 1.68 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above, 1.68 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above, 1.68 to 1.95 V	—	1000	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above, 1.68 to 1.95 V	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above, 1.68 to 1.95 V	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above, 1.68 to 1.95 V	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above, 1.68 to 1.95 V	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above, 1.68 to 1.95 V	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above, 1.68 to 1.95 V	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	2.70 V or above, 1.68 to 1.95 V	1000	—	ns
	STOP condition input setup time	t_{STOS}	2.70 V or above, 1.68 to 1.95 V	1000	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above, 1.68 to 1.95 V	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above, 1.68 to 1.95 V	0	—	ns
	SCL, SDA capacitive load	C_b*1	2.70 V or above, 1.68 to 1.95 V	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: TCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

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Table 2.48 IIC timing(1)-2

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	2.70 V or above, 1.68 to 1.95 V	10 (18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above, 1.68 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above, 1.68 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above, 1.68 to 1.95 V	20	300	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above, 1.68 to 1.95 V	20 × (external pull-up voltage/3.6 V)	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above, 1.68 to 1.95 V	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above, 1.68 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled		2.70 V or above, 1.68 to 1.95 V	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above, 1.68 to 1.95 V	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled		2.70 V or above, 1.68 to 1.95 V	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	2.70 V or above, 1.68 to 1.95 V	300	—	ns
	STOP condition input setup time	t_{STOS}	2.70 V or above, 1.68 to 1.95 V	300	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above, 1.68 to 1.95 V	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above, 1.68 to 1.95 V	0	—	ns
	SCL, SDA capacitive load	C_b*1	2.70 V or above, 1.68 to 1.95 V	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: TCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

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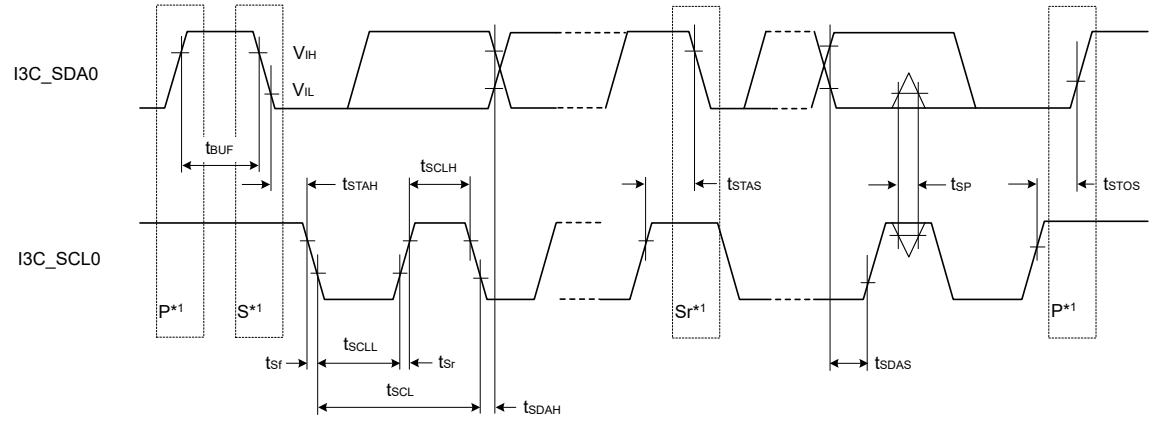
Table 2.49 IIC timing(1)-3

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Fast-mode +) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	2.70 V or above	10 (18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above	5 (9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above	5 (9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above	—	120	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above	20 × (external pull-up voltage/3.3V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	5 (9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled			5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120		ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled			1(5) × t_{I3Ccyc} + t_{Tcyc} + 120		ns
	Restart condition input setup time	t_{STAS}	2.70 V or above	120	—	ns
	Stop condition input setup time	t_{STOS}	2.70 V or above	120	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns
	SCL, SDA capacitive load	C_b*1	2.70 V or above	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle. t_{Tcyc}: TCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

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Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA (BFCTL.FMPE = 0)
V_{OL} = 0.4 V, I_{OL} = 15 mA (BFCTL.FMPE = 1)

Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.66 I^2C bus interface input/output timing

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Table 2.50 IIC timing(2)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	VCC	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	3.00 V or above	47 (49) × t_{I3Ccyc}	—	ns
				1.68 to 1.95 V	48 (50) × t_{I3Ccyc}	—	
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	3.00 V or above	36 (37) × t_{I3Ccyc}	—	ns
				1.68 to 1.95 V	31 (32) × t_{I3Ccyc}	—	
		Cb = 100 pF		3.00 V or above	18 (19) × t_{I3Ccyc}	—	
				1.68 to 1.95 V	19 (20) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	3.00 V or above	61 (62) × t_{I3Ccyc}	—	ns
				1.68 to 1.95 V	61 (62) × t_{I3Ccyc}	—	
		Cb = 100 pF		3.00 V or above	29 (30) × t_{I3Ccyc}	—	
				1.68 to 1.95 V	29 (30) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	3.00 V or above	—	80	ns
				1.68 to 1.95 V	—	80	
		Cb = 100 pF		3.00 V or above	—	40	
				1.68 to 1.95 V	—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	3.00 V or above	—	160	ns
				1.68 to 1.95 V	—	160	
		Cb = 100 pF		3.00 V or above	—	80	
				1.68 to 1.95 V	—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	3.00 V or above	—	80	ns
				1.68 to 1.95 V	—	80	
		Cb = 100 pF		3.00 V or above	—	40	
				1.68 to 1.95 V	—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	3.00 V or above	—	160	ns
				1.68 to 1.95 V	—	160	
		Cb = 100 pF		3.00 V or above	—	80	
				1.68 to 1.95 V	—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	3.00 V or above	0	1 (1) × t_{I3Ccyc}	ns
				1.68 to 1.95 V	0	1 (1) × t_{I3Ccyc}	
	Repeated START condition input setup time		t_{STAS}	3.00 V or above	40	—	ns
				1.68 to 1.95 V	40	—	
	STOP condition input setup time		t_{STOS}	3.00 V or above	40	—	ns
				1.68 to 1.95 V	40	—	
	Data input setup time		t_{SDAS}	3.00 V or above	10	—	ns
				1.65 to 1.95 V	10	—	
	Data input hold time	Cb = 400 pF	t_{SDAH}	3.00 V or above	0	150	ns
				1.68 to 1.95 V	0	150	
		Cb = 100 pF		3.00 V or above	0	70	
				1.68 to 1.95 V	0	70	
	SCL, SDA capacitive load		C_b*1	3.00 V or above	—	400	pF
				1.68 to 1.95 V	—	400	

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Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

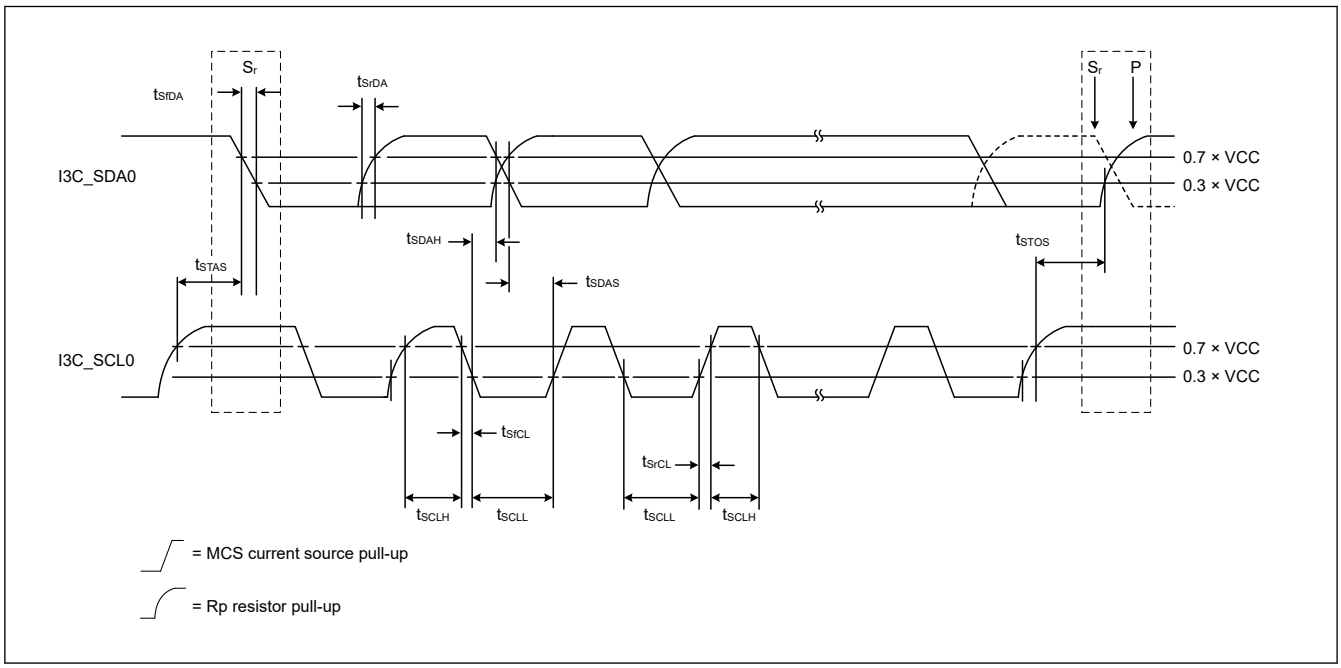


Figure 2.67 I²C bus interface input/output timing (Hs-mode)

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Table 2.51 I3C timing (Open Drain Timing Parameters)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	3.00 V or above	200	—	ns	Figure 2.70
			1.68 to 1.95 V	200	—		
		$t_{DIG_OD_L}$	3.00 V or above	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	Figure 2.70
			1.68 to 1.95 V	t_{LOW_ODmin} + t_{fDA_ODmin}	—		
	SCL Clock High Period	t_{HIGH} *3 *4	3.00 V or above	—	41	ns	Figure 2.68
			1.68 to 1.95 V	—	41		
		t_{DIG_H}	3.00 V or above	—	t_{HIGH} + t_{CF}	ns	Figure 2.68
			1.68 to 1.95 V	—	t_{HIGH} + t_{CF}		
	SDA Signal Fall Time	t_{fDA_OD}	3.00 V or above	t_{CF}	12	ns	Figure 2.70
			1.68 to 1.95 V	t_{CF}	12		
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	3.00 V or above	12	—	ns	Figure 2.69
			1.68 to 1.95 V	18	—		
	Clock After START (S) Condition	t_{CAS} *5 *6	3.00 V or above	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.70
					For ENAS1: 100 µ		
					For ENAS2: 2 milli		
					For ENAS3: 50 milli		
			1.68 to 1.95 V	38.4 nano	For ENAS0: 1 µ		
					For ENAS1: 100 µ		
					For ENAS2: 2 milli		
					For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	3.00 V or above	t_{CASmin} / 2	—	seconds	Figure 2.71
			1.68 to 1.95 V	t_{CASmin} / 2	—		
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	3.00 V or above	$t_{DIG_OD_Lmin}$	—	ns	Figure 2.77
			1.68 to 1.95 V	$t_{DIG_OD_Lmin}$	—		
	Bus Available Condition	t_{AVAL} *7	3.00 V or above	1	—	µs	—
			1.68 to 1.95 V	1	—		
	Bus Idle Condition	t_{IDLE}	3.00 V or above	1	—	ms	—
			1.68 to 1.95 V	1	—		
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	3.00 V or above	$t_{AVALmin}$	—	µs	Figure 2.77
			1.68 to 1.95 V	$t_{AVALmin}$			

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_Odmin}.

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.

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Note 5. On a Legacy Bus where I^2C Devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a Mixed Bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.52 I3C timing (Push-Pull Timing Parameters for SDR and HDR-DDR Modes)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	VCC	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes	SCL Clock Frequency		f_{SCL} *1	3.00 V or above	0.01	12.5	MHz	—
				1.68 to 1.95 V	0.01	12.5		
	SCL Clock Low Period		t_{LOW}	3.00 V or above	27	—	ns	Figure 2.68
				1.68 to 1.95 V	32	—		
			t_{DIG_L} *2 *4	3.00 V or above	35	—	ns	Figure 2.68
				1.68 to 1.95 V	40	—		
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	3.00 V or above	24	—	ns	Figure 2.68
				1.68 to 1.95 V	27	—		
			$t_{DIG_H_MIXED}$ *2 *3	3.00 V or above	32	45	ns	Figure 2.68
				1.68 to 1.95 V	35	45		
	SCL Clock High Period		t_{HIGH}	3.00 V or above	24	—	ns	Figure 2.68
				1.68 to 1.95 V	27	—		
			t_{DIG_H} *2	3.00 V or above	32	—	ns	Figure 2.68
				1.68 to 1.95 V	35	—		
	Clock in to Data Out for Slave		t_{SCO}	3.00 V or above	—	12	ns	Figure 2.73
				1.68 to 1.95 V	—	12		
	SCL Clock Rise Time		t_{CR}	3.00 V or above	—	150 × 1 / f_{SCL} (capped at 60)	ns	Figure 2.68
				1.68 to 1.95 V	—	150 × 1 / f_{SCL} (capped at 60)		
	SCL Clock Fall Time		t_{CF}	3.00 V or above	—	150 × 1 / f_{SCL} (capped at 60)	ns	Figure 2.68
				1.68 to 1.95 V	—	150 × 1 / f_{SCL} (capped at 60)		
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4*5	3.00 V or above	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.72
				1.68 to 1.95 V	t_{CR} + 3 and t_{CF} + 3	—		
		Slave	t_{HD_PP} *5	3.00 V or above	0	—	—	Figure 2.72
				1.68 to 1.95 V	0	—		
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	3.00 V or above	12	N/A	ns	Figure 2.74
				1.68 to 1.95 V	18	N/A		
	Clock After Repeated START (Sr)		t_{CASr}	3.00 V or above	t_{CASmin}	N/A	ns	Figure 2.76
				1.68 to 1.95 V	t_{CASmin}	N/A		
	Clock Before Repeated START (Sr)		t_{CBSr}	3.00 V or above	t_{CASmin} / 2	N/A	ns	Figure 2.76
				1.68 to 1.95 V	t_{CASmin} / 2	N/A		
	Capacitive Load per Bus Line (SDA/SCL)		C_b	3.00 V or above	—	50	pF	—
				1.68 to 1.95 V	—	50		

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Note 1. $f_{SCL} = 1 / (t_{DIG_L} + t_{DIG_H})$
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG_H_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.
Note 5. In SDR Mode the Hold time parameter is referred to as t_{HD_SDR}, and in DDR Mode it is referred to as t_{HD_DDR}.

Table 2.53 I3C timing (Push-Pull Timing Parameters for HDR-TSP and HDR-TSL Modes)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for HDR-TSP and HDR-TSL Modes	Edge-to-Edge Period	t_{EDGE} *1 *2	3.00 V or above	t_{DIG_H}	—	ns	Figure 2.68
			1.68 to 1.95 V	t_{DIG_H}	—		
	Allowed Difference Between Signals for 'Simultaneous' Change	t_{SKEW}	3.00 V or above	—	10	ns	
			1.68 to 1.95 V	—	10		
	Stable Condition Between Symbols	t_{EYE}	3.00 V or above	12	—	ns	
			1.68 to 1.95 V	12	—		
	Time Between Successive Symbols	t_{SYMBOL}	3.00 V or above	$t_{EDGE\ Min}$	—	ns	
			1.68 to 1.95 V	$t_{EDGE\ Min}$	—		
	Symbol Clock	t_{CLOCK}	3.00 V or above	1 / f_{SCL} (Max)	—	—	
			1.68 to 1.95 V	1 / f_{SCL} (Max)	—		

Note 1. Edges occur at the rate of 1 / (t_{EDGE} × 2)
Note 2. In a Mixed Bus, HDR-TSL shall respect the maximum $t_{DIG_H_MIXED}$ shown in Figure 2.71.

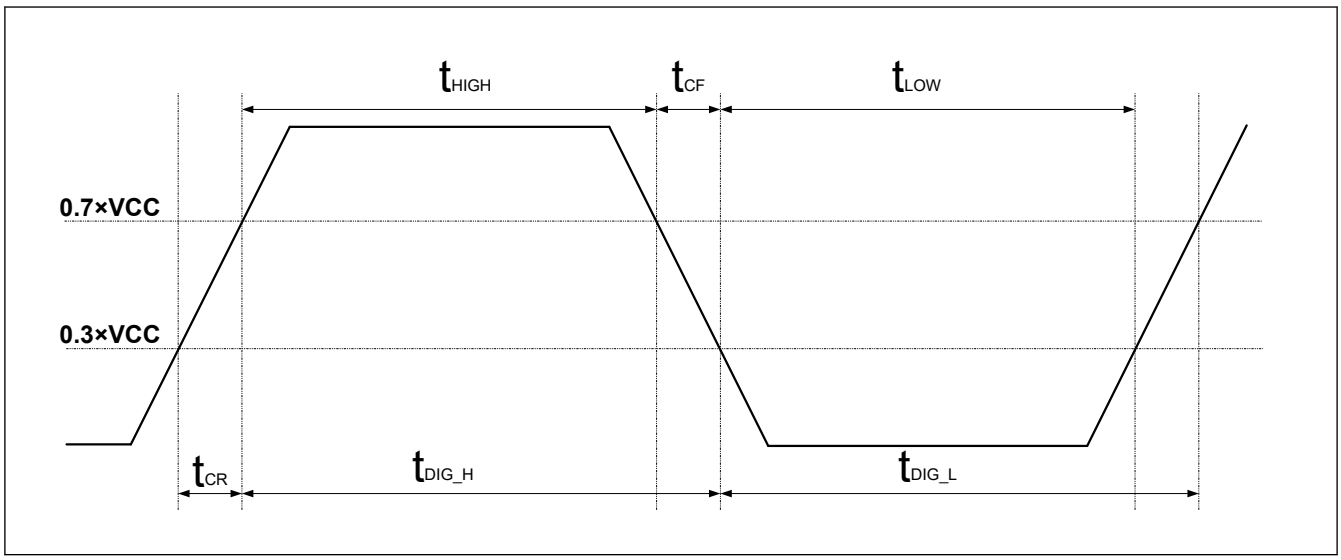


Figure 2.68 t_{DIG_H} and t_{DIG_L}

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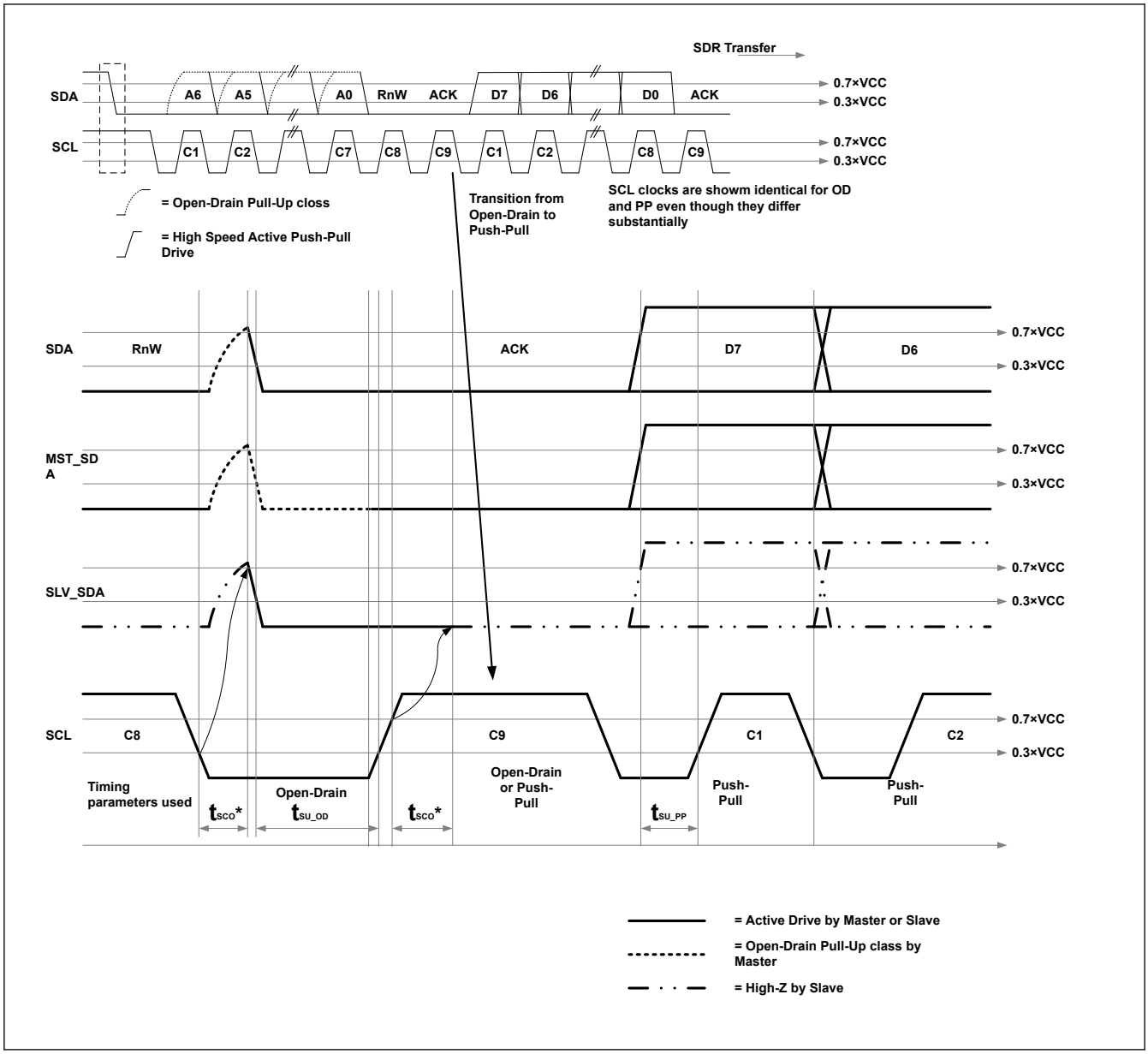


Figure 2.69 I3C Data Transfer – ACK by Slave

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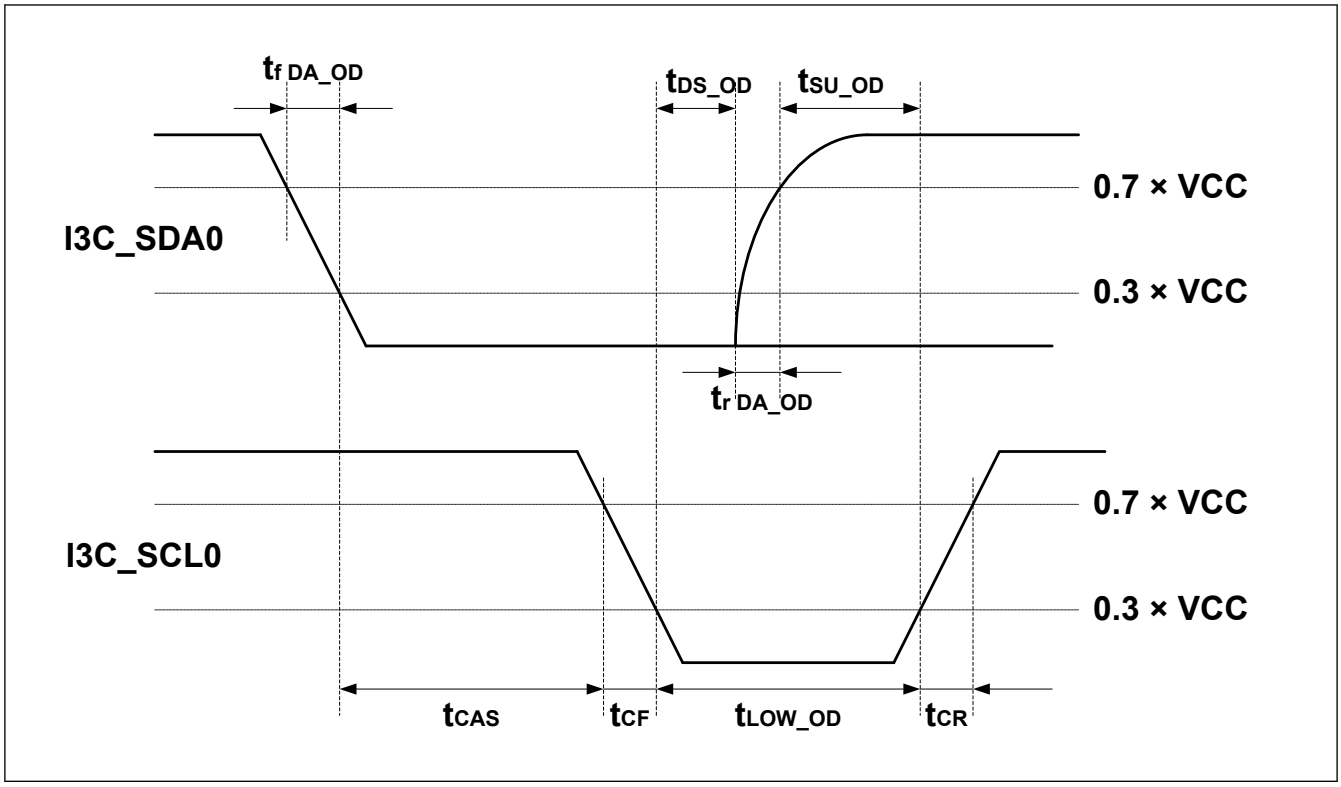


Figure 2.70 I3C START condition Timing

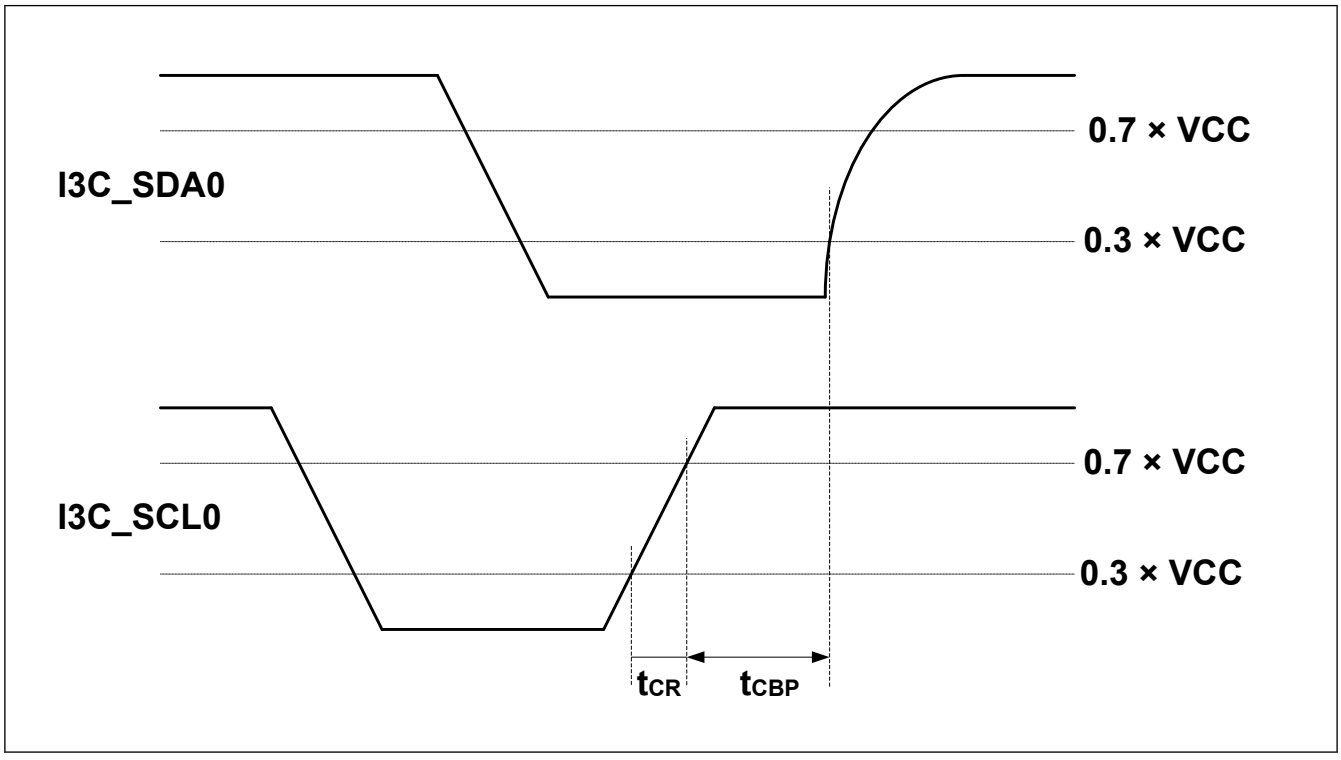


Figure 2.71 I3C STOP condition Timing

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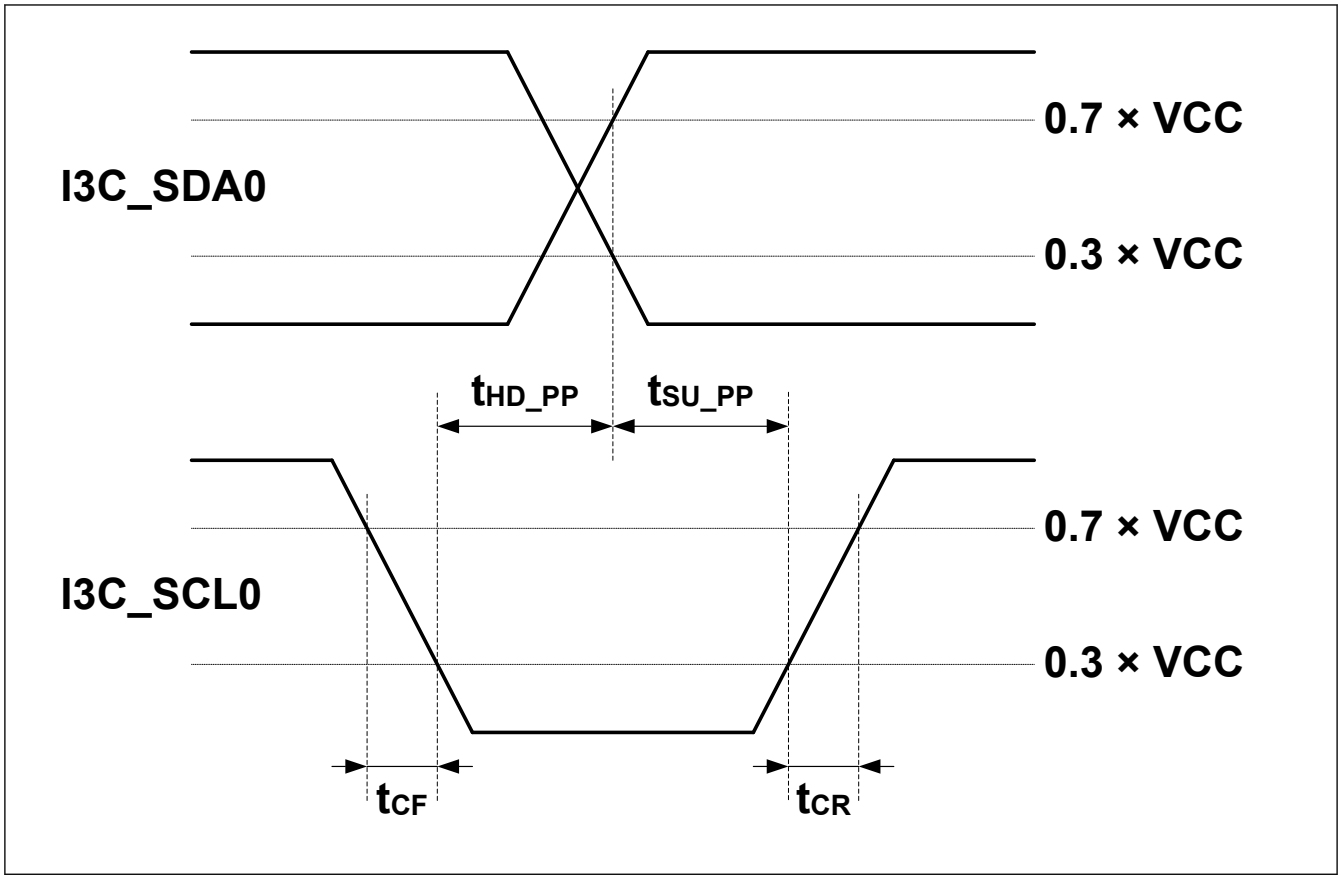


Figure 2.72 I3C Master Out Timing

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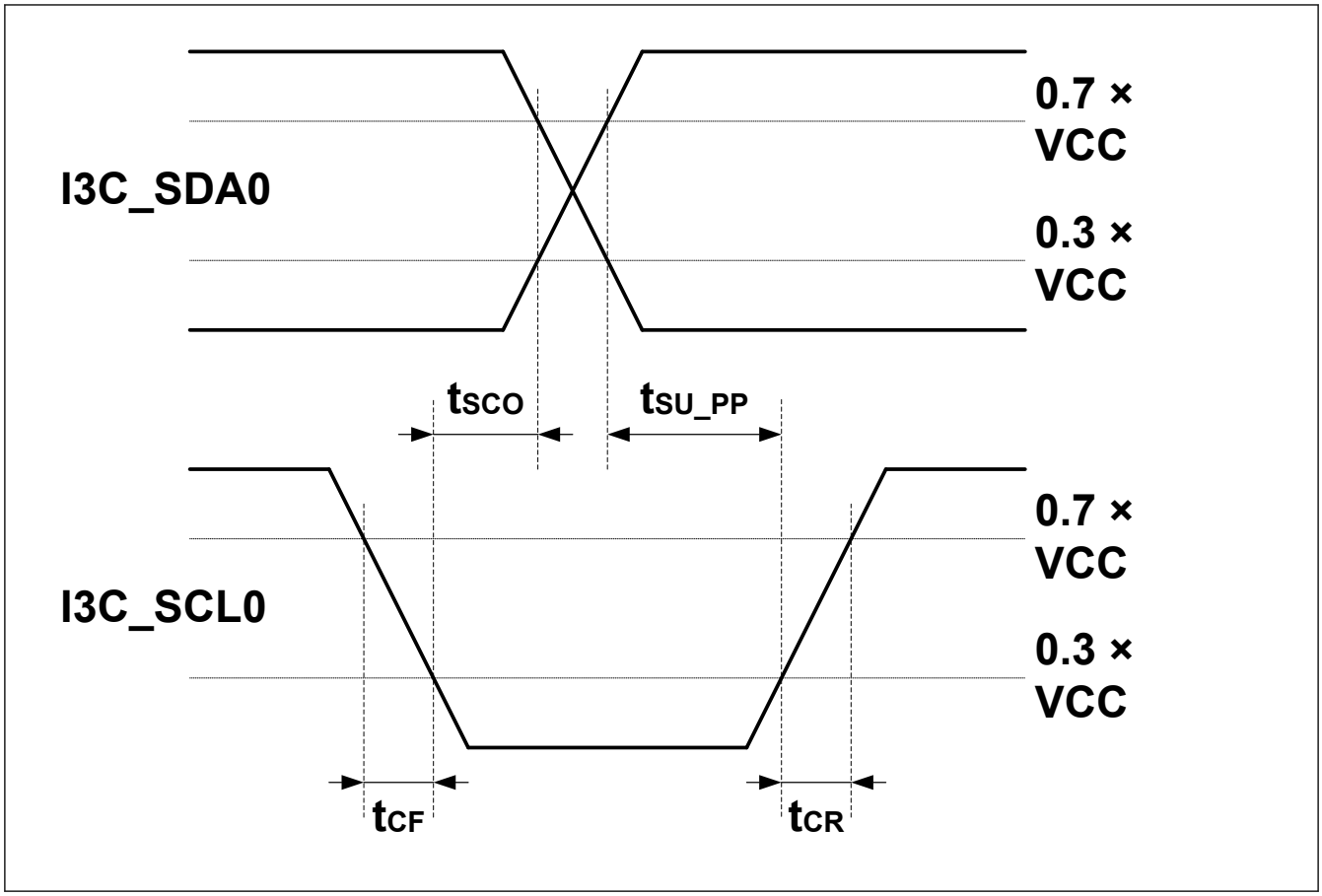


Figure 2.73 I3C Slave Out Timing

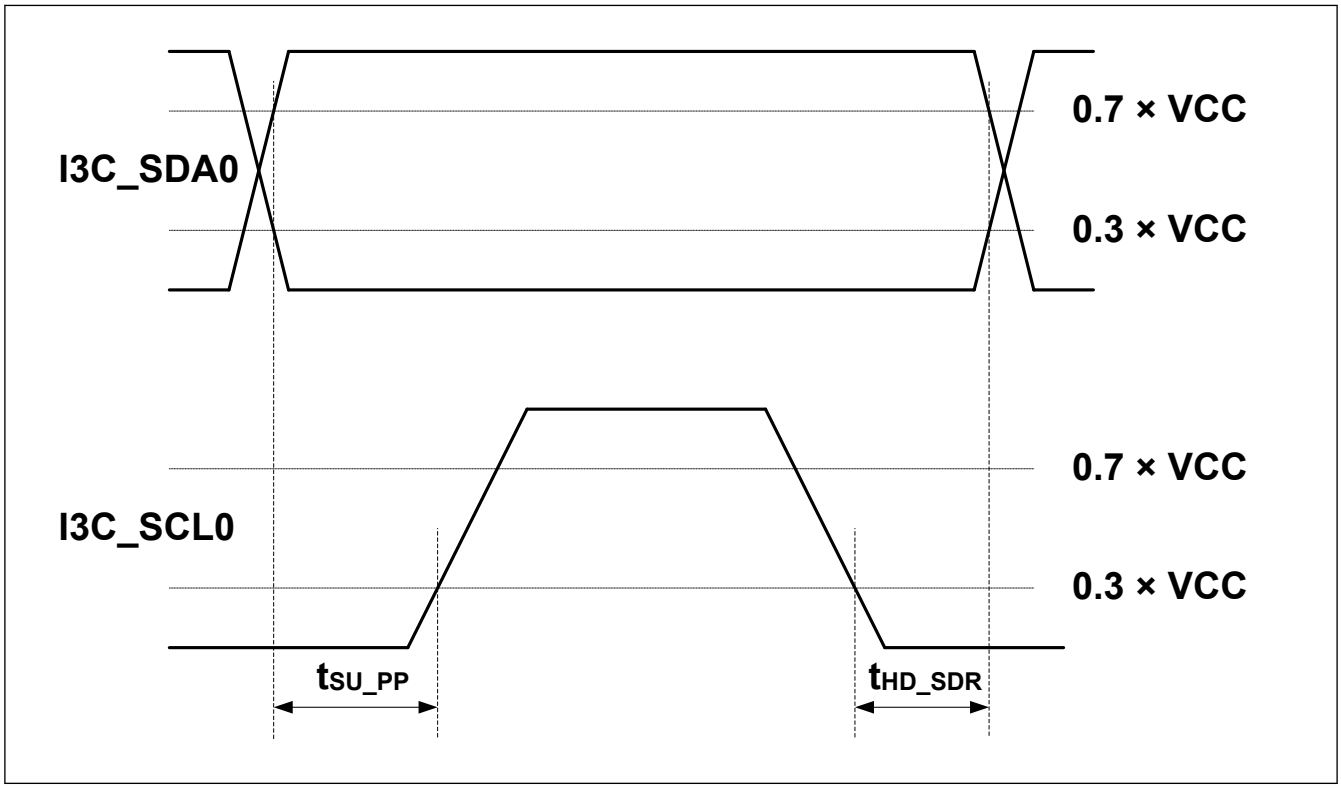


Figure 2.74 Master SDR Timing

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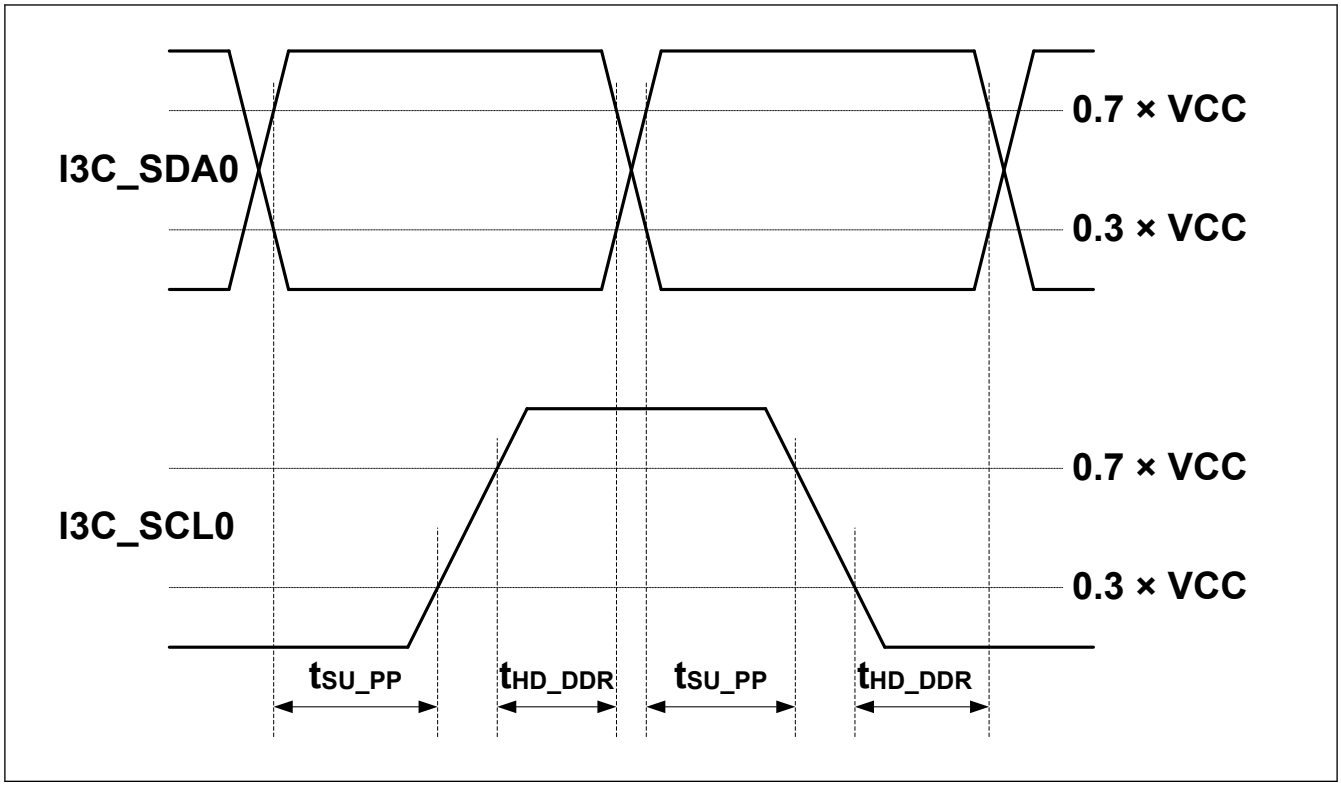


Figure 2.75 Master DDR Timing

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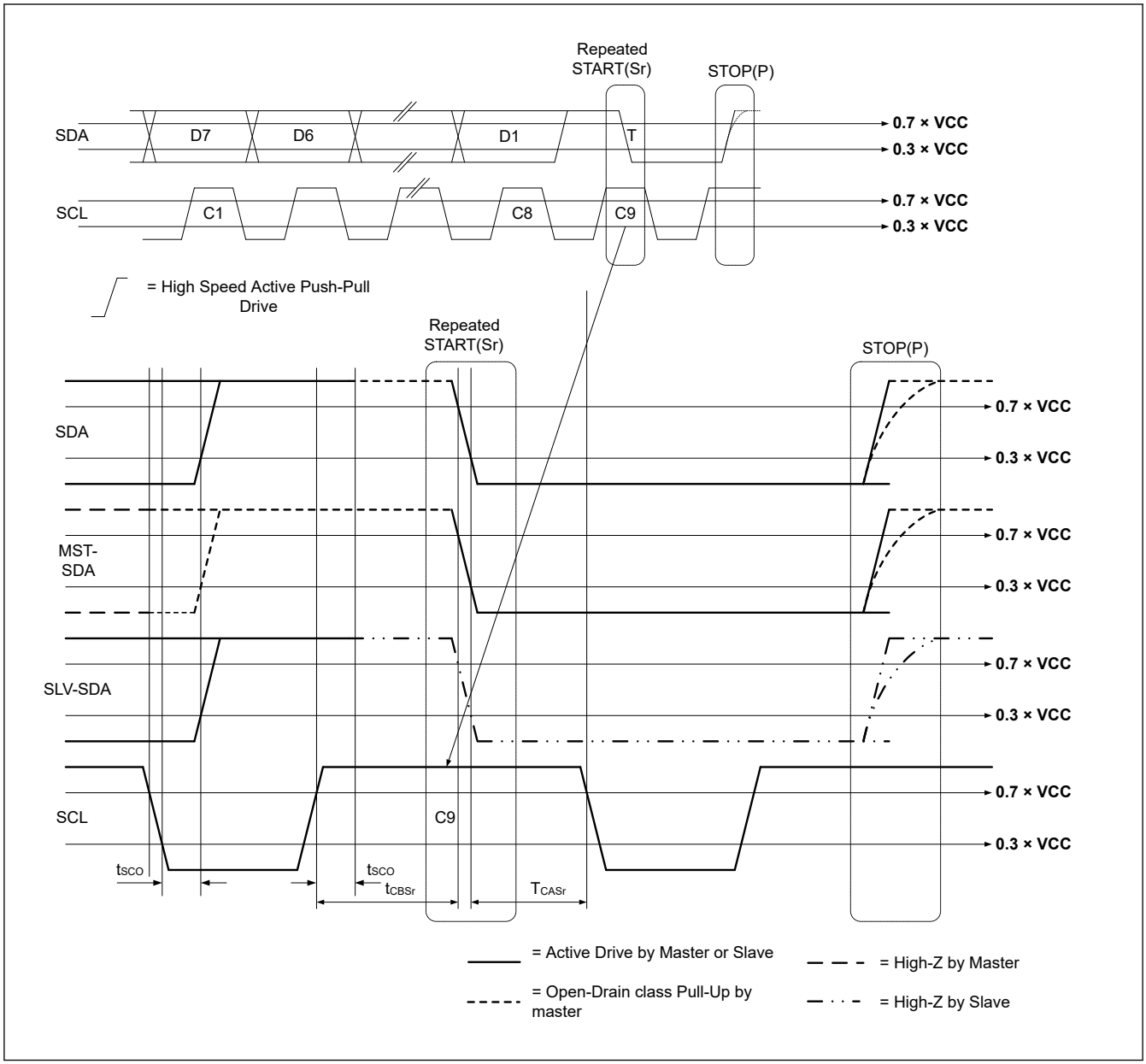


Figure 2.76 T-Bit When Master Ends Read with Repeated START and STOP

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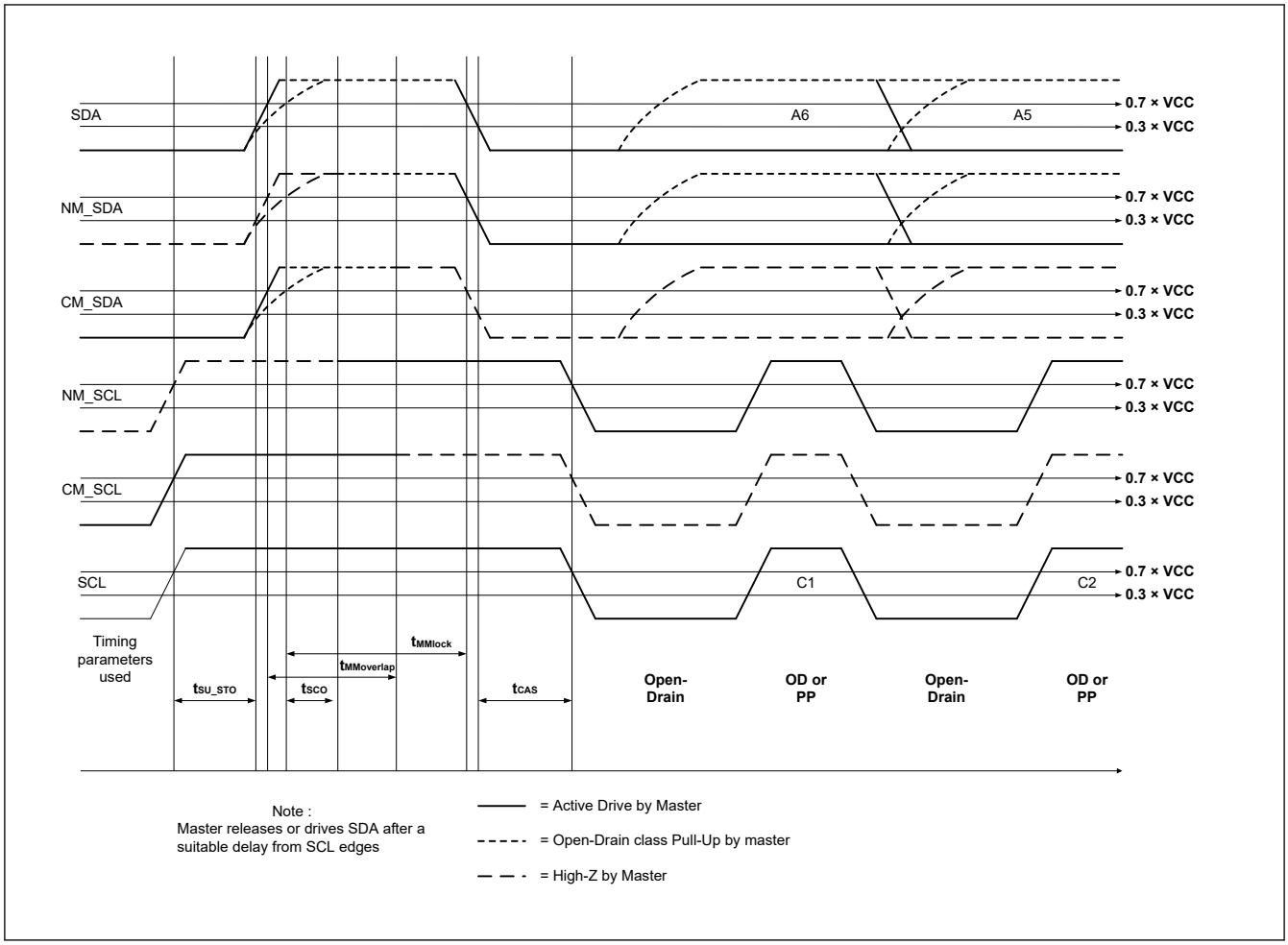
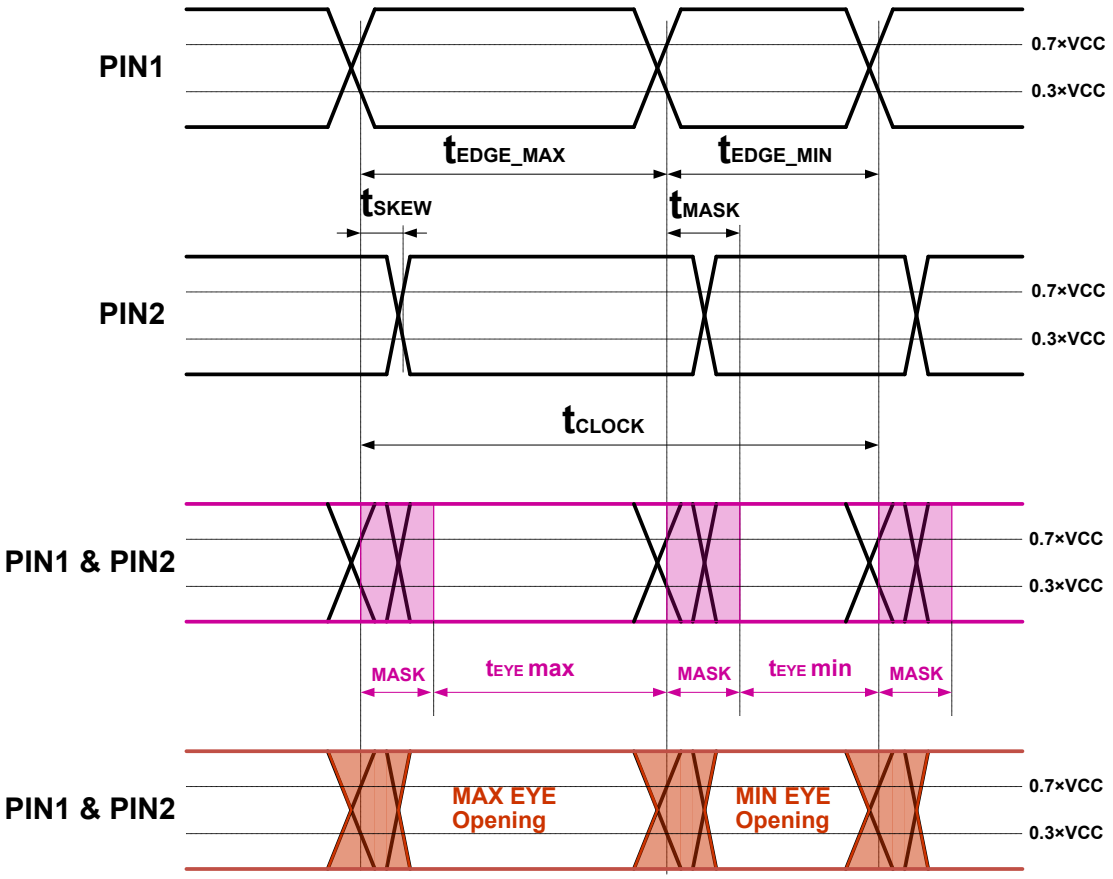


Figure 2.77 Master to Master Bus Handoff

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Design Conditions

1. The The differences of load magnitude and drive strength between the SDA and SCL lines result in different slopes, as shown
2. MASK period ≧ MAX t_{SKEW} + MAX rise/fall time between 0.3 × V_{DD} and 0.7 × V_{DD}, respectively, decreased by the time crossing the hysteresis window.

Simplifying Assumptions

1. t_{SKEW} is the same for both edges
2. Base CLOCK (e.g. 12.5MHz) is asymmetrical
3. Falling edges are equal rising edges
4. The MASK is shown as starting, from the last possible moment, whereas in reality it could be shifted left (towards the start point) delayed by the hysteresis window

Figure 2.78 Ternary Protocol Timing

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2.3.13 SD/MMC Host Interface Timing

Table 2.54 SD/MMC Host Interface signal timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
High-speed high drive output is selected in specific condition, please see note 1.
Clock duty ratio is 50%.

Parameter	Symbol	VCC/VCC2	Min	Max	Unit	Test conditions
SDnCLK clock cycle	t_{SDCYC}	2.70V or above	20	—	ns	Figure 2.79
		1.70 to1.95V*1	20	—		
		1.70 to1.95V	40	—		
SDnCLK clock high pulse width	t_{SDWH}	2.70V or above	6.5	—	ns	
		1.70 to1.95V*1	6.5	—		
		1.70 to1.95V	13.0	—		
SDnCLK clock low pulse width	t_{SDWL}	2.70V or above	6.5	—	ns	
		1.70 to1.95V*1	6.5	—		
		1.70 to1.95V	13.0	—		
SDnCLK clock rise time	t_{SDLH}	2.70V or above	—	3.0	ns	
		1.70 to1.95V*1	—	4.0		
		1.70 to1.95V	—	8.0		
SDnCLK clock fall time	t_{SDHL}	2.70V or above	—	3.0	ns	
		1.70 to1.95V*1	—	4.0		
		1.70 to1.95V	—	8.0		
SDnCMD/SDnDATm output data delay	t_{SDODLY}	2.70V or above	–7.0	4.0	ns	
		1.70 to1.95V*1	–7.0	7.0		
		1.70 to1.95V	–15.0	15.0		
SDnCMD/SDnDATm input data setup	t_{SDIS}	2.70V or above	4.5	—	ns	
		1.70 to1.95V*1	4.5	—		
		1.70 to1.95V	20.0	—		
SDnCMD/SDnDATm input data hold	t_{SDIH}	2.70V or above	1.5	—	ns	
		1.70 to1.95V	1.5	—		

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.
Note: If SD1DAT4_A~SD1DAT7_A are used, characteristics above is guaranteed only when VCC = VCC2.
Note 1. Only supported for Ch0 group B ("SD0*_B") and Ch1 group A ("SD1*_A")
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins:
SD0CLK_B, SD1CLK_A

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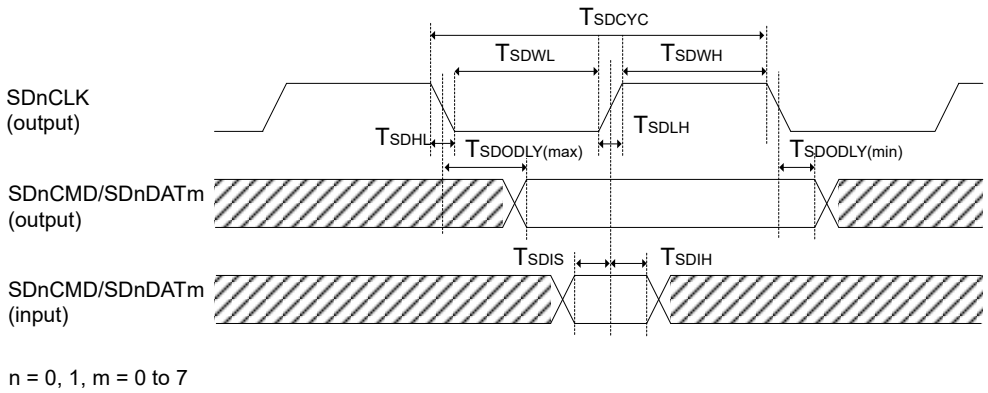


Figure 2.79 SD/MMC Host Interface signal timing

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2.3.14 ETHERC Timing

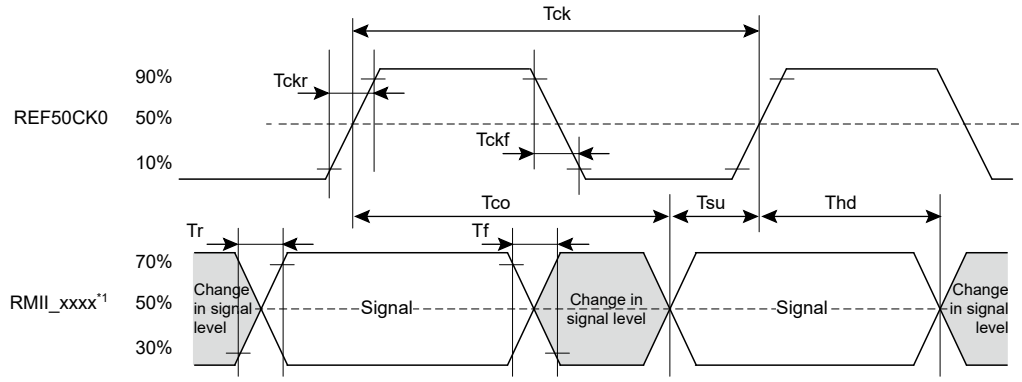
Table 2.55 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ETHERC (RMII)	REF50CK0 cycle time	T_{ck}	2.70V or above	20	—	ns	Figure 2.80 to Figure 2.83
	REF50CK0 frequency, typical 50 MHz	—		—	50 + 100 ppm	MHz	
	REF50CK0 duty	—		35	65	%	
	REF50CK0 rise/fall time	$T_{ckr/ckf}$		0.5	3.5	ns	
	RMII_xxxx*1 output delay	T_{co}		2.5	12.0	ns	
	RMII_xxxx*2 setup time	T_{su}		3	—	ns	
	RMII_xxxx*2 hold time	T_{hd}		1	—	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f		0.5	5.0	ns	
	ET0_WOL output delay	t_{WOLd}		1	23.5	ns	Figure 2.84
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}		40	—	ns	—
	ET0_TX_EN output delay	t_{TENd}		1	20	ns	Figure 2.85
	ET0_ETXD0 to ET_ETXD3 output delay	t_{MTDd}		1	20	ns	
	ET0_CRS setup time	t_{CRSs}		10	—	ns	
	ET0_CRS hold time	t_{CRSh}		10	—	ns	
	ET0_COL setup time	t_{COLs}		10	—	ns	Figure 2.86
	ET0_COL hold time	t_{COLh}		10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}		40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}		10	—	ns	Figure 2.87
	ET0_RX_DV hold time	t_{RDVh}		10	—	ns	
	ET0_ERXD0 to ET_ERXD3 setup time	t_{MRDs}		10	—	ns	
	ET0_ERXD0 to ET_ERXD3 hold time	t_{MRDh}		10	—	ns	
	ET0_RX_ER setup time	t_{RERs}		10	—	ns	Figure 2.88
	ET0_RX_ER hold time	t_{RESh}		10	—	ns	
	ET0_WOL output delay	t_{WOLd}		1	23.5	ns	Figure 2.89

Note: The following pins must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B.
Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.

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Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 2.80 REF50CK0 and RMII signal timing

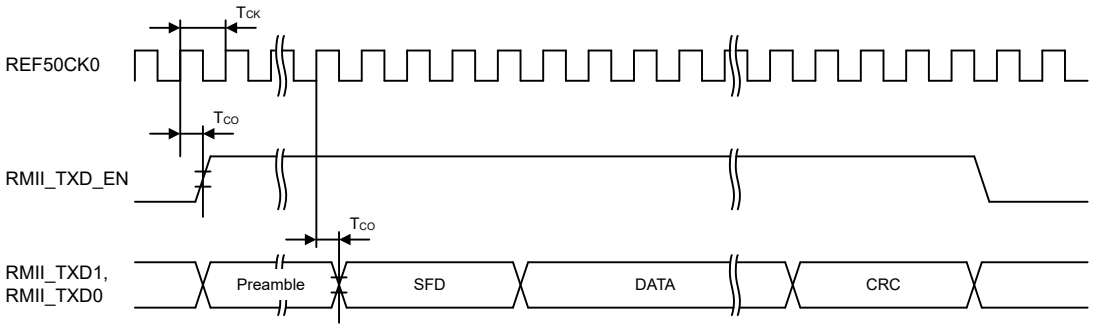


Figure 2.81 RMII transmission timing

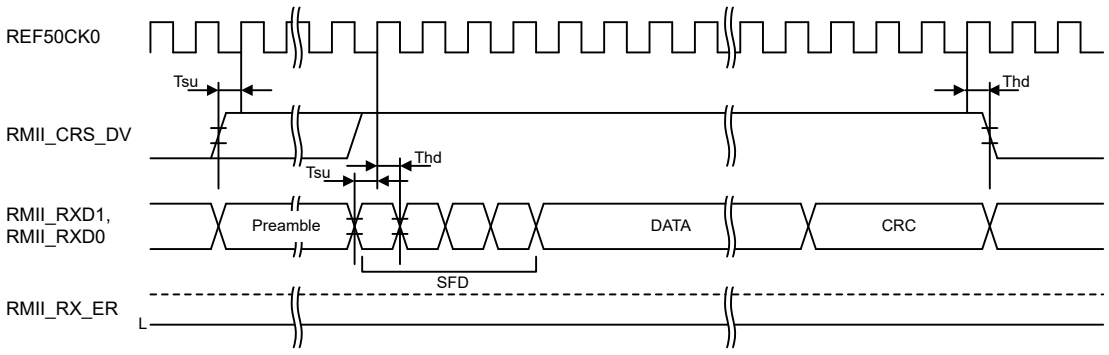


Figure 2.82 RMII reception timing in normal operation

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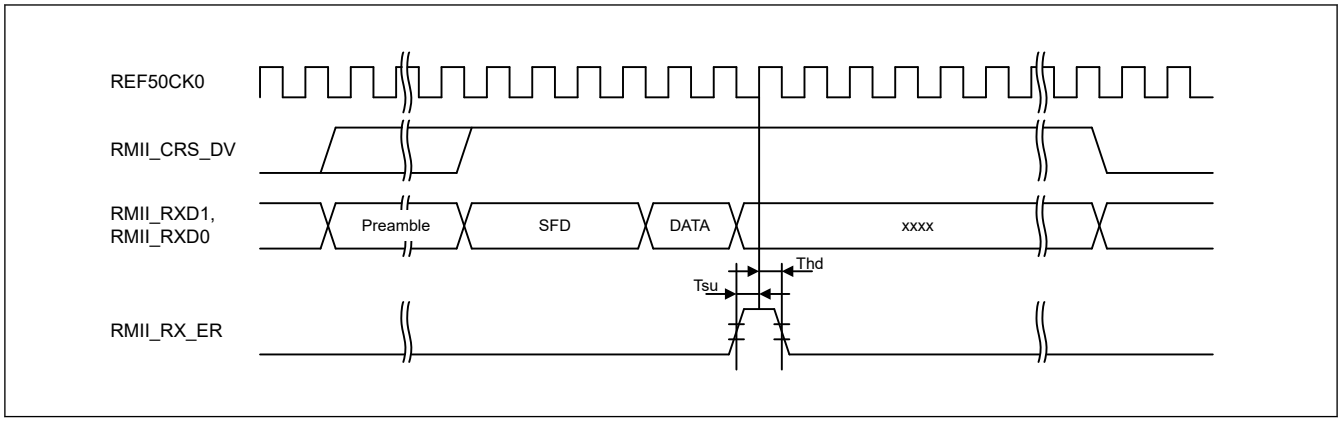


Figure 2.83 RMII reception timing when an error occurs

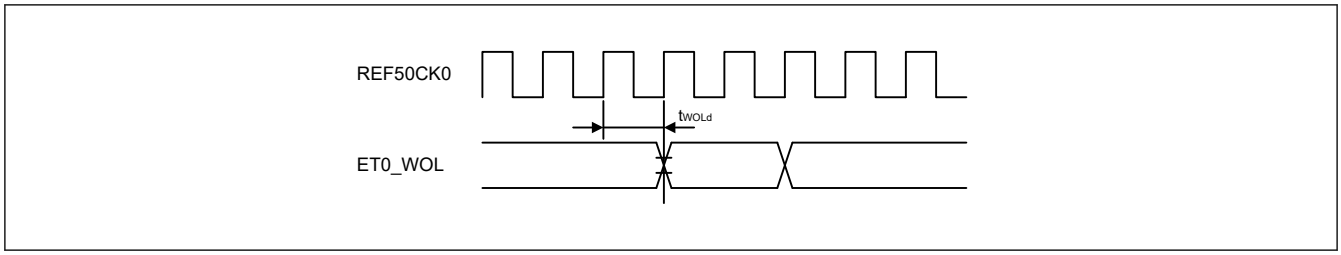


Figure 2.84 WOL output timing for RMII

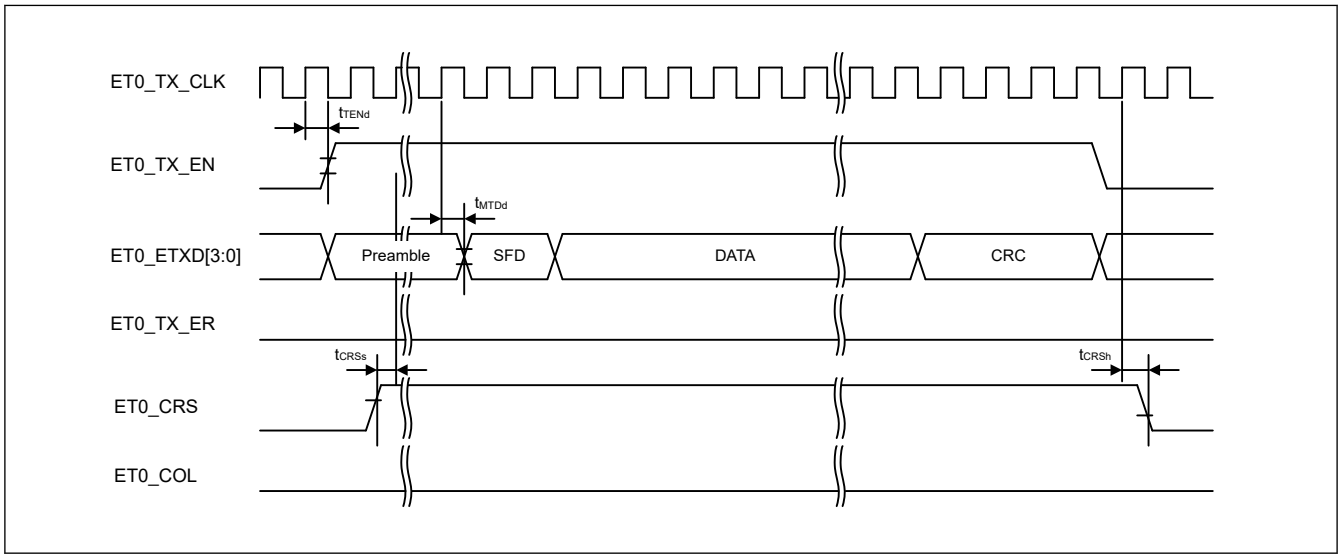


Figure 2.85 MII transmission timing in normal operation

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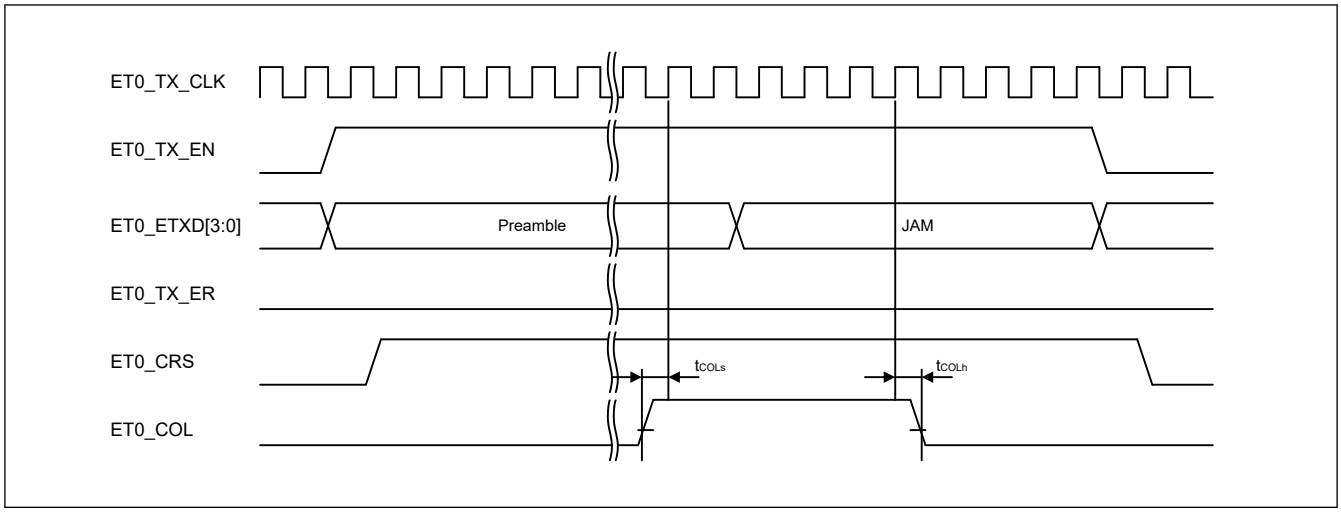


Figure 2.86 MII transmission timing when a conflict occurs

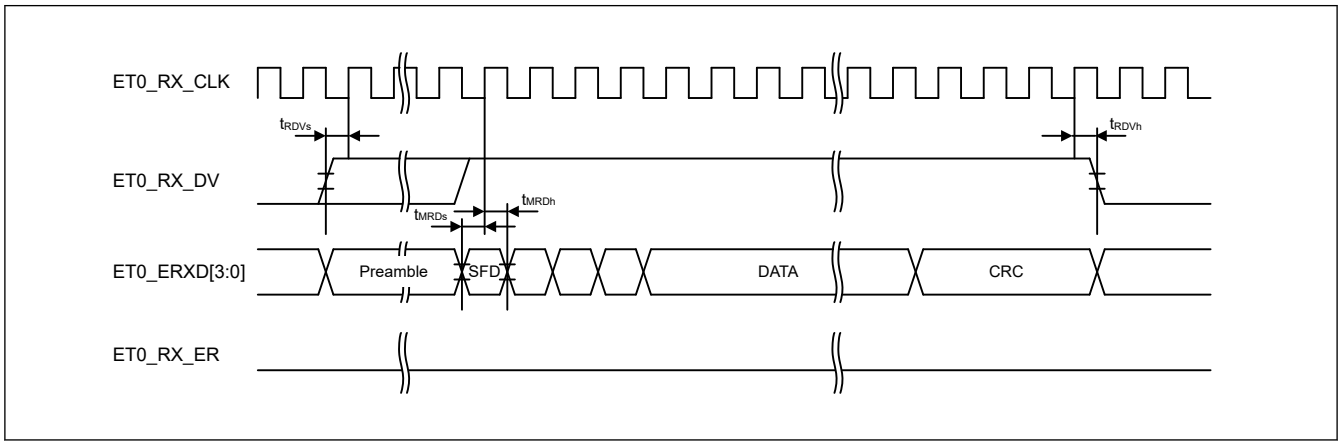


Figure 2.87 MII reception timing in normal operation

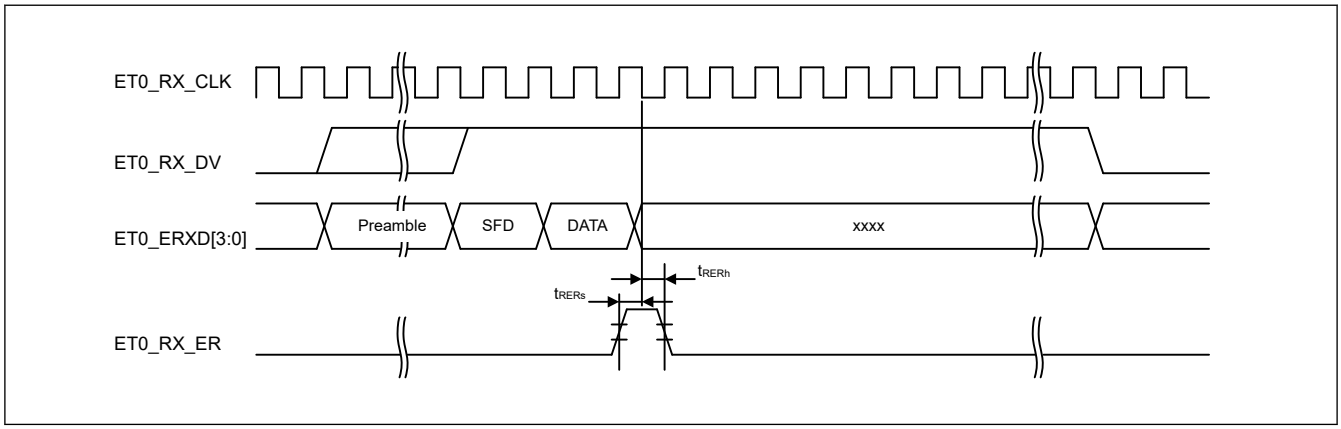


Figure 2.88 MII reception timing when an error occurs

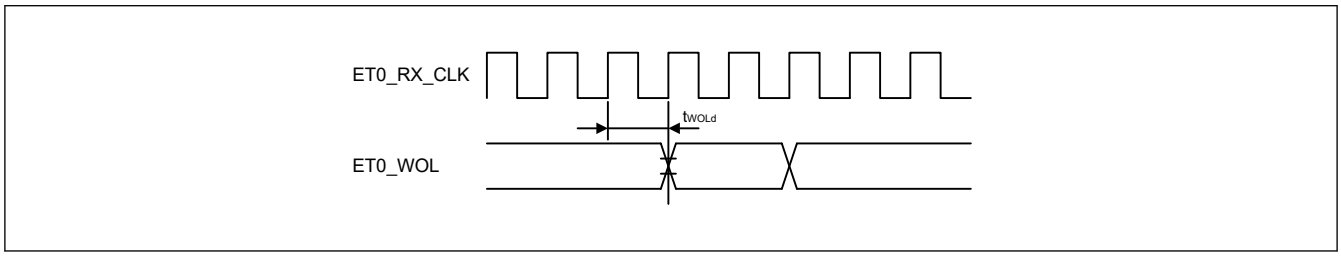


Figure 2.89 WOL output timing for MII

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2.3.15 CANFD Timing

Table 2.56 CANFD interface timing

Parameter	Symbol	VCC/VCC2	Min	Max	Unit	Test conditions
Internal delay time	t_{node}	2.70 V or above	—	50	ns	Figure 2.90
		1.68 V or above (VCC) 1.65 V or above (VCC2)	—	50		

Note: Internal delay time (t_{node}) = Internal transfer delay time (t_{output}) + Internal receive delay time (t_{input})

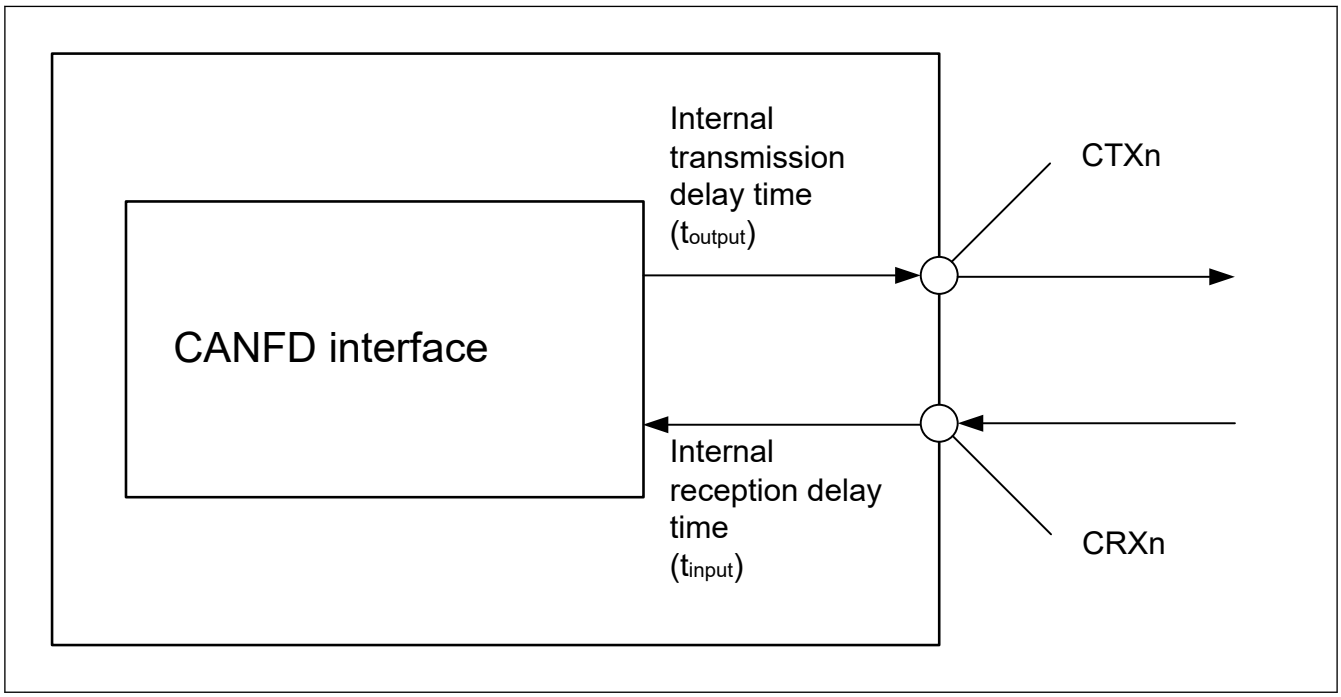


Figure 2.90 CANFD interface condition

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.57 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.91
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}

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Table 2.57 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

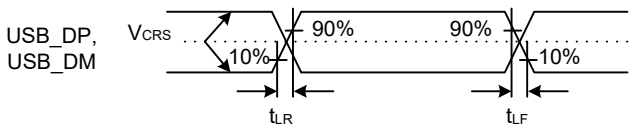


Figure 2.91 USB_DP and USB_DM output timing in low-speed mode

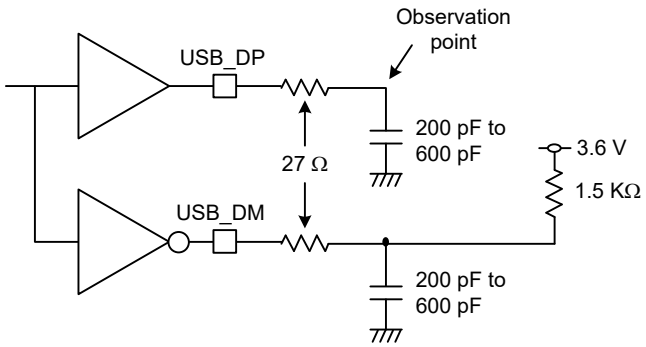


Figure 2.92 Test circuit in low-speed mode

Table 2.58 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.93
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

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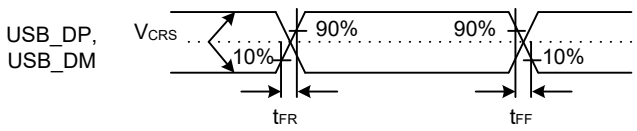


Figure 2.93 USB_DP and USB_DM output timing in full-speed mode

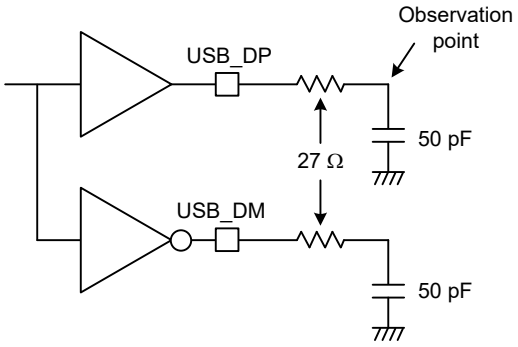


Figure 2.94 Test circuit in full-speed mode

2.5 ADC12 Characteristics

Table 2.59 A/D conversion characteristics for unit 0 (DCDC mode) (1 of 3)

Conditions: PCLKC = 1 to 60 MHz

Parameter	Min	Typ	Max	Unit	Test conditions
Frequency	1	—	60	MHz	—
Analog input capacitance	—	—	30	pF	—
Quantization error	—	±0.5	—	LSB	—
Resolution	—	—	12	Bits	—

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Table 2.59 A/D conversion characteristics for unit 0 (DCDC mode) (2 of 3)

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time[*1] (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)[*2]	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Absolute accuracy		—	±2.5	±10.5	LSB	LQFP package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
			—	±2.5	±7.5		LQFP package AVCC0 = VREFH0 = 2.7 to 3.6V
			—	±2.5	±5.5		BGA package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
	DNL differential nonlinearity error		—	±1.0	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.5	±4.0	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	µs	—
	Dynamic range		0.25	—	VREFH 0 - 0.25	V	—
High-precision channels, Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002, AN004 to AN008)	Conversion time[*1] (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)[*2]	—	—	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)[*2]	—	—	µs	Sampling in 11 states AVCC0 = VREFH0 = 3.0 to 3.6 V
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±3.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	LQFP package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
			—	±2.0	±6.0		LQFP package AVCC0 = VREFH0 = 2.7 to 3.6V
			—	±2.0	±5.5		BGA package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
	DNL differential nonlinearity error		—	±0.5	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—

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Table 2.59 A/D conversion characteristics for unit 0 (DCDC mode) (3 of 3)

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Normal-precision channels (AN016 to AN019)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	—	—	µs	Sampling in 40 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±10.0	LSB	LQFP package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
			—	±2.0	±7.5		LQFP package AVCC0 = VREFH0 = 2.7 to 3.6V
			—	±2.0	±7.5		BGA package AVCC0 = 2.7 to 3.6V VREFH0 = 2.7V to AVCC0
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when only one A/D is operating and D/A and ACMPHS are not operating and there is no access to the external bus during A/D conversion.
If other A/D, D/A, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.60 A/D conversion characteristics for unit 1 (DCDC mode) (1 of 2)

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	60	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision channels (AN100 to AN102, AN104 to AN106)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	—	—	µs	Sampling in 11 states AVCC0 = VREFH = 3.0 to 3.6 V
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±3.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	LQFP package AVCC0 = 2.7 to 3.6V VREFH = 2.7V to AVCC0
			—	±2.0	±6.0		LQFP package AVCC0 = VREFH = 2.7 to 3.6V
			—	±2.0	±5.5		BGA package AVCC0 = 2.7 to 3.6V VREFH = 2.7V to AVCC0
	DNL differential nonlinearity error		—	±0.5	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—

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Table 2.60 A/D conversion characteristics for unit 1 (DCDC mode) (2 of 2)

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Normal-precision channels (AN116 to AN122)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	—	—	µs	Sampling in 40 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±10.0	LSB	LQFP package AVCC0 = 2.7 to 3.6V VREFH = 2.7V to AVCC0
			—	±2.0	±7.5		LQFP package AVCC0 = VREFH = 2.7 to 3.6V
			—	±2.0	±7.5		BGA package AVCC0 = 2.7 to 3.6V VREFH = 2.7V to AVCC0
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when only one A/D is operating and D/A and ACMPHS are not operating and there is no access to the external bus during A/D conversion.
If other A/D, D/A, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.61 A/D conversion characteristics for unit 0 (External VDD mode) (1 of 2)

Conditions: PCLKC = 1 to 60 MHz
AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	60	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Absolute accuracy		—	±2.5	±5.5	LSB	—
	DNL differential nonlinearity error		—	±1.0	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.5	±3.0	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	µs	—
	Dynamic range		0.25	—	VREFH 0 - 0.25	V	—

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Table 2.61 A/D conversion characteristics for unit 0 (External VDD mode) (2 of 2)

Conditions: PCLKC = 1 to 60 MHz
AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels, Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002, AN004 to AN008)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	—	—	µs	Sampling in 11 states AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±3.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision channels (AN016 to AN019)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	—	—	µs	Sampling in 40 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when only one A/D is operating and D/A and ACMPHS are not operating and there is no access to the external bus during A/D conversion.
If other A/D, D/A, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.62 A/D conversion characteristics for unit 1 (External VDD mode) (1 of 2)

Conditions: PCLKC = 1 to 60 MHz
AVCC0 = 2.7 to 3.6 V, VREFH = 2.7 to 3.6 V

Parameter	Min	Typ	Max	Unit	Test conditions
Frequency	1	—	60	MHz	—
Analog input capacitance	—	—	30	pF	—
Quantization error	—	±0.5	—	LSB	—
Resolution	—	—	12	Bits	—

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Table 2.62 A/D conversion characteristics for unit 1 (External VDD mode) (2 of 2)

Conditions: PCLKC = 1 to 60 MHz
AVCC0 = 2.7 to 3.6 V, VREFH = 2.7 to 3.6 V

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN100 to AN102, AN104 to AN106)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	—	—	µs	Sampling in 11 states AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±3.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision channels (AN116 to AN122)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	—	—	µs	Sampling in 40 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when only one A/D is operating and D/A and ACMPHS are not operating and there is no access to the external bus during A/D conversion.
If other A/D, D/A, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.63 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.28	V	—
Sampling time	4.15	—	—	µs	—

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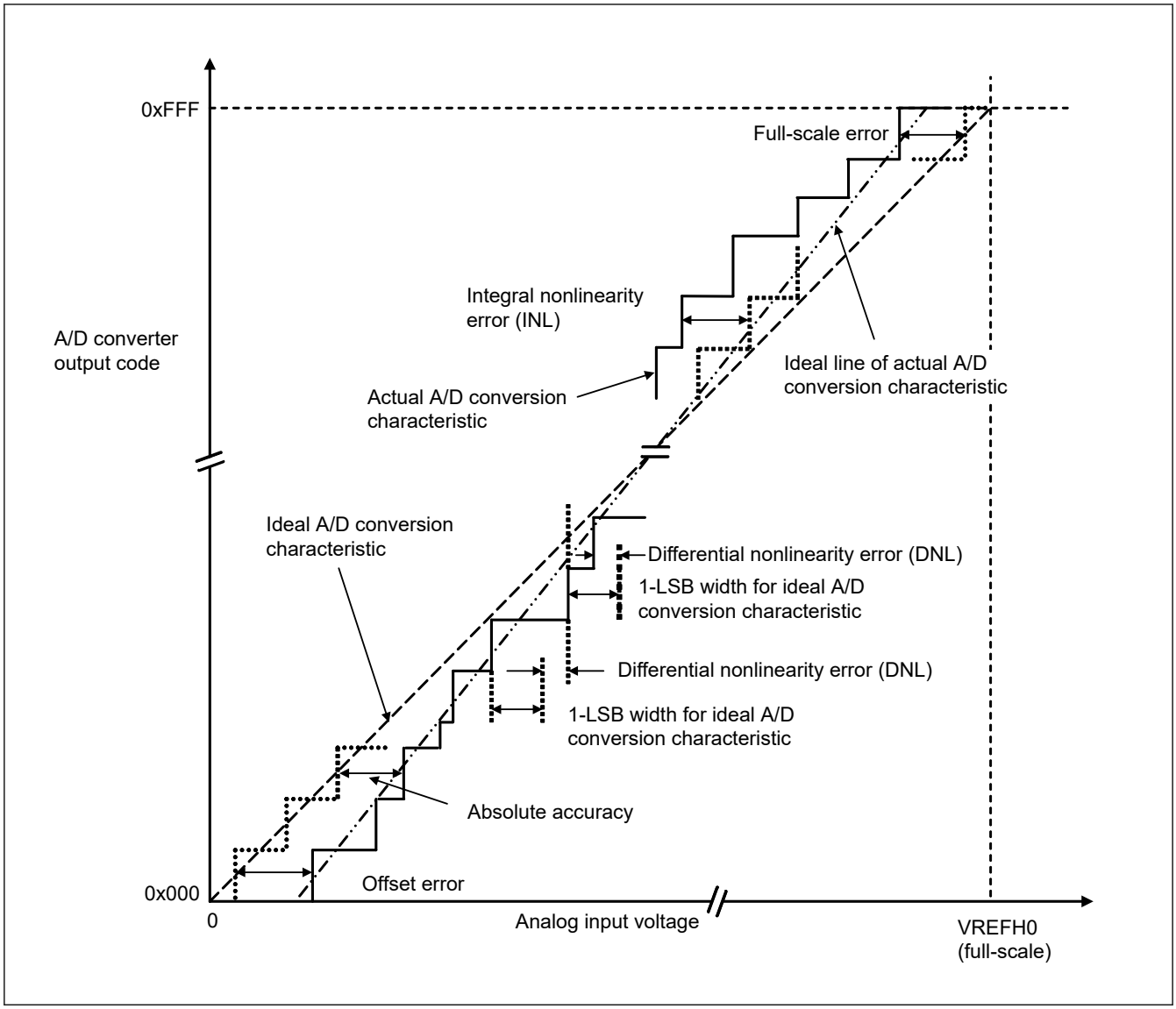


Figure 2.95 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

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Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

Table 2.64 A/D input voltage range for each input channel

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	Unit 0	AN000 to AN002, AN004 to AN008	VI	VREFL0	—	VREFH0	V	—
		AN016 to AN018		VREFL0	—	VREFH0		VREFH0 ≤ VCC
				VREFL0	—	VCC		VCC < VREFH0
		AN019		VREFL0	—	VREFH0		VREFH0 ≤ VCC2
				VREFL0	—	VCC2		VCC2 < VREFH0
	Unit 1	AN100 to AN102, AN104 to AN106		VREFL	—	VREFH		—
		AN116 to AN118		VREFL	—	VREFH		VREFH ≤ VCC
				VREFL	—	VCC		VCC < VREFH
		AN119 to AN122		VREFL	—	VREFH		VREFH ≤ VCC2
				VREFL	—	VCC2		VCC2 < VREFH

2.6 DAC12 Characteristics

Table 2.65 D/A conversion characteristics (1 of 2)

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		—	—	12	Bits	—
Without output amplifier (for pin output, AVCC0 ≥ 1.65V)						
Absolute accuracy	VREFH ≥ 2.7V	—	—	±24	LSB	Resistive load 2 MΩ
	VREFH < 2.7V	—	—	±36		
INL	VREFH ≥ 2.7V	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
	VREFH < 2.7V	—	±2.0	±8.0		
DNL	VREFH ≥ 2.7V	—	±1.0	±2.0	LSB	—
	VREFH < 2.7V		±1.0	±3.0		
Output impedance		—	8.5	—	kΩ	—
Conversion time	VREFH ≥ 2.7V	—	—	3.0	µs	Resistive load 2 MΩ, Capacitive load 20 pF
	VREFH < 2.7V	—	—	6.0		
Output voltage range		0	—	VREFH	V	—
Without output amplifier (for internal output, AVCC0 ≥ 1.65V)						
Absolute accuracy	VREFH≥2.7V	—	—	±4.0	LSB	—
	VREFH < 2.7V	—	—	±6.0		
Conversion time	VREFH ≥ 2.7V	—	—	3.0	µs	—
	VREFH < 2.7V	—	—	6.0		

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Table 2.65 D/A conversion characteristics (2 of 2)

Parameter		Min	Typ	Max	Unit	Test conditions
Output voltage range		0	—	VREFH	V	—
With output amplifier (AVCC0 ≥ 2.70V)						
INL		—	±2.0	±4.0	LSB	—
DNL		—	±1.0	±2.0	LSB	—
Conversion time		—	—	3.5	µs	—
Resistive load		5	—	—	kΩ	—
Capacitive load		—	—	50	pF	—
Output voltage range	VREFH ≥ 2.7V	0.20	—	VREFH – 0.20	V	—
	VREFH < 2.7V	0.22	—	VREFH – 0.22		—

2.7 TSN Characteristics

Table 2.66 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

2.8 OSC Stop Detect Characteristics

Table 2.67 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.96

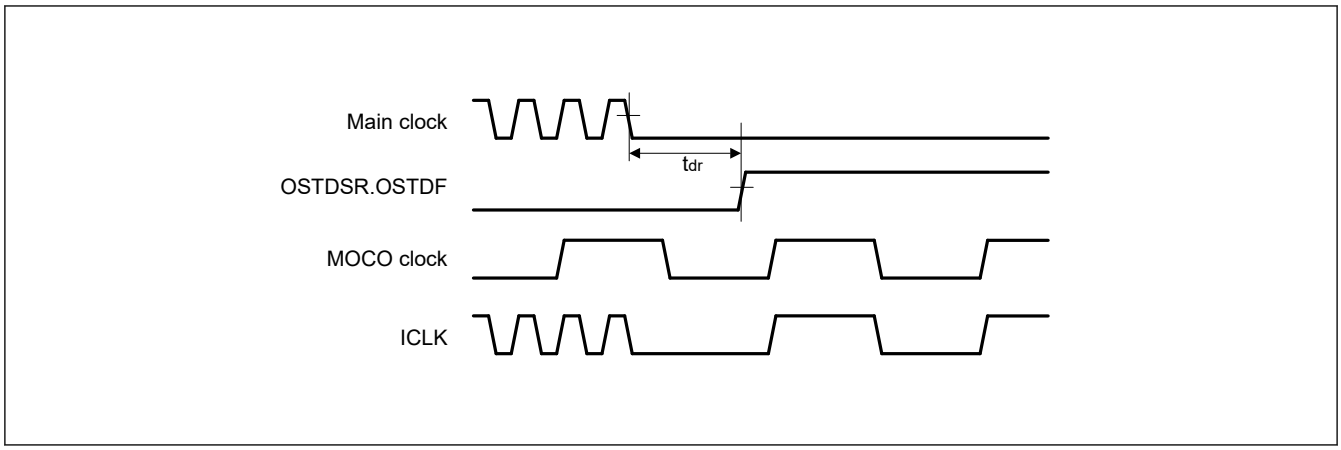


Figure 2.96 Oscillation stop detection timing

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2.9 POR and PVD Characteristics

Table 2.68 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	Tj = 25℃	V_{POR1}	1.55	1.60	1.68	V	Figure 2.97
		Tj = 125℃		1.55	1.60	1.70		
		Tj = 25℃	V_{POR2}	1.65	1.70	1.79		
		Tj = 125℃		1.65	1.70	1.81		
	Voltage detection circuit (PVD0)		V_{det0_0}	2.76	2.85	2.99		Figure 2.98
			V_{det0_1}	2.50	2.58	2.71		
			V_{det0_2}	2.08	2.15	2.27		
			V_{det0_3}	1.94	2.00	2.12		
			V_{det0_4}	1.84	1.90	2.01		
			V_{det0_5}	1.74	1.80	1.91		
			V_{det0_6}	1.65	1.70	1.81		
			V_{det0_7}	1.55	1.60	1.70		
	Voltage detection circuit (PVDn) (n = 1, 2)		$V_{detn_3_rise}$	3.78	3.92	4.10		Figure 2.99
			$V_{detn_3_fall}$	3.72	3.86	4.04		
			$V_{detn_4_rise}$	3.09	3.20	3.35		
			$V_{detn_4_fall}$	3.03	3.14	3.29		
			$V_{detn_5_rise}$	3.05	3.16	3.31		
			$V_{detn_5_fall}$	2.99	3.10	3.25		
			$V_{detn_6_rise}$	3.03	3.14	3.29		
			$V_{detn_6_fall}$	2.97	3.08	3.23		
			$V_{detn_7_rise}$	2.81	2.91	3.05		
			$V_{detn_7_fall}$	2.75	2.85	2.99		
			$V_{detn_8_rise}$	2.79	2.89	3.03		
			$V_{detn_8_fall}$	2.73	2.83	2.97		
			$V_{detn_9_rise}$	2.76	2.86	3.00		
			$V_{detn_9_fall}$	2.70	2.80	2.94		
			$V_{detn_10_rise}$	2.58	2.67	2.80		
			$V_{detn_10_fall}$	2.53	2.62	2.75		
			$V_{detn_11_rise}$	2.30	2.38	2.51		
			$V_{detn_11_fall}$	2.25	2.33	2.46		
Voltage detection level	Voltage detection circuit (PVDn) (n = 1, 2)		$V_{detn_12_rise}$	1.88	1.94	2.05	V	Figure 2.99
			$V_{detn_12_fall}$	1.84	1.90	2.01		
			$V_{detn_13_rise}$	1.84	1.90	2.01		
			$V_{detn_13_fall}$	1.80	1.86	1.97		
			$V_{detn_14_rise}$	1.72	1.78	1.89		
			$V_{detn_14_fall}$	1.68	1.74	1.85		
			$V_{detn_15_rise}$	1.69	1.75	1.85		
			$V_{detn_15_fall}$	1.65	1.71	1.81		

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Table 2.68 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Internal reset time*1	Power-on reset time		t_{POR1}	—	—	8.2	ms	Figure 2.97
			t_{POR2}	—	—	4.5		Figure 2.97
	PVD0 reset time		t_{PVD0}	—	—	*1		Figure 2.97
	PVD1 reset time		t_{PVD1}	—	—	*1		Figure 2.98
	PVD2 reset time		t_{PVD2}	—	—	*1		
Minimum VCC down time (POR)*2	100mV < VD		t_{VOFFP}	500	—	—	µs	Figure 2.97
	50mV < VD ≤ 100mV			900	—	—		
	VD ≤ 50mV			2000	—	—		
Minimum VCC down time (PVD)*2	PVD0 (OFS1(_SEC).PVDLPSEL = 0 in Deep Software Standby mode 1, 2)		t_{VOFF}	400	—	—	µs	Figure 2.98
	PVD0 (Other than above), PVD1, PVD2			200	—	—	µs	Figure 2.98
Response delay time (POR)	100mV < VD		t_{detp}	—	—	500	µs	Figure 2.97
	50mV < VD ≤ 100mV			—	—	900		
	VD ≤ 50mV			—	—	2000		
Response delay time (PVD)	PVD0 (OFS1(_SEC).PVDLPSEL = 0 in Deep Software Standby mode 1, 2)	50mV < VD	t_{det}	—	—	200	µs	Figure 2.98, Figure 2.99
		50mV ≥ VD		—	—	400		
	PVD0 (Other than above), PVD1, PVD2	100mV < VD		—	—	10		
		100mV ≥ VD		—	—	200		
PVD operation stabilization time (after PVD is enabled)			$T_{d\ (E-A)}$	—	—	20	µs	Figure 2.99

Note 1. The maximum value of t_{PVD0} is equal to t_{DSBY} because the internal reset time is maximized when returning from Deep Software Standby mode.
The maximum value of t_{PVD1}, t_{PVD2} are equal to t_{DSTBY} because the internal reset time is maximized when returning from Deep Software Standby mode.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR1}, V_{det1}, and V_{det2} for the POR / PVD.

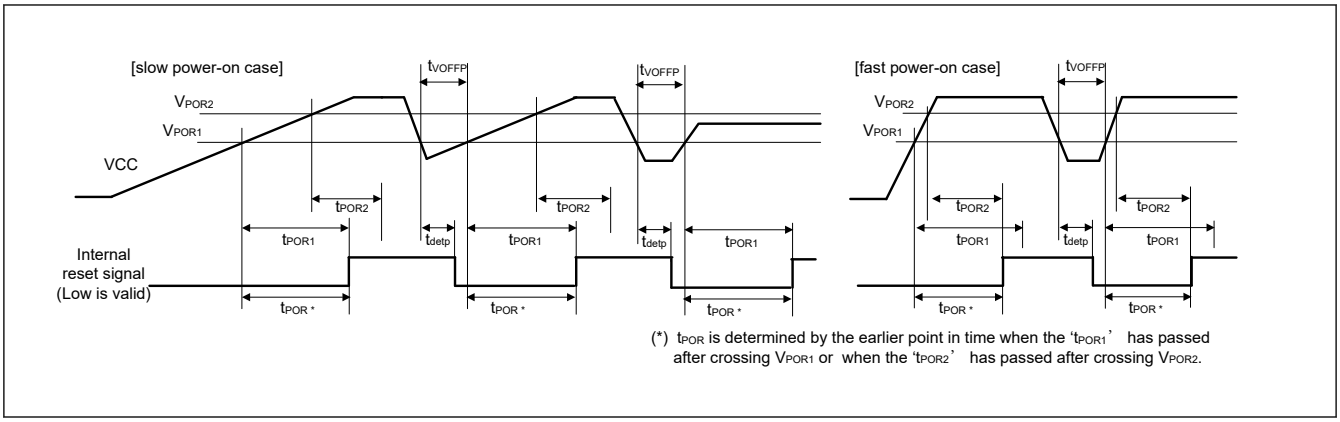


Figure 2.97 Power-on reset timing

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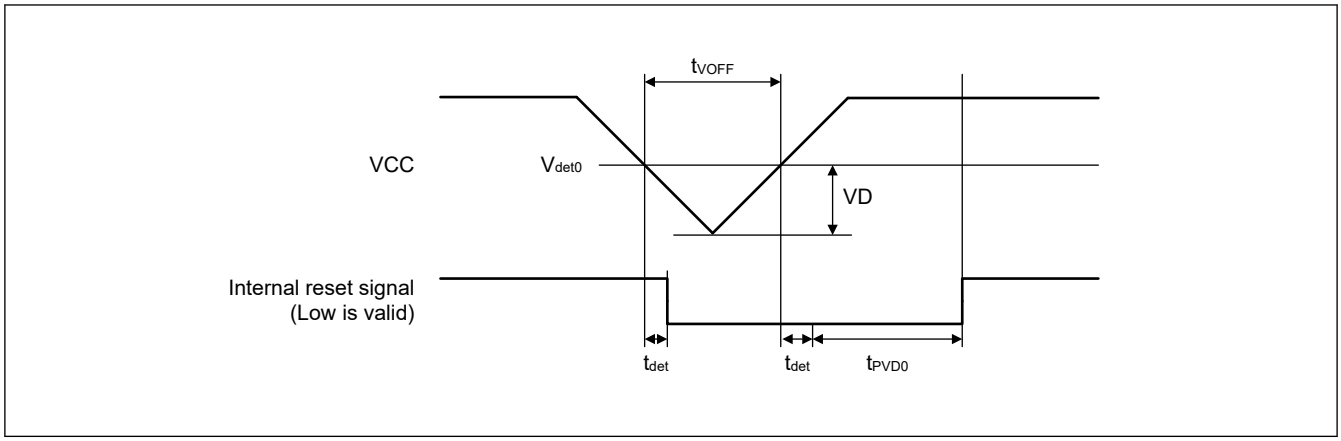


Figure 2.98 Voltage detection circuit timing (V_{det0})

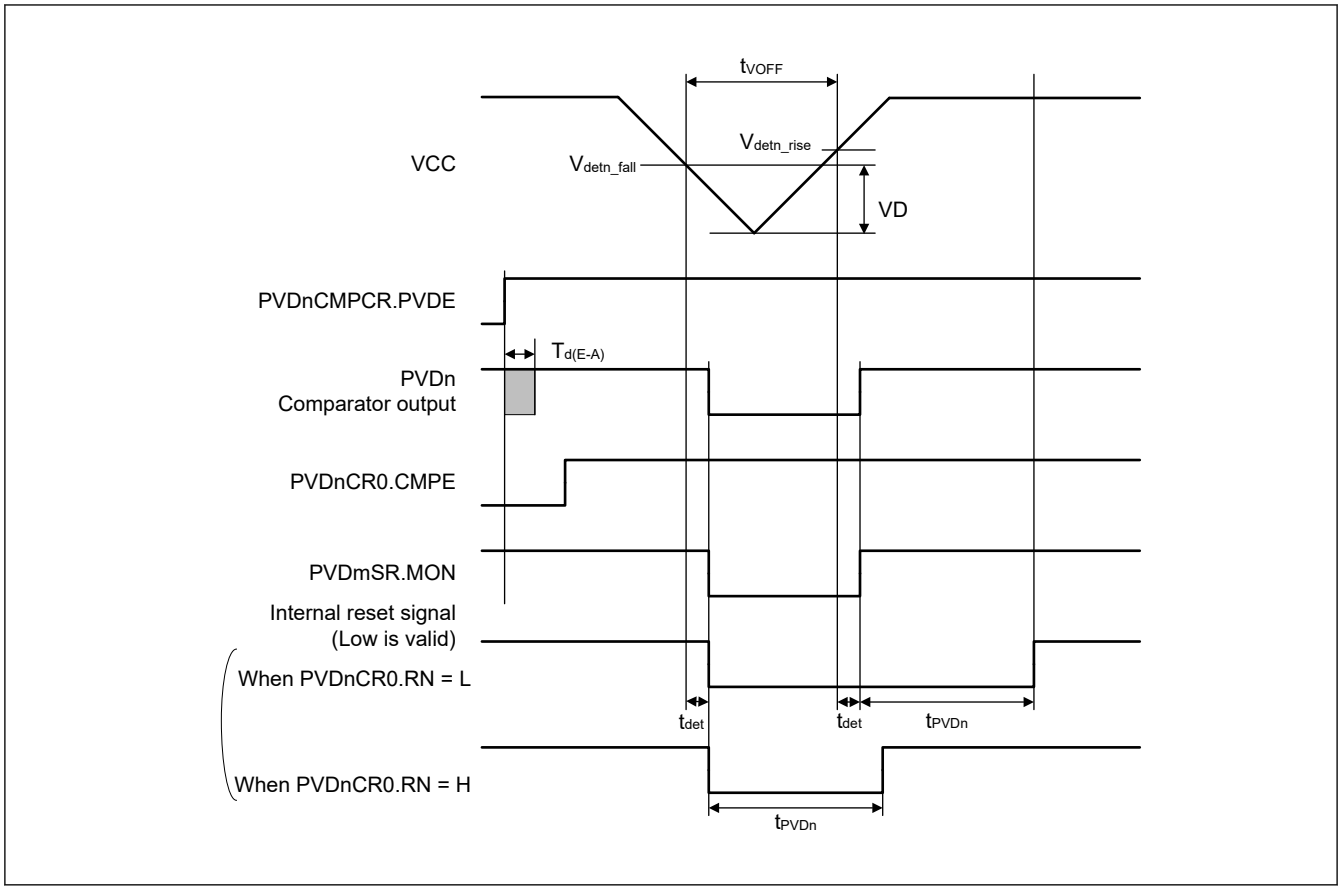


Figure 2.99 Voltage detection circuit timing (V_{detn}) (n = 1, 2)

2.10 ACMPHS Characteristics

Table 2.69 ACMPHS (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range			VREF	0	—	AVCC0	V	—
Input voltage range	ACMPHS0		VI	0	—	AVCC0	V	—
	ACMPHS1	IVCMP1 to IVCMP3		0	—	AVCC0		—
		IVCMP0		0	—	AVCC0		VCC >= AVCC0
				0	—	VCC		VCC < AVCC0

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Table 2.69 ACMPHS (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output delay*1			Td	—	50	100	ns	VI = VREF ± 100mV
Internal reference voltage			Vref	1.13	1.18	1.28	V	—

Note 1. This value is the internal propagation delay.

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.70 Code flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	Tj = +125°C
			20*2 *3	—	—	20*2 *3	—	—		Tj = +105°C
			30*2 *3	—	—	30*2 *3	—	—		Tj = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

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Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

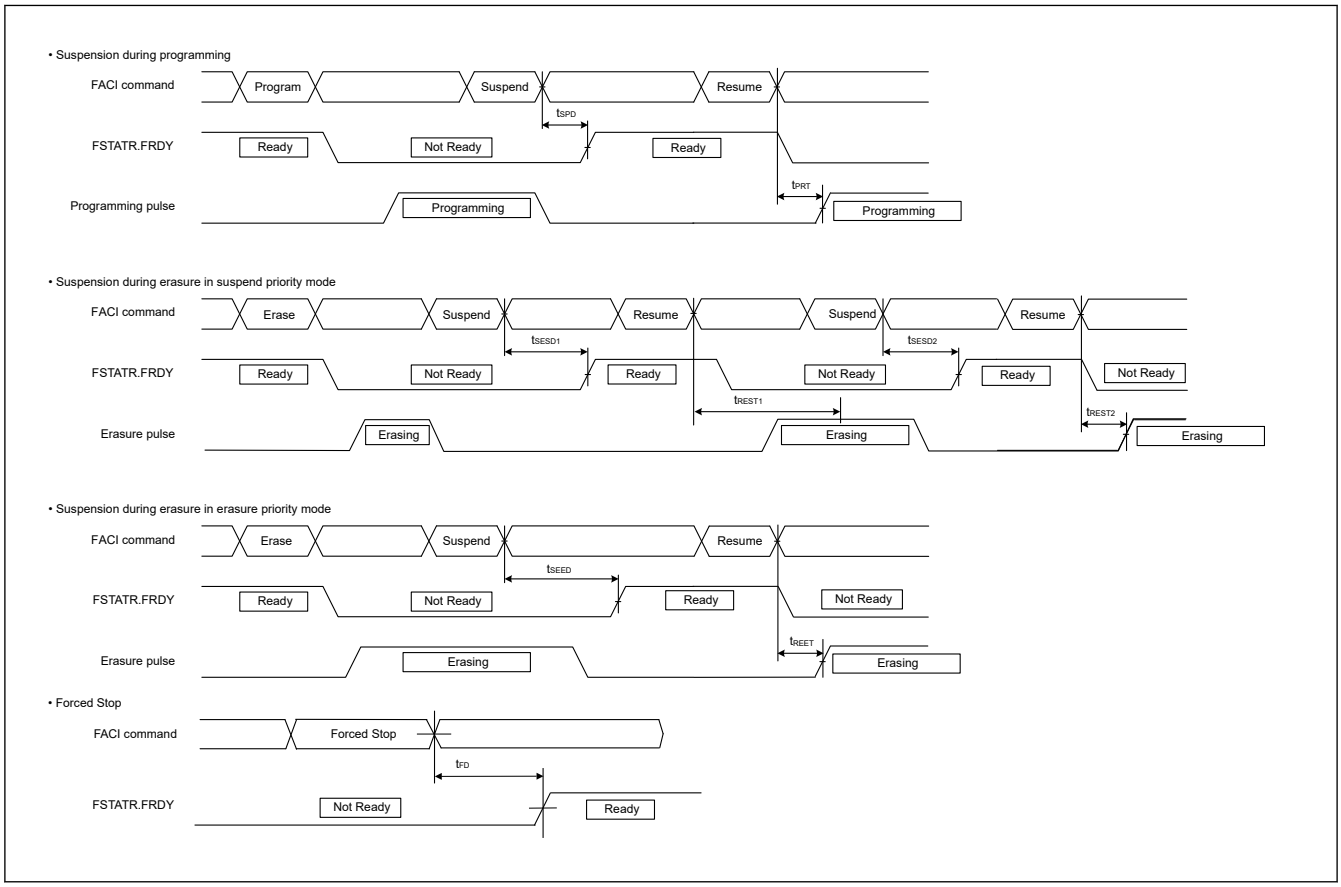


Figure 2.100 Suspension and forced stop timing for flash memory programming and erasure

2.11.2 Data Flash Memory Characteristics

Table 2.71 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	

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Table 2.71 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	Tj = +125°C
			20*3 *4	—	—	20*3 *4	—	—		Tj = +105°C
			30*3 *4	—	—	30*3 *4	—	—		Tj = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

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2.11.3 Option Setting Memory (Code flash memory) Characteristics

Table 2.72 Option setting memory (Code flash memory) characteristics

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 200 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 200 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	Tj = +125°C
		20*2 *3	—	—	20*2 *3	—	—		Tj = +105°C
		30*2 *3	—	—	30*2 *3	—	—		Tj = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.11.4 Option Setting Memory (Data flash memory) Characteristics

Table 2.73 Option Setting Memory (Data flash memory) characteristics

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Command time for configuration set (4 / 16 Byte)	t_{DCCT}	—	68	515	—	35	255	ms	
Update Cycles in Configuration area	N_{cupc}	125000 *1	—	—	125000 *1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	Tj = +125°C
		20*2 *3	—	—	20*2 *3	—	—		Tj = +105°C
		30*2 *3	—	—	30*2 *3	—	—		Tj = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.11.5 Anti-rollback counter Characteristics

Table 2.74 Anti-rollback counter characteristics (1 of 2)

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Command time for increment counter and refresh counter	t_{IRCT}	—	11.9	81	—	6.3	42	ms	
Command time for read counter	t_{RCT}	—	—	25	—	—	5	µs	

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Table 2.74 Anti-rollback counter characteristics (2 of 2)

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Update Cycles (total of increment and refreshing)	N_{cupc}	125000 *1	—	—	125000 *1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	Tj = +125°C
		20*2 *3	—	—	20*2 *3	—	—		Tj = +105°C
		30*2 *3	—	—	30*2 *3	—	—		Tj = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.12 Boundary Scan

Table 2.75 Boundary scan characteristics

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	1.68 V or above	t_{TCKcyc}	100	—	—	ns	Figure 2.101
TCK clock high pulse width	1.68 V or above	t_{TCKH}	0.45	—	—	t_{TCKcyc}	
TCK clock low pulse width	1.68 V or above	t_{TCKL}	0.45	—	—	t_{TCKcyc}	
TCK clock rise time	1.68 V or above	t_{TCKr}	—	—	0.05*2	t_{TCKcyc}	
TCK clock fall time	1.68 V or above	t_{TCKf}	—	—	0.05*2	t_{TCKcyc}	
TMS setup time	1.68 V or above	t_{TMSS}	20	—	—	ns	Figure 2.102
TMS hold time	1.68 V or above	t_{TMSH}	20	—	—	ns	
TDI setup time	1.68 V or above	t_{TDIS}	20	—	—	ns	
TDI hold time	1.68 V or above	t_{TDIH}	20	—	—	ns	
TDO data delay	1.68 V or above	t_{TDOD}	—	—	40	ns	
Capture register setup time	1.68 V or above	t_{CAPTS}	20	—	—	ns	Figure 2.103
Capture register hold time	1.68 V or above	t_{CAPTH}	20	—	—	ns	
Update register delay time	1.68 V or above	$t_{UPDATED}$	—	—	40	ns	
Boundary scan circuit startup time*1	1.68 V or above	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 2.104

Note 1. Boundary scan does not function until the power-on reset becomes negative.
Note 2. 1 µs at the longest

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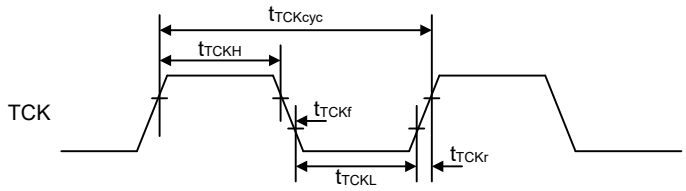


Figure 2.101 Boundary scan TCK timing

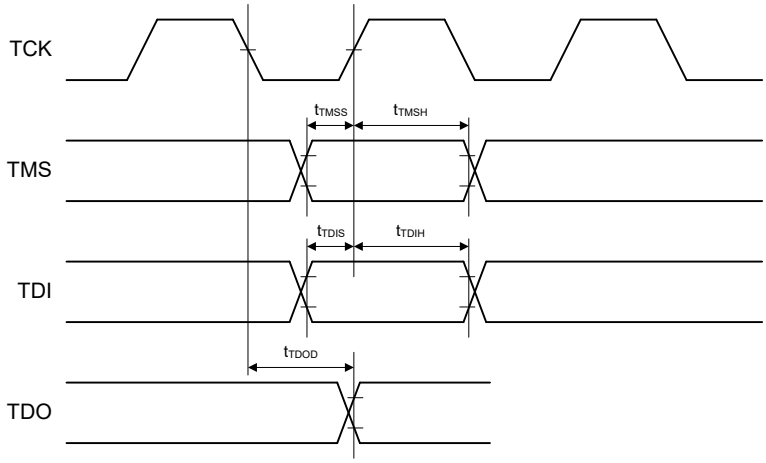


Figure 2.102 Boundary scan input/output timing (1)

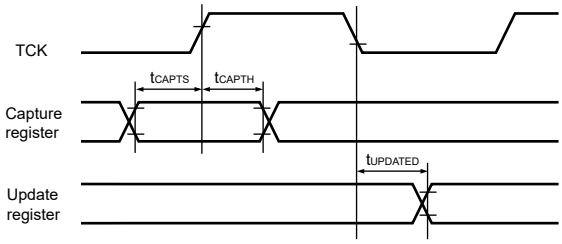


Figure 2.103 Boundary scan input/output timing (2)

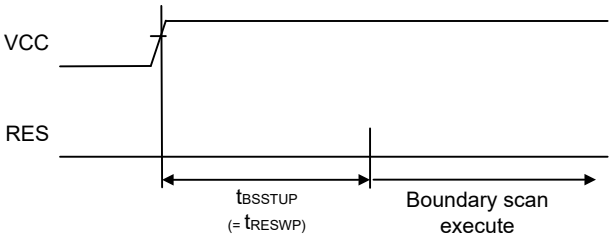


Figure 2.104 Boundary scan circuit startup timing

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2.13 Joint European Test Action Group (JTAG)

Table 2.76 JTAG

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	2.7 V or above	t_{TCKcyc}	40.0	—	—	ns	Figure 2.105
	1.68 V or above		40.0	—	—	ns	
TCK clock high pulse width	2.7 V or above	t_{TCKH}	0.375	—	—	t_{TCKcyc}	
	1.68 V or above		0.375	—	—	t_{TCKcyc}	
TCK clock low pulse width	2.7 V or above	t_{TCKL}	0.375	—	—	t_{TCKcyc}	
	1.68 V or above		0.375	—	—	t_{TCKcyc}	
TCK clock rise time	2.7 V or above	t_{TCKr}	—	—	0.125*1	t_{TCKcyc}	
	1.68 V or above		—	—	0.125*1	t_{TCKcyc}	
TCK clock fall time	2.7 V or above	t_{TCKf}	—	—	0.125*1	t_{TCKcyc}	
	1.68 V or above		—	—	0.125*1	t_{TCKcyc}	
TMS setup time	2.7 V or above	t_{TMSS}	8.0	—	—	ns	Figure 2.106
	1.68 V or above		8.0	—	—	ns	
TMS hold time	2.7 V or above	t_{TMSH}	8.0	—	—	ns	
	1.68 V or above		8.0	—	—	ns	
TDI setup time	2.7 V or above	t_{TDIS}	8.0	—	—	ns	
	1.68 V or above		8.0	—	—	ns	
TDI hold time	2.7 V or above	t_{TDIH}	8.0	—	—	ns	
	1.68 V or above		8.0	—	—	ns	
TDO data delay time	2.7 V or above	t_{TDOD}	—	—	20.0	ns	
	1.68 V or above		—	—	28.0	ns	

Note 1. 1 µs at the longest

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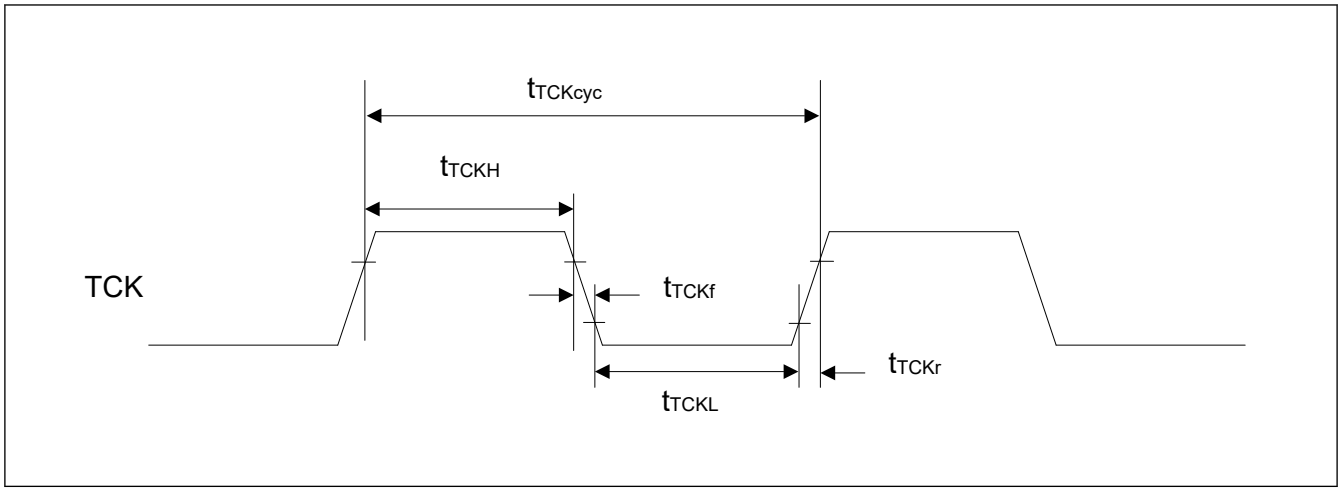


Figure 2.105 JTAG TCK timing

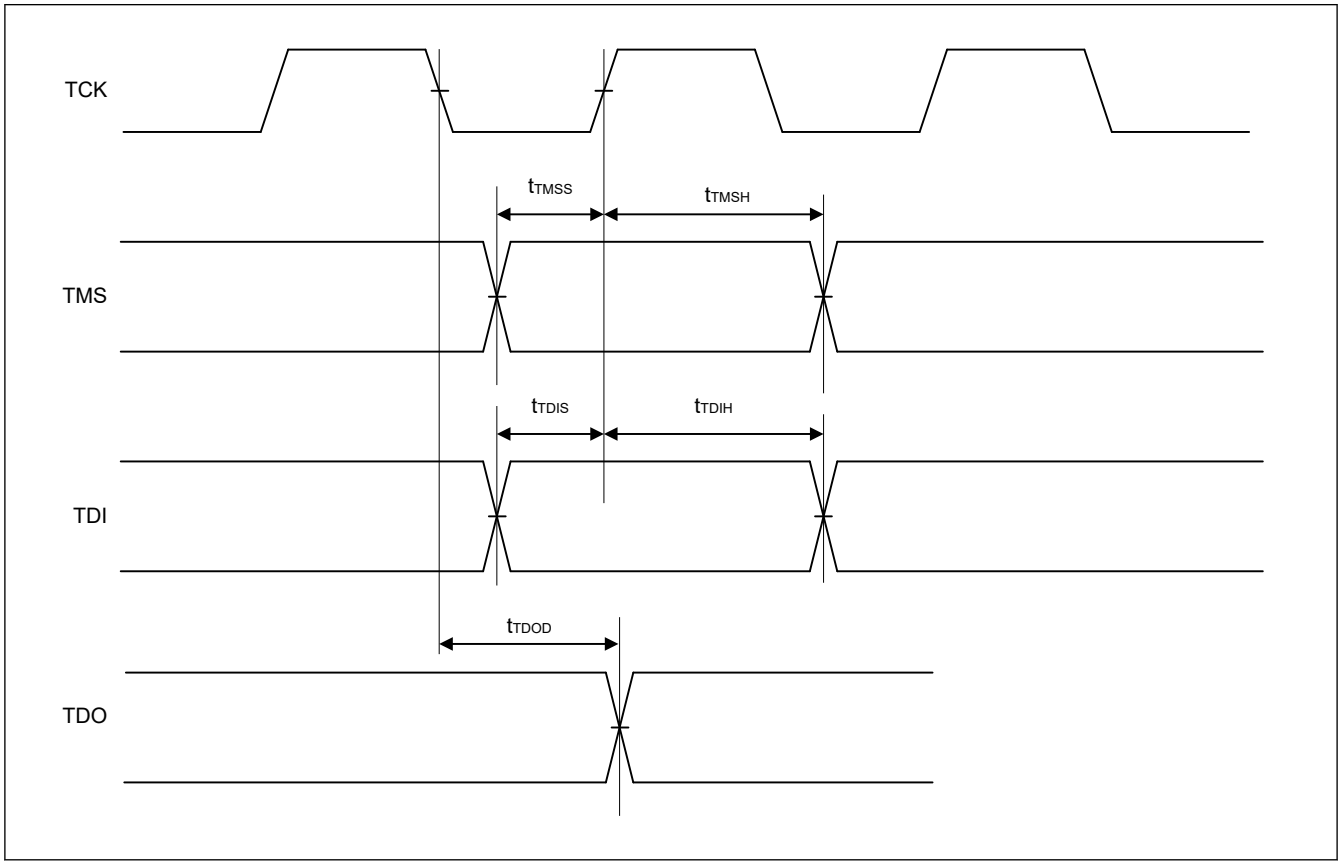


Figure 2.106 JTAG input/output timing

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2.14 Serial Wire Debug (SWD)

Table 2.77 SWD

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	2.7 V or above	$t_{SWCKcyc}$	40.0	—	—	ns	Figure 2.107
	1.68 V or above		40.0	—	—	ns	
SWCLK clock high pulse width	2.7 V or above	t_{SWCKH}	0.375	—	—	$t_{SWCKcyc}$	
	1.68 V or above		0.375	—	—	$t_{SWCKcyc}$	
SWCLK clock low pulse width	2.7 V or above	t_{SWCKL}	0.375	—	—	$t_{SWCKcyc}$	
	1.68 V or above		0.375	—	—	$t_{SWCKcyc}$	
SWCLK clock rise time	2.7 V or above	t_{SWCKr}	—	—	0.125*1	$t_{SWCKcyc}$	
	1.68 V or above		—	—	0.125*1	$t_{SWCKcyc}$	
SWCLK clock fall time	2.7 V or above	t_{SWCKf}	—	—	0.125*1	$t_{SWCKcyc}$	
	1.68 V or above		—	—	0.125*1	$t_{SWCKcyc}$	
SWDIO setup time	2.7 V or above	t_{SWDS}	8.0	—	—	ns	Figure 2.108
	1.68 V or above		8.0	—	—	ns	
SWDIO hold time	2.7 V or above	t_{SWDH}	8.0	—	—	ns	
	1.68 V or above		8.0	—	—	ns	
SWDIO data delay time	2.7 V or above	t_{SWDD}	2.0	—	28.0	ns	
	1.68 V or above		2.0	—	32.0	ns	

Note 1. 1 µs at the longest

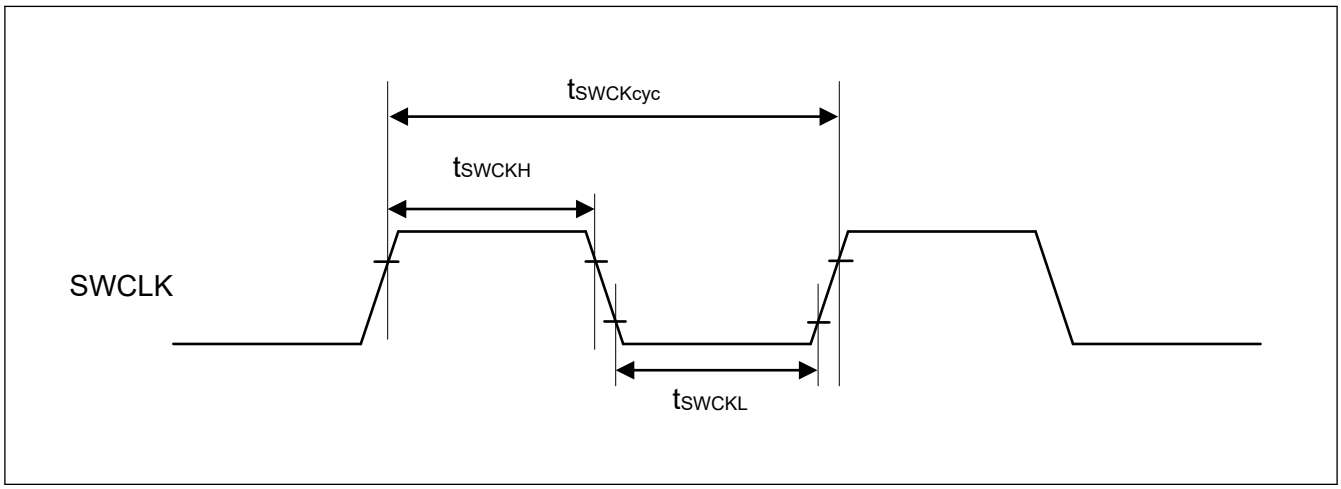


Figure 2.107 SWD SWCLK timing

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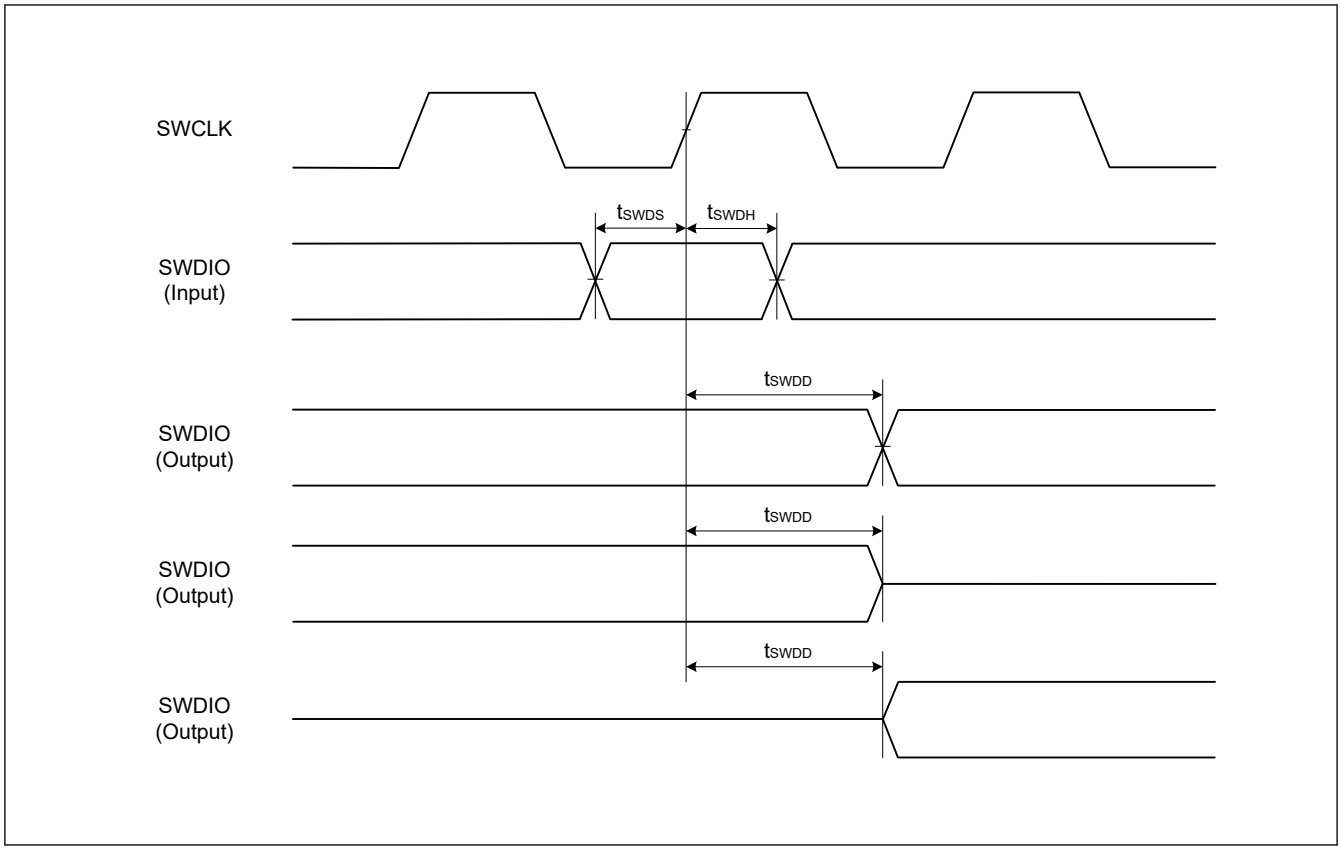


Figure 2.108 SWD input/output timing

2.15 Embedded Trace Macro Interface (ETM)

Table 2.78 ETM (1 of 2)

Conditions: High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	2.7 V or above	$t_{TCLKcyc}$	16.6	—	—	ns	Figure 2.109
	1.68 V or above		16.6	—	—	ns	
TCLK clock high pulse width	2.7 V or above	t_{TCLKH}	7.3	—	—	ns	
	1.68 V or above		6.3	—	—	ns	
TCLK clock low pulse width	2.7 V or above	t_{TCLKL}	7.3	—	—	ns	
	1.68 V or above		6.3	—	—	ns	
TCLK clock rise time	2.7 V or above	t_{TCLKr}	—	—	1.0	ns	
	1.68 V or above		—	—	2.0	ns	
TCLK clock fall time	2.7 V or above	t_{TCLKf}	—	—	1.0	ns	
	1.68 V or above		—	—	2.0	ns	

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Table 2.78 ETM (2 of 2)

Conditions: High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TDATA[3:0] output valid time	2.7 V or above	t_{TRDV}	—	—	$t_{TCLKcyc}/4 + 1.6$	ns	Figure 2.110
	1.68 V or above		—	—	$t_{TCLKcyc}/4 + 1.6$	ns	
TDATA[3:0] output hold time	2.7 V or above	t_{TRDH}	1.5	—	—	ns	
	1.68 V or above		1.5	—	—	ns	

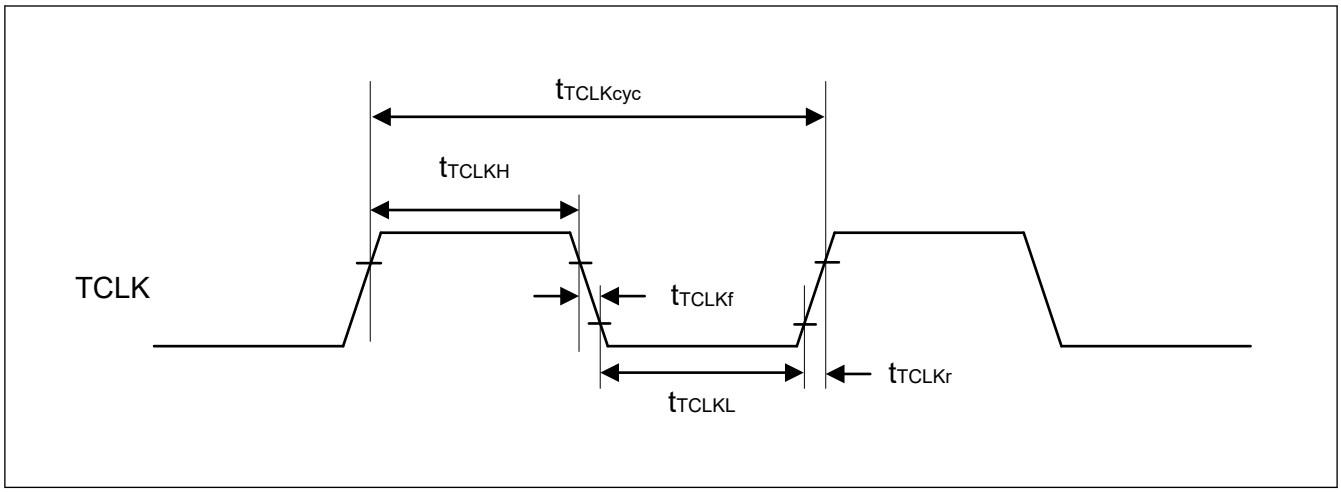


Figure 2.109 ETM TCLK timing

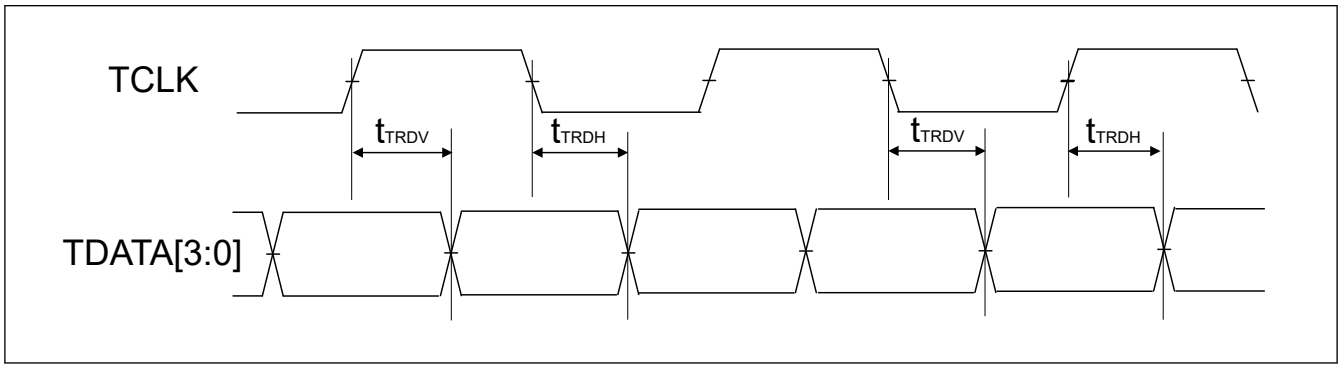


Figure 2.110 ETM output timing

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Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode(SSTBY)		Deep Software Standby mode 1,2,3 (DSTBY1,2,3)		After Deep Software Standby mode is canceled (return to startup mode)	
			OPE=0	OPE=1	DSTBY1	DSTBY2/ DSTBY3	IOKEEP = 0	IOKEEP = 1[*1]
Mode	MD	Pull-up	Keep-I		Keep		Pull-up	Keep
JTAG/SWD	TCK/TMS/TDI/SWCLK	Pull-up	TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input	
	TDO	Output	TDO output		TDO output		TDO output	
	SWDIO	Pull-up	SWDIO inout		SWDIO inout		SWDIO inout	
Trace	TCLK/TDATAx/SWO	TCLK/ TDATAx/SWO output	TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output	
IRQ	IRQx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	IRQx-DS (x:Other than 5)	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	Keep
	IRQ5-DS	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	
AGT	AGTIOn	Hi-Z	AGTIOn inout		Keep		Hi-Z	Keep
	AGTOn/AGTOAn/ AGTOBn	Hi-Z	AGTOn/AGTOAn/AGTOBn output		Keep		Hi-Z	Keep
ULPT	ULPTEEn/ULPTEVIn	Hi-Z	ULPTEEn/ULPTEVIn input		Keep		Hi-Z	Keep
	ULPTEEn-DS/ ULPTEVIn-DS	Hi-Z	ULPTEEn-DS/ULPTEVIn-DS input		ULPTEEn-DS/ ULPTEVIn-DS input	Hi-Z	Hi-Z	Keep
	ULPTOn/ ULPTOAn/ ULPTOBn	Hi-Z	ULPTOn/ULPTOAn/ULPTOBn output		Keep		Hi-Z	Keep
	ULPTOn-DS/ ULPTOAn-DS/ ULPTOBn-DS	Hi-Z	ULPTOn/ULPTOAn-DS/ ULPTOBn-DS output		ULPTOn/ ULPTOAn-DS/ ULPTOBn-DS output	Keep	Hi-Z	From DSTBY1: ULPTOn/ ULPTOAn-DS/ ULPTOBn-DS output From DSTBY2,3: Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O[*2]		Keep		Hi-Z	Keep
I3C	I3C_SCL0/I3C_SDA0	Hi-Z	Keep-O[*2]		Hi-Z		Hi-Z	
USBFS	USB_OVRCURx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	USB_OVRCURx-DS/ USB_VBUS	Hi-Z	Hi-Z[*2]		Keep[*3]	Keep	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O[*4]		Keep[*3]	Keep	Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output		Keep		Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	CLKOUT output		Keep		Hi-Z	Keep
DAC	DAn	Hi-Z	D/A output retained		Hi-Z		Hi-Z	
External bus (CS, SDRAM area)	EBCLK/SDCLK	Hi-Z	High-level output		Keep		Hi-Z	Keep
	Dxx/DQxx	Hi-Z	Hi-Z		Hi-Z		Hi-Z	
	Axx/DQMx	Hi-Z	Hi-Z	Keep-O	Keep		Hi-Z	Keep
	BC0	Hi-Z	Hi-Z	*5	Keep		Hi-Z	Keep
	BC1 to BC3/CSx/RD/WRx/WE	Hi-Z	Hi-Z	High-level output	Keep		Hi-Z	Keep
	ALE	Hi-Z	Hi-Z	Low-level output	Keep		Hi-Z	Keep
	CKE/SDCS/RAS/CAS	Hi-Z	Hi-Z	SDSELF.SFEN = 0: High-level output SDSELF.SFEN = 1: Low-level output	Keep		Hi-Z	Keep
P400/P401	Other than function IRQ5-DS	Hi-Z	Keep-O[*2]		Hi-Z		Hi-Z	

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Function	Pin function	Reset	Software Standby mode(SSTBY)		Deep Software Standby mode 1,2,3 (DSTBY1,2,3)		After Deep Software Standby mode is canceled (return to startup mode)	
			OPE=0	OPE=1	DSTBY1	DSTBY2/ DSTBY3	IOKEEP = 0	IOKEEP = 1*1
Others	—	Hi-Z	Keep-O		Keep		Hi-Z	Keep

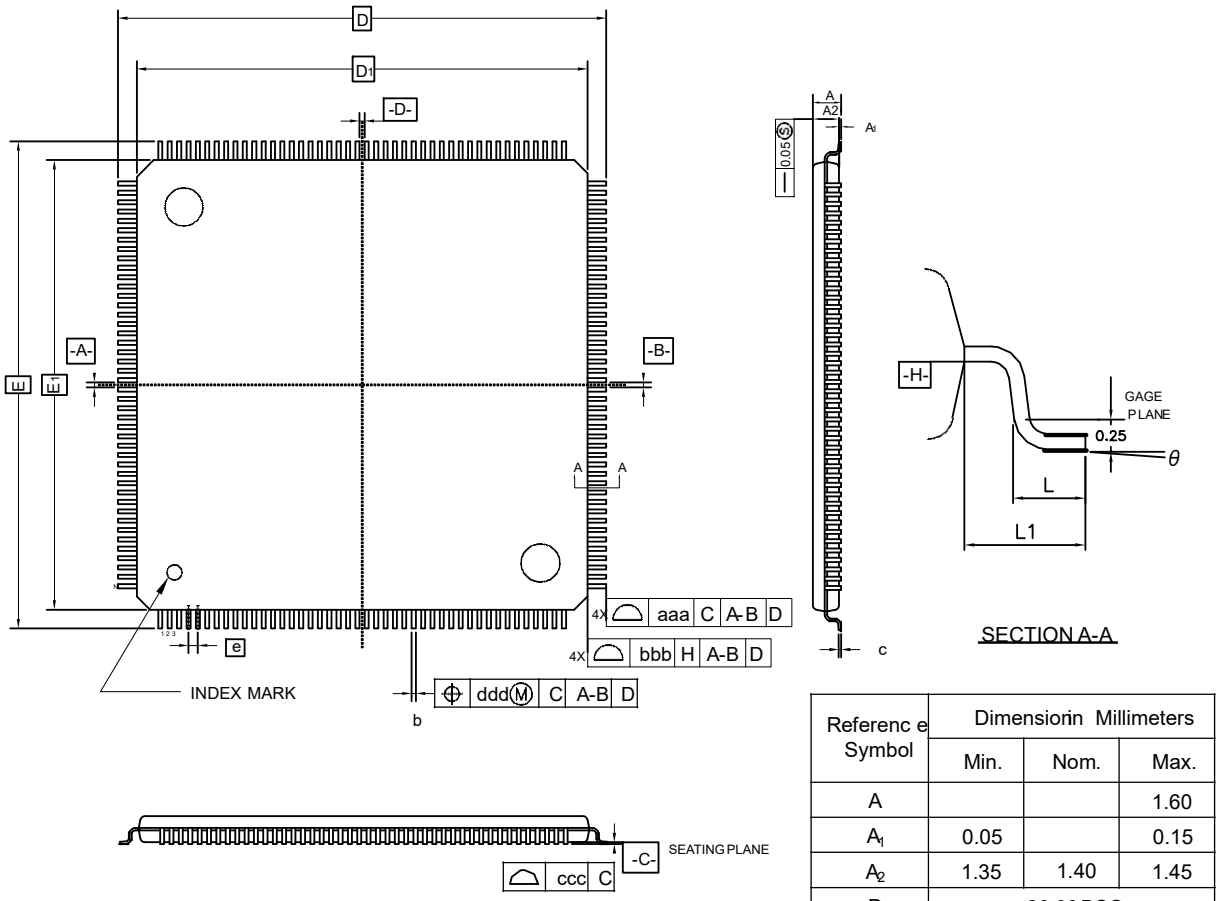
Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep-I: Pin states are retained same as during periods in Normal mode.
Keep: Pin states are retained same as during periods in Software Standby mode.
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input pin.
Note 5. Depending on the operation before the transition to Software Standby Mode, either High-level or Low-level is output. See the usage notes in 13. Buses of the User's Manual: Hardware.

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Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP176-24x24-0.50	PLQP0176KJ-A	1.90

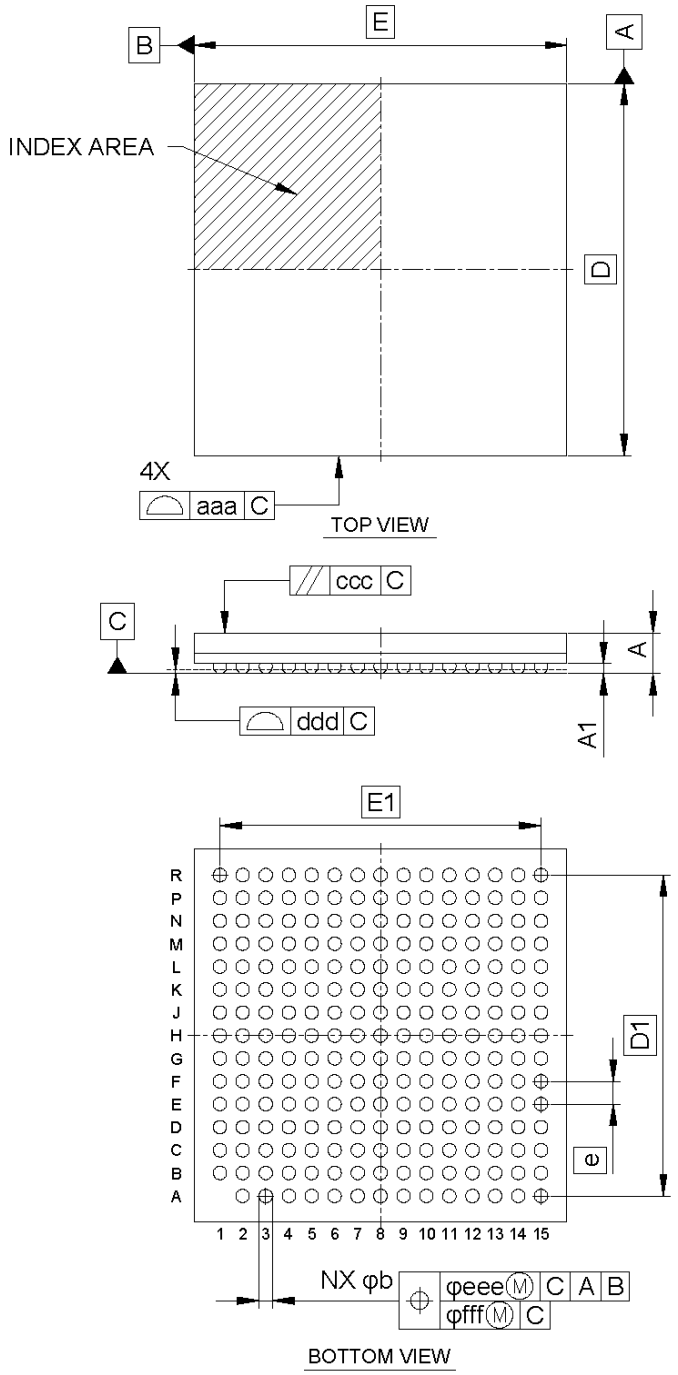


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
D		26.00 BSC.	
D_1		24.00 BSC.	
E		26.00 BSC.	
E_1		24.00 BSC.	
N		176	
e		0.50 BSC.	
b	0.17	0.22	0.27
c	0.09		0.20
q	0	3.5	7
L	0.45	0.60	0.75
L_1		1.00 REF.	
aaa			0.20
bbb			0.20
ccc			0.08
ddd			0.08

Figure A2.1 LQFP 176-pin

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JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA224-13x13-0.80	PLBG0224GD-A	0.44



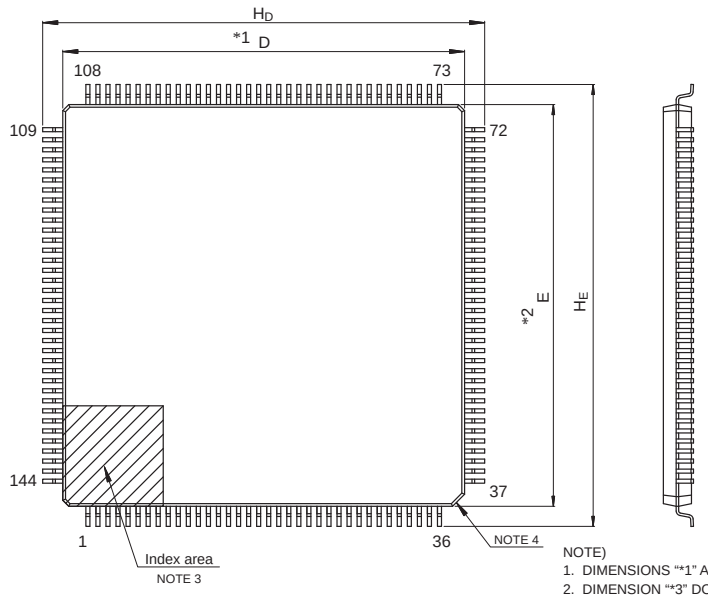
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	13.00	—
E	—	13.00	—
D1	—	11.20	—
E1	—	11.20	—
A	—	—	1.47
A1	0.29	—	—
b	0.42	0.47	0.52
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.12
eee	—	—	0.15
fff	—	—	0.08
N	—	224	—

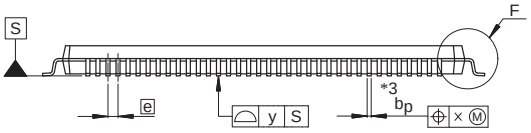
Figure A2.2 BGA 224-pin

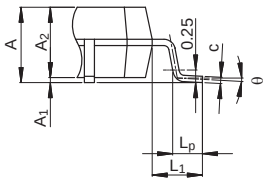
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JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

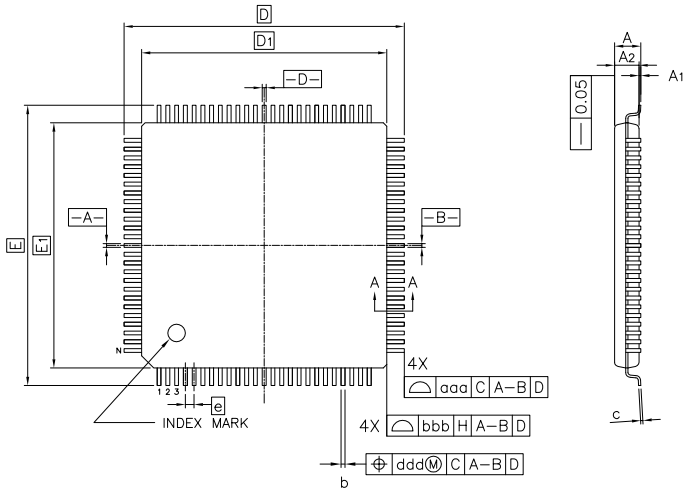
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

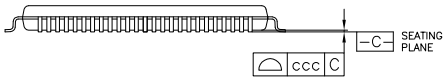
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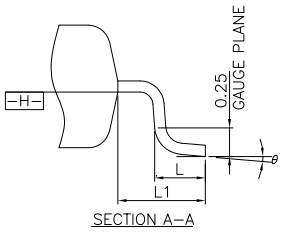
Figure A2.3 LQFP 144-pin

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JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP100-14x14-0.50	PLQP0100KP-A	0.67







Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	16.00	–
D_1	–	14.00	–
E	–	16.00	–
E_1	–	14.00	–
N	–	100	–
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

Figure A2.4 LQFP 100-pin

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Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 3)

Description	Name of Secure registers	Base address of Secure registers in Secure alias region	Name of Non-secure registers	Base address of Non-secure registers in Non-secure alias region
Renesas Memory Protection Unit	RMPU	0x4000_0000	RMPU_NS	0x5000_0000
SRAM Control	SRAM	0x4000_2000	SRAM_NS	0x5000_2000
BUS Control	BUS	0x4000_3000	BUS_NS	0x5000_3000
Common Interrupt Controller	ICU_COMMON	0x4000_6000	ICU_COMMON_NS	0x5000_6000
CPU System Security Control Unit	CPSCU	0x4000_8000	CPSCU_NS	0x5000_8000
Direct memory access controller 00	DMAC00	0x4000_A000	DMAC00_NS	0x5000_A000
Direct memory access controller 01	DMAC01	0x4000_A040	DMAC01_NS	0x5000_A040
Direct memory access controller 02	DMAC02	0x4000_A080	DMAC02_NS	0x5000_A080
Direct memory access controller 03	DMAC03	0x4000_A0C0	DMAC03_NS	0x5000_A0C0
Direct memory access controller 04	DMAC04	0x4000_A100	DMAC04_NS	0x5000_A100
Direct memory access controller 05	DMAC05	0x4000_A140	DMAC05_NS	0x5000_A140
Direct memory access controller 06	DMAC06	0x4000_A180	DMAC06_NS	0x5000_A180
Direct memory access controller 07	DMAC07	0x4000_A1C0	DMAC07_NS	0x5000_A1C0
DMAC Module Activation 0	DMA0	0x4000_A800	DMA0_NS	0x5000_A800
Data Transfer Controller 0	DTC0	0x4000_AC00	DTC0_NS	0x5000_AC00
Interrupt Controller	ICU	0x4000_C000	ICU_NS	0x5000_C000
CPU Control Registers	CPU_CTRL	0x4000_F000	CPU_CTRL_NS	0x5000_F000
On-Chip Debug	OCD_CPU	0x4001_1000	OCD_CPU_NS	0x5001_1000
DAP Function	OCD_DAP	0x8001_1000	—	—
Debug Function	CPU_DBG	0x4001_B000	CPU_DBG_NS	0x5001_B000
System Control	SYSC	0x4001_E000	SYSC_NS	0x5001_E000
Temperature Sensor Data	TSD	0x4011_B000	TSD_NS	0x5011_B000
Event Link Controller	ELC	0x4020_1000	ELC_NS	0x5020_1000
Realtime Clock	RTC	0x4020_2000	RTC_NS	0x5020_2000
Independent Watchdog Timer	IWDT	0x4020_2200	IWDT_NS	0x5020_2200
Clock Frequency Accuracy Measurement Circuit	CAC	0x4020_2400	CAC_NS	0x5020_2400
Watchdog Timer 0	WDT0	0x4020_2600	WDT0_NS	0x5020_2600
Module Stop Control A,B,C,D,E	MSTP	0x4020_3000	MSTP_NS	0x5020_3000
Peripheral Security Control Unit	PSCU	0x4020_4000	PSCU_NS	0x5020_4000
Port Output Enable Module for GPT	POEG	0x4021_2000	POEG_NS	0x5021_2000
Ultra-Low Power Timer 0	ULPT0	0x4022_0000	ULPT0_NS	0x5022_0000
Ultra-Low Power Timer 1	ULPT1	0x4022_0100	ULPT1_NS	0x5022_0100

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Table A3.1 Peripheral base address (2 of 3)

Description	Name of Secure registers	Base address of Secure registers in Secure alias region	Name of Non-secure registers	Base address of Non-secure registers in Non-secure alias region
Low Power Asynchronous General purpose Timer 0	AGT0	0x4022_1000	AGT0_NS	0x5022_1000
Low Power Asynchronous General purpose Timer 1	AGT1	0x4022_1100	AGT1_NS	0x5022_1100
Temperature Sensor	TSN	0x4023_5000	TSN_NS	0x5023_5000
High-Speed Analog Comparator 0	ACMPHS0	0x4023_6000	ACMPHS0_NS	0x5023_6000
High-Speed Analog Comparator 1	ACMPHS1	0x4023_6100	ACMPHS1_NS	0x5023_6100
USB 2.0 FS Module	USBFS	0x4025_0000	USBFS_NS	0x5025_0000
SD Host Interface 0	SDHI0	0x4025_2000	SDHI0_NS	0x5025_2000
SD Host Interface 1	SDHI1	0x4025_2400	SDHI1_NS	0x5025_2400
Inter-Integrated Circuit 0	IIC0	0x4025_E000	IIC0_NS	0x5025_E000
Inter-Integrated Circuit 0 Wake-up Unit	IIC0WU	0x4025_E014	IIC0WU_NS	0x5025_E014
Inter-Integrated Circuit 1	IIC1	0x4025_E100	IIC1_NS	0x5025_E100
CRC Calculator	CRC	0x4031_0000	CRC_NS	0x5031_0000
Data Operation Circuit	DOC_B	0x4031_1000	DOC_B_NS	0x5031_1000
General PWM 32-bit Timer 0	GPT320	0x4032_2000	GPT320_NS	0x5032_2000
General PWM 32-bit Timer 1	GPT321	0x4032_2100	GPT321_NS	0x5032_2100
General PWM 32-bit Timer 2	GPT322	0x4032_2200	GPT322_NS	0x5032_2200
General PWM 32-bit Timer 3	GPT323	0x4032_2300	GPT323_NS	0x5032_2300
General PWM 32-bit Timer 4	GPT324	0x4032_2400	GPT324_NS	0x5032_2400
General PWM 32-bit Timer 5	GPT325	0x4032_2500	GPT325_NS	0x5032_2500
General PWM 32-bit Timer 6	GPT326	0x4032_2600	GPT326_NS	0x5032_2600
General PWM 32-bit Timer 7	GPT327	0x4032_2700	GPT327_NS	0x5032_2700
General PWM 16-bit Timer 8	GPT168	0x4032_2800	GPT168_NS	0x5032_2800
General PWM 16-bit Timer 9	GPT169	0x4032_2900	GPT169_NS	0x5032_2900
General PWM 16-bit Timer 10	GPT1610	0x4032_2A00	GPT1610_NS	0x5032_2A00
General PWM 16-bit Timer 11	GPT1611	0x4032_2B00	GPT1611_NS	0x5032_2B00
General PWM 16-bit Timer 12	GPT1612	0x4032_2C00	GPT1612_NS	0x5032_2C00
General PWM 16-bit Timer 13	GPT1613	0x4032_2D00	GPT1613_NS	0x5032_2D00
Output Phase Switching Controller	GPT_OPS	0x4032_3F00	GPT_OPS_NS	0x5032_3F00
12bit A/D Converter 0	ADC120	0x4033_2000	ADC120_NS	0x5033_2000
12bit A/D Converter 1	ADC121	0x4033_2200	ADC121_NS	0x5033_2200
12-bit D/A converter	DAC12	0x4033_3000	DAC12_NS	0x5033_3000
DMA Controller for the Ethernet Controller Channel 0	EDMAC0	0x4035_4000	EDMAC0_NS	0x5035_4000
Ethernet Controller Channel 0	ETHERC0	0x4035_4100	ETHERC0_NS	0x5035_4100
Serial Communication Interface 0	SCI0_B	0x4035_8000	SCI0_B_NS	0x5035_8000
Serial Communication Interface 1	SCI1_B	0x4035_8100	SCI1_B_NS	0x5035_8100
Serial Communication Interface 2	SCI2_B	0x4035_8200	SCI2_B_NS	0x5035_8200
Serial Communication Interface 3	SCI3_B	0x4035_8300	SCI3_B_NS	0x5035_8300

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Table A3.1 Peripheral base address (3 of 3)

Description	Name of Secure registers	Base address of Secure registers in Secure alias region	Name of Non-secure registers	Base address of Non-secure registers in Non-secure alias region
Serial Communication Interface 4	SCI4_B	0x4035_8400	SCI4_B_NS	0x5035_8400
Serial Communication Interface 9	SCI9_B	0x4035_8900	SCI9_B_NS	0x5035_8900
Serial Peripheral Interface 0	SPI0	0x4035_C000	SPI0_NS	0x5035_C000
Serial Peripheral Interface 1	SPI1	0x4035_C100	SPI1_NS	0x5035_C100
I3C Bus Interface	I3C	0x4035_F000	I3C_NS	0x5035_F000
Error correction circuit for MBRAM0	ECCMB0	0x4036_F200	ECCMB0_NS	0x5036_F200
Error correction circuit for MBRAM1	ECCMB1	0x4036_F300	ECCMB1_NS	0x5036_F300
CANFD Module 0	CANFD0	0x4038_0000	CANFD0_NS	0x5038_0000
CANFD Module 1	CANFD1	0x4038_2000	CANFD1_NS	0x5038_2000
Port 0 Control Registers	PORT0	0x4040_0000	PORT0_NS	0x5040_0000
Port 1 Control Registers	PORT1	0x4040_0020	PORT1_NS	0x5040_0020
Port 2 Control Registers	PORT2	0x4040_0040	PORT2_NS	0x5040_0040
Port 3 Control Registers	PORT3	0x4040_0060	PORT3_NS	0x5040_0060
Port 4 Control Registers	PORT4	0x4040_0080	PORT4_NS	0x5040_0080
Port 5 Control Registers	PORT5	0x4040_00A0	PORT5_NS	0x5040_00A0
Port 6 Control Registers	PORT6	0x4040_00C0	PORT6_NS	0x5040_00C0
Port 7 Control Registers	PORT7	0x4040_00E0	PORT7_NS	0x5040_00E0
Port 8 Control Registers	PORT8	0x4040_0100	PORT8_NS	0x5040_0100
Port 9 Control Registers	PORT9	0x4040_0120	PORT9_NS	0x5040_0120
Port A Control Registers	PORTA	0x4040_0140	PORTA_NS	0x5040_0140
Port B Control Registers	PORTB	0x4040_0160	PORTB_NS	0x5040_0160
Pmn Pin Function Control Register	PFS	0x4040_0800	PFS_NS	0x5040_0800
Flash Cache	FCACHE	0x4001_C100	FCACHE_NS	0x5001_C100
Data Flash	FLAD	0x4011_C000	FLAD_NS	0x5011_C000
Flash Application Command Interface	FACI	0x4011_E000	FACI_NS	0x5011_E000
Data Flash Security Setting	FDFS	0x2703_0000	—	—

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.

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- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripheral base address symbol	Address*1		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*2			
	From	To	Read	Write	Read	Write		
RMPU, SRAM, BUS, ICU_COMMON, CPSCU, DMAC0n, DMA0, DTC0, ICU, CPU_CTRL	0x4000_0000	0x4001_CFFF	3	2	3	2	ICLK	Renesas Memory Protection Unit, SRAM Control, BUS Control, Common Interrupt Controller, CPU System Security Control Unit, Direct memory access controller 0 n, DMAC Module Activation 0, Data Transfer Controller 0, Interrupt Controller, CPU Control Registers
CPU_OCD	0x4001_1004	0x4001_1FFF	7	2	7	2	ICLK	On-Chip Debug
CPU_DBG, FCACHE	0x4000_B000	0x4001_CFFF	3	2	3	2	ICLK	Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E9FF	4	3	2 to 4	1 to 3	PCLKB	System Control
SYSC	0x4001_EA00	0x4001_ED7F	7	6	5 to 7	4 to 6	PCLKB	System Control
TSD	0x4011_B17C	0x4011_B17C	4	3	4	3	ICLK	Temperature Sensor Data
ELC	0x4020_1000	0x4020_21FF	4	3	2 to 4	1 to 3	PCLKB	Event Link Controller
IWDT	0x4020_2200	0x4020_22FF	4	65	2 to 4	63 to 65	PCLKB	Independent Watchdog Timer
CAC, WDT0, MSTP, PSCU, POEG	0x4020_2400	0x4021_2FFF	4	3	2 to 4	1 to 3	PCLKB	Clock Frequency Accuracy Measurement Circuit, Watchdog Timer 0, Module Stop Control, Peripheral Security Control Unit, Port Outupt Enable Module for GPT
ULPTn	0x4022_0000	0x4022_01FF	6	65	4 to 6	63 to 65	PCLKB	Ultra-Low Power Timer n
AGTn	0x4022_1000	0x4022_11FF	6	3	4 to 6	1 to 3	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x4023_5000	0x4023_5FFF	4	3	2 to 4	1 to 3	PCLKB	Temperature Sensor
ACMPHSn	0x4023_6000	0x4023_61FF	3	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator n
USBFS	0x4025_0000	0x4025_03FF	5	4	3 to 5	2 to 4	PCLKB	USB 2.0 FS Module
USBFS	0x4025_0400	0x4025_04FF	4	65	2 to 4	63 to 65	PCLKB	USB 2.0 FS Module
SDHIn, IICn	0x4025_2000	0x4026_88FF	4	3	2 to 4	1 to 3	PCLKB	SD Host Interface n, Inter-Integretad Circuit n
CRC, DOC	0x4031_0000	0x4031_1FFF	4	3	2 to 4	1 to 3	PCLKA	CRC Calculator, Data Operation Circuit
GPT32n, GPT16n, GPT_OPS	0x4032_2000	0x4032_3FFF	7	4	5 to 7	2 to 4	PCLKA	General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12n	0x4033_2000	0x4034_6FFF	4	3	2 to 4	1 to 3	PCLKA	12-bit A/D Converter n, 12-bit D/A Converter n
EDMAC0	0x4035_4000	0x4035_40FF	5	4	3 to 5	2 to 4	PCLKA	DMA Controller for the Ethernet Controller Channel 0
ETHERC0	0x4035_4100	0x4035_43FF	14	13	12 to 14	11 to 13	PCLKA	Ethernet Controller Channel 0

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Table A3.2 Access cycles (2 of 3)

Peripheral base address symbol	Address*1		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*2		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
SCIn, SPIn, I3C	0x4035_8000	0x4035_FFFF	4	3	2 to 4	1 to 3	PCLKA	Serial Communication Interface n, Serial Peripheral Interface n, I3C Bus Interface
ECCMBn	0x4036_F200	0x4036_F3FF	5	4	3 to 5	2 to 4	PCLKA	Error correction circuit for MBRAMn
CANFDn	0x4038_0000	0x4038_3FFF	4	3	2 to 4	1 to 3	PCLKA	CANFD Module n
PORTn	0x4040_0000	0x4040_01FF	4	2	4	2	ICLK	Port n Control Registers
PFS	0x4040_0800	0x4040_0FFF	8	2	8	2	ICLK	Pmn Pin Function Control Register
RSIP-E51A	—	—	1 to 3	2	1 to 3	1 to 2	PCLKA	Renesas Security IP

Table A3.2 Access cycles (3 of 3)

Peripheral base address symbol	Address*1		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*2		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x4011_C040	0x4011_EFFF	4	3	4	3	FCLK	Data Flash, Flash Application Command Interface

Note 1. This table only shows secure address. Access cycle of the non-secure address is the same as its secure address.
Note 2. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

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Appendix 4. Note for Register R/W

- A secure bus master issues a "secure access" using an address marked as secure by IDAU/SAU or MSAU.
- A secure bus master issues a "non-secure access" using an address marked as non-secure by IDAU/SAU or MSAU.
- A non-secure bus master issues a "non-secure access" using an address marked as non-secure by IDAU/SAU or MSAU.

Table A4.1 Type of Register Notes (S-TYPE)

TYPE	UM Description
S-TYPE-1	Only Secure access can write to this register. Read access is always allowed. Non-secure write access is ignored, but TrustZone access error is not generated.
S-TYPE-2	Read access is always allowed If the security attribution is configured as Secure, ● Secure write access is allowed. ● Non-secure write access is ignored, but TrustZone access error is not generated.
	If the security attribution is configured as Non-secure, ● Secure write access is ignored, but TrustZone access error is not generated. ● Non-secure access is allowed.
S-TYPE-3	If the security attribution is configured as Secure, ● Secure access is allowed. ● Non-secure write access is ignored and Non-secure read access is read as 0, TrustZone access error is generated
	If the security attribution is configured as Non-secure, ● Secure write access is ignored and Secure read access is read as 0, TrustZone access error is generated. ● Non-secure access is allowed
S-TYPE-4	If the security attribution is configured as Secure, ● Secure access is allowed ● Non-secure write access is ignored and Non-secure read access is read as 0, but TrustZone access error is not generated.
	If the security attribution is configured as Non-secure, ● Secure write access is ignored and Secure read access is read as 0, but TrustZone access error is not generated. ● Non-secure access is allowed.
S-TYPE-5	Access is always allowed.
S-TYPE-6	Secure access is allowed. Non-secure write access is ignored, and Non-secure read access is read as 0, TrustZone access error is generated.
S-TYPE-7	Secure write access is ignored, and Secure read access is read as 0, TrustZone access error is generated. Non-secure access is allowed.

Note: A non-secure bus master does NOT issue any access using an address marked as secure by IDAU/SAU or MSAU.

Table A4.2 Type of Register Notes (P-TYPE)

TYPE	UM Description
P-TYPE-1	Privileged write access is allowed. Read access is always allowed. Unprivileged write access is ignored, but TrustZone access error is not generated.
P-TYPE-2	Privileged access is allowed. Unprivileged write access is ignored, and Unprivileged read access is read as 0, TrustZone access error is generated.
P-TYPE-3	If the privilege attribution is configured as Privileged, ● Privileged access is allowed. ● Unprivileged write access is ignored and Unprivileged read access is read as 0, TrustZone access error is generated.
	If the privilege attribution is configured as Unprivilege, ● Privileged access and Unprivileged access are allowed.
P-TYPE-4	If the privilege attribution is configured as Privileged, ● Privileged access is allowed. ● Unprivileged write access is ignored and Unprivileged read access is read as 0, TrustZone access error is not generated.
	If the privilege attribution is configured as Unprivilege, ● Privileged access and Unprivileged access are allowed.
P-TYPE-5	Access is always allowed.

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Appendix 5. Peripheral Variant

Table A5.1 shows the correspondence between the module name used in this manual and the Peripheral Variant.

Table A5.1 Module name vs Peripheral Variant

Module name	Peripheral variant
SCI	SCI_B
SPI	SPI_B
DOC	DOC_B

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Revision History

Revision 1.10 — January 23, 2024

First edition, issued

Revision 1.20 — November 22, 2024

Features:
- Updated Security and Encryption.

1. Overview:
- Updated Table 1.13 Function Comparison.

2. Electrical Characteristics:
- Updated Table 2.8 Current of high-speed mode, maximum condition (MVE and peripheral operation) (DCDC mode).
- Updated Table 2.9 Current of high-speed mode, maximum condition (MVE and peripheral operation) (External VDD mode).
- Updated Table 2.27 Power consumption of each unit.
- Updated Table 2.56 CANFD interface timing.

Appendix 5. Peripheral Variant:
- Added Appendix 5. Peripheral Variant.

Revision 1.30 — December 19, 2025

1. Overview:
- Updated Figure 1.2 Part numbering scheme.
- Updated Table 1.13 Function Comparison.
- Updated Table 1.15 Pin list.

2. Electrical Characteristics:
- Updated Table 2.6 I/O I_{OH}, I_{OL}.
- Updated Table 2.54 SD/MMC Host Interface signal timing.
- Added Table 2.64 A/D input voltage range for each input channel.

Appendix 4. Note for Register R/W:
- Updated Table A4.1 Type of Register Notes(S-TYPE).
- Updated Table A4.2 Type of Register Notes(P-TYPE).

Appendix 5. Peripheral Variant:
- Updated Table A5.1 Module name vs Peripheral Variant.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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