

THC63LVD104C

112MHz 30Bits COLOR LVDS Receiver

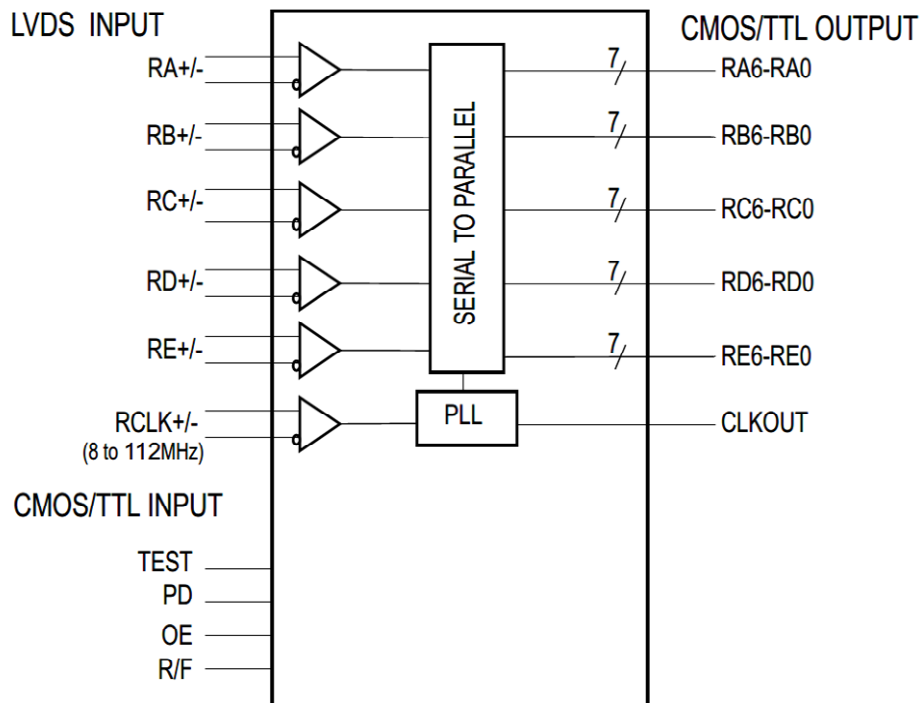
General Description

The THC63LVD104C receiver is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA resolutions. The THC63LVD104C converts the LVDS data streams back into 35bits of CMOS/TTL data with the choice of the rising edge or falling edge clock for the convenience with a variety of LCD panel controllers. At a transmit clock frequency of 112MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted at an effective rate of 784Mbps per LVDS channel. Using a 112MHz clock, the data throughput is 490Mbytes per second

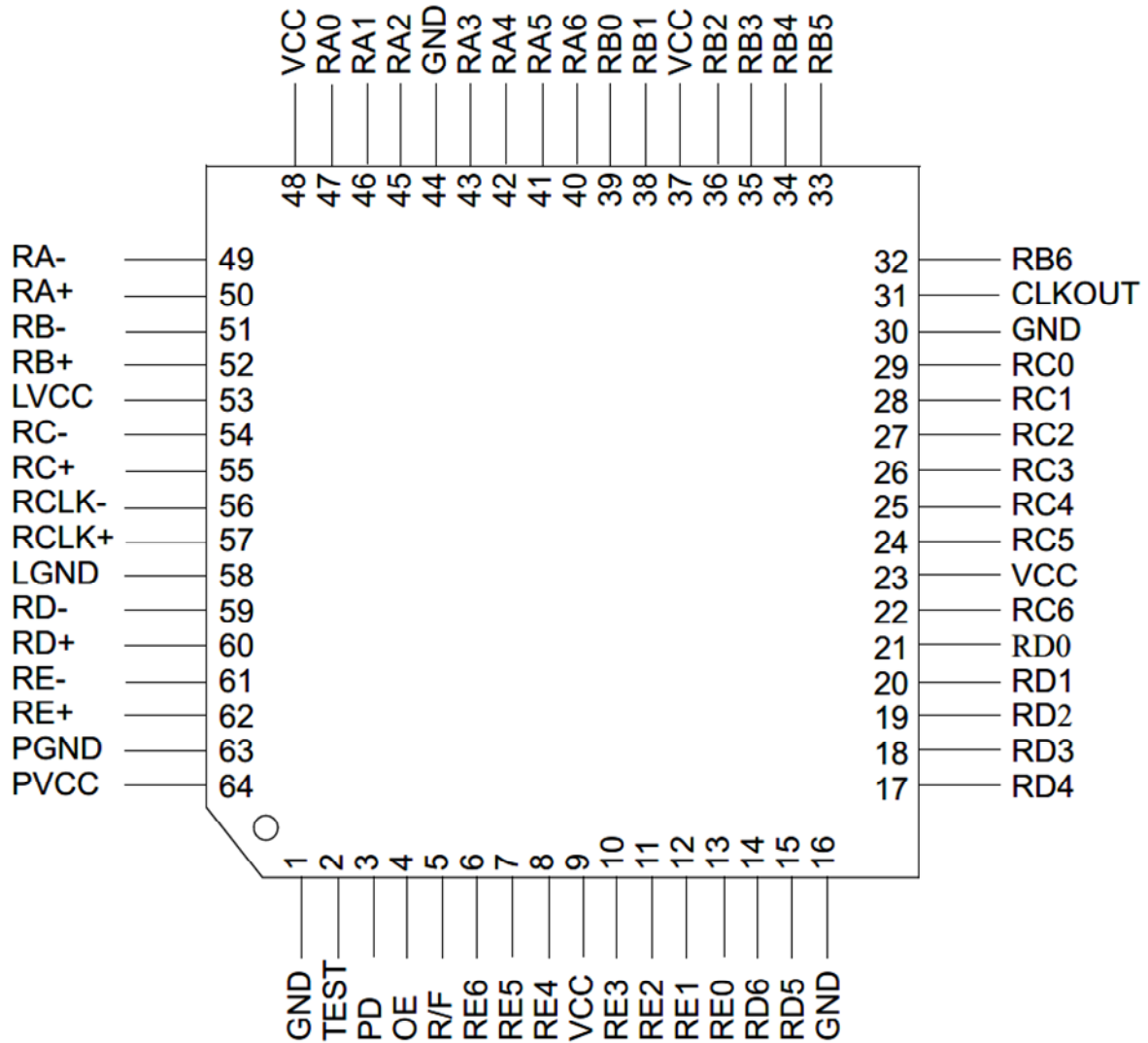
Features

- Wide dot clock range: 8-112MHz suited for NTSC, VGA, SVGA, XGA, and SXGA
- PLL requires no external components
- 50% output clock duty cycle
- TTL clock edge programmable
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Backward compatible with THC63LVDF64x (18bits) / F84x(24bits)
- Pin compatible with THC63LVD104A
- Fail-safe for Open LVDS Input

Block Diagram



Pin Diagram



| Pin Name | Pin # | Type | Description |
|--------------|----------------------|---------|---|
| RA+, RA- | 50, 49 | LVDS IN | LVDS Data In. |
| RB+, RB- | 52, 51 | LVDS IN | |
| RC+, RC- | 55, 54 | LVDS IN | |
| RD+, RD- | 60, 59 | LVDS IN | |
| RE+, RE- | 62, 61 | LVDS IN | |
| RCLK+, RCLK- | 57, 56 | LVDS IN | LVDS Clock In. |
| RA6 ~ RA0 | 40,41,42,43,45,46,47 | OUT | CMOS/TTL Data Outputs. |
| RB6 ~ RB0 | 32,33,34,35,36,38,39 | OUT | |
| RC6 ~ RC0 | 22,24,25,26,27,28,29 | OUT | |
| RD6 ~ RD0 | 14,15,17,18,19,20,21 | OUT | |
| RE6 ~ RE0 | 6,7,8,10,11,12,13 | OUT | |
| TEST | 2 | IN | Test pin, must be "L" for normal operation. |
| PD | 3 | IN | H: Normal operation, L: Power down (all outputs are "L") |
| OE | 4 | IN | H: Output enable (Normal operation). L: Output disable(all outputs are Hi-Z) |
| R/F | 5 | IN | Output Clock Triggering Edge Select. H: Rising edge, L: Falling edge |
| VCC | 9,23,37,48 | Power | Power Supply Pins for TTL outputs and digital circuitry. |
| CLKOUT | 31 | OUT | Clock out. |
| GND | 1,16,30,44 | Ground | Ground Pins for TTL outputs and digital circuitry. |
| LVCC | 53 | Power | Power Supply Pin for LVDS inputs. |
| LGND | 58 | Ground | Ground Pin for LVDS inputs. |
| PVCC | 64 | Power | Power Supply Pin for PLL circuitry. |
| PGND | 63 | Ground | Ground Pin for PLL circuitry. |

| PD | R/F | OE | Data Outputs (Rxn) | CLKOUT |
|----|-----|----|--------------------|--|
| 0 | 0 | 0 | Hi-Z | Hi-Z |
| 0 | 0 | 1 | All 0 | Fixed Low |
| 0 | 1 | 0 | Hi-Z | Hi-Z |
| 0 | 1 | 1 | All 0 | Fixed Low |
| 1 | 0 | 0 | Hi-Z | Hi-Z |
| 1 | 0 | 1 | Data Out | The falling edge closer to the center of the data eye. |
| 1 | 1 | 0 | Hi-Z | Hi-Z |
| 1 | 1 | 1 | Data Out | The rising edge closer to the center of the data eye. |

** Rxn

x = A,B,C,D,E

n = 0,1,2,3,4,5,6

Absolute Maximum Ratings *1

| | |
|--|----------------------------------|
| Supply Voltage (V _{CC} =V _{CC} =LV _{CC} =PV _{CC}) | -0.3V ~ +4.0V |
| CMOS/TTL Input Voltage | -0.3V ~ (V _{CC} + 0.3V) |
| CMOS/TTL Output Voltage | -0.3V ~ (V _{CC} + 0.3V) |
| LVDS Receiver Input Voltage | -0.3V ~ (V _{CC} + 0.3V) |
| Output Current | -30mA ~ 30mA |
| Junction Temperature | +125 °C |
| Storage Temperature Range | -55 °C ~ +150 °C |
| Reflow Peak Temperature / Time | +260 °C / 10sec. |
| Maximum Power Dissipation @+25 °C | 2.1W |

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} =LV_{CC}=PV_{CC}= 3.0V ~ 3.6V, Ta = -20° C~ +85°C

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------|---------------------------|---|------|------|-----------------|-------|
| V _{IH} | High Level Input Voltage | - | 2.0 | - | V _{CC} | V |
| V _{IL} | Low Level Input Voltage | - | GND | - | 0.8 | V |
| V _{OH} | High Level Output Voltage | I _{OH} = -4mA (data) I _{OH} = -8mA (clock) | 2.4 | - | - | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = 4mA (data) I _{OL} = 8mA (clock) | - | - | 0.4 | V |
| I _{INC} | Input Current | 0V δ V _{IN} δ V _{CC} | - | - | ±10 | μA |

LVDS Receiver DC Specifications

V_{CC} =LV_{CC}=PV_{CC}= 3.0V ~ 3.6V, Ta = -20° C~ +85°C

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------|-----------------------------------|---|------|------|------|-------|
| V _{TH} | Differential Input High Threshold | V _{IC} = 1.2V | - | - | 100 | mV |
| V _{TL} | Differential Input Low Threshold | V _{IC} = 1.2V | -100 | - | - | mV |
| I _{INL} | Input Current | V _{IN} = 2.4V / 0V V _{CC} = 3.6V | - | - | 30 | μA |

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

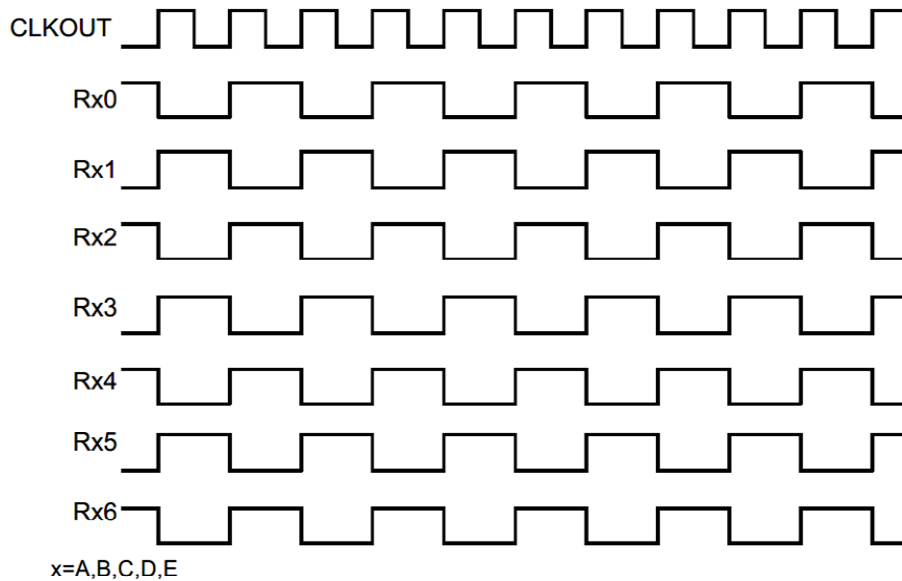
Supply Current

VCC =LVCC=PVCC= 3.0V ~ 3.6V, Ta = -20° C~ +85°C

| Symbol | Parameter | Conditions | Typ. | Max. | Units |
|--------|--|------------------|------|------|-------|
| IRCCW | Receiver Supply Current (LVDS Full Toggle) | fCLKOUT = 75MHz | - | 205 | mA |
| | | fCLKOUT = 90MHz | | 236 | mA |
| | | fCLKOUT = 112MHz | - | 280 | mA |
| IRCCS | Receiver Power Down Supply Current | PD = L | - | 25 | μA |

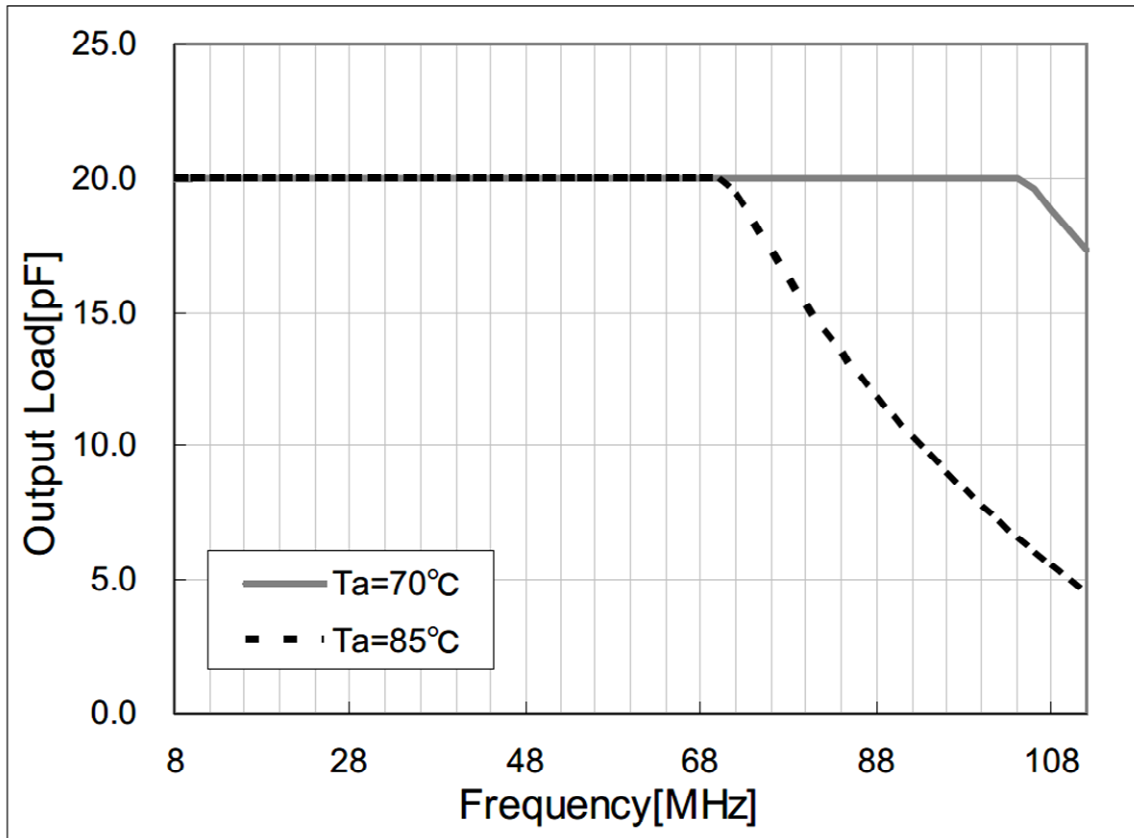
*The trade-off between the output load and the ambient temperature exists so that the junction temperature does not exceed 125°C.

LVDS Full Toggle Pattern



Output load limitation

The output load is limited so that the junction temperature does not exceed 125°C.



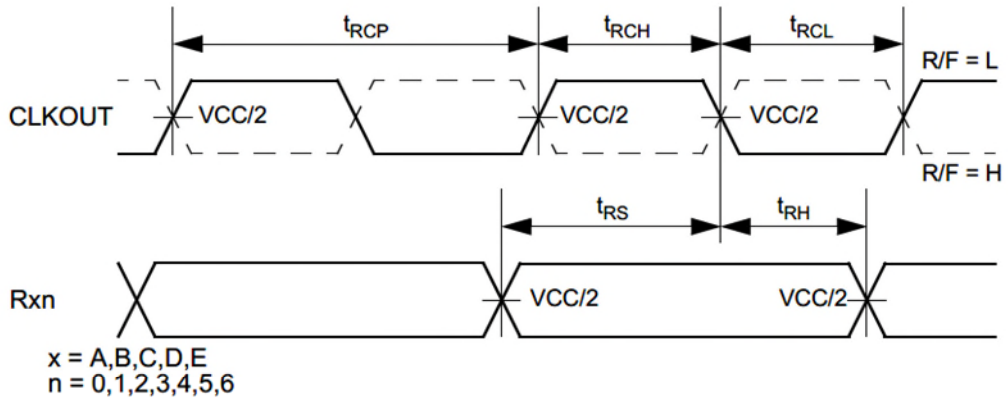
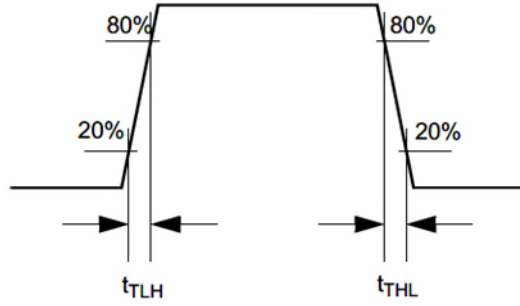
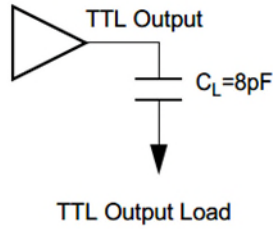
Switching Characteristics

VCC =LVCC=PVCC= 3.0V ~ 3.6V, Ta = -20° C ~+85°C

| Symbol | Parameter | Min. | Typ. | Max. | Units | |
|--------|---------------------------------|----------------------|-------|----------------------|-------|----|
| tRCP | CLKOUT Period | 8.92 | T | 125.0 | ns | |
| tRCH | CLKOUT High Time | - | T/2 | - | ns | |
| tRCL | CLKOUT Low Time | - | T/2 | - | ns | |
| tRS | TTL Data Setup to CLKOUT | $4/7t_{RCP}-1$ | - | - | ns | |
| tRH | TTL Data Hold from CLKOUT | $3/7t_{RCP}-1$ | - | - | ns | |
| tTLH | TTL Low to High Transition Time | - | 1.0 | 3.0 | ns | |
| tTHL | TTL High to Low Transition Time | - | 1.0 | 3.0 | ns | |
| tSK | Receiver Skew Margin | CLKOUT=50MHz | -1000 | 0 | 1000 | ps |
| | | CLKOUT=75MHz | -550 | 0 | 550 | ps |
| | | CLKOUT=90MHz | -400 | 0 | 400 | ps |
| | | CLKOUT=112MHz | -250 | 0 | 250 | ps |
| tRIP1 | Input Data Position0 | -t _{SK} | 0 | +t _{SK} | ns | |
| tRIP0 | Input Data Position1 | T/7-t _{SK} | T/7 | T/7+t _{SK} | ns | |
| tRIP6 | Input Data Position2 | 2T/7-t _{SK} | 2T/7 | 2T/7+t _{SK} | ns | |
| tRIP5 | Input Data Position3 | 3T/7-t _{SK} | 3T/7 | 3T/7+t _{SK} | ns | |
| tRIP4 | Input Data Position4 | 4T/7-t _{SK} | 4T/7 | 4T/7+t _{SK} | ns | |
| tRIP3 | Input Data Position5 | 5T/7-t _{SK} | 5T/7 | 5T/7+t _{SK} | ns | |
| tRIP2 | Input Data Position6 | 6T/7-t _{SK} | 6T/7 | 6T/7+t _{SK} | ns | |
| tRPLL | Phase Lock Loop Set | - | - | 10.0 | ms | |
| tRCD | RCLK +/- to CLKOUT Delay | CLKOUT=75MHz 46.5 | - | 52.5 | ns | |
| tRCIP | CLKIN Period | 8.92 | - | 125.0 | ns | |

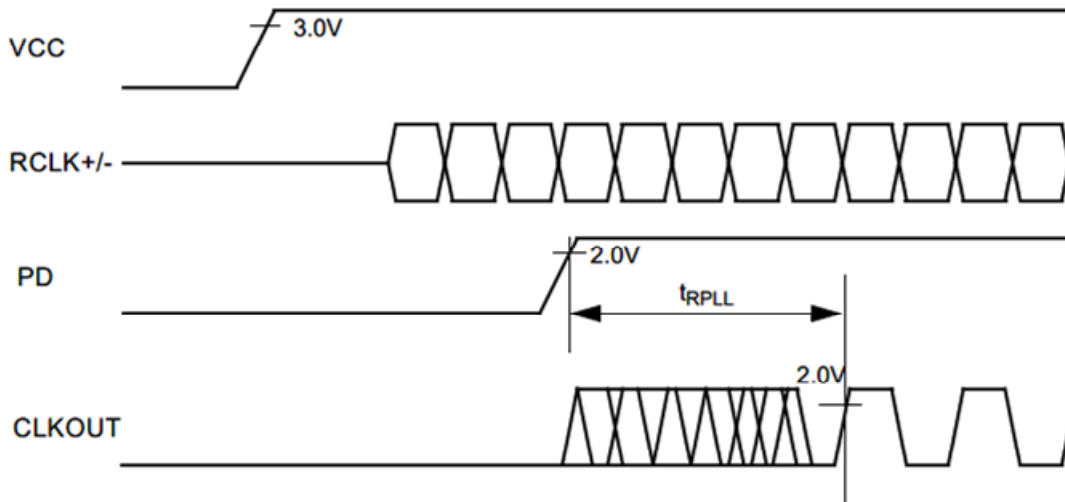
Switching Characteristics

TTL Outputs



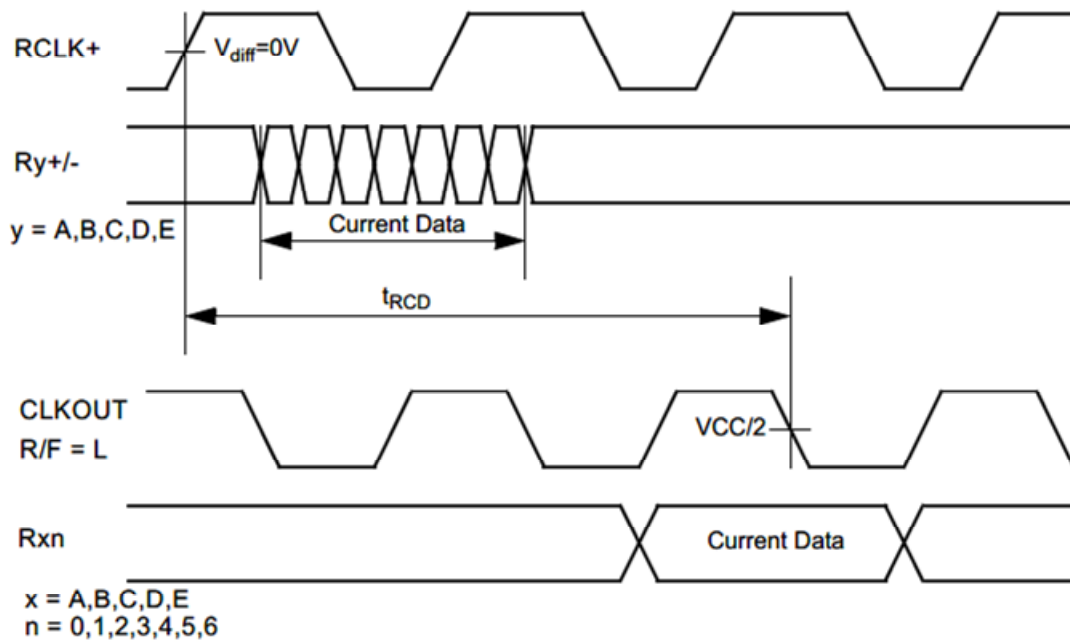
AC Timing Diagram

Phase Lock Loop Set Time

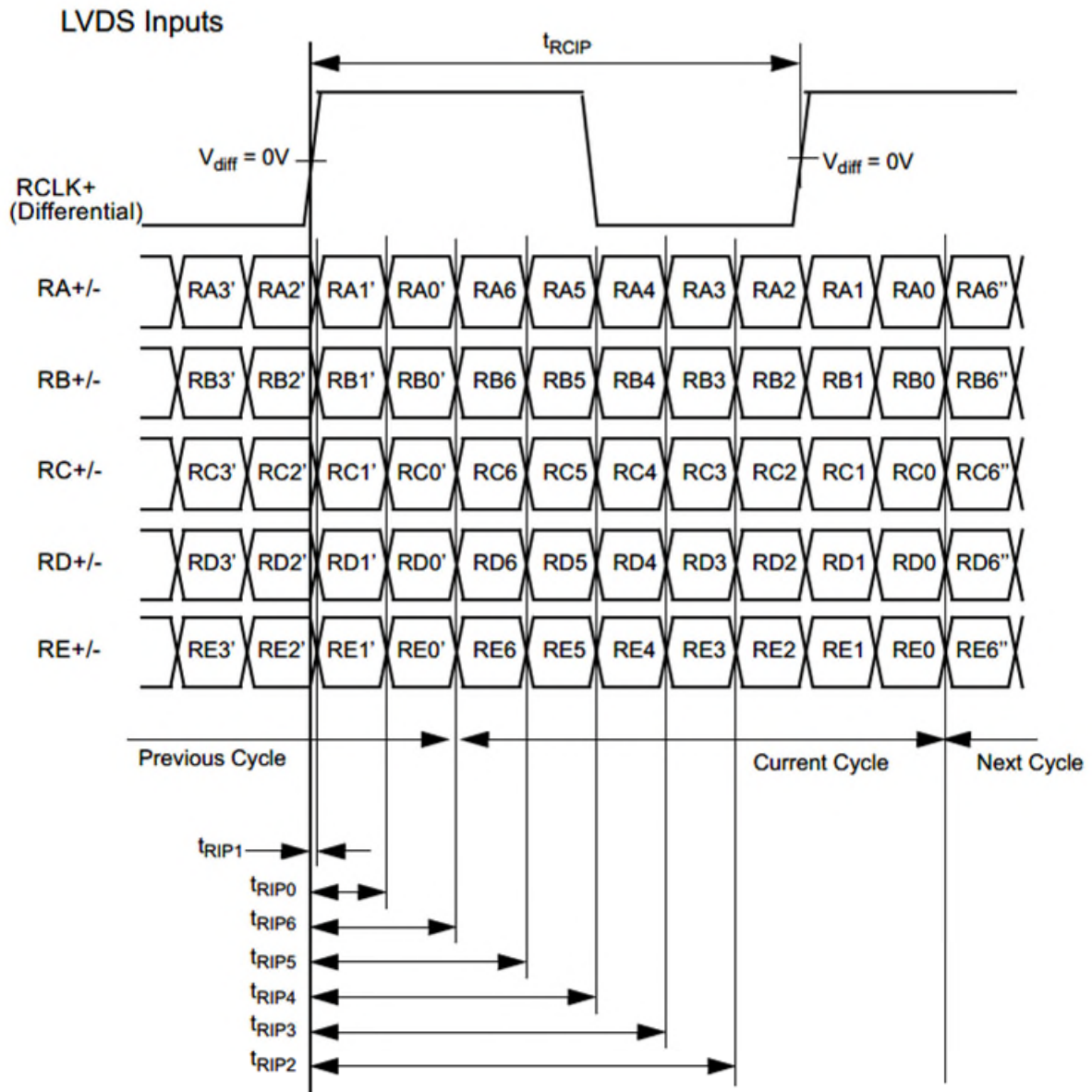


RCLK +/- to CLKOUT Delay

Note:
1) $V_{diff} = (RCLK+) - (RCLK-)$



AC Timing Diagram



Note

1)Power On Sequence

Power on LVDS-Tx after THC63LVD104C.

2)Cable Connection and Disconnection

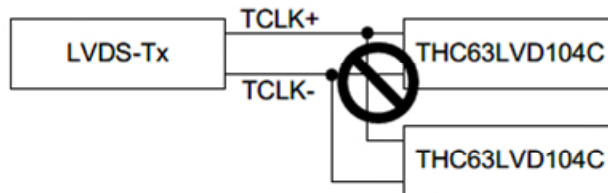
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which LVDS-Tx and THC63LVD104C on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

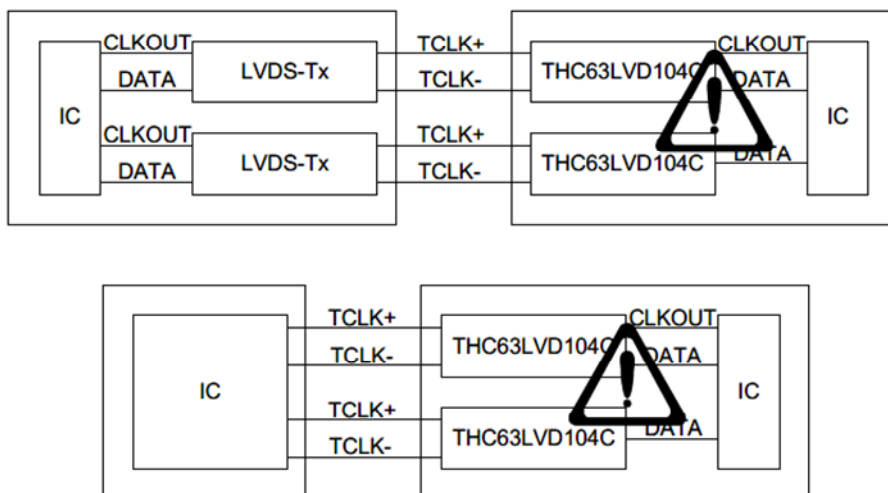
4)Multi Drop Connection

Multi drop connection is not recommended.

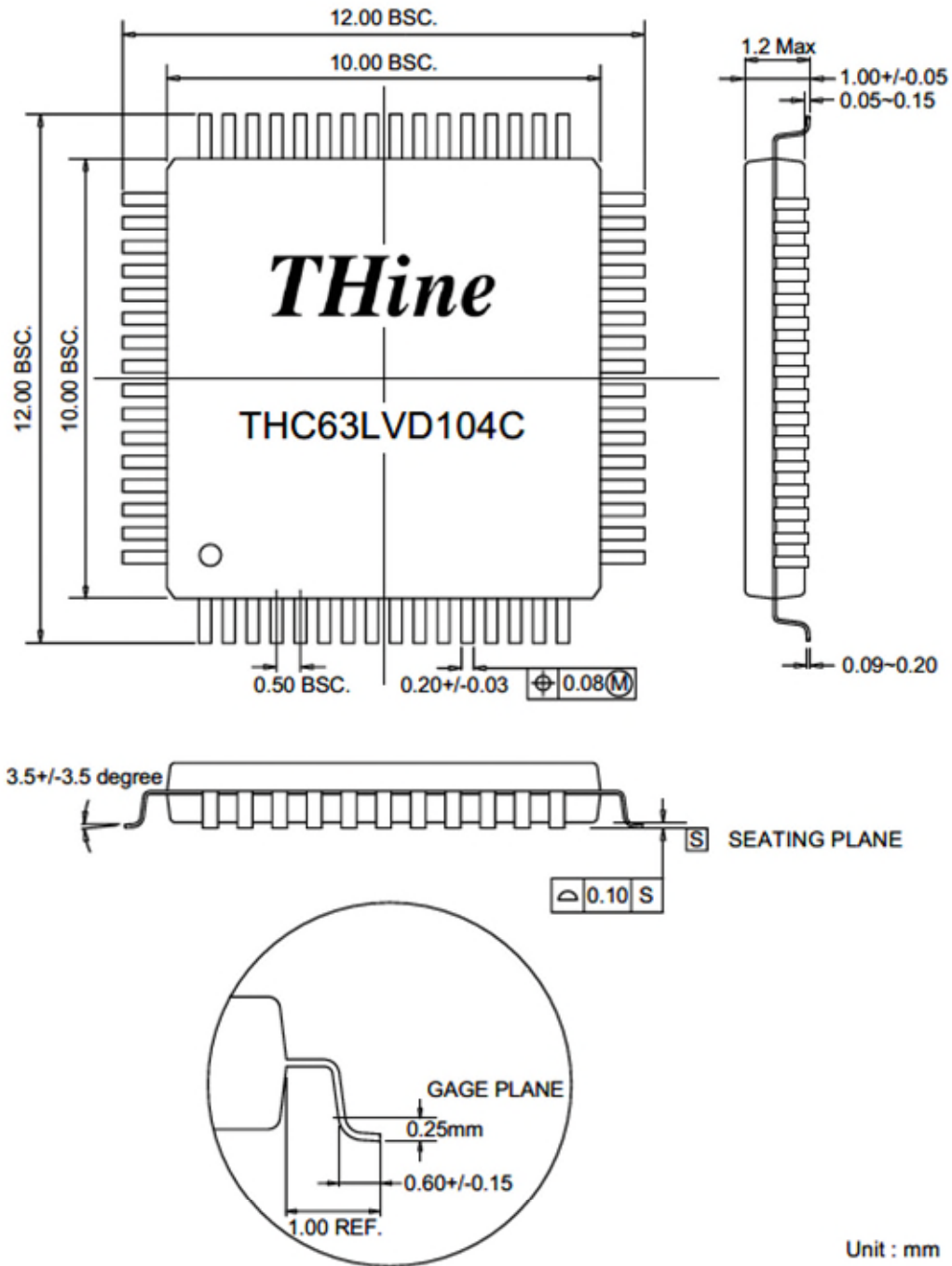


5)Asynchronous use

Asynchronous use such as following systems are not recommended.



Package



Unit : mm

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