MT9J003I12STMUH-GEVB

MT9J003 Evaluation Board User's Manual

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to clock, I/Os and other miscellaneous signals.

Features

- Clock Input
 - Default 10 MHz crystal oscillator
 - Optional Demo 2X controlled MClk
- Two Wire Serial Interface
 - Selectable base address
- Parallel Interface
- ROHS Compliant



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EVAL BOARD USER'S MANUAL



Figure 1. MT9J003 Evaluation Board

Block Diagram

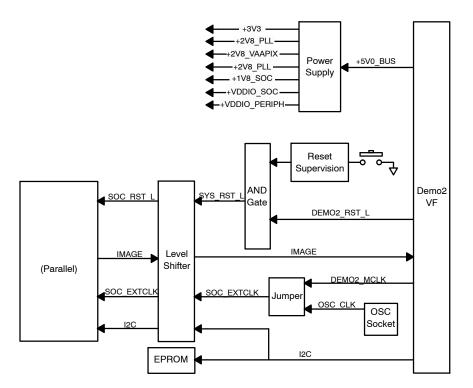


Figure 2. Block Diagram of MT9F002l12STMUH-GEVB

MT9J003l12STMUH-GEVB

Top View

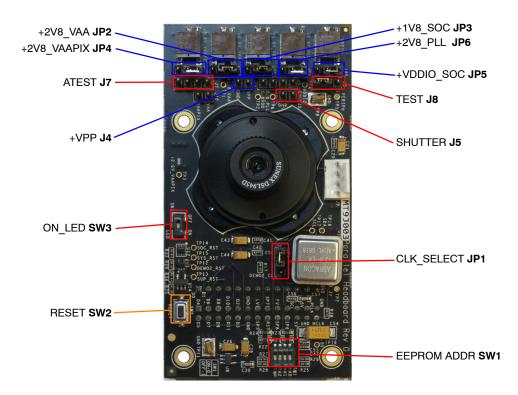


Figure 3. Top View of Evaluation Board - Default Jumpers

Bottom View

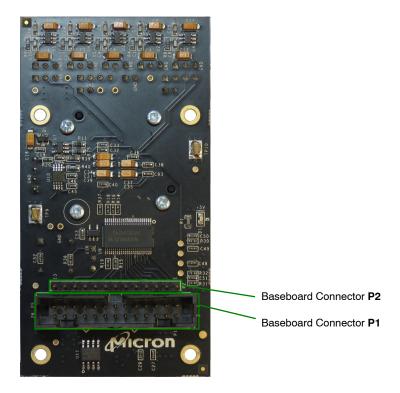


Figure 4. Bottom View of the Evaluation Board - Connector

MT9J003l12STMUH-GEVB

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

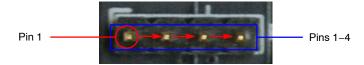


Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

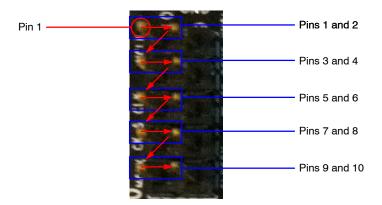


Figure 6. Pin Locations and Assignments of Grouped Jumpers.

Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

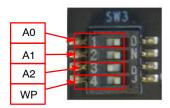


Figure 7. EEPROM Switches in their Default Positions. The First Switch (A0) of SW1 is OFF, the Second Switch (A1) is OFF, the Third Switch (A2) is ON, and the Fourth Switch (WP) is OFF

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
J4	+VPP	Open (Default)	For connection to external +VPP power supply (for OTPM)
J5	SHUTTER	Open (Default)	For connection to external shutter
J7	ATEST	Open (Default)	For Debug/Testing
J8	TEST	2-3 (Default)	Normal Operation
		1–2	Test Mode
JP2	+2V8_VAA	1-2 (Default)	Connects to on-board +2V8_VAA power supply
		2–3	External power supply connection
JP3	+1V8_SOC	1-2 (Default)	Connects to on-board +1V8_SOC power supply
		2–3	External power supply connection

MT9J003l12STMUH-GEVB

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
JP4	+2V8_VAAPIX	1-2 (Default)	Connects to on-board +2V8_VAAPIX power supply
		2–3	External power supply connection
JP5	+VDDIO_SOC	1-2 (Default)	Connects to on-board +VDDIO_SOC power supply
		2–3	External power supply connection
JP6	+2V8_PLL	1-2 (Default)	Connects to on-board +2V8_PLL power supply
		2–3	External power supply connection
SW1	EEPROM ADDR	A0 on, A1 on, A2 off, WP on (Default)	EEPROM Address set to 0xA8
		A0 off, A1 off, A2 off, WP on	EEPROM Address set to 0xAC
		A0 on, A1 off, A2 on, WP on	EEPROM Address set to 0xA4
		A0 on, A1 on, A2 on, WP on	EEPROM Address set to 0xA0
SW2	RESET	N/A	When pushed, 200 ms reset signal will be sent to MT9J003
SW3	ON_LED	Off (Default)	Turn off +5V bus LED indicator
		On	Turn on +5V bus LED indicator

Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor Demo 2X baseboard has a similar 26-pin connector and 13-pin connector which mate with P1 and P2 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

Shorted Jumpers for power measurement

Different supplies to the evaluation board are provided by trace shorted jumper, for any voltage and power measurements. To conduct current for current measurement on a given power rail, cut the trace between the two pins of their respective JP, and insert an ammeter prior to powering up the system. The figure below shows where the trace to cut is located.

Table 2. SHORTED JUMPERS FOR POWER MEASUREMENTS

Jumper	Voltage (V)
JP2 (+2V8_VAA)	2.8
JP3 (+1V8_SOC)	1.8
JP4 (+2V8_VAAPIX)	2.8
JP5 (+VDDIO_SOC)	2.8
JP6 (+2V8_PLL)	2.8

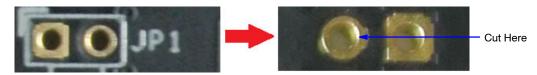


Figure 8. Top and Bottom View of Shorted Jumper.

The Bottom View Shows the Trace Location to Cut for Current Measurement

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