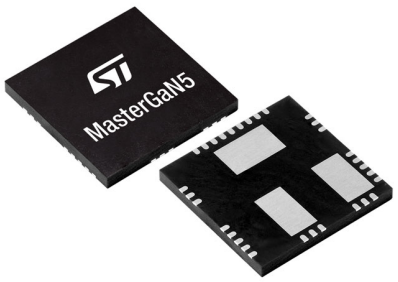
MASTERGAN5

Datasheet

High power density 600 V half-bridge driver with two enhancement mode GaNHEMT



QFN 9x9x1 mm

Features

- 600 V system-in-package integrating half-bridge gate driver and high-voltage GaN power transistors:
  - QFN 9 x 9 x 1 mm package
  - $R_{DS(ON)}$ = 450 mΩ
  - $I_{DS(MAX)}$ = 4 A
- Reverse current capability
- Zero reverse recovery loss
- UVLO protection on low-side and high-side
- Internal bootstrap diode
- Interlocking function
- Dedicated pin for shut down functionality
- Accurate internal timing match
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Over temperature protection
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design.

Applications

Switch-mode power supplies

Chargers and adapters

High-voltage PFC, DC-DC and DC-AC Converters

Product status link

MASTERGAN5

Product label

SUSTAINABLE TECHNOLOGY

Description

The MASTERGAN5 is an advanced power system-in-package integrating a gate driver and two enhancement mode GaN power transistors in half bridge configuration. The integrated power GaNs have 650 V drain-source blocking voltage and $R_{DS(ON)}$ of 450 mΩ, while the high side of the embedded gate driver can be easily supplied by the integrated bootstrap diode.

The MASTERGAN5 features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions.

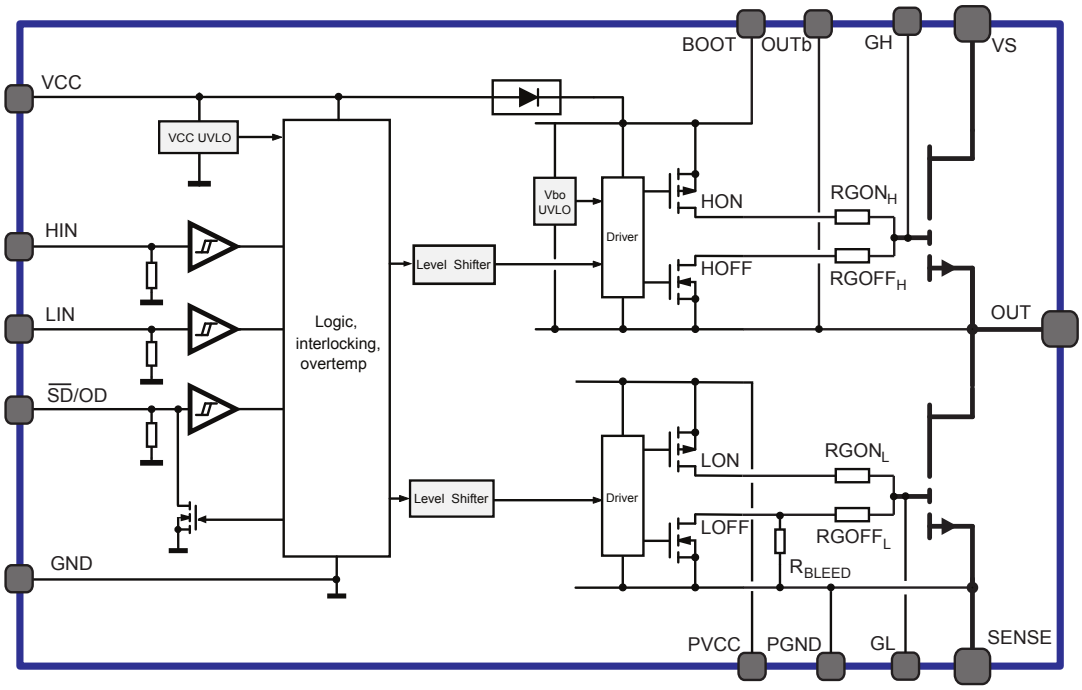
The extended range of the input pins allows easy interfacing with microcontrollers, DSP units or Hall effect sensors.

The MASTERGAN5 operates in the industrial temperature range, -40°C to 125°C.

The device is available in a compact 9x9 mm QFN package.

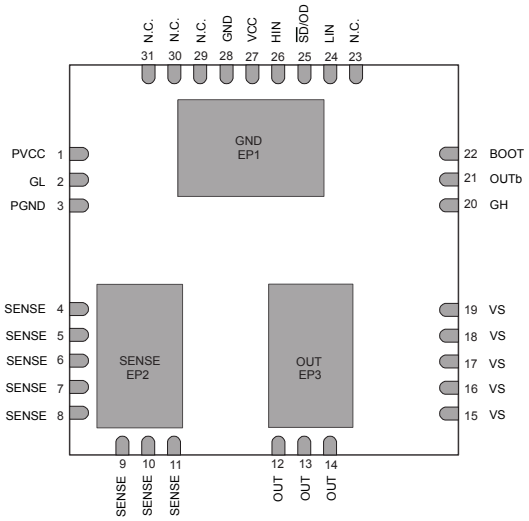
1 Block diagram

Figure 1. **Block diagram**



2 Pin descriptions and connection diagram

Figure 2. **Pin connections (top view)**



2.1 Pin list

Table 1. **Pin descriptions**

Pin Number	Pin Name	Type	Function
15, 16, 17, 18, 19	VS	Power Supply	High voltage supply (high-side GaN Drain)
12, 13, 14, EP3	OUT	Power Output	Half-bridge output
4, 5, 6, 7, 8, 9, 10, 11, EP2	SENSE	Power Supply	Half-bridge sense (low-side GaN Source)
22	BOOT	Power Supply	Gate driver high-side supply voltage
21	OUTb	Power Supply	Gate driver high-side supply voltage, used only for Bootstrap capacitor connection. Internally connected to OUT.
27	VCC	Power Supply	Logic supply voltage
1	PVCC	Power Supply	Gate driver low-side supply voltage
28, EP1	GND	Power Supply	Gate driver ground
3	PGND	Power Supply	Gate driver low-side buffer ground. Internally connected to SENSE.
26	HIN	Logic Input	High-Side driver logic input
24	LIN	Logic Input	Low-Side driver logic input
25	SD/OD	Logic Input-output	Driver Shut-Down input and Fault Open-Drain
2	GL	Output	Low-Side GaN gate.
20	GH	Output	High-Side GaN gate.
23, 29, 30, 31	N.C.	Not Connected	Leave floating

3 Electrical Data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Each voltage referred to GND unless otherwise specified

Symbol	Parameter	Test Condition	Value	Unit
V_{DS}	GaN Drain-to-Source Voltage	T_J = 25 °C	620	V
VCC	Logic supply voltage	-	-0.3 to 11	V
PVCC-PGND	Low-side driver supply voltage(1)	-	-0.3 to 7	V
VCC-PGND	Logic supply vs Low-side driver ground	-	-0.3 to 18.3	V
PVCC	Low-side driver supply vs logic ground	-	-0.3 to 18.3	V
PGND	Low-side driver ground vs logic ground	-	-7.3 to 11.3	V
V_{BO}	BOOT to OUTb voltage(2)	-	-0.3 to 7	V
BOOT	Bootstrap voltage	-	-0.3 to 620	V
CGL, CGH	Maximum external capacitance between GL and PGND and between GH and OUTb	F_{SW} = 500 kHz(3)	3.9	nF
RGL, RGH	Minimum external pull down resistance between GL and PGND and GH and OUTb	-	6.8	kΩ
I_D	Drain current	DC @ T_{CB} = 25 °C(4) (5)	4	A
		DC @ T_{CB} = 100 °C(4) (5)	2.6	A
		Peak @ T_{CB} = 25 °C(4) (5) (6)	7	A
SR_{out}	Half-bridge outputs slew rate (10% - 90%)	-	100	V/ns
V_i	Logic inputs voltage range	-	-0.3 to 21	V
T_J	Junction temperature	-	-40 to 150	°C
T_s	Storage temperature	-	-40 to 150	°C

1. *PGND internally connected to SENSE.*
2. *OUTb internally connected to OUT*
3. *CGx < 0.08/(Pvcc^2*Fsw)-(330*10-12)*
4. *T_{CB} is temperature of case exposed pad*
5. *Range estimated by characterization, not tested in production*
6. *Value specified by design factor, pulse duration limited to 50 µs and junction temperature*

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Each voltage referred to GND unless otherwise specified

Symbol	Parameter	Note	Min	Max	Unit
VS	High voltage bus	-	0	520	V
VCC	Supply voltage	-	4.75	9.5	V
PVCC-PGND	PVCC to PGND Low side supply(1)	-	4.75	6.5	V

Symbol	Parameter	Note	Min	Max	Unit
PVCC-PGND	PVCC to PGND Low side supply(1)	Best performance	5	6.5	V
PVCC	Low-side driver supply	-	3	8.5	V
VCC-PVCC	VCC to PVCC pin voltage	-	-3	3	V
PGND	Low-side driver ground(1)	-	-2	2	V
DT	Suggested minimum dead time	-	5	-	ns
T_{IN_MIN}	Minimum duration of input pulse to obtain undistorted output pulse(2)	-	120	-	ns
V_{BO}	BOOT to OUTb pin voltage(3)	-	4.4	6.5	V
		Best performance	5	6.5	V
BOOT	BOOT to GND voltage	-	0(4)	530	V
V_i	Logic inputs voltage range	-	0	20	V
T_J	Junction temperature	-	-40	125	°C

1. *PGND internally connected to SENSE*
2. *See Logic inputs for more detail*
3. *OUTb internally connected to OUT*
4. *5 V is recommended during High Side turn-on*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-CB)\_HS}$	Thermal resistance of each transistor's junction to relevant exposed pad, typical	4.7	°C/W
$R_{th(J-A)}$	Thermal resistance junction-to-ambient(1)	18.8	°C/W

The junction to ambient thermal resistance is obtained simulating the device mounted on a 2s2p (4 layer) FR4 board as per JESD51-5,7 with 6 thermal vias for each exposed pad. Power dissipation is uniformly distributed over the two GaN transistors.

4 Electrical characteristics

4.1 Driver

Table 5. Driver electrical characteristics

VCC = PVCC = 6 V, SENSE = GND, TJ = 25 °C, unless otherwise specified
Each voltage referred to GND unless otherwise specified

Symbol	-	Parameter	Test condition	Min	Typ	Max	Unit
Logic section supply							
VCC_{thON}	VCC vs. GND	VCC UV turn ON threshold(1)	-	4.2	4.5	4.75	V
VCC_{thOFF}		VCC UV turn OFF threshold(1)	-	3.9	4.2	4.5	V
VCC_{hys}		VCC UV hysteresis(1)	-	0.2	0.3	0.45	V
I_{QVCCU}		VCC undervoltage quiescent supply current	VCC = PVCC = 3.8 V	-	320	410	µA
I_{QVCC}		VCC quiescent supply current	SD/OD = LIN = 5 V; HIN = 0 V; BOOT = 7 V	-	680	900	µA
I_{SVCC}		VCC switching supply current	SD/OD = 5 V; V_{BO} = 6.5 V; VS = 0 V; F_{SW} = 500 kHz	-	0.8	-	mA
Low-side driver section supply							
I_{QPVCC}	PVCC vs. PGND	PVCC quiescent supply current	SD/OD = LIN = 5 V	-	150	-	µA
I_{SPVCC}		PVCC switching supply current	VS = 0 V F_{SW} = 500 kHz	-	1.0	-	mA
R_{BLEED}	GL vs. PGND	Low side gate bleeder	PVCC = PGND	75	100	125	kΩ
RON_L	-	Low side turn on resistance(2)	I(GL) = 1 mA (source)	-	77	-	Ω
$ROFF_L$	-	Low side turn off resistance(2)	I(GL) = 1 mA (sink)	-	2	-	Ω
High-side floating section supply							
V_{BOthON}	BOOT vs. OUTb	V_{BO} UV turn ON threshold(3)	-	3.6	4.0	4.4	V
$V_{BOthOFF}$		V_{BO} UV turn OFF threshold (3)	-	3.4	3.7	4.0	V
V_{BOhys}		V_{BO} UV hysteresis(3)	-	0.1	0.3	0.5	V
I_{QBOU}		V_{BO} undervoltage quiescent supply current(3)	V_{BO} = 3.4 V	-	140	200	µA

Symbol	-	Parameter	Test condition	Min	Typ	Max	Unit
I_{QBO}	BOOT vs. OUTb	V_{BO} quiescent supply current(3)	V_{BO} = 6 V; LIN = GND; SD/OD = HIN = 5 V;	-	180	-	µA
I_{SBO}	BOOT	BOOT switching supply current	V_{BO} =6 V; SD/OD = 5 V; VS = 0 V; F_{SW} = 500 kHz	-	1.1	-	mA
I_{LK}	BOOT vs. SGND	High voltage leakage current	BOOT = OUT = 600 V	-	-	11	µA
R_{DBoot}	VCC vs. BOOT	Bootstrap diode on-resistance(4)	SD/OD = LIN = 5 V; HIN = GND = PGND VCC – BOOT = 0.5 V	-	140	175	Ω
RON_H	-	High side turn on resistance(2)	I(GH) = 1 mA (source)	-	77	-	Ω
$ROFF_H$	-	High side turn off resistance(2)	I(GH) = 1 mA (sink)	-	2	-	Ω
Logic inputs							
V_{il}	LIN, HIN, SD/OD	Low level logic threshold voltage	T_J = 25 °C	1.1	1.31	1.45	V
			Full Temperature range(5)	0.8	-	-	
V_{ih}		High level logic threshold voltage	T_J = 25 °C	2	2.17	2.5	V
			Full Temperature range(5)	-	-	2.7	
V_{ihys}		Logic input threshold hysteresis		0.7	0.96	1.2	V
I_{INh}	LIN, HIN	Logic ‘1’ input bias current	LIN, HIN = 5 V	23	33	55	µA
I_{INl}		Logic ‘0’ input bias current	LIN, HIN = GND	-	-	1	µA
R_{PD_IN}		Input pull-down resistor	LIN, HIN = 5 V	90	150	220	kΩ
I_{SDh}	SD/OD	Logic “1” input bias current	SD/OD = 5 V	11	15	20	µA
I_{SDl}	SD/OD	Logic “0” input bias current	SD/OD = 0 V	-	-	1	µA
R_{PD_SD}	SD/OD	Pull-down resistor	SD/OD = 5 V OpenDrain OFF	250	330	450	kΩ
V_{TSD}	SD/OD	Thermal shutdown unlatch threshold	T_J = 25 °C(6)	0.5	0.75	1	V
R_{ON_OD}	SD/OD	Open drain ON resistance	T_J = 25 °C; I_{OD} = 400 mV(6)	8	10	18	Ω
I_{OL_OD}	SD/OD	Open Drain low level sink current	T_J = 25 °C; V_{OD} = 400 mV(6)	22	40	50	mA
T_{d_GL}	LIN, GL	Prop. delay from LIN to GL	(6)	-	46	-	ns

Symbol	-	Parameter	Test condition	Min	Typ	Max	Unit
T_{d_GH}	HIN, GH	Prop. delay from HIN to GH	(6)	-	46	-	ns
Over temperature protection							
T_{TSD}	-	Shut down temperature	(5)	-	175	-	°C
T_{HYS}	-	Temperature hysteresis	(5)	-	20	-	°C

1. *VCC UVLO is referred to VCC - GND*
2. *Turn on and turn off total resistances include the values of the gate resistors and the driver Rdson*
3. *$V_{BO} = V_{BOOT} - V_{OUT}$*
4. *$R_{BD(on)}$ is tested in the following way*
   $R_{BD(on)} = [(VCC - V_{BOOTa}) - (VCC - V_{BOOTb})] / [I_a - I_b]$
   Where: I_a is BOOT pin current when $V_{BOOT} = V_{BOOTa}$; I_b is BOOT pin current when $V_{BOOT} = V_{BOOTb}$
5. *Range estimated by characterization, not tested in production*
6. *Tested at wafer level*

4.2 GaN power transistor

Table 6. GaN power transistor electrical characteristics

V_{GS} = 6 V; T_J = 25 °C, unless otherwise specified.

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
GaN on/off states							
$V_{(BR)DS}$	Drain-source blocking voltage	I_{DSS} < 6.6 µA(1) V_{GS} = 0 V		650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V V_{GS} = 0 V		-	0.3	-	µA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ I_D = 1.7 mA(1)		-	1.7	-	V
I_{GS}	Gate to source current	V_{DS} = 0 V(2)		-	20	-	µA
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 1.2 A	T_J = 25°C	-	450	600	mΩ
			T_J = 125°C (2)	-	1012	-	

1. *Tested at wafer level*
2. *Range estimated by characterization, not tested in production*

5 Device characterization values

The information in Table 7 and Table 8 represent typical values based on characterization and simulation results and are not tested in production.

Table 7. GaN power transistor characterization values (each transistor)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Q_G	Total gate charge	V_{GS} = 6 V, T_J = 25 °C V_{DS} = 0 to 400 V	-	0.8	-	nC
Q_{OSS}	Output charge	V_{GS} = 0 V, V_{DS} = 400 V	-	7	-	nC
E_{OSS}	Output Capacitance stored energy		-	0.9	-	µJ
C_{OSS}	Output capacitance		-	7	-	pF
$C_{O(ER)}$	Effective output capacitance energy related(1)	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	11	-	pF
$C_{O(TR)}$	Effective output capacitance time related(2)		-	17	-	pF
Q_{RR}	Reverse recovery charge	-	-	0	-	nC
I_{RRM}	Reverse recovery current	-	-	0	-	A

1. *$C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}*
2. *$C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}*

Table 8. Inductive load switching characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{(on)}$(1)	Turn-on time	V_S = 400 V, V_{GS} = 6 V, I_D = 1.2 A See Figure 3	-	70	-	ns
$t_{C(on)}$(2)	Crossover time (on)		-	25	-	ns
$t_{(off)}$(2)	Turn-off time		-	70	-	ns
$t_{C(off)}$(1)	Crossover time (off)		-	10	-	ns
t_{SD}	Shutdown to high/low-side propagation delay		-	70	-	ns
E_{on}	Turn-on switching losses		-	4.5	-	µJ
E_{off}	Turn-off switching losses		-	2.5	-	µJ

1. *$t_{(on)}$ and $t_{(off)}$ include the propagation delay time of the internal driver and GaN Turn on time*
2. *$t_{C\ (on)}$ and $t_{C\ (off)}$ are the switching times of GaN transistor itself under the internally given gate driving conditions*

Figure 3. **Switching time definition**

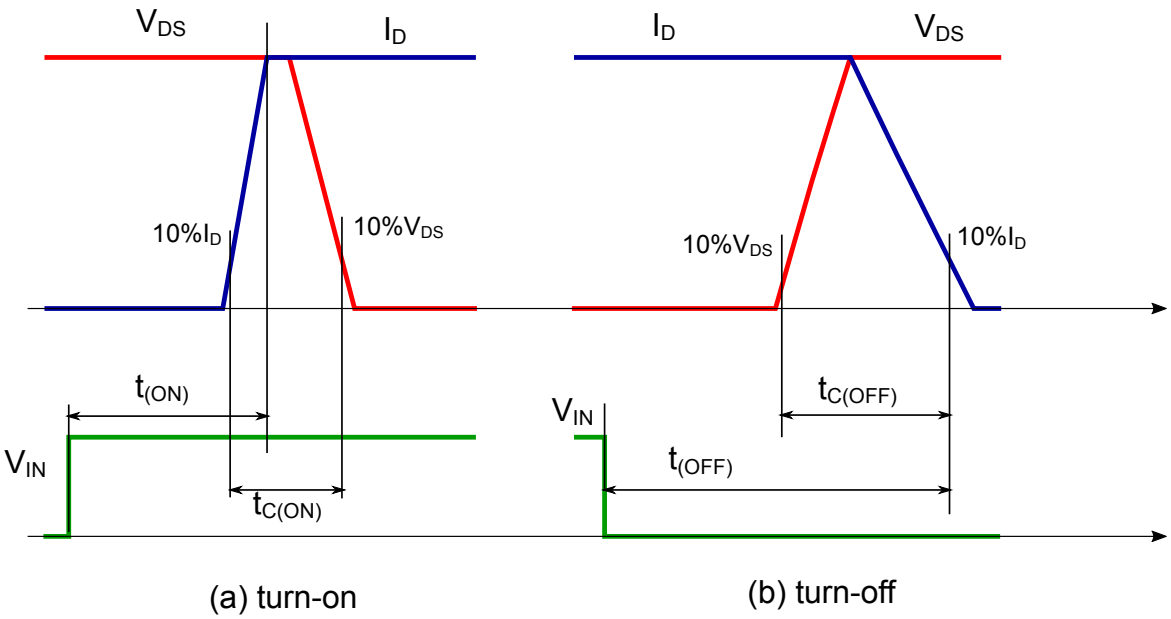


Figure 4. **Typ I_D vs V_{DS} at T_J=25°C**

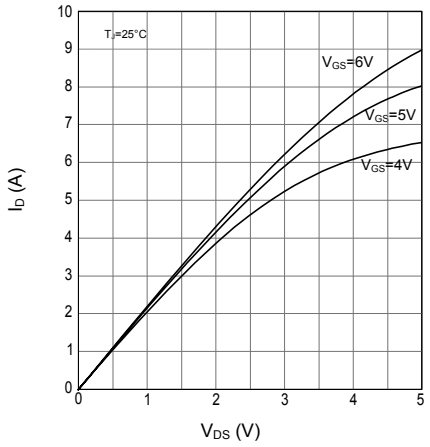


Figure 5. **Typ I_D vs V_{DS} at T_J=125°C**

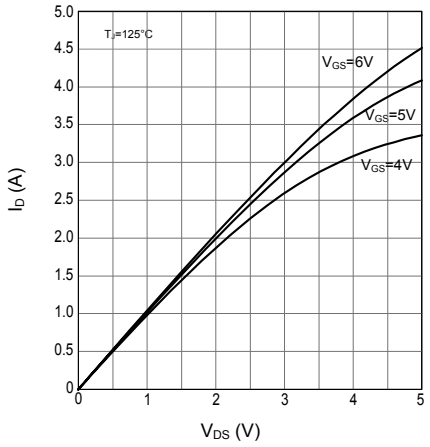


Figure 6. Typ $R_{DS(ON)}$ vs I_D at T_J=25°C

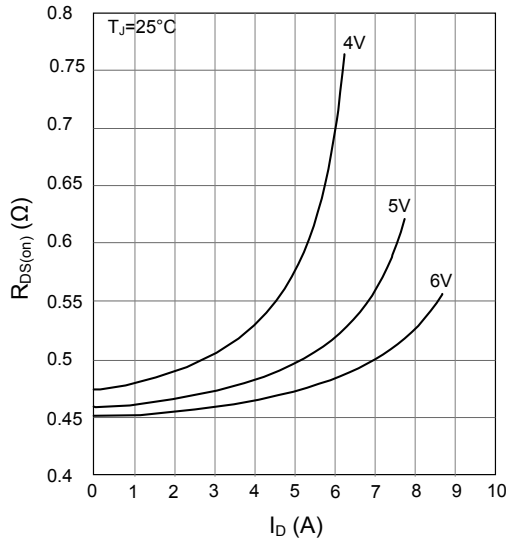


Figure 7. Typ $R_{DS(ON)}$ vs I_D at T_J=125°C

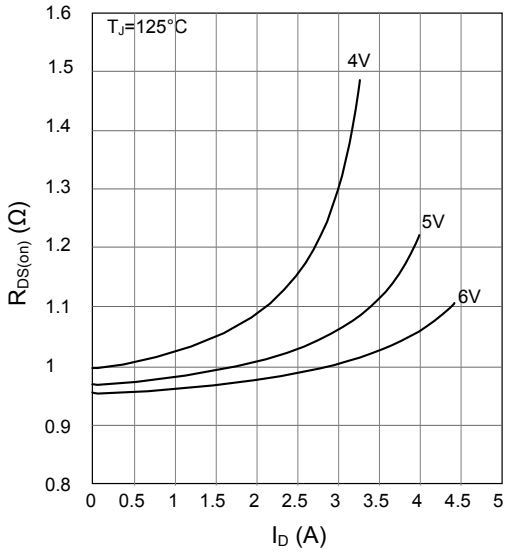


Figure 8. Typ $I_{D(ON)}$ vs V_{DS}

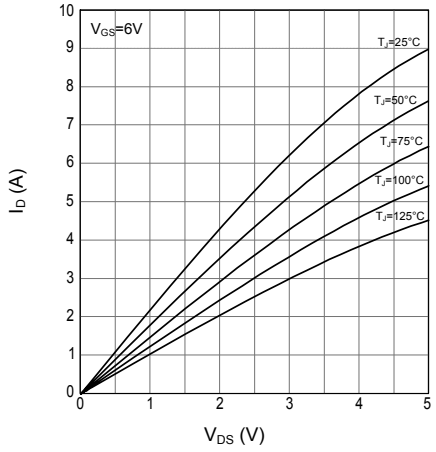


Figure 9. Typ $R_{DS(ON)}$_x vs T_J, normalized at 25°C

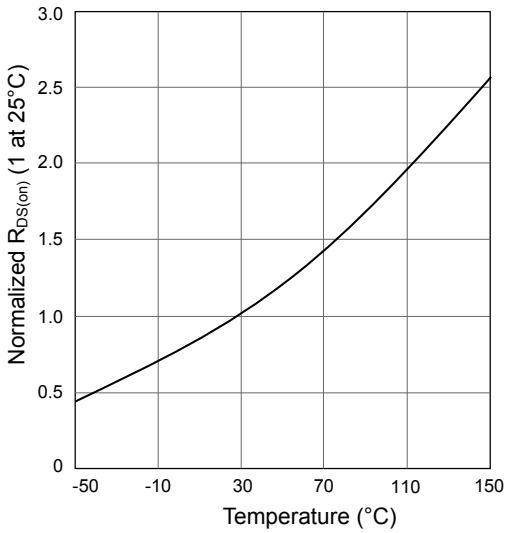


Figure 10. Typ I_{SD} vs V_{SD}, at T_J=25°C

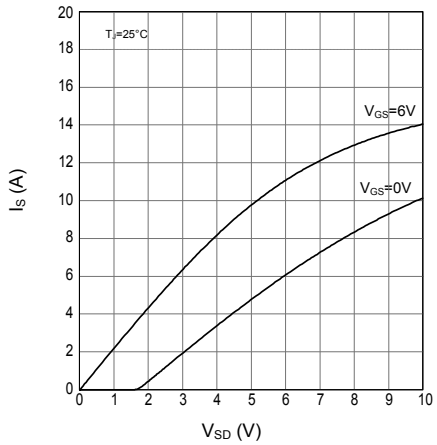


Figure 11. Typ I_{SD} vs V_{SD}, at T_J=125°C

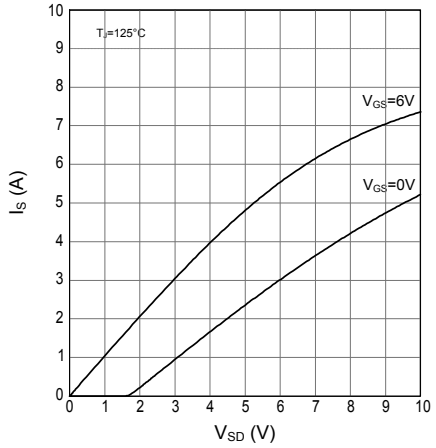


Figure 12. Safe Operating Area at T_J=25°C

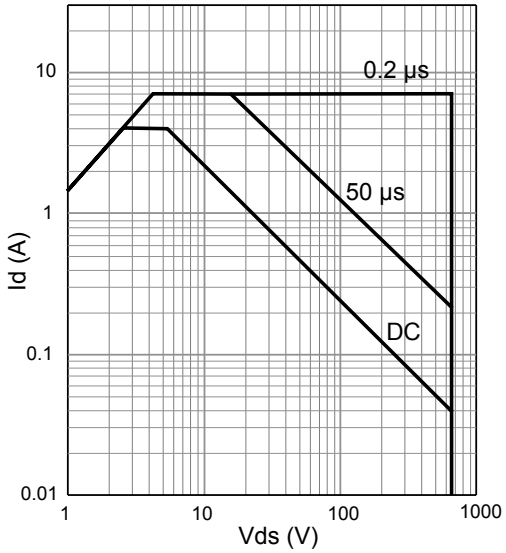


Figure 13. Typ Gate Charge at T_J=25°C

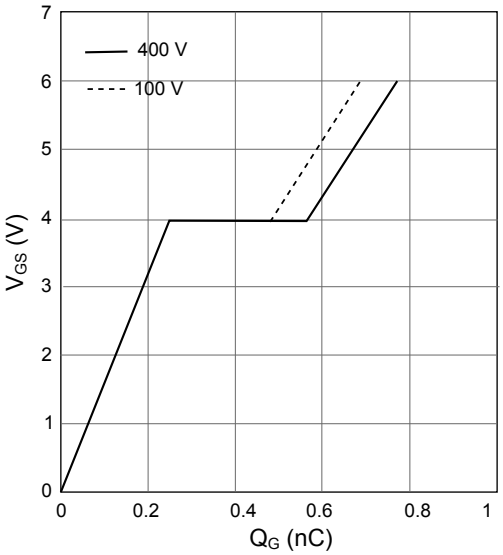


Figure 14. **Derating Curve**

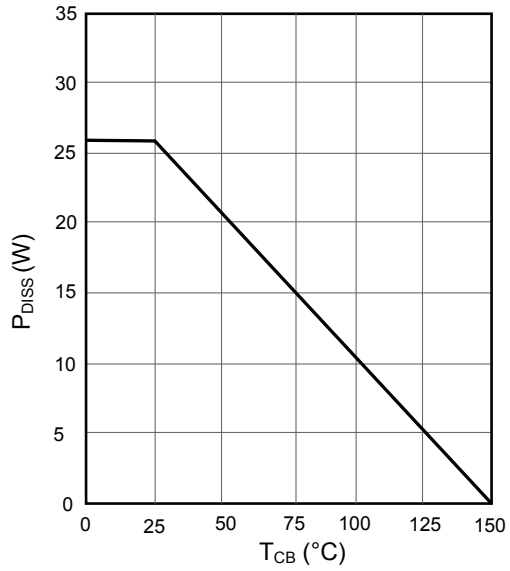
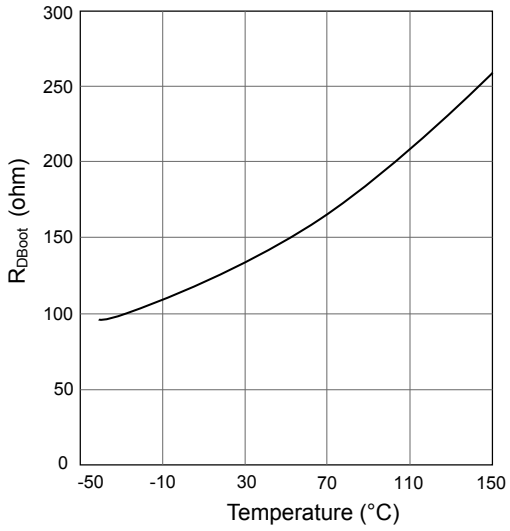


Figure 15. **Typ R_{Dboot} vs T_J**



5.1 Logic inputs

The MASTERGAN5 features a half-bridge gate driver with three logic inputs to control the internal high-side and low-side GaN transistors.

The devices are controlled through following logic inputs:

- $\overline{SD}$/OD: Shut-down input, active low;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high.

Table 9. **Inputs truth table (applicable when device is not in UVLO)**

Input pins			GaN transistors status	
$\overline{SD}$/OD	LIN	HIN	LS	HS
L	X(1)	X(1)	OFF	OFF
H	L	L	OFF	OFF
H	L	H	OFF	ON
H	H	L	ON	OFF
H	H(2)	H(2)	OFF	OFF

1. *X: Don't care*
2. *Interlocking*

The logic inputs have internal pull-down resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state conditions.

If logic inputs are left floating, the gate driver outputs are set to low level and the corresponding GaN transistors are turned off.

The minimum duration of the on time of the pulses applied to LIN is T_{IN_MIN} = 120ns; shorter pulses could be either extended to T_{IN_MIN} or blanked, if shorter than 30ns (typ). Minimum duration of the off time of the pulses applied to LIN is 60ns or could be blanked if they are shorter.

The minimum duration of the off time of the pulses applied to HIN is T_{IN_MIN} = 120ns; shorter pulses shall be either extended to T_{IN_MIN} or blanked, if shorter than 30ns (typ). Minimum duration of the on time of the pulses applied to HIN is 60ns or could be blanked if they are shorter.

Interlocking feature interrupts running T_{IN_MIN} to avoid unexpected cross-conduction.

Matched, short propagation delay between low side and high side are there.

5.2 Bootstrap structure

Bootstrap circuitry is typically used to supply the high-voltage section. MASTERGAN5 integrates this structure by means of a patented integrated high-voltage DMOS to reduce the external components.

The Boostrap integrated circuit is connected to VCC pin and is driven synchronously with the low-side driver.

The use of an external bootstrap diode in parallel to the integrated structure is possible, especially when the operating frequency is generally higher than 500 kHz.

5.3 VCC supply pins and UVLO function

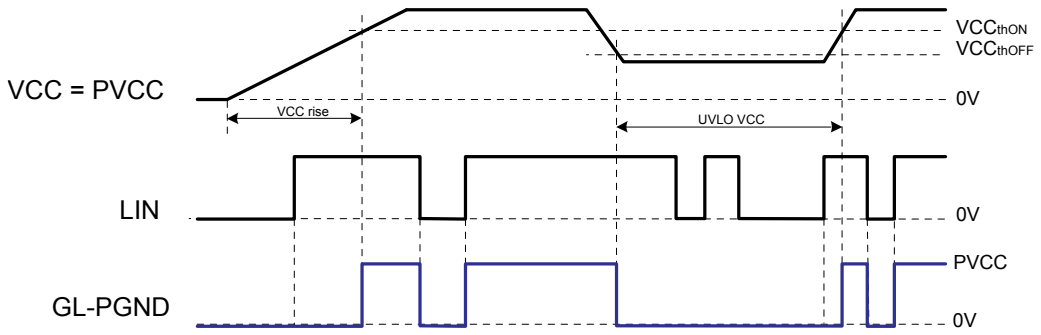
The VCC pin supplies current to the logic circuit, level-shifters in the low-side section and the integrated bootstrap diode.

The PVCC pin supplies low-side output buffer. During outputs commutations the average current used to provide gate charge to the high-side and low-side GaN transistors flow through this pin.

The PVCC pin can be connected either to the same supply voltage of the VCC pin or to a separated voltage source. In case the same voltage source is used, it is suggested to connect VCC and PVCC pins by means of a small decoupling resistance. The use of dedicated bypass ceramic capacitors located as close as possible to each supply pin is highly recommended.

The MASTERGAN5 VCC supply voltage is continuously monitored by under-voltage lockout (UVLO) circuitry that turns the high-side and low-side GaN transistors off when the supply voltage goes below the V_{CC_thOFF} threshold. The UVLO circuitry turns on the GaN, accordingly to LIN and HIN status, approximately 20µs (typ) after the supply voltage goes above the V_{CCthON} voltage. A V_{CChys} hysteresis is provided for noise rejection purposes.

Figure 16. VCC UVLO and Low Side

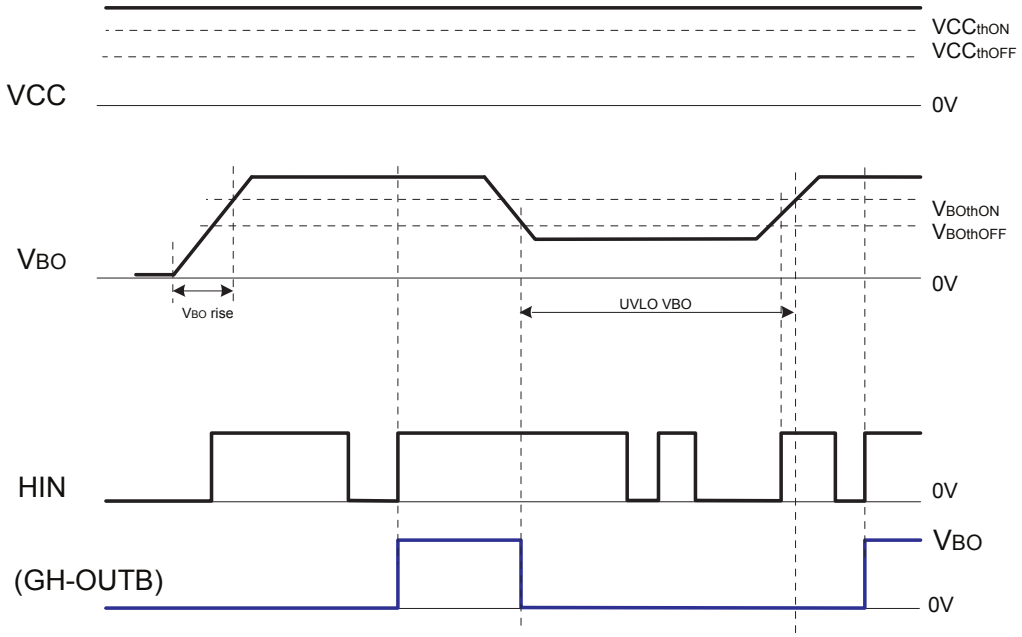


5.4 V_{BO} UVLO protection

Dedicated under-voltage protection is available on the bootstrap section between BOOT and OUTb supply pins. In order to avoid intermittent operation, a hysteresis set the turn-off threshold with respect to the turn-on threshold.

When the V_{BO} voltage falls below the $V_{BOthOFF}$ threshold, the high-side GaN transistor is switched off. Approximately 5µs (typ) after the V_{BO} voltage reaches the V_{BOthON} threshold, the device returns to normal operation and the output remains off until the next input pin transition that requests the high-side to turn on.

Figure 17. V_{BO} UVLO and High Side



5.5 Thermal shutdown

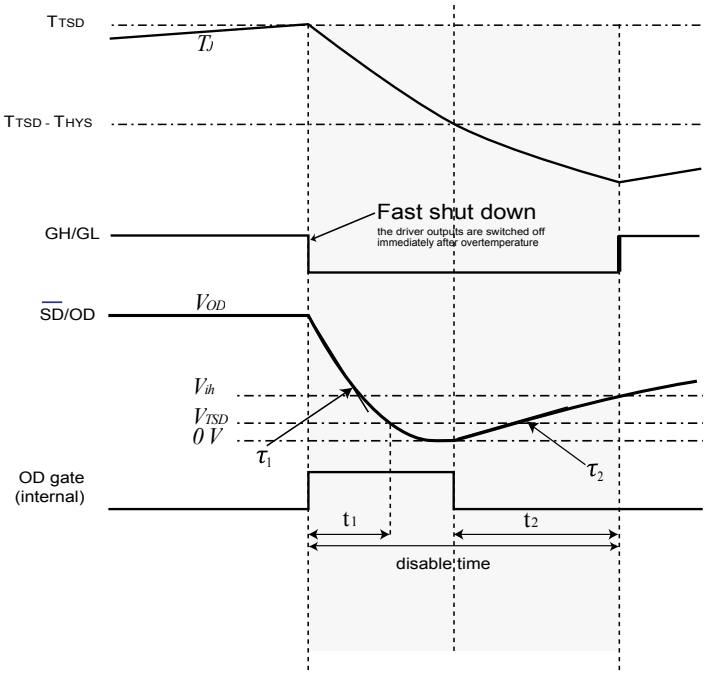
The integrated gate driver has a thermal shutdown protection.

When junction temperature reaches the T_{TSD} temperature threshold, the device turns off both GaN transistors leaving the half-bridge in 3-state and signaling the state forcing $\overline{SD}$/OD pin low. $\overline{SD}$/OD pin is released when junction temperature is below T_{TSD}-T_{HYS} and $\overline{SD}$/OD is below V_{TSD}.

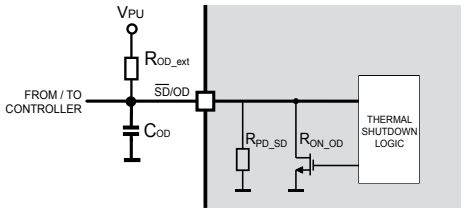
GaN are driven again according to inputs when $\overline{SD}$/OD rise above V_{ih}.

The thermal smart shutdown system gives the possibility to increase the time constant of the external RC network (that determines the disable time after the overtemperature event) up to very large values without delaying the protection.

Figure 18. **Thermal Shutdown timing waveform**



THERMAL SHUTDOWN CIRCUIT



6 Typical application diagrams

Figure 19. **Typical application diagram – Resonant LLC converter**

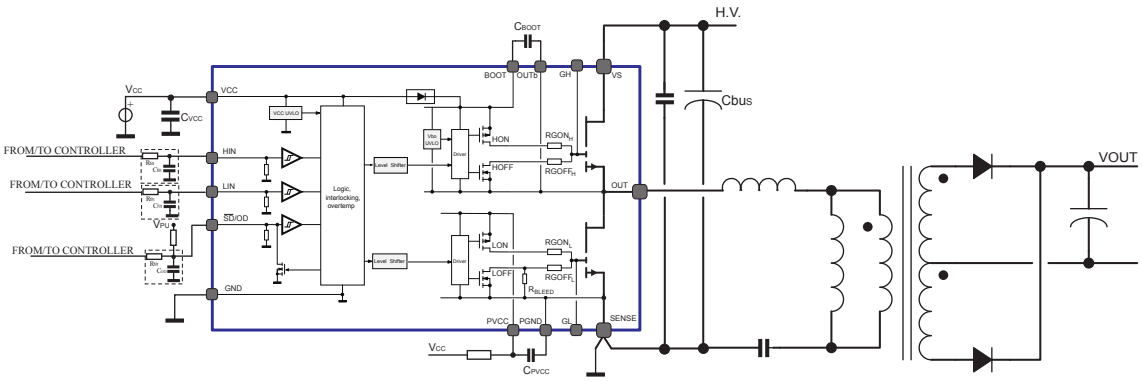
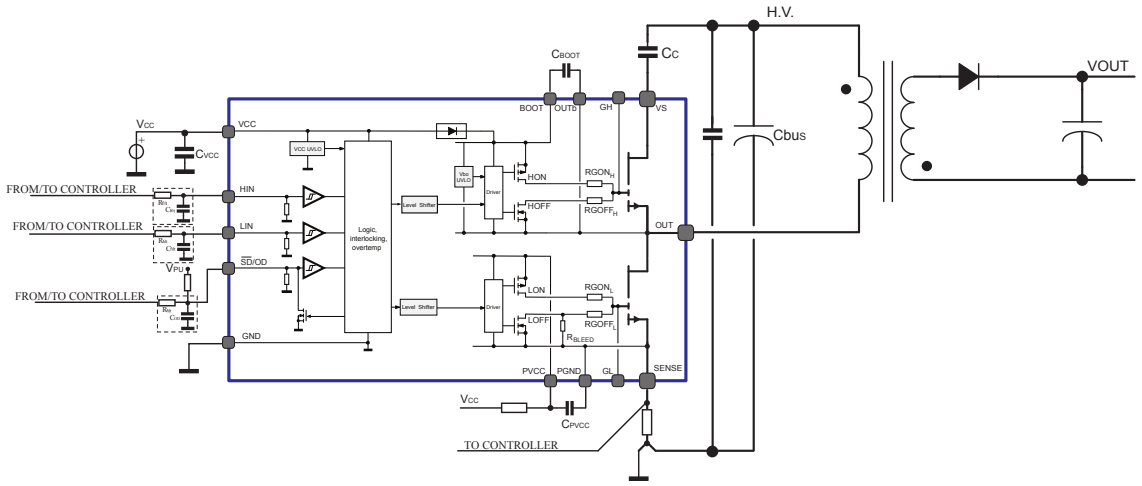


Figure 20. **Typical application diagram – Active clamp flyback**



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

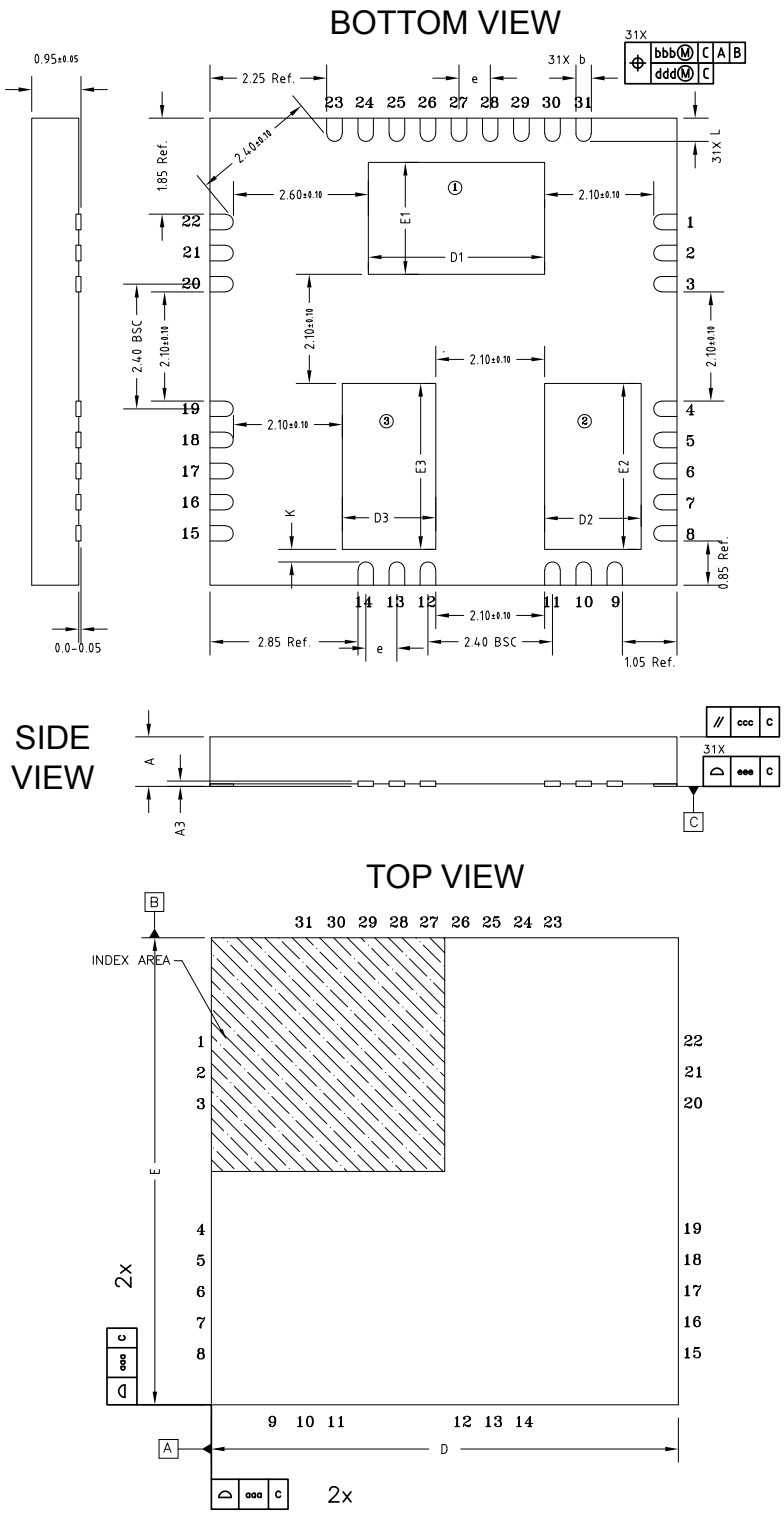
7.1 QFN 9 x 9 x 1 mm, 31 leads, pitch 0.6 mm package information

Table 10. QFN 9 x 9 x 1 mm package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A3	-	0.10	-
b	0.25	0.30	0.35
D	8.96	9.00	9.04
E	8.96	9.00	9.04
D1	3.30	3.40	3.50
E1	2.06	2.16	2.26
D2	1.76	1.86	1.96
E2	3.10	3.20	3.30
D3	1.70	1.80	1.90
E3	3.10	3.20	3.30
e	-	0.60	-
K	-	0.24	-
L	0.35	0.45	0.55
N	31		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
- *Dimensioning and tolerances conform to ASME Y14.5-2009*
- *All dimensions are in millimeters*
- *N total number of terminals*
- *Dimensions do not include mold protrusion, not to exceed 0.15 mm*
- *Package outline exclusive of metal burr dimensions*

Figure 21. **QFN 9 x 9 x 1 mm package dimensions**



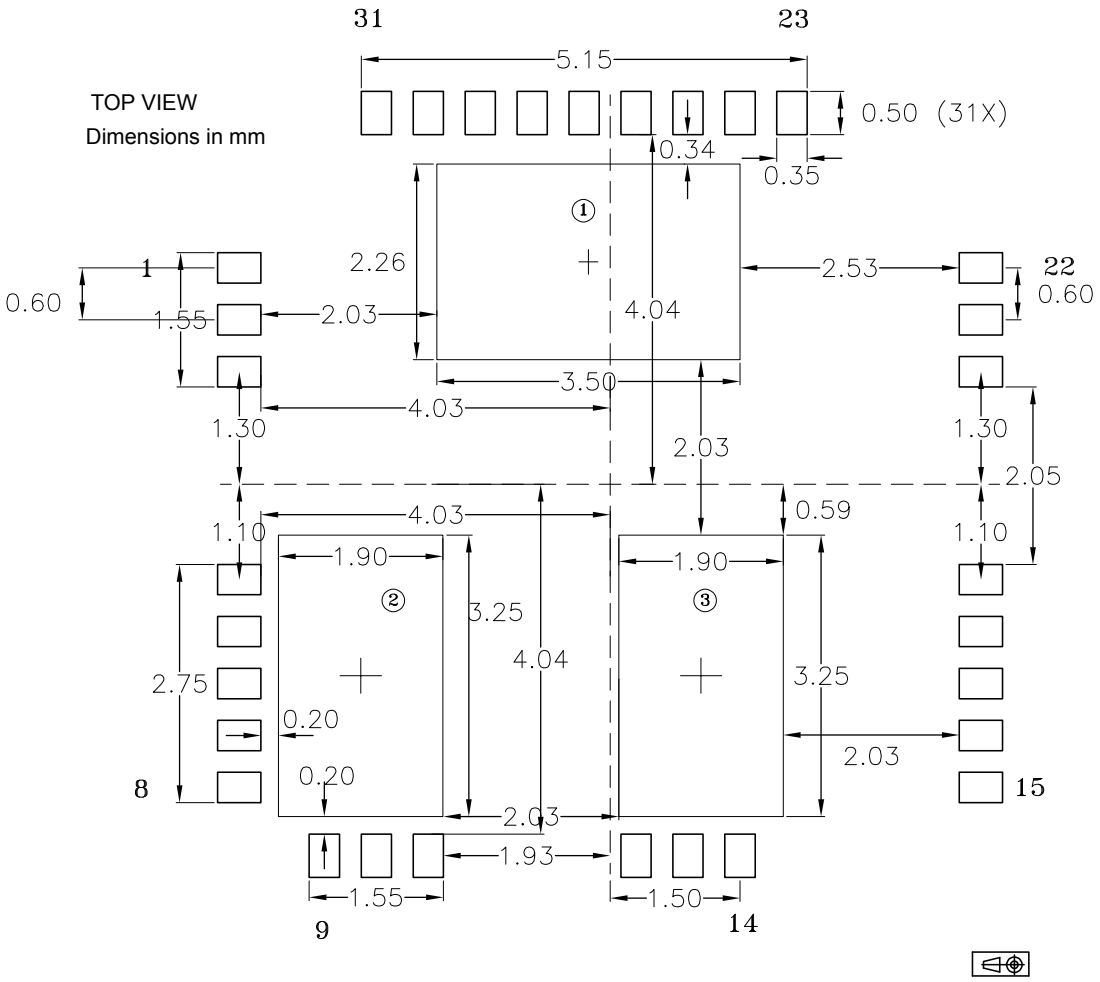
8 Suggested footprint

The MASTERGAN5 footprint for the PCB layout is usually defined based on several design factors as assembly plant technology capabilities and board component density. For easy device usage and evaluation, ST provides the following footprint design, which is suitable for the largest variety of PCBs.

The following footprint indicates the copper area which should be free from the solder mask,

while the copper area shall extend beyond the indicated areas especially for EP2 and EP3. To aid thermal dissipation, it is recommended to add thermal vias under these EPADs to transfer and dissipate device heat to the other PCB copper layers. A PCB layout example is available with the MASTERGAN5 evaluation board.

Figure 22. Suggested footprint (top view drawing)



9 Ordering information

Table 11. **Order codes**

Order code	Package	Package Marking	Packaging
MASTERGAN5	QFN 9 x 9 x 1 mm	MASTERGAN5	Tray
MASTERGAN5TR	QFN 9 x 9 x 1 mm	MASTERGAN5	Tape and Reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
26-Jul-2021	1	Initial release.

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