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FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

*16-bit Microcontroller*

**CMOS**

# F²MC-16LX MB90920 Series

## MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

## ■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

## ■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

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For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : $f_{CP}$, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 μs (at $f_{CP}$ = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at $f_{CP}$ = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)



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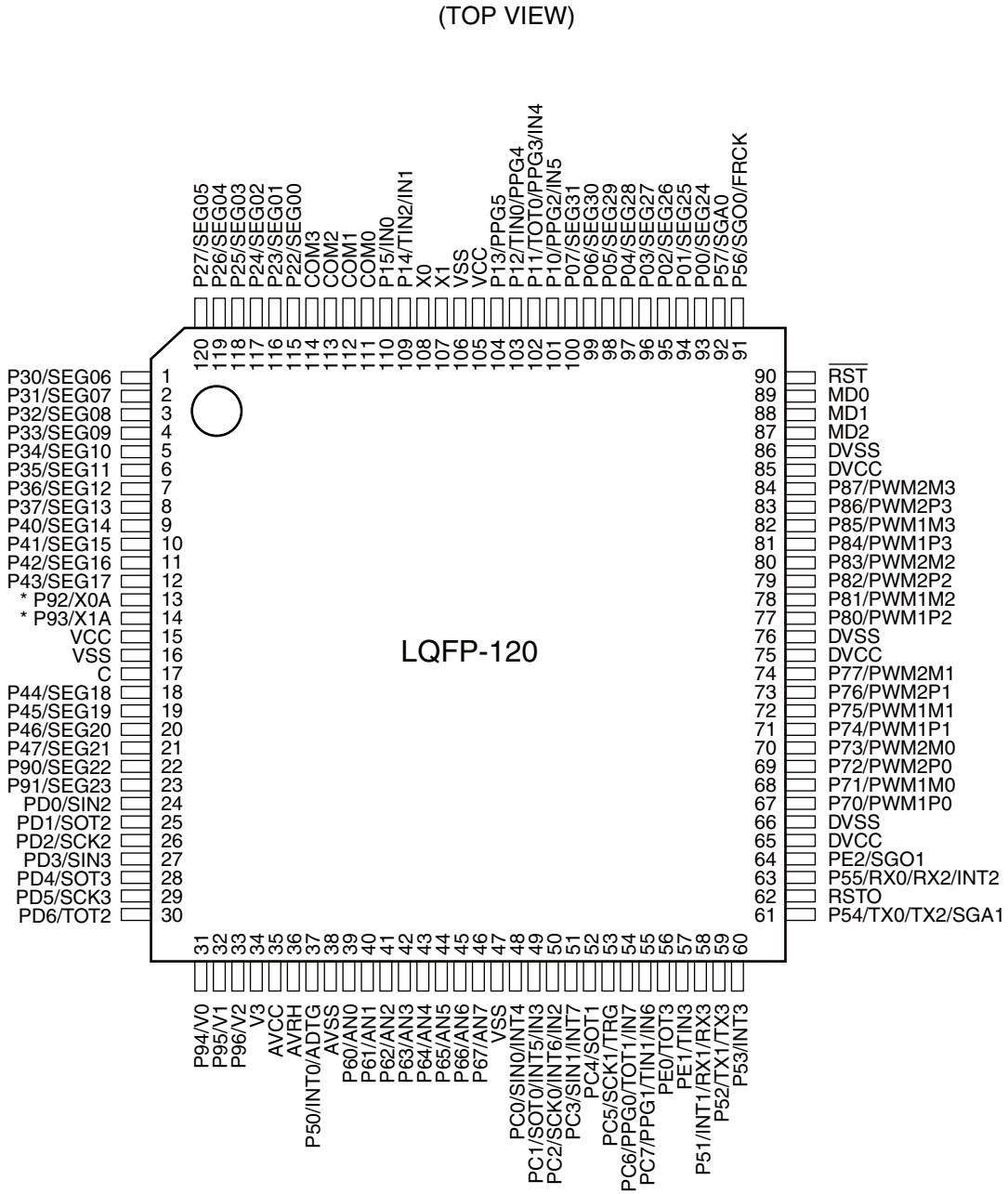
## ■ PRODUCT LINEUP

| Parameter \ Part number | MB90 F922NC | MB90 F922NCS | MB90 F923NC | MB90 F923NCS | MB90 F924NC | MB90 F924NCS | MB90 922NCS | MB90 V920-101 | MB90 V920-102 |
|---|---|---|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | | MASK ROM product | Evaluation product | |
| CPU | $F^2MC$-16LX CPU | | | | | | | | |
| System clock | PLL clock multiplier circuit ( × 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped)<br>Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8) | | | | | | | | |
| Sub clock pins (X0A, X1A) | Yes | No | Yes | No | Yes | No | No | No | Yes |
| ROM | Flash memory 256 Kbytes | | Flash memory 384 Kbytes | | Flash memory 512 Kbytes | | 256 K bytes | External | |
| RAM | 10 Kbytes | | 16 Kbytes | | 24 Kbytes | | 10 K bytes | 30 Kbytes | |
| I/O port | 91 ports | 93 ports | 91 ports | 93 ports | 91 ports | 93 ports | 93 ports | 93 ports | 91 ports |
| LCD controller | 32 segment × 4 common | | | | | | | | |
| LIN-UART | UART (LIN/SCI) 4 channels | | | | | | | | |
| CAN interface | 4 channels | | | | | | | | |
| 16-bit input capture | 8 channels | | | | | | | | |
| 16-bit reload timer | 4 channels | | | | | | | | |
| 16-bit free-run timer | 1 channel | | | | | | | | |
| Real time watch timer | 1 channel | | | | | | | | |
| 16-bit PPG timer | 6 channels | | | | | | | | |
| External interrupt | 8 channels | | | | | | | | |
| 8/10-bit A/D converter | 8 channels | | | | | | | | |
| Low-voltage/ CPU operating detection reset | Yes | | | | | | | No | |
| Stepping motor controller | 4 channels | | | | | | | | |
| Sound generator | 2 channels | | | | | | | | |
| Flash memory security | Yes | | | | | | — | | |
| Operating voltage | 4.0 V to 5.5 V | | | | | | | 4.5 V to 5.5 V | |
| Package | LQFP-120 | | | | | | | PGA-299 | |



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## ■ PIN ASSIGNMENT




(FPT-120P-M21)

* : MB90V920-101, MB90F922NCS,MB90F923NCS,MB90F924NCS,MB90922NCS : P92, P93
MB90V920-102, MB90F922NC,MB90F923NC,MB90F924NC : X0A, X1A



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## ■ PIN DESCRIPTIONS

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 108 | X0 | A | High-speed oscillation input pin |
| 107 | X1 | | High-speed oscillation output pin |
| 13 | X0A | B | Low-speed oscillation input pin |
| | P92 | I | General-purpose I/O port |
| 14 | X1A | B | Low-speed oscillation output pin |
| | P93 | I | General-purpose I/O port |
| 90 | $\overline{\text{RST}}$ | C | Reset input pin |
| 93 | P00 | F | General-purpose I/O port |
| | SEG24 | | LCD controller/driver segment output pin |
| 94 | P01 | F | General-purpose I/O port |
| | SEG25 | | LCD controller/driver segment output pin |
| 95 | P02 | F | General-purpose I/O port |
| | SEG26 | | LCD controller/driver segment output pin |
| 96 | P03 | F | General-purpose I/O port |
| | SEG27 | | LCD controller/driver segment output pin |
| 97 | P04 | F | General-purpose I/O port |
| | SEG28 | | LCD controller/driver segment output pin |
| 98 | P05 | F | General-purpose I/O port |
| | SEG29 | | LCD controller/driver segment output pin |
| 99 | P06 | F | General-purpose I/O port |
| | SEG30 | | LCD controller/driver segment output pin |
| 100 | P07 | F | General-purpose I/O port |
| | SEG31 | | LCD controller/driver segment output pin |
| 101 | P10 | I | General-purpose I/O port |
| | PPG2 | | 16-bit PPG ch.2 output pin |
| | IN5 | | Input capture ch.5 trigger input pin |
| 102 | P11 | I | General-purpose I/O port |
| | TOT0 | | 16-bit reload timer ch.0 TOT output pin |
| | PPG3 | | 16-bit PPG ch.3 output pin |
| | IN4 | | Input capture ch.4 trigger input pin |
| 103 | P12 | I | General-purpose I/O port |
| | TIN0 | | 16-bit reload timer ch.0 TIN input pin |
| | PPG4 | | 16-bit PPG ch.4 output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 104 | P13 | I | General-purpose I/O port |
| | PPG5 | | 16-bit PPG ch.5 output pin |
| 109 | P14 | I | General-purpose I/O port |
| | TIN2 | | 16-bit reload timer ch.2 TIN input pin |
| | IN1 | | Input capture ch.1 trigger input pin |
| 110 | P15 | I | General-purpose I/O port |
| | IN0 | | Input capture ch.0 trigger input pin |
| 111 | COM0 | P | LCD controller/driver common output pin |
| 112 | COM1 | P | LCD controller/driver common output pin |
| 113 | COM2 | P | LCD controller/driver common output pin |
| 114 | COM3 | P | LCD controller/driver common output pin |
| 115 | P22 | F | General-purpose I/O port |
| | SEG00 | | LCD controller/driver segment output pin |
| 116 | P23 | F | General-purpose I/O port |
| | SEG01 | | LCD controller/driver segment output pin |
| 117 | P24 | F | General-purpose I/O port |
| | SEG02 | | LCD controller/driver segment output pin |
| 118 | P25 | F | General-purpose I/O port |
| | SEG03 | | LCD controller/driver segment output pin |
| 119 | P26 | F | General-purpose I/O port |
| | SEG04 | | LCD controller/driver segment output pin |
| 120 | P27 | F | General-purpose I/O port |
| | SEG05 | | LCD controller/driver segment output pin |
| 1 | P30 | F | General-purpose I/O port |
| | SEG06 | | LCD controller/driver segment output pin |
| 2 | P31 | F | General-purpose I/O port |
| | SEG07 | | LCD controller/driver segment output pin |
| 3 | P32 | F | General-purpose I/O port |
| | SEG08 | | LCD controller/driver segment output pin |
| 4 | P33 | F | General-purpose I/O port |
| | SEG09 | | LCD controller/driver segment output pin |
| 5 | P34 | F | General-purpose I/O port |
| | SEG10 | | LCD controller/driver segment output pin |
| 6 | P35 | F | General-purpose I/O port |
| | SEG11 | | LCD controller/driver segment output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 7 | P36 | F | General-purpose I/O port |
| | SEG12 | | LCD controller/driver segment output pin |
| 8 | P37 | F | General-purpose I/O port |
| | SEG13 | | LCD controller/driver segment output pin |
| 9 | P40 | F | General-purpose I/O port |
| | SEG14 | | LCD controller/driver segment output pin |
| 10 | P41 | F | General-purpose I/O port |
| | SEG15 | | LCD controller/driver segment output pin |
| 11 | P42 | F | General-purpose I/O port |
| | SEG16 | | LCD controller/driver segment output pin |
| 12 | P43 | F | General-purpose I/O port |
| | SEG17 | | LCD controller/driver segment output pin |
| 18 | P44 | F | General-purpose I/O port |
| | SEG18 | | LCD controller/driver segment output pin |
| 19 | P45 | F | General-purpose I/O port |
| | SEG19 | | LCD controller/driver segment output pin |
| 20 | P46 | F | General-purpose I/O port |
| | SEG20 | | LCD controller/driver segment output pin |
| 21 | P47 | F | General-purpose I/O port |
| | SEG21 | | LCD controller/driver segment output pin |
| 37 | P50 | I | General-purpose I/O port |
| | INT0 | | INT0 external interrupt input pin |
| | ADTG | | A/D converter external trigger input pin |
| 58 | P51 | I | General-purpose I/O port |
| | INT1 | | INT1 external interrupt input pin |
| | RX1 | | CAN interface 1 RX input pin |
| | RX3 | | CAN interface 3 RX input pin |
| 59 | P52 | I | General-purpose I/O port |
| | TX1 | | CAN interface 1 TX output pin |
| | TX3 | | CAN interface 3 TX output pin |
| 60 | P53 | I | General-purpose I/O port |
| | INT3 | | INT3 external interrupt input pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 61 | P54 | I | General-purpose I/O port |
| | TX0 | | CAN interface 0 TX output pin |
| | TX2 | | CAN interface 2 TX output pin |
| | SGA1 | | Sound generator ch.1 SGA output pin |
| 63 | P55 | I | General-purpose I/O port |
| | RX0 | | CAN interface 0 RX input pin |
| | RX2 | | CAN interface 2 RX input pin |
| | INT2 | | INT2 external interrupt input pin |
| 91 | P56 | I | General-purpose I/O port |
| | SGO0 | | Sound generator ch.0 SGO output pin |
| | FRCK | | Free-run timer clock input pin |
| 92 | P57 | I | General-purpose I/O port |
| | SGA0 | | Sound generator ch.0 SGA output pin |
| 39 | P60 | H | General-purpose I/O port |
| | AN0 | | A/D converter input pin |
| 40 | P61 | H | General-purpose I/O port |
| | AN1 | | A/D converter input pin |
| 41 | P62 | H | General-purpose I/O port |
| | AN2 | | A/D converter input pin |
| 42 | P63 | H | General-purpose I/O port |
| | AN3 | | A/D converter input pin |
| 43 | P64 | H | General-purpose I/O port |
| | AN4 | | A/D converter input pin |
| 44 | P65 | H | General-purpose I/O port |
| | AN5 | | A/D converter input pin |
| 45 | P66 | H | General-purpose I/O port |
| | AN6 | | A/D converter input pin |
| 46 | P67 | H | General-purpose I/O port |
| | AN7 | | A/D converter input pin |
| 67 | P70 | L | General-purpose output-only port |
| | PWM1P0 | | Stepping motor controller ch.0 output pin |
| 68 | P71 | L | General-purpose output-only port |
| | PWM1M0 | | Stepping motor controller ch.0 output pin |
| 69 | P72 | L | General-purpose output-only port |
| | PWM2P0 | | Stepping motor controller ch.0 output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 70 | P73 | L | General-purpose output-only port |
| | PWM2M0 | | Stepping motor controller ch.0 output pin |
| 71 | P74 | L | General-purpose output-only port |
| | PWM1P1 | | Stepping motor controller ch.1 output pin |
| 72 | P75 | L | General-purpose output-only port |
| | PWM1M1 | | Stepping motor controller ch.1 output pin |
| 73 | P76 | L | General-purpose output-only port |
| | PWM2P1 | | Stepping motor controller ch.1 output pin |
| 74 | P77 | L | General-purpose output-only port |
| | PWM2M1 | | Stepping motor controller ch.1 output pin |
| 77 | P80 | L | General-purpose output-only port |
| | PWM1P2 | | Stepping motor controller ch.2 output pin |
| 78 | P81 | L | General-purpose output-only port |
| | PWM1M2 | | Stepping motor controller ch.2 output pin |
| 79 | P82 | L | General-purpose output-only port |
| | PWM2P2 | | Stepping motor controller ch.2 output pin |
| 80 | P83 | L | General-purpose output-only port |
| | PWM2M2 | | Stepping motor controller ch.2 output pin |
| 81 | P84 | L | General-purpose output-only port |
| | PWM1P3 | | Stepping motor controller ch.3 output pin |
| 82 | P85 | L | General-purpose output-only port |
| | PWM1M3 | | Stepping motor controller ch.3 output pin |
| 83 | P86 | L | General-purpose output-only port |
| | PWM2P3 | | Stepping motor controller ch.3 output pin |
| 84 | P87 | L | General-purpose output-only port |
| | PWM2M3 | | Stepping motor controller ch.3 output pin |
| 22 | P90 | F | General-purpose I/O port |
| | SEG22 | | LCD controller/driver segment output pin |
| 23 | P91 | F | General-purpose I/O port |
| | SEG23 | | LCD controller/driver segment output pin |
| 31 | P94 | G | General-purpose I/O port |
| | V0 | | LCD controller/driver reference power supply pin |
| 32 | P95 | G | General-purpose I/O port |
| | V1 | | LCD controller/driver reference power supply pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 33 | P96 | G | General-purpose I/O port |
| | V2 | | LCD controller/driver reference power supply pin |
| 34 | V3 | — | LCD controller/driver reference power supply pin |
| 48 | PC0 | J | General-purpose I/O port |
| | SIN0 | | UART ch.0 serial data input pin |
| | INT4 | | INT4 external interrupt input pin |
| 49 | PC1 | I | General-purpose I/O port |
| | SOT0 | | UART ch.0 serial data output pin |
| | INT5 | | INT5 external interrupt input pin |
| | IN3 | | Input capture ch.3 trigger input pin |
| 50 | PC2 | I | General-purpose I/O port |
| | SCK0 | | UART ch.0 serial clock I/O pin |
| | INT6 | | INT6 external interrupt input pin |
| | IN2 | | Input capture ch.2 trigger input pin |
| 51 | PC3 | J | General-purpose I/O port |
| | SIN1 | | UART ch.1 serial data input pin |
| | INT7 | | INT7 external interrupt input pin |
| 52 | PC4 | I | General-purpose I/O port |
| | SOT1 | | UART ch.1 serial data output pin |
| 53 | PC5 | I | General-purpose I/O port |
| | SCK1 | | UART ch.1 serial clock I/O pin |
| | TRG | | 16-bit PPG ch.0 to ch.5 external trigger input pin |
| 54 | PC6 | I | General-purpose I/O port |
| | PPG0 | | 16-bit PPG ch.0 output pin |
| | TOT1 | | 16-bit reload timer ch.1 TOT output pin |
| | IN7 | | Input capture ch.7 trigger input pin |
| 55 | PC7 | I | General-purpose I/O port |
| | PPG1 | | 16-bit PPG ch.1 output pin |
| | TIN1 | | 16-bit reload timer ch.1 TIN input pin |
| | IN6 | | Input capture ch.6 trigger input pin |
| 24 | PD0 | J | General-purpose I/O port |
| | SIN2 | | UART ch.2 serial data input pin |
| 25 | PD1 | I | General-purpose I/O port |
| | SOT2 | | UART ch.2 serial data output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 26 | PD2 | I | General-purpose I/O port |
| | SCK2 | | UART ch.2 serial clock I/O pin |
| 27 | PD3 | J | General-purpose I/O port |
| | SIN3 | | UART ch.3 serial data input pin |
| 28 | PD4 | I | General-purpose I/O port |
| | SOT3 | | UART ch.3 serial data output pin |
| 29 | PD5 | I | General-purpose I/O port |
| | SCK3 | | UART ch.3 serial clock I/O pin |
| 30 | PD6 | I | General-purpose I/O port |
| | TOT2 | | 16-bit reload timer ch.2 TOT output pin |
| 56 | PE0 | I | General-purpose I/O port |
| | TOT3 | | 16-bit reload timer ch.3 TOT output pin |
| 57 | PE1 | I | General-purpose I/O port |
| | TIN3 | | 16-bit reload timer ch.3 TIN input pin |
| 64 | PE2 | I | General-purpose I/O port |
| | SGO1 | | Sound generator ch.1 SGO output pin |
| 62 | RSTO | N | Internal reset signal output pin |
| 65, 75, 85 | DVCC | — | Power supply input pins dedicated for high current output buffer |
| 66, 76, 86 | DVSS | — | Power supply GND pins dedicated for high current output buffer |
| 35 | AVCC | — | A/D converter dedicated power supply input pin |
| 38 | AVSS | — | A/D converter dedicated power supply GND pin |
| 36 | AVRH | — | A/D converter Vref+ input pin. Vref- is fixed to AVSS. |
| 89 | MD0 | D | Mode setting input pin. Connect to VCC pin. |
| 88 | MD1 | D | Mode setting input pin. Connect to VCC pin. |
| 87 | MD2 | D/E*2 | Mode setting input pin. Connect to VSS pin. |
| 17 | C | — | External capacitor pin.<br>Connect a 0.1 µF capacitor between this pin and the VSS pin. |
| 15, 105 | VCC | — | Power supply input pins |
| 16, 47, 106 | VSS | — | GND power supply pins |

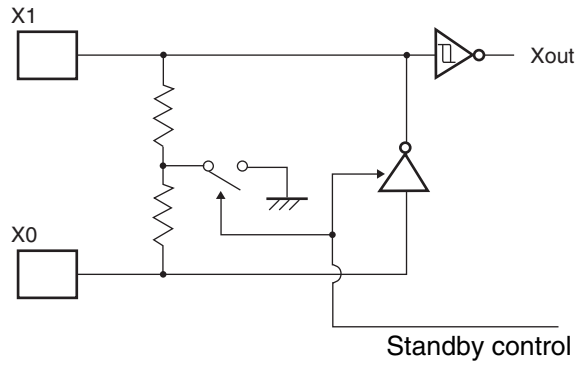
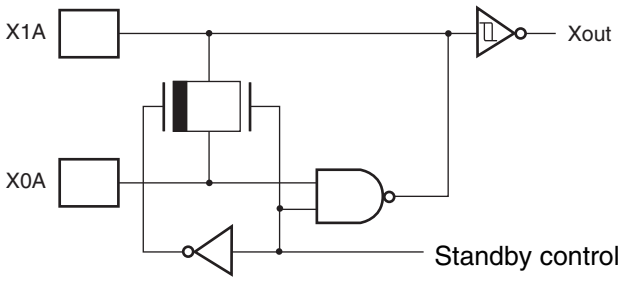
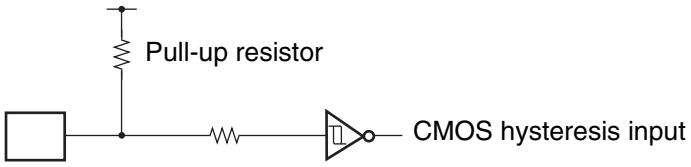
*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.



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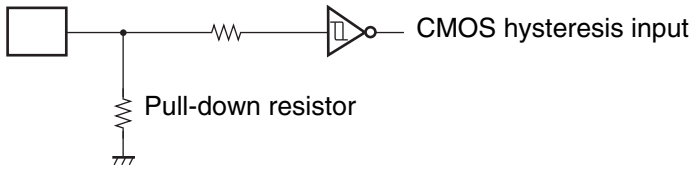
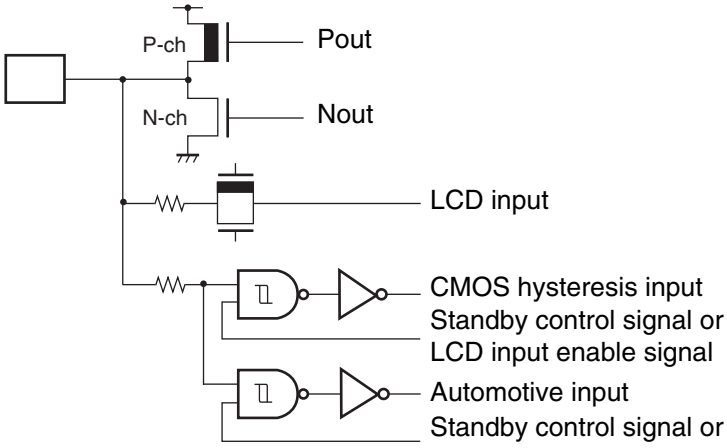
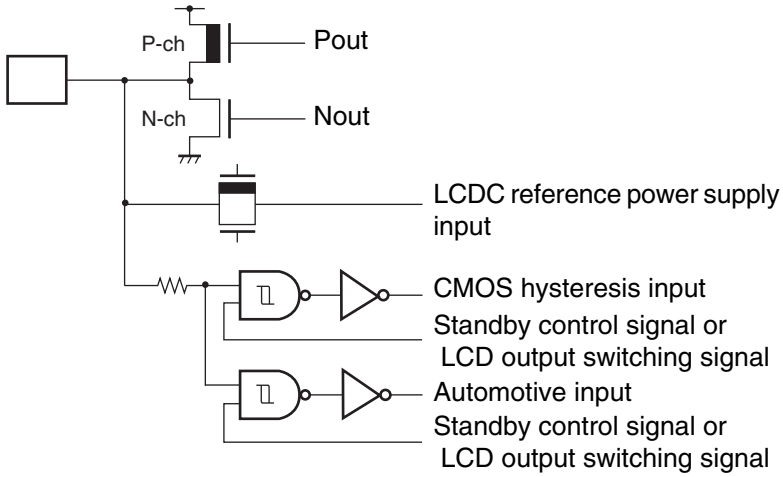
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>High-speed oscillation feedback resistance :<br>approx. 1 MΩ<br>(Flash memory product/MASK ROM product/Evaluation product) |
| B |  | Oscillation circuit<br>Low-speed oscillation feedback resistance : approx. 10 MΩ |
| C |  | Input-only pin (with pull-up resistance)<br>• Attached pull-up resistor : approx. 50 kΩ<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$) |
| D |  | Input-only pin<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>Note: The MD2 pin of the Flash memory products uses this circuit type. |

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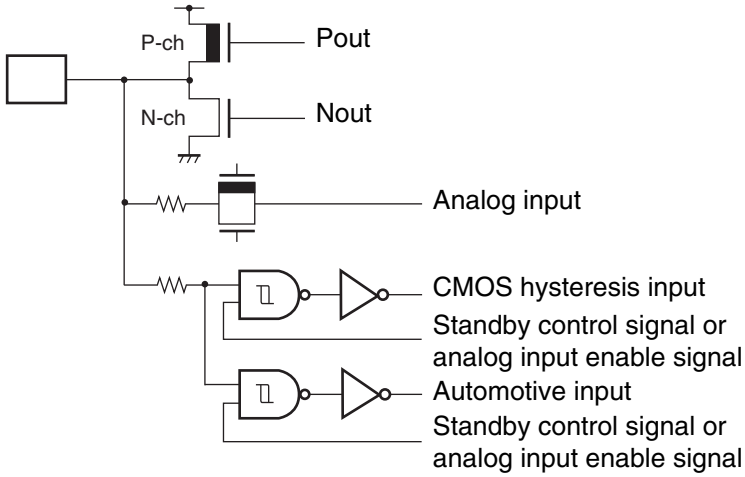
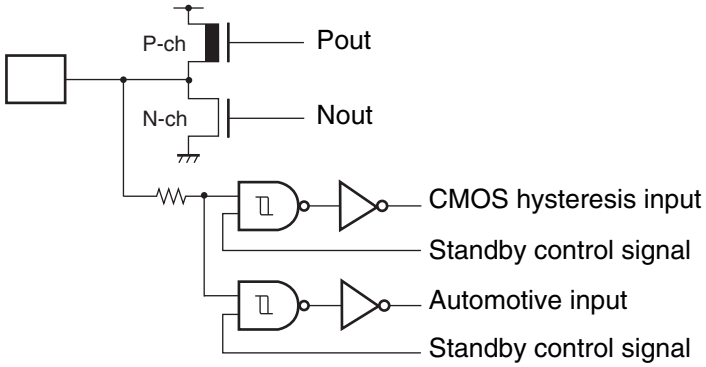
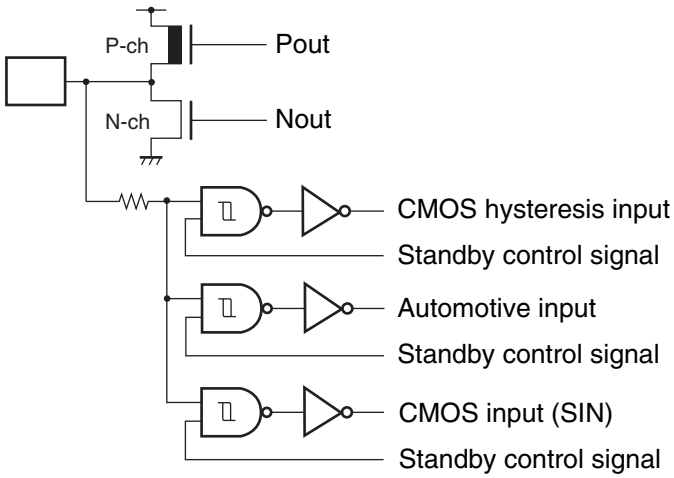
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| Type | Circuit | Remarks |
|---|---|---|
| E |  | Input-only pin (with pull-down resistance)<br>• Attached pull-down resistance: approx. 50 kΩ<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>Note: The MD2 pin of the evaluation products uses this circuit type. |
| F |  | LCD output common general-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• Hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| G |  | LCDC reference power supply common general-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |

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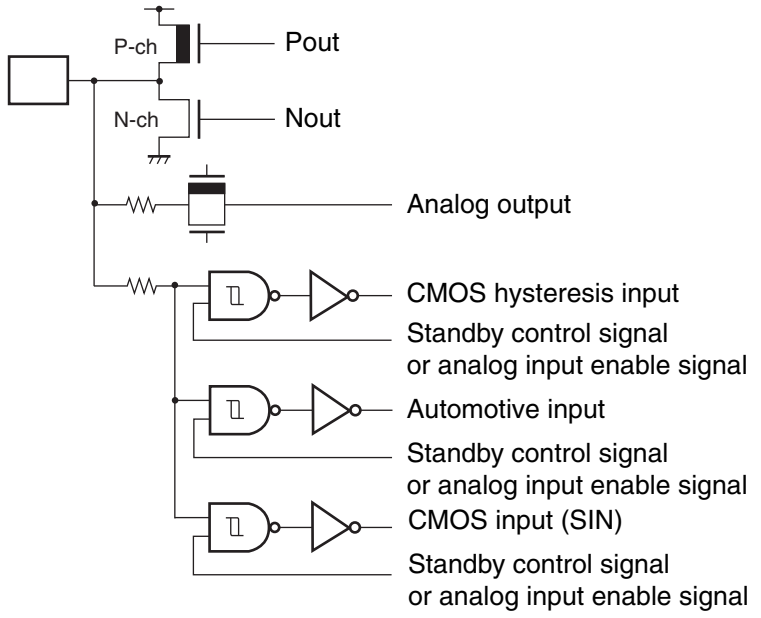
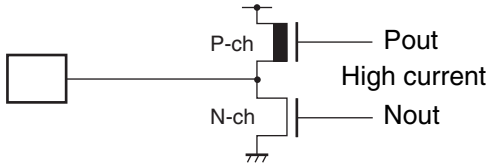
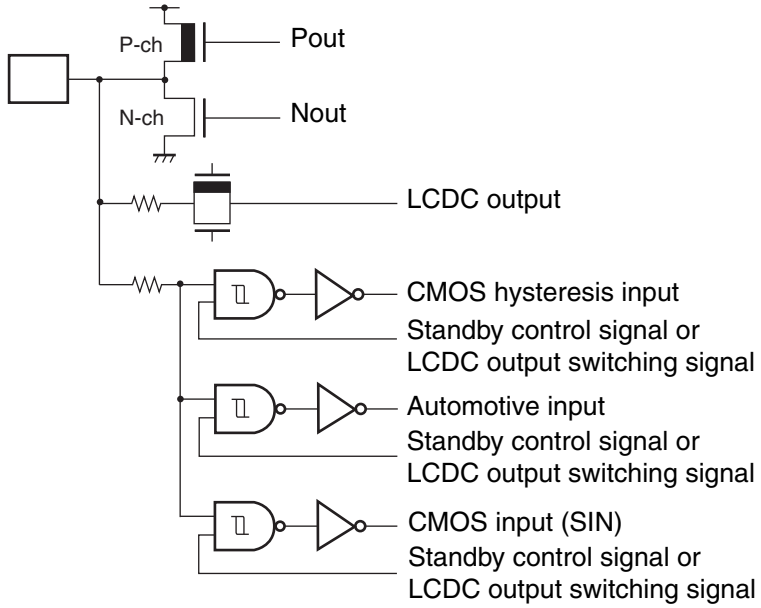
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| Type | Circuit | Remarks |
|---|---|---|
| H |  | A/D converter input common general-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| I |  | General-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| J |  | General-purpose port (serial input)<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |

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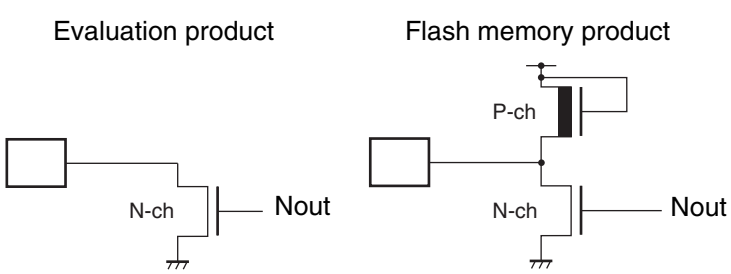
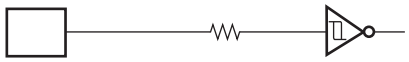
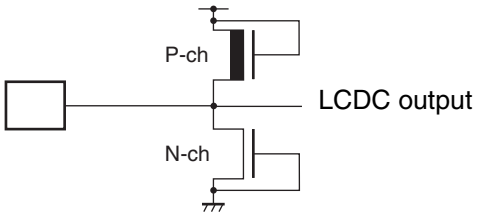
| Type | Circuit | Remarks |
|---|---|---|
| K |  | A/D converter input common general-purpose port (serial input)<br>• CMOS output ($I_{OH}/I_{OL}$ = ±4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| L |  | High current output port (SMC pin)<br>CMOS output ($I_{OH}/I_{OL}$ = ±30 mA) |
| M |  | LCDC output common general-purpose port (serial input) )<br>• CMOS output ($I_{OH}/I_{OL}$ = ±4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |

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| Type | Circuit | Remarks |
|---|---|---|
| N |  | N-ch open-drain pin<br>$I_{OL}$ = 4 mA |
| O |  | Input-only pin<br>Automotive input<br>($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| P |  | LCDC output pin (COM pin) |



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## ■ HANDLING DEVICES

- **Strictly observe maximum rated voltages (preventing latch-up)**

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than $V_{CC}$ or lower than $V_{SS}$ are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply ($AV_{CC}$, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins ($DV_{CC}$) in excess of the digital power supply voltage ($V_{CC}$).

Once the digital power supply voltage ($V_{CC}$) has been disconnected, the analog power supply ($AV_{CC}$, AVRH) and the power supply voltage for the high current output buffer pins ($DV_{CC}$) may be turned on in any sequence.

- **Supply voltage stabilization**

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard $V_{CC}$ value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

- **Precautions when turning the power on**

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 µs.

- **Handling unused pins**

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

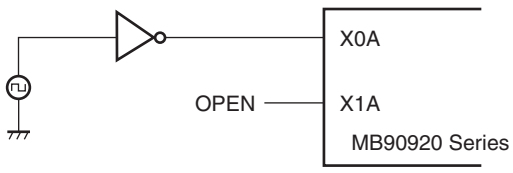
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

- **Handling A/D converter power supply pins**

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

- **Notes on using an external clock**

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.




Sample external clock connection



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- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

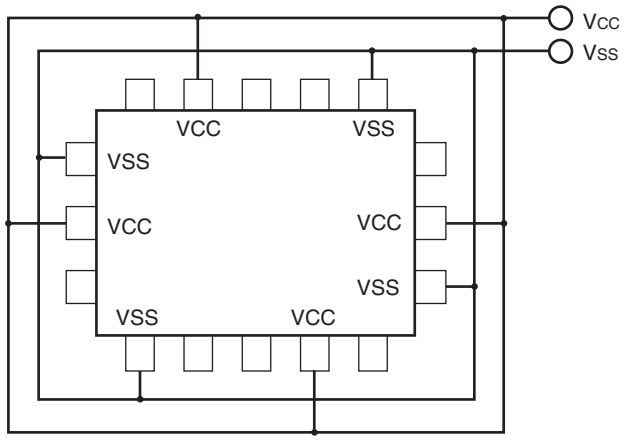
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.




Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 µF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply ($AV_{CC}$, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply ($V_{CC}$) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off ($V_{CC}$). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).



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- **Handling the power supply for high-current output buffer pins** ($DV_{CC}$, $DV_{SS}$)

  - **Flash memory products and MASK ROM products (MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/F924NC/F924NCS)**

    In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is isolated from the digital power supply ($V_{CC}$).
    Therefore, DVcc can therefore be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is supplied before the digital power supply ($V_{CC}$), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply ($V_{CC}$) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$).

  - **Evaluation product** (**MB90V920-101**/**MB90V920-102**)

    In the evaluation products, the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is not isolated from the digital power supply ($V_{CC}$). Therefore, $DV_{CC}$ must therefore be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) must always be applied after the digital power supply ($V_{CC}$) has been connected, and disconnected before the digital power supply (Vcc) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).
    Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$).

- **Pull-up/pull-down resistors**

MB90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

- **Precautions when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

- **Notes on operating when the external clock is stopped**

The MB90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

- **Flash memory security function**

A security bit is located within the Flash memory region. The security function is activated by writing the protection code $01_H$ to the security bit.
Do not write the value $01_H$ to this address if you are not using the security function.
Please refer to following table for the address of the security bit.

| | Flash memory size | Address for security bit |
|---|---|---|
| MB90F922NC<br>MB90F922NCS | Built-in 2 Mbits Flash Memory | FC0001$_H$ |
| MB90F923NCS | Built-in 3 Mbits Flash Memory | F80001$_H$ |
| MB90F924NCS | Built-in 4 Mbits Flash Memory | F80001$_H$ |



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- **Serial communication**

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

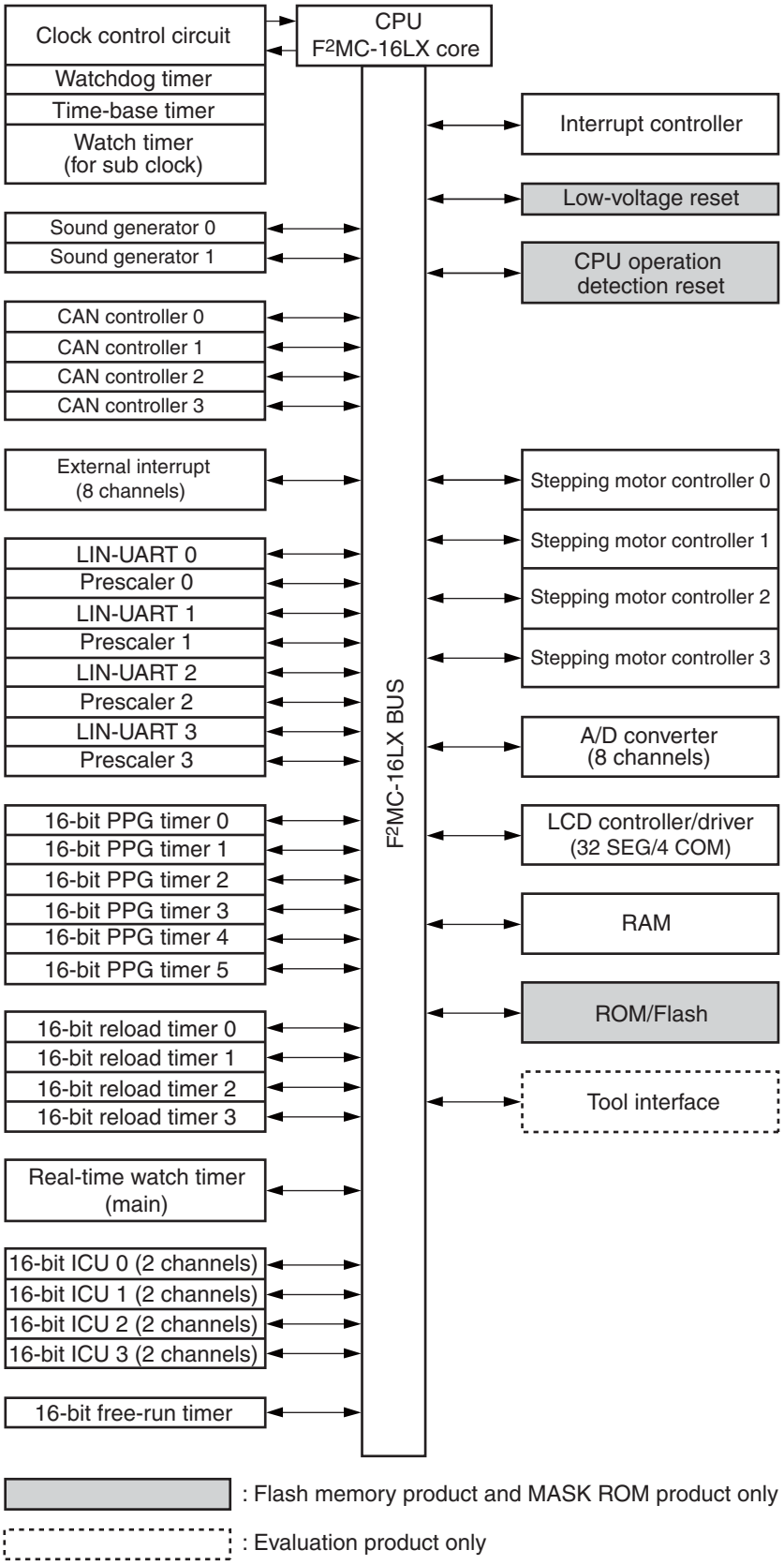
In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.



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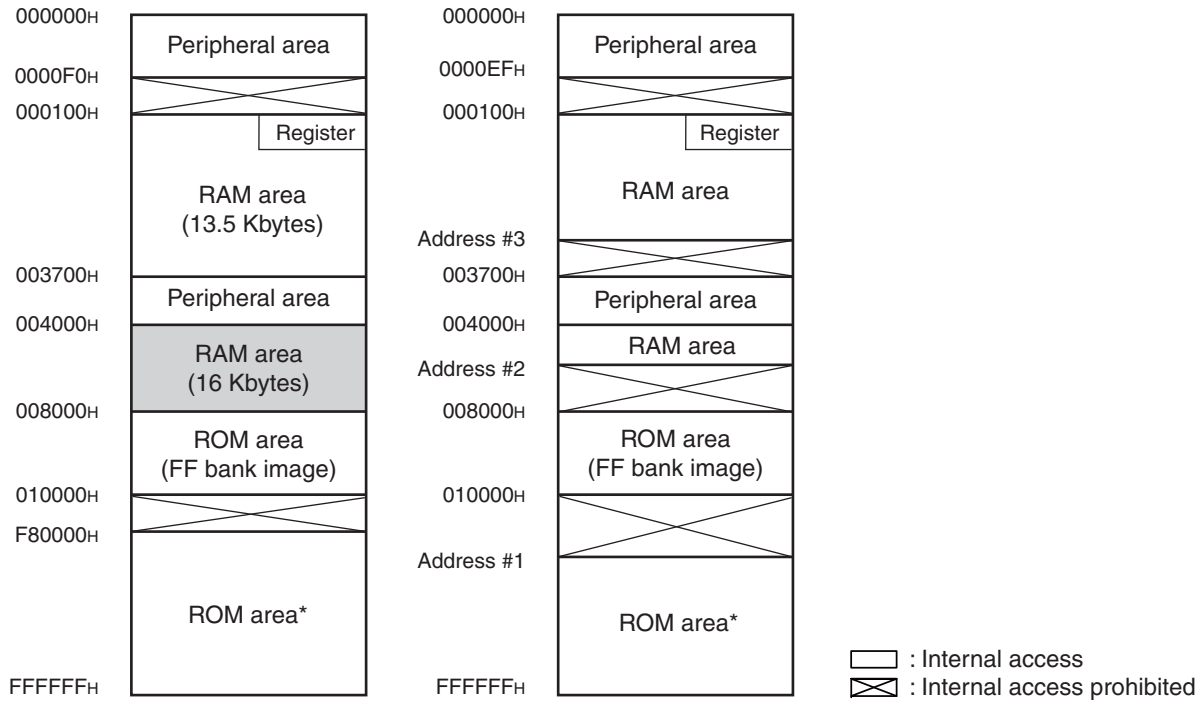
## ■ BLOCK DIAGRAM






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## ■ MEMORY MAP




| Parts No. | ROM (Flash) capacitance | RAM capacitance | Address #1 | Address #2 | Address #3 |
|---|---|---|---|---|---|
| MB90F922NC/F922NCS/922NCS | 256 Kbytes | 10 Kbytes | FC0000H | 004000H | 002900H |
| MB90F923NC/F923NCS | 384 Kbytes | 16 Kbytes | FA0000H | 004A00H | 003700H |
| MB90F924NC/F924NCS | 512 Kbytes | 24 Kbytes | F80000H | 006A00H | 003700H |

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.



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## ■ I/O MAP

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000000H | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXXB |
| 000001H | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXXB |
| 000002H | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXXB |
| 000003H | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXXB |
| 000004H | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXXB |
| 000005H | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXXB |
| 000006H | Port 6 data register | PDR6 | R/W | Port 6 | XXXXXXXXB |
| 000007H | Port 7 data register | PDR7 | R/W | Port 7 | XXXXXXXXB |
| 000008H | Port 8 data register | PDR8 | R/W | Port 8 | XXXXXXXXB |
| 000009H | Port 9 data register | PDR9 | R/W | Port 9 | XXXXXXXXB |
| 00000AH, 00000BH | (Disabled) | | | | |
| 00000CH | Port C data register | PDRC | R/W | Port C | XXXXXXXXB |
| 00000DH | Port D data register | PDRD | R/W | Port D | XXXXXXXXB |
| 00000EH | Port E data register | PDRE | R/W | Port E | XXXXXXXXB |
| 00000FH | (Disabled) | | | | |
| 000010H | Port 0 direction register | DDR0 | R/W | Port 0 | 00000000B |
| 000011H | Port 1 direction register | DDR1 | R/W | Port 1 | XX000000B |
| 000012H | Port 2 direction register | DDR2 | R/W | Port 2 | 000000XXB |
| 000013H | Port 3 direction register | DDR3 | R/W | Port 3 | 00000000B |
| 000014H | Port 4 direction register | DDR4 | R/W | Port 4 | 00000000B |
| 000015H | Port 5 direction register | DDR5 | R/W | Port 5 | 00000000B |
| 000016H | Port 6 direction register | DDR6 | R/W | Port 6 | 00000000B |
| 000017H | Port 7 direction register | DDR7 | R/W | Port 7 | 00000000B |
| 000018H | Port 8 direction register | DDR8 | R/W | Port 8 | 00000000B |
| 000019H | Port 9 direction register | DDR9 | R/W | Port 9 | X0000000B |
| 00001AH | Analog input enable | ADER6 | R/W | Port 6, A/D | 11111111B |
| 00001BH | (Disabled) | | | | |
| 00001CH | Port C direction register | DDRC | R/W | Port C | 00000000B |
| 00001DH | Port D direction register | DDRD | R/W | Port D | X0000000B |
| 00001EH | Port E direction register | DDRE | R/W | Port E | XXXXX000B |
| 00001FH | (Disabled) | | | | |
| 000020H | Lower A/D control status register | ADCS0 | R/W | A/D converter | 000XXXX0B |
| 000021H | Higher A/D control status register | ADCS1 | R/W | | 0000000XB |
| 000022H | Lower A/D control status register | ADCR0 | R | | 00000000B |
| 000023H | Higher A/D data register | ADCR1 | R | | XXXXXX00B |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000024H | Compare clear register | CPCLR | R/W | 16-bit free-run timer | XXXXXXXXB |
| 000025H | | | R/W | | XXXXXXXXB |
| 000026H | Timer data register | TCDT | R/W | | 00000000B |
| 000027H | | | R/W | | 00000000B |
| 000028H | Lower timer control status register | TCCSL | R/W | | 00000000B |
| 000029H | Higher timer control status register | TCCSH | R/W | | 01-00000B |
| 00002AH | Lower PPG0 control status register | PCNTL0 | R/W | 16-bit PPG0 | 00000000B |
| 00002BH | Higher PPG0 control status register | PCNTH0 | R/W | | 00000001B |
| 00002CH | Lower PPG1 control status register | PCNTL1 | R/W | 16-bit PPG1 | 00000000B |
| 00002DH | Higher PPG1 control status register | PCNTH1 | R/W | | 00000001B |
| 00002EH | Lower PPG2 control status register | PCNTL2 | R/W | 16-bit PPG2 | 00000000B |
| 00002FH | Higher PPG2 control status register | PCNTH2 | R/W | | 00000001B |
| 000030H | External interrupt enable | ENIR | R/W | External interrupt | 00000000B |
| 000031H | External interrupt request | EIRR | R/W | | 00000000B |
| 000032H | Lower external interrupt level | ELVRL | R/W | | 00000000B |
| 000033H | Higher external interrupt level | ELVRH | R/W | | 00000000B |
| 000034H | Serial mode register 0 | SMR0 | R/W, W | UART (LIN/SCI) 0 | 00000000B |
| 000035H | Serial control register 0 | SCR0 | R/W, W | | 00000000B |
| 000036H | Reception/transmission data register 1 | RDR0/ TDR0 | R/W | | 00000000B |
| 000037H | Serial status register 0 | SSR0 | R/W, R | | 00001000B |
| 000038H | Extended communication control register 0 | ECCR0 | R/W, R | | 000000XXB |
| 000039H | Extended status control register 0 | ESCR0 | R/W | | 00000100B |
| 00003AH | Baud rate generator register 00 | BGR00 | R/W | | 00000000B |
| 00003BH | Baud rate generator register 01 | BGR01 | R/W, R | | 00000000B |
| 00003CH to 00003FH | (Disabled) | | | | |
| 000040H to 00004FH | Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS” | | | | |
| 000050H | Lower timer control status register 0 | TMCSR0L | R/W | 16-bit reload timer 0 | 00000000B |
| 000051H | Higher timer control status register 0 | TMCSR0H | R/W | | XXX10000B |
| 000052H | Timer register 0/reload register 0 | TMR0/ TMRLR0 | R/W | | XXXXXXXXB |
| 000053H | | | | | XXXXXXXXB |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000054H | Lower timer control status register 1 | TMCSR1L | R/W | 16-bit reload timer 1 | 00000000B |
| 000055H | Higher timer control status register 1 | TMCSR1H | R/W | | XXX10000B |
| 000056H | Timer register 1/reload register 1 | TMR1/ TMRLR1 | R/W | | XXXXXXXXB |
| 000057H | | | | | XXXXXXXXB |
| 000058H | LCD output control register 1 | LOCR1 | R/W | LCDC | 11111111B |
| 000059H | LCD output control register 2 | LOCR2 | R/W | | 00000000B |
| 00005AH | Lower sound control register 0 | SGCRL0 | R/W | Sound generator 0 | 00000000B |
| 00005BH | Higher sound control register 0 | SGCRH0 | R/W | | 0XXXX100B |
| 00005CH | Frequency data register 0 | SGFR0 | R/W | | XXXXXXXXB |
| 00005DH | Amplitude data register 0 | SGAR0 | R/W | | 00000000B |
| 00005EH | Decrement grade register 0 | SGDR0 | R/W | | XXXXXXXXB |
| 00005FH | Tone count register 0 | SGTR0 | R/W | | XXXXXXXXB |
| 000060H | Input capture register 0 | IPCP0 | R | Input capture 0/1 | XXXXXXXXB |
| 000061H | | | | | XXXXXXXXB |
| 000062H | Input capture register 1 | IPCP1 | R | | XXXXXXXXB |
| 000063H | | | | | XXXXXXXXB |
| 000064H | Input capture register 2 | IPCP2 | R | Input capture 2/3 | XXXXXXXXB |
| 000065H | | | | | XXXXXXXXB |
| 000066H | Input capture register 3 | IPCP3 | R | | XXXXXXXXB |
| 000067H | | | | | XXXXXXXXB |
| 000068H | Input capture control status 0/1 | ICS01 | R/W | Input capture 0/1 | 00000000B |
| 000069H | Input capture edge register 0/1 | ICE01 | R/W | | XXX0X0XXB |
| 00006AH | Input capture control status 2/3 | ICS23 | R/W | Input capture 2/3 | 00000000B |
| 00006BH | Input capture edge register 2/3 | ICE23 | R/W | | XXXXXXXXB |
| 00006CH | Lower LCD control register | LCRL | R/W | LCD controller/ driver | 00010000B |
| 00006DH | Higher LCD control register | LCRH | R/W | | 00000000B |
| 00006EH | Low voltage/CPU operation detection reset control register | LVRC | R/W | Low voltage/CPU operation detection reset | 00111000B |
| 00006FH | ROM mirror | ROMM | W | ROM mirror | XXXXXXX1B |
| 000070H to 00007FH | Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 000080H | PWM control register 0 | PWC0 | R/W | Stepping motor controller 0 | 000000X0B |
| 000081H | (Disabled) | | | | |
| 000082H | PWM control register 1 | PWC1 | R/W | Stepping motor controller 1 | 000000X0B |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000083H | (Disabled) | | | | |
| 000084H | PWM control register 2 | PWC2 | R/W | Stepping motor controller 2 | 000000X0B |
| 000085H | (Disabled) | | | | |
| 000086H | PWM control register 3 | PWC3 | R/W | Stepping motor controller 3 | 000000X0B |
| 000087H | (Disabled) | | | | |
| 000088H | LCD output control register 3 | LOCR3 | R/W | LCDC | XXXXX111B |
| 000089H | (Disabled) | | | | |
| 00008AH | A/D setting register 0 | ADSR0 | R/W | A/D converter | 00000000B |
| 00008BH | A/D setting register 1 | ADSR1 | R/W | | 00000000B |
| 00008CH | Port input level select 0 | PIL0 | R/W | Port input level select | 00000000B |
| 00008DH | Port input level select 1 | PIL1 | R/W | | XXXX0000B |
| 00008EH | Port input level select 2 | PIL2 | R/W | | XXXX0000B |
| 00008FH to 00009DH | (Disabled) | | | | |
| 00009EH | Program address detection control register | PACSR | R/W | Address match detection | XXXX0X0XB |
| 00009FH | Delayed Interrupt/Release Register | DIRR | R/W | Delay interrupt | XXXXXXX0B |
| 0000A0H | Power saving mode control register | LPMCR | R/W | Power saving control circuit | 00011000B |
| 0000A1H | Clock select register | CKSCR | R/W, R | | 11111100B |
| 0000A2H to 0000A7H | (Disabled) | | | | |
| 0000A8H | Watchdog timer control register | WDTC | R, W | Watchdog timer | XXXXX111B |
| 0000A9H | Time-base timer control register | TBTC | R/W, W | Time-base timer | 1XX00100B |
| 0000AAH | Watch timer control register | WTC | R/W, W, R | Watch timer (sub clock) | 10001000B |
| 0000ABH to 0000ADH | (Disabled) | | | | |
| 0000AEH | Flash memory control status register | FMCS | R/W | Flash interface | 000X0000B |
| 0000AFH | (Disabled) | | | | |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000B0H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111B |
| 0000B1H | Interrupt control register 01 | ICR01 | R/W | | 00000111B |
| 0000B2H | Interrupt control register 02 | ICR02 | R/W | | 00000111B |
| 0000B3H | Interrupt control register 03 | ICR03 | R/W | | 00000111B |
| 0000B4H | Interrupt control register 04 | ICR04 | R/W | | 00000111B |
| 0000B5H | Interrupt control register 05 | ICR05 | R/W | | 00000111B |
| 0000B6H | Interrupt control register 06 | ICR06 | R/W | | 00000111B |
| 0000B7H | Interrupt control register 07 | ICR07 | R/W | | 00000111B |
| 0000B8H | Interrupt control register 08 | ICR08 | R/W | | 00000111B |
| 0000B9H | Interrupt control register 09 | ICR09 | R/W | | 00000111B |
| 0000BAH | Interrupt control register 10 | ICR10 | R/W | | 00000111B |
| 0000BBH | Interrupt control register 11 | ICR11 | R/W | | 00000111B |
| 0000BCH | Interrupt control register 12 | ICR12 | R/W | | 00000111B |
| 0000BDH | Interrupt control register 13 | ICR13 | R/W | | 00000111B |
| 0000BEH | Interrupt control register 14 | ICR14 | R/W | | 00000111B |
| 0000BFH | Interrupt control register 15 | ICR15 | R/W | | 00000111B |
| 0000C0H to 0000C3H | (Disabled) | | | | |
| 0000C4H | Serial mode register 1 | SMR1 | R/W, W | UART (LIN/SCI) 1 | 00000000B |
| 0000C5H | Serial control register 1 | SCR1 | R/W, W | | 00000000B |
| 0000C6H | Reception/transmission data register 1 | RDR1/ TDR1 | R/W | | 00000000B |
| 0000C7H | Serial status register 1 | SSR1 | R/W, R | | 00001000B |
| 0000C8H | Extended communication control register 1 | ECCR1 | R/W, R | | 000000XXB |
| 0000C9H | Extended status control register 1 | ESCR1 | R/W | | 00000100B |
| 0000CAH | Baud rate generator register 10 | BGR10 | R/W | | 00000000B |
| 0000CBH | Baud rate generator register 11 | BGR11 | R/W, R | | 00000000B |
| 0000CCH | Lower watch timer control register | WTCRL | R/W | Real-time watch timer | 000XXXX0B |
| 0000CDH | Middle watch timer control register | WTCRM | R/W | | 00000000B |
| 0000CEH | Higher watch timer control register | WTCRH | R/W | | XXXXXX00B |
| 0000CFH | Sub clock control register | PSCCR | W | Sub clock | XXXX0000B |
| 0000D0H | Input capture control status 4/5 | ICS45 | R/W | Input capture 4/5 | 00000000B |
| 0000D1H | Input capture edge register 4/5 | ICE45 | R/W, R | | XXXXXXXXB |
| 0000D2H | Input capture control status 6/7 | ICS67 | R/W | Input capture 6/7 | 00000000B |
| 0000D3H | Input capture edge register 6/7 | ICE67 | R/W, R | | XXX0X0XXB |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000D4H | Lower timer control status register 2 | TMCSR2L | R/W | 16-bit reload timer 2 | 00000000B |
| 0000D5H | Higher timer control status register 2 | TMCSR2H | R/W | | XXX10000B |
| 0000D6H | Lower timer control status register 3 | TMCSR3L | R/W | 16-bit reload timer 3 | 00000000B |
| 0000D7H | Higher timer control status register 3 | TMCSR3H | R/W | | XXX10000B |
| 0000D8H | Lower sound control register 1 | SGCRL1 | R/W | Sound generator 1 | 00000000B |
| 0000D9H | Higher sound control register 1 | SGCRH1 | R/W | | 0XXXX100B |
| 0000DAH | Lower PPG3 control status register | PCNTL3 | R/W | 16-bit PPG3 | 00000000B |
| 0000DBH | Higher PPG3 control status register | PCNTH3 | R/W | | 00000001B |
| 0000DCH | Lower PPG4 control status register | PCNTL4 | R/W | 16-bit PPG4 | 00000000B |
| 0000DDH | Higher PPG4 control status register | PCNTH4 | R/W | | 00000001B |
| 0000DEH | Lower PPG5 control status register | PCNTL5 | R/W | 16-bit PPG5 | 00000000B |
| 0000DFH | Higher PPG5 control status register | PCNTH5 | R/W | | 00000001B |
| 0000E0H | Serial mode register 2 | SMR2 | R/W, W | UART (LIN/SCI) 2 | 00000000B |
| 0000E1H | Serial control register 2 | SCR2 | R/W, W | | 00000000B |
| 0000E2H | Reception/transmission data register 2 | RDR2/ TDR2 | R/W | | 00000000B |
| 0000E3H | Serial status register 2 | SSR2 | R/W, R | | 00001000B |
| 0000E4H | Extended communication control register 2 | ECCR2 | R/W, R | | 000000XXB |
| 0000E5H | Extended status control register 2 | ESCR2 | R/W | | 00000100B |
| 0000E6H | Baud rate generator register 20 | BGR20 | R/W | | 00000000B |
| 0000E7H | Baud rate generator register 21 | BGR21 | R/W, R | | 00000000B |
| 0000E8H | Serial mode register 3 | SMR3 | R/W, W | UART (LIN/SCI) 3 | 00000000B |
| 0000E9H | Serial control register 3 | SCR3 | R/W, W | | 00000000B |
| 0000EAH | Reception/transmission data register 3 | RDR3/ TDR3 | R/W | | 00000000B |
| 0000EBH | Serial status register 3 | SSR3 | R/W, R | | 00001000B |
| 0000ECH | Extended communication control register 3 | ECCR3 | R/W, R | | 000000XXB |
| 0000EDH | Extended status control register 3 | ESCR3 | R/W | | 00000100B |
| 0000EEH | Baud rate generator register 30 | BGR30 | R/W | | 00000000B |
| 0000EFH | Baud rate generator register 31 | BGR31 | R/W, R | | 00000000B |
| 001FF0H | Program address detection register 0 | PADR0 | R/W | Address match detection | XXXXXXXXB |
| 001FF1H | Program address detection register 1 | PADR0 | R/W | | XXXXXXXXB |
| 001FF2H | Program address detection register 2 | PADR0 | R/W | | XXXXXXXXB |
| 001FF3H | Program address detection register 3 | PADR1 | R/W | | XXXXXXXXB |
| 001FF4H | Program address detection register 4 | PADR1 | R/W | | XXXXXXXXB |
| 001FF5H | Program address detection register 5 | PADR1 | R/W | | XXXXXXXXB |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 003700H to 0037FFH | Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS" | | | | |
| 003800H to 0038FFH | Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS" | | | | |
| 003900H to 00391FH | (Disabled) | | | | |
| 003920H | PPG0 down counter register | PDCR0 | R | 16-bit PPG0 | 11111111B |
| 003921H | | | | | 11111111B |
| 003922H | PPG0 cycle setting register | PCSR0 | W | | 11111111B |
| 003923H | | | | | 11111111B |
| 003924H | PPG0 duty setting register | PDUT0 | W | 16-bit PPG0 | 00000000B |
| 003925H | | | | | 00000000B |
| 003926H | PPG0 output division setting register | PPGDIV0 | R/W, R | | 11111100B |
| 003927H | (Disabled) | | | | |
| 003928H | PPG1 down counter register | PDCR1 | R | 16-bit PPG1 | 11111111B |
| 003929H | | | | | 11111111B |
| 00392AH | PPG1 cycle setting register | PCSR1 | W | | 11111111B |
| 00392BH | | | | | 11111111B |
| 00392CH | PPG1 duty setting register | PDUT1 | W | | 00000000B |
| 00392DH | | | | | 00000000B |
| 00392EH | PPG1output division setting register | PPGDIV1 | R/W, R | | 11111100B |
| 00392FH | (Disabled) | | | | |
| 003930H | PPG2 down counter register | PDCR2 | R | 16-bit PPG2 | 11111111B |
| 003931H | | | | | 11111111B |
| 003932H | PPG2 cycle setting register | PCSR2 | W | | 11111111B |
| 003933H | | | | | 11111111B |
| 003934H | PPG2 duty setting register | PDUT2 | W | | 00000000B |
| 003935H | | | | | 00000000B |
| 003936H | PPG2 output division setting register | PPGDIV2 | R/W, R | | 11111100B |
| 003937H to 00393FH | (Disabled) | | | | |
| 003940H | Input capture register 4 | IPCP4 | R | Input capture 4/5 | XXXXXXXXB |
| 003941H | | | | | XXXXXXXXB |
| 003942H | Input capture register 5 | IPCP5 | R | | XXXXXXXXB |
| 003943H | | | | | XXXXXXXXB |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 003944H | Input capture register 6 | IPCP6 | R | Input capture 6/7 | XXXXXXXXB |
| 003945H | | | | | XXXXXXXXB |
| 003946H | Input capture register 7 | IPCP7 | R | | XXXXXXXXB |
| 003947H | | | | | XXXXXXXXB |
| 003948H to 00394FH | (Disabled) | | | | |
| 003950H | Minute data register 2/Reload register 2 | TMR2/ TMRLR2 | R/W | 16-bit reload timer 2 | XXXXXXXXB |
| 003951H | | | | | XXXXXXXXB |
| 003952H | Minute data register 3/Reload register 3 | TMR3/ TMRLR3 | R/W | 16-bit reload timer 3 | XXXXXXXXB |
| 003953H | | | | | XXXXXXXXB |
| 003954H to 003957H | (Disabled) | | | | |
| 003958H | Sub second data register | WTBR | R/W | Real time watch timer | XXXXXXXXB |
| 003959H | | | | | XXXXXXXXB |
| 00395AH | | | | | XXXXXXXXB |
| 00395BH | Second data register | WTSR | R/W | | XX000000B |
| 00395CH | Minute data register | WTMR | R/W | | XX000000B |
| 00395DH | Hour data register | WTHR | R/W | | XXX00000B |
| 00395EH | Day data register | WTDR | R/W | | 00X00001B |
| 00395FH | (Disabled) | | | | |
| 003960H | LCD display RAM | VRAM | R/W | LCD controller/ driver | XXXXXXXXB |
| 003961H | | | | | XXXXXXXXB |
| 003962H | | | | | XXXXXXXXB |
| 003963H | | | | | XXXXXXXXB |
| 003964H | | | | | XXXXXXXXB |
| 003965H | | | | | XXXXXXXXB |
| 003966H | | | | | XXXXXXXXB |
| 003967H | | | | | XXXXXXXXB |
| 003968H | | | | | XXXXXXXXB |
| 003969H | | | | | XXXXXXXXB |
| 00396AH | | | | | XXXXXXXXB |
| 00396BH | | | | | XXXXXXXXB |
| 00396CH | | | | | XXXXXXXXB |
| 00396DH | | | | | XXXXXXXXB |
| 00396EH | | | | | XXXXXXXXB |
| 00396FH | | | | | XXXXXXXXB |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 003970H to 003973H | (Disabled) | | | | |
| 003974H | Frequency data register 1 | SGFR1 | R/W | Sound generator 1 | XXXXXXXXB |
| 003975H | Amplitude data register 1 | SGAR1 | R/W | | 00000000B |
| 003976H | Decrement grade register 1 | SGDR1 | R/W | | XXXXXXXXB |
| 003977H | Tone count register 1 | SGTR1 | R/W | | XXXXXXXXB |
| 003978H to 00397FH | (Disabled) | | | | |
| 003980H | PWM1 compare register 0 | PWC10 | R/W | Stepping motor controller 0 | XXXXXXXXB |
| 003981H | | | | | XXXXXXXXB |
| 003982H | PWM2 compare register 0 | PWC20 | R/W | | XXXXXXXXB |
| 003983H | | | | | XXXXXXXXB |
| 003984H | PWM1 select register 0 | PWS10 | R/W | | 00000000B |
| 003985H | PWM2 select register 0 | PWS20 | R/W | | X0000000B |
| 003986H, 003987H | (Disabled) | | | | |
| 003988H | PWM1 compare register 1 | PWC11 | R/W | Stepping motor controller 1 | XXXXXXXXB |
| 003989H | | | | | XXXXXXXXB |
| 00398AH | PWM2 compare register 1 | PWC21 | R/W | | XXXXXXXXB |
| 00398BH | | | | | XXXXXXXXB |
| 00398CH | PWM1 select register 1 | PWS11 | R/W | | 00000000B |
| 00398DH | PWM2 select register 1 | PWS21 | R/W | | X0000000B |
| 00398EH, 00398FH | (Disabled) | | | | |
| 003990H | PWM1 compare register 2 | PWC12 | R/W | Stepping motor controller 2 | XXXXXXXXB |
| 003991H | | | | | XXXXXXXXB |
| 003992H | PWM2 compare register 2 | PWC22 | R/W | | XXXXXXXXB |
| 003993H | | | | | XXXXXXXXB |
| 003994H | PWM1 select register 2 | PWS12 | R/W | | 00000000B |
| 003995H | PWM2 select register 2 | PWS22 | R/W | | X0000000B |
| 003996H, 003997H | (Disabled) | | | | |

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| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 003998H | PWM1 compare register 3 | PWC13 | R/W | Stepping motor controller 3 | XXXXXXXXB |
| 003999H | | | | | XXXXXXXXB |
| 00399AH | PWM2 compare register 3 | PWC23 | R/W | | XXXXXXXXB |
| 00399BH | | | | | XXXXXXXXB |
| 00399CH | PWM1 select register 3 | PWS13 | R/W | | 00000000B |
| 00399DH | PWM2 select register 3 | PWS23 | R/W | | X0000000B |
| 00399EH to 0039A5H | (Disabled) | | | | |
| 0039A6H | Flash write control register 0 | FWR0 | R/W | Flash I/F | 00000000B |
| 0039A7H | Flash write control register 1 | FWR1 | | | 00000000B |
| 0039A8H to 0039BFH | (Disabled) | | | | |
| 0039C0H to 0039DFH | Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS" | | | | |
| 0039E0H to 0039FFH | Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS" | | | | |
| 003A00H to 003AFFH | Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS" | | | | |
| 003B00H to 003BFFH | Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 003C00H to 003CFFH | Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS" | | | | |
| 003D00H to 003DFFH | Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 003E00H to 003EFFH | Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS" | | | | |
| 003F00H to 003FFFH | Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS" | | | | |



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## ■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers(1)**

| Address | | | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003C00H | 003D00H | 003E00H | 003F00H | Control status register | CSR | R/W, R | 00---000B<br>0----0-1B |
| 003C01H | 003D01H | 003E01H | 003F01H | | | | |
| 003C02H | 003D02H | 003E02H | 003F02H | Last event indicator register | LEIR | R/W | --------B<br>000-0000B |
| 003C03H | 003D03H | 003E03H | 003F03H | | | | |
| 003C04H | 003D04H | 003E04H | 003F04H | RX/TX error counter | RTEC | R | 00000000B<br>00000000B |
| 003C05H | 003D05H | 003E05H | 003F05H | | | | |
| 003C06H | 003D06H | 003E06H | 003F06H | Bit timing register | BTR | R/W | -1111111B<br>11111111B |
| 003C07H | 003D07H | 003E07H | 003F07H | | | | |



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**List of Control Registers(2)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 000040H | 000070H | 0039C0H | 0039D0H | Message buffer valid register | BVALR | R/W | 00000000B |
| 000041H | 000071H | 0039C1H | 0039D1H | | | | 00000000B |
| 000042H | 000072H | 0039C2H | 0039D2H | Transmit request register | TREQR | R/W | 00000000B |
| 000043H | 000073H | 0039C3H | 0039D3H | | | | 00000000B |
| 000044H | 000074H | 0039C4H | 0039D4H | Transmit cancel register | TCANR | W | 00000000B |
| 000045H | 000075H | 0039C5H | 0039D5H | | | | 00000000B |
| 000046H | 000076H | 0039C6H | 0039D6H | Transmit complete register | TCR | R/W | 00000000B |
| 000047H | 000077H | 0039C7H | 0039D7H | | | | 00000000B |
| 000048H | 000078H | 0039C8H | 0039D8H | Receive complete register | RCR | R/W | 00000000B |
| 000049H | 000079H | 0039C9H | 0039D9H | | | | 00000000B |
| 00004AH | 00007AH | 0039CAH | 0039DAH | Remote request receive register | RRTRR | R/W | 00000000B |
| 00004BH | 00007BH | 0039CBH | 0039DBH | | | | 00000000B |
| 00004CH | 00007CH | 0039CCH | 0039DCH | Receive overrun register | ROVRR | R/W | 00000000B |
| 00004DH | 00007DH | 0039CDH | 0039DDH | | | | 00000000B |
| 00004EH | 00007EH | 0039CEH | 0039DEH | Receive interrupt enable register | RIER | R/W | 00000000B |
| 00004FH | 00007FH | 0039CFH | 0039DFH | | | | 00000000B |
| 003C08H | 003D08H | 003E08H | 003F08H | IDE register | IDER | R/W | XXXXXXXXB |
| 003C09H | 003D09H | 003E09H | 003F09H | | | | XXXXXXXXB |
| 003C0AH | 003D0AH | 003E0AH | 003F0AH | Transmit RTR register | TRTRR | R/W | 00000000B |
| 003C0BH | 003D0BH | 003E0BH | 003F0BH | | | | 00000000B |
| 003C0CH | 003D0CH | 003E0CH | 003F0CH | Remote frame receive wait register | RFWTR | R/W | XXXXXXXXB |
| 003C0DH | 003D0DH | 003E0DH | 003F0DH | | | | XXXXXXXXB |
| 003C0EH | 003D0EH | 003E0EH | 003F0EH | Transmit interrupt enable register | TIER | R/W | 00000000B |
| 003C0FH | 003D0FH | 003E0FH | 003F0FH | | | | 00000000B |
| 003C10H | 003D10H | 003E10H | 003F10H | Acceptance mask select register | AMSR | R/W | XXXXXXXXB |
| 003C11H | 003D11H | 003E11H | 003F11H | | | | XXXXXXXXB |
| 003C12H | 003D12H | 003E12H | 003F12H | | | | XXXXXXXXB |
| 003C13H | 003D13H | 003E13H | 003F13H | | | | XXXXXXXXB |
| 003C14H | 003D14H | 003E14H | 003F14H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXXB |
| 003C15H | 003D15H | 003E15H | 003F15H | | | | XXXXXXXXB |
| 003C16H | 003D16H | 003E16H | 003F16H | | | | XXXXX---B |
| 003C17H | 003D17H | 003E17H | 003F17H | | | | XXXXXXXXB |
| 003C18H | 003D18H | 003E18H | 003F18H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXXB |
| 003C19H | 003D19H | 003E19H | 003F19H | | | | XXXXXXXXB |
| 003C1AH | 003D1AH | 003E1AH | 003F1AH | | | | XXXXX---B |
| 003C1BH | 003D1BH | 003E1BH | 003F1BH | | | | XXXXXXXXB |



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**List of Message Buffers (ID Registers)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A00H to 003A1FH | 003B00H to 003B1FH | 003700H to 00371FH | 003800H to 00381FH | General-purpose RAM | — | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A20H | 003B20H | 003720H | 003820H | ID register 0 | IDR0 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A21H | 003B21H | 003721H | 003821H | | | | |
| 003A22H | 003B22H | 003722H | 003822H | | | | XXXXX---B XXXXXXXXB |
| 003A23H | 003B23H | 003723H | 003823H | | | | |
| 003A24H | 003B24H | 003724H | 003824H | ID register 1 | IDR1 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A25H | 003B25H | 003725H | 003825H | | | | |
| 003A26H | 003B26H | 003726H | 003826H | | | | XXXXX---B XXXXXXXXB |
| 003A27H | 003B27H | 003727H | 003827H | | | | |
| 003A28H | 003B28H | 003728H | 003828H | ID register 2 | IDR2 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A29H | 003B29H | 003729H | 003829H | | | | |
| 003A2AH | 003B2AH | 00372AH | 00382AH | | | | XXXXX---B XXXXXXXXB |
| 003A2BH | 003B2BH | 00372BH | 00382BH | | | | |
| 003A2CH | 003B2CH | 00372CH | 00382CH | ID register 3 | IDR3 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A2DH | 003B2DH | 00372DH | 00382DH | | | | |
| 003A2EH | 003B2EH | 00372EH | 00382EH | | | | XXXXX---B XXXXXXXXB |
| 003A2FH | 003B2FH | 00372FH | 00382FH | | | | |
| 003A30H | 003B30H | 003730H | 003830H | ID register 4 | IDR4 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A31H | 003B31H | 003731H | 003831H | | | | |
| 003A32H | 003B32H | 003732H | 003832H | | | | XXXXX---B XXXXXXXXB |
| 003A33H | 003B33H | 003733H | 003833H | | | | |
| 003A34H | 003B34H | 003734H | 003834H | ID register 5 | IDR5 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A35H | 003B35H | 003735H | 003835H | | | | |
| 003A36H | 003B36H | 003736H | 003836H | | | | XXXXX---B XXXXXXXXB |
| 003A37H | 003B37H | 003737H | 003837H | | | | |
| 003A38H | 003B38H | 003738H | 003838H | ID register 6 | IDR6 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A39H | 003B39H | 003739H | 003839H | | | | |
| 003A3AH | 003B3AH | 00373AH | 00383AH | | | | XXXXX---B XXXXXXXXB |
| 003A3BH | 003B3BH | 00373BH | 00383BH | | | | |
| 003A3CH | 003B3CH | 00373CH | 00383CH | ID register 7 | IDR7 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A3DH | 003B3DH | 00373DH | 00383DH | | | | |
| 003A3EH | 003B3EH | 00373EH | 00383EH | | | | XXXXX---B XXXXXXXXB |
| 003A3FH | 003B3FH | 00373FH | 00383FH | | | | |

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*(Continued)*

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A40H | 003B40H | 003740H | 003840H | ID register 8 | IDR8 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A41H | 003B41H | 003741H | 003841H | | | | |
| 003A42H | 003B42H | 003742H | 003842H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A43H | 003B43H | 003743H | 003843H | | | | |
| 003A44H | 003B44H | 003744H | 003844H | ID register 9 | IDR9 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A45H | 003B45H | 003745H | 003845H | | | | |
| 003A46H | 003B46H | 003746H | 003846H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A47H | 003B47H | 003747H | 003847H | | | | |
| 003A48H | 003B48H | 003748H | 003848H | ID register 10 | IDR10 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A49H | 003B49H | 003749H | 003849H | | | | |
| 003A4AH | 003B4AH | 00374AH | 00384AH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A4BH | 003B4BH | 00374BH | 00384BH | | | | |
| 003A4CH | 003B4CH | 00374CH | 00384CH | ID register 11 | IDR11 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A4DH | 003B4DH | 00374DH | 00384DH | | | | |
| 003A4EH | 003B4EH | 00374EH | 00384EH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A4FH | 003B4FH | 00374FH | 00384FH | | | | |
| 003A50H | 003B50H | 003750H | 003850H | ID register 12 | IDR12 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A51H | 003B51H | 003751H | 003851H | | | | |
| 003A52H | 003B52H | 003752H | 003852H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A53H | 003B53H | 003753H | 003853H | | | | |
| 003A54H | 003B54H | 003754H | 003854H | ID register 13 | IDR13 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A55H | 003B55H | 003755H | 003855H | | | | |
| 003A56H | 003B56H | 003756H | 003856H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A57H | 003B57H | 003757H | 003857H | | | | |
| 003A58H | 003B58H | 003758H | 003858H | ID register 14 | IDR14 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A59H | 003B59H | 003759H | 003859H | | | | |
| 003A5AH | 003B5AH | 00375AH | 00385AH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A5BH | 003B5BH | 00375BH | 00385BH | | | | |
| 003A5CH | 003B5CH | 00375CH | 00385CH | ID register 15 | IDR15 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A5DH | 003B5DH | 00375DH | 00385DH | | | | |
| 003A5EH | 003B5EH | 00375EH | 00385EH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A5FH | 003B5FH | 00375FH | 00385FH | | | | |



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**List of Message Buffers (DLC Registers)**

| Address | | | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A60H | 003B60H | 003760H | 003860H | DLC register 0 | DLCR0 | R/W | ----XXXXB |
| 003A61H | 003B61H | 003761H | 003861H | | | | |
| 003A62H | 003B62H | 003762H | 003862H | DLC register 1 | DLCR1 | R/W | ----XXXXB |
| 003A63H | 003B63H | 003763H | 003863H | | | | |
| 003A64H | 003B64H | 003764H | 003864H | DLC register 2 | DLCR2 | R/W | ----XXXXB |
| 003A65H | 003B65H | 003765H | 003865H | | | | |
| 003A66H | 003B66H | 003766H | 003866H | DLC register 3 | DLCR3 | R/W | ----XXXXB |
| 003A67H | 003B67H | 003767H | 003867H | | | | |
| 003A68H | 003B68H | 003768H | 003868H | DLC register 4 | DLCR4 | R/W | ----XXXXB |
| 003A69H | 003B69H | 003769H | 003869H | | | | |
| 003A6AH | 003B6AH | 00376AH | 00386AH | DLC register 5 | DLCR5 | R/W | ----XXXXB |
| 003A6BH | 003B6BH | 00376BH | 00386BH | | | | |
| 003A6CH | 003B6CH | 00376CH | 00386CH | DLC register 6 | DLCR6 | R/W | ----XXXXB |
| 003A6DH | 003B6DH | 00376DH | 00386DH | | | | |
| 003A6EH | 003B6EH | 00376EH | 00386EH | DLC register 7 | DLCR7 | R/W | ----XXXXB |
| 003A6FH | 003B6FH | 00376FH | 00386FH | | | | |
| 003A70H | 003B70H | 003770H | 003870H | DLC register 8 | DLCR8 | R/W | ----XXXXB |
| 003A71H | 003B71H | 003771H | 003871H | | | | |
| 003A72H | 003B72H | 003772H | 003872H | DLC register 9 | DLCR9 | R/W | ----XXXXB |
| 003A73H | 003B73H | 003773H | 003873H | | | | |
| 003A74H | 003B74H | 003774H | 003874H | DLC register 10 | DLCR10 | R/W | ----XXXXB |
| 003A75H | 003B75H | 003775H | 003875H | | | | |
| 003A76H | 003B76H | 003776H | 003876H | DLC register 11 | DLCR11 | R/W | ----XXXXB |
| 003A77H | 003B77H | 003777H | 003877H | | | | |
| 003A78H | 003B78H | 003778H | 003878H | DLC register 12 | DLCR12 | R/W | ----XXXXB |
| 003A79H | 003B79H | 003779H | 003879H | | | | |
| 003A7AH | 003B7AH | 00377AH | 00387AH | DLC register 13 | DLCR13 | R/W | ----XXXXB |
| 003A7BH | 003B7BH | 00377BH | 00387BH | | | | |
| 003A7CH | 003B7CH | 00377CH | 00387CH | DLC register 14 | DLCR14 | R/W | ----XXXXB |
| 003A7DH | 003B7DH | 00377DH | 00387DH | | | | |
| 003A7EH | 003B7EH | 00377EH | 00387EH | DLC register 15 | DLCR15 | R/W | ----XXXXB |
| 003A7FH | 003B7FH | 00377FH | 00387FH | | | | |



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**List of Message Buffers (Data register)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A80H to 003A87H | 003B80H to 003B87H | 003780H to 003787H | 003880H to 003887H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A88H to 003A8FH | 003B88H to 003B8FH | 003788H to 00378FH | 003888H to 00388FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A90H to 003A97H | 003B90H to 003B97H | 003790H to 003797H | 003890H to 003897H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A98H to 003A9FH | 003B98H to 003B9FH | 003798H to 00379FH | 003898H to 00389FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AA0H to 003AA7H | 003BA0H to 003BA7H | 0037A0H to 0037A7H | 0038A0H to 0038A7H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AA8H to 003AAFH | 003BA8H to 003BAFH | 0037A8H to 0037AFH | 0038A8H to 0038AFH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AB0H to 003AB7H | 003BB0H to 003BB7H | 0037B0H to 0037B7H | 0038B0H to 0038B7H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AB8H to 003ABFH | 003BB8H to 003BBFH | 0037B8H to 0037BFH | 0038B8H to 0038BFH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AC0H to 003AC7H | 003BC0H to 003BC7H | 0037C0H to 0037C7H | 0038C0H to 0038C7H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AC8H to 003ACFH | 003BC8H to 003BCFH | 0037C8H to 0037CFH | 0038C8H to 0038CFH | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AD0H to 003AD7H | 003BD0H to 003BD7H | 0037D0H to 0037D7H | 0038D0H to 0038D7H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AD8H to 003ADFH | 003BD8H to 003BDFH | 0037D8H to 0037DFH | 0038D8H to 0038DFH | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AE0H to 003AE7H | 003BE0H to 003BE7H | 0037E0H to 0037E7H | 0038E0H to 0038E7H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AE8H to 003AEFH | 003BE8H to 003BEFH | 0037E8H to 0037EFH | 0038E8H to 0038EFH | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AF0H to 003AF7H | 003BF0H to 003BF7H | 0037F0H to 0037F7H | 0038F0H to 0038F7H | Data register 14 (8 bytes) | DTR14 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AF8H to 003AFFH | 003BF8H to 003BFFH | 0037F8H to 0037FFH | 0038F8H to 0038FFH | Data register 15 (8 bytes) | DTR15 | R/W | XXXXXXXXB to XXXXXXXXB |



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## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt source | EI²OS corresponding | Interrupt vector | | | Interrupt control register | | Priority *2 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| Reset | × | #08 | 08H | FFFFDCH | — | — | High |
| INT9 instruction | × | #09 | 09H | FFFFD8H | — | — | |
| Exception processing | × | #10 | 0AH | FFFFD4H | — | — | |
| CAN0 received/CAN2 received | × | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H*1 | |
| CAN0 transmitted/node status/ CAN2 transmitted/node status | × | #12 | 0CH | FFFFCCH | | | |
| CAN1 received/CAN3 received | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H*1 | |
| CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO | × | #14 | 0EH | FFFFC4H | | | |
| Input capture 0 | △ | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H*1 | |
| DTP/ external interrupt - ch.0/ch.1 detected | △ | #16 | 10H | FFFFBCH | | | |
| Reload timer 0 | △ | #17 | 11H | FFFFB8H | ICR03 | 0000B3H*1 | |
| Reload timer 2 | △ | #18 | 12H | FFFFB4H | | | |
| Input capture 1 | △ | #19 | 13H | FFFFB0H | ICR04 | 0000B4H*1 | |
| DTP/ external interrupt - ch.2/ch.3 detected | △ | #20 | 14H | FFFFACH | | | |
| Input capture 2 | △ | #21 | 15H | FFFFA8H | ICR05 | 0000B5H*1 | |
| Reload timer 3 | △ | #22 | 16H | FFFFA4H | | | |
| Input capture 3/4/5/6/7 | △ | #23 | 17H | FFFFA0H | ICR06 | 0000B6H*1 | |
| DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX | △ | #24 | 18H | FFFF9CH | | | |
| PPG timer 0 | △ | #25 | 19H | FFFF98H | ICR07 | 0000B7H*1 | |
| DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX | △ | #26 | 1AH | FFFF94H | | | |
| PPG timer 1 | △ | #27 | 1BH | FFFF90H | ICR08 | 0000B8H*1 | |
| Reload timer 1 | △ | #28 | 1CH | FFFF8CH | | | |
| PPG timer 2/3/4/5 | ○ | #29 | 1DH | FFFF88H | ICR09 | 0000B9H*1 | |
| Real time watch timer watch timer (sub clock) | × | #30 | 1EH | FFFF84H | | | |
| Free-run timer overflow/clear | × | #31 | 1FH | FFFF80H | ICR10 | 0000BAH *1 | |
| A/D converter conversion complete | ○ | #32 | 20H | FFFF7CH | | | |
| Sound generator 0/1 | × | #33 | 21H | FFFF78H | ICR11 | 0000BBH*1 | |
| Time-base timer | × | #34 | 22H | FFFF74H | | | |
| UART2 RX | ○ | #35 | 23H | FFFF70H | ICR12 | 0000BCH*1 | |
| UART2 TX | △ | #36 | 24H | FFFF6CH | | | Low |

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*(Continued)*

| Interrupt source | EI²OS corresponding | Interrupt vector | | | Interrupt control register | | Priority *2 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| UART 1 RX | ◎ | #37 | 25H | FFFF68H | ICR13 | 0000BDH*1 | High |
| UART 1 TX | △ | #38 | 26H | FFFF64H | | | |
| UART 0 RX | ◎ | #39 | 27H | FFFF60H | ICR14 | 0000BEH*1 | |
| UART 0 TX | △ | #40 | 28H | FFFF5CH | | | |
| Flash memory status | × | #41 | 29H | FFFF58H | ICR15 | 0000BFH*1 | |
| Delay interrupt generator module | × | #42 | 2AH | FFFF54H | | | Low |

◎ : Usable, and has expanded intelligent I/O services (EI²OS) stop function
○ : Usable
△ : Usable when interrupt sources sharing ICR are not in use
× : Unusable

*1 : • Peripheral functions that share the ICR register have the same interrupt level.
• If the expanded intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.
• When the expanded intelligent I/O service (EI²OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2 : Priority applies when interrupts of the same level are generated.



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## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} = V_{CC}$*2 |
| | AVRH | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq$ AVRH*2 |
| | $DV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $DV_{CC} = V_{CC}$*2 |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | |
| Maximum clamp current | $I_{CLAMP}$ | – 4 | + 4 | mA | *7 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP} \rvert$ | — | 40 | mA | *7 |
| "L" level maximum output current*4 | $I_{OL1}$ | — | 15 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OL2}$ | — | 40 | mA | P70 to P77 and P80 to P87 |
| "L" level average output current*5 | $I_{OLAV1}$ | — | 4 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OLAV2}$ | — | 30 | mA | P70 to P77 and P80 to P87 |
| "L" level maximum total output current | $\Sigma I_{OL1}$ | — | 100 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OL2}$ | — | 330 | mA | P70 to P77 and P80 to P87 |
| "L" level average total output current | $\Sigma I_{OLAV1}$ | — | 50 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OLAV2}$ | — | 250 | mA | P70 to P77 and P80 to P87 |
| "H" level maximum output current | $I_{OH1}$*4 | — | –15 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OH2}$*4 | — | –40 | mA | P70 to P77 and P80 to P87 |
| "H" level average output current | $I_{OHAV1}$*5 | — | –4 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OHAV2}$*5 | — | –30 | mA | P70 to P77 and P80 to P87 |
| "H" level maximum total output current | $\Sigma I_{OH1}$ | — | –100 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OH2}$ | — | –330 | mA | P70 to P77 and P80 to P87 |
| "H" level average total output current | $\Sigma I_{OHAV1}$*6 | — | –50 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OHAV2}$*6 | — | –250 | mA | P70 to P77 and P80 to P87 |
| Power consumption | $P_D$ | — | 625 | mW | |
| Operating temperature | $T_A$ | – 40 | + 105 | °C | |
| Storage temperature | $T_{STG}$ | – 55 | + 150 | °C | |

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : $AV_{CC}$, AVRH must not exceed $V_{CC}$, and AVRH must not exceed $AV_{CC}$.
When using an evaluation product, $DV_{CC}$ must not exceed $V_{CC}$ (however, $DV_{CC}$ can be set to a higher voltage than $V_{CC}$ when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, $I_{CLAMP}$ is the applicable rating instead of $V_I$.

*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

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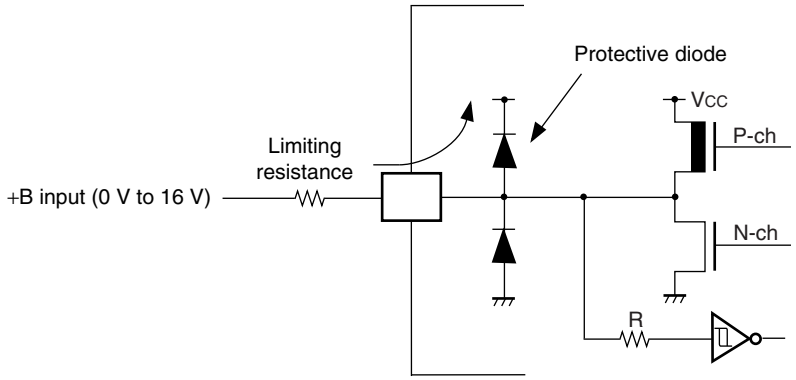
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*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

- Input/output equivalent circuit




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



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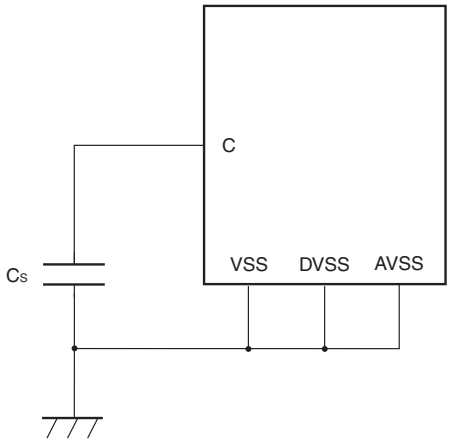
## 2. Recommended Operating Conditions

($V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$<br>$AV_{CC}$<br>$DV_{CC}$ | 4.0 | 5.5 | V | The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| | | 4.4 | 5.5 | V | Maintain stop operation status<br>The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| Smoothing capacitor* | $C_S$ | 0.1 | 1.0 | µF | Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the $V_{CC}$ pin. |
| Operating temperature | $T_A$ | − 40 | + 105 | °C | |

* : Refer to the following diagram for details on the connection of the smoothing capacitor $C_S$.

• C pin connection diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



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### 3. DC Characteristics

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHA}$ | — | — | 0.8 $V_{CC}$ | — | — | V | Pin inputs if Automotive input levels are selected |
| | $V_{IHS}$ | — | — | 0.8 $V_{CC}$ | — | — | V | Pin inputs if CMOS hysteresis input levels are selected |
| | $V_{IHC}$ | — | — | 0.7 $V_{CC}$ | — | — | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| "L" level input voltage | $V_{ILA}$ | — | — | — | — | 0.5 $V_{CC}$ | V | Pin inputs if Automotive input levels are selected |
| | $V_{ILS}$ | — | — | — | — | 0.2 $V_{CC}$ | V | Pin inputs if CMOS hysteresis input levels are selected |
| | $V_{ILR}$ | — | — | — | — | 0.3 $V_{CC}$ | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | Maximum operating frequency $F_{CP}$ = 32 MHz, normal operation | — | 35 | 45 | mA | |
| | | | Maximum operating frequency $F_{CP}$ = 32 MHz, writing Flash memory | — | 55 | 65 | mA | |
| | $I_{CCS}$ | | Operating frequency $F_{CP}$ = 32 MHz, sleep mode | — | 13 | 20 | mA | |
| | $I_{CTS}$ | | Operating frequency $F_{CP}$ = 2 MHz, time-base timer mode | — | 0.6 | 1.0 | mA | |
| | $I_{CTSPLL}$ | | Operating frequency $F_{CP}$ = 32 MHz, PLL timer mode, External frequency = 4 MHz | — | 2.5 | 4 | mA | |
| | $I_{CCL}$ | | Operating frequency $F_{CP}$ = 8 kHz, $T_A$ = + 25 °C, sub clock operation | — | 120 | 270 | µA | |
| | $I_{CCLS}$ | | Operating frequency $F_{CP}$ = 8 kHz, $T_A$ = + 25 °C, sub sleep operation | — | 100 | 200 | µA | |
| | $I_{CCT}$ | | Operating frequency $F_{CP}$ = 8 kHz, $T_A$ = + 25 °C, watch mode | — | 90 | 180 | µA | |
| | $I_{CCH}$ | | $T_A$ = + 25 °C, stop mode | — | 80 | 170 | µA | |

*(Continued)*



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($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current | $I_{IL}$ | All input pins | $V_{CC}$ = $DV_{CC}$ = $AV_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | — | — | 10 | µA | |
| Input capacitance 1 | $C_{IN1}$ | All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87 | — | — | — | 15 | pF | |
| Input capacitance 2 | $C_{IN2}$ | P70 to P77, P80 to P87 | — | — | — | 45 | pF | |
| Pull-up resistance | $R_{UP}$ | $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |
| Pull-down resistance | $R_{DOWN}$ | MD2 | — | — | — | 100 | kΩ | Excluding Flash memory product |
| General-purpose output “H” voltage | $V_{OH1}$ | All pins except P70 to P77, P80 to P87 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Stepping motor output “H” voltage | $V_{OH2}$ | P70 to P77, P80 to P87 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –30.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| General-purpose output “L” voltage | $V_{OL1}$ | All pins except P70 to P77, P80 to P87 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| Stepping motor output “L” voltage | $V_{OL2}$ | P70 to P77, P80 to P87 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 30.0 mA | — | — | 0.55 | V | |
| Stepping motor output phase variation “H” | $\Delta V_{OH}$ | PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –30.0 mA, maximum deviation $V_{OH2}$ | — | — | 90 | mV | |
| Stepping motor output phase variation “L” | $\Delta V_{OL}$ | PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 30.0 mA, maximum deviation $V_{OH2}$ | — | — | 90 | mV | |
| LCD internal divider resistance | $R_{LCD}$ | Between V0 and V1, Between V1 and V2, Between V2 and V3 | — | 50 | 100 | 200 | kΩ | Evaluation product |
| | | | | 8.75 | 12.5 | 17.0 | kΩ | Flash memory product |

*(Continued)*



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*(Continued)*

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| LCDC leakage current | $I_{LCDC}$ | V0 to V3, COMm (m = 0 to 3) , SEGn, (n = 00 to 31) | — | — | — | 5.0 | µA | |
| LCD output impedance | Rvcom | COMn (n = 0 to 3) | — | — | — | 4.5 | kΩ | |
| | Rvseg | SEGn (n = 00 to 31) | — | — | — | 17 | kΩ | |

* : Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.



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## 4. AC Characteristics

### (1) Clock timing

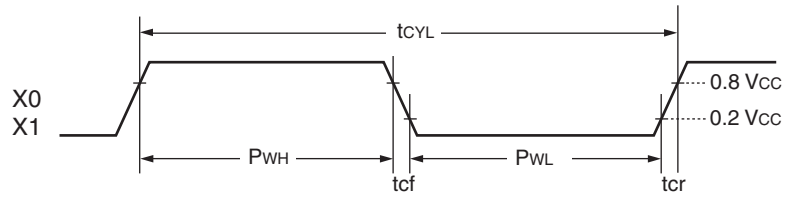
($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Condi-tions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_C$ | X0, X1 | — | 3 | — | 16 | MHz | 1/2 (PLL stopped) When using the oscillator circuit |
| | | | | 3 | — | 32 | MHz | 1/2 (PLL stopped) When using an external clock |
| | | | | 4 | — | 32 | MHz | PLL multiplied by 1 |
| | | | | 3 | — | 16 | MHz | PLL multiplied by 2 |
| | | | | 3 | — | 10.7 | MHz | PLL multiplied by 3 |
| | | | | 3 | — | 8 | MHz | PLL multiplied by 4 |
| | | | | 3 | — | 5.33 | MHz | PLL multiplied by 6 |
| | | | | 3 | — | 4 | MHz | PLL multiplied by 8 |
| | $F_{LC}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | | 62.5 | — | 333 | ns | When using an oscillator |
| | | | | 31.25 | — | 333 | ns | External clock input |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | | 5 | — | — | ns | Use duty ratio of 50% ± 3% as a guideline |
| | $P_{WLH}$, $P_{WLL}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rise and fall time | tcr, tcf | X0 | | — | — | 5 | ns | When using an external clock signal |
| Internal operating clock frequency | $F_{CP}$ | — | | 1.5 | — | 32 | MHz | Using main clock (PLL clock) |
| | $F_{LCP}$ | — | | — | 8.192 | — | kHz | Using sub clock |
| Internal operating clock cycle time | $t_{CP}$ | — | | 31.25 | — | 666 | ns | Using main clock (PLL clock) |
| | $t_{LCP}$ | — | | — | 122.1 | — | µs | Using sub clock |

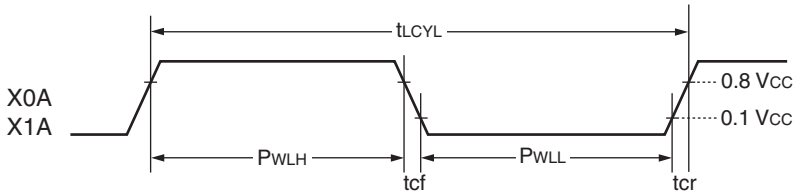


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• X0, X1 clock timing




• X0A, X1A clock timing

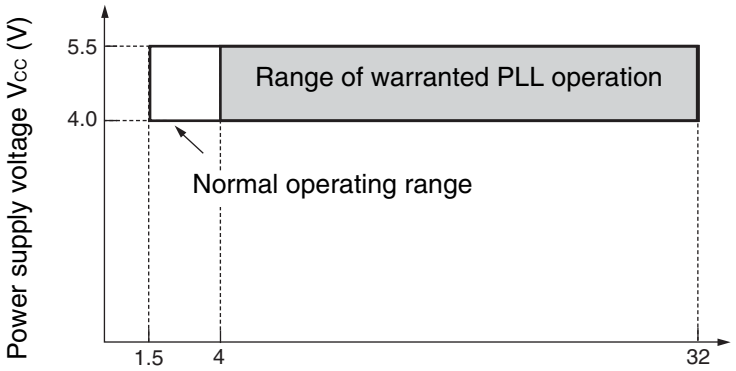





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• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage




Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

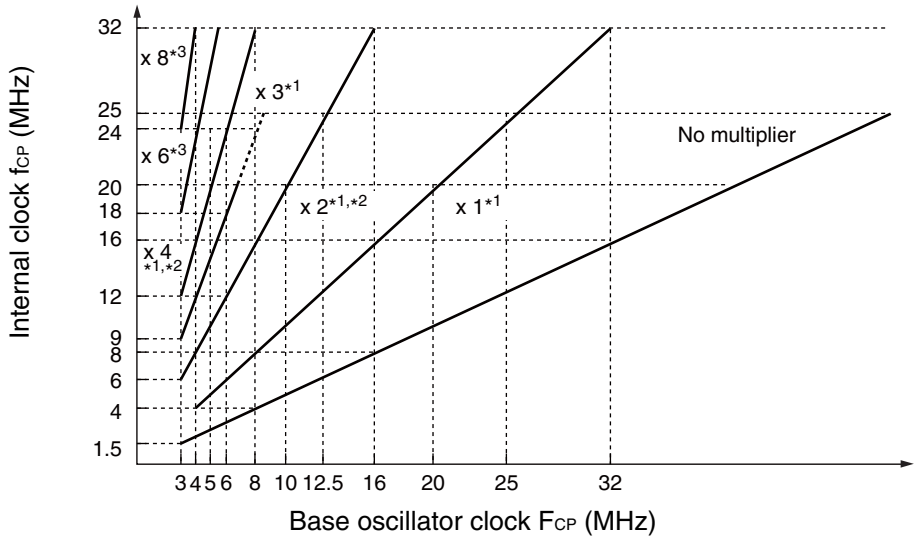
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Base oscillator frequency vs. Internal operating clock frequency




*1 : When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example] When using a base oscillator frequency of 24 MHz at PLL × 1 :
CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4,CS2 bit = "1"
[Example] When using a base oscillator frequency of 6 MHz at PLL × 3 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, the following settings are also supported.
PLL × 2 : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4 : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3 : When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example] When using a base oscillator frequency of 4 MHz at PLL × 6 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"
[Example] When using a base oscillator frequency of 3 MHz at PLL × 8 :
CKSCR register : CS1 bit = "1", CS0 bit = "1"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".



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### (2) Reset input

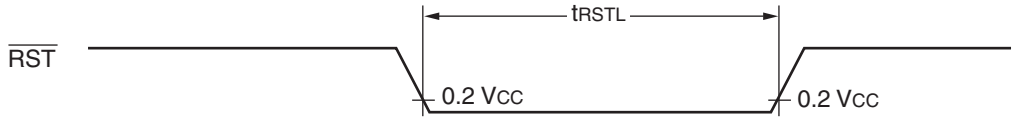
($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500 | — | ns | During normal operation |
| | | | Oscillator oscillation time* + 16 $t_{CP}$ | — | ms | In stop mode, sub clock mode, sub sleep mode, and watch mode |
| | | | 100 | — | µs | In time-base timer mode |

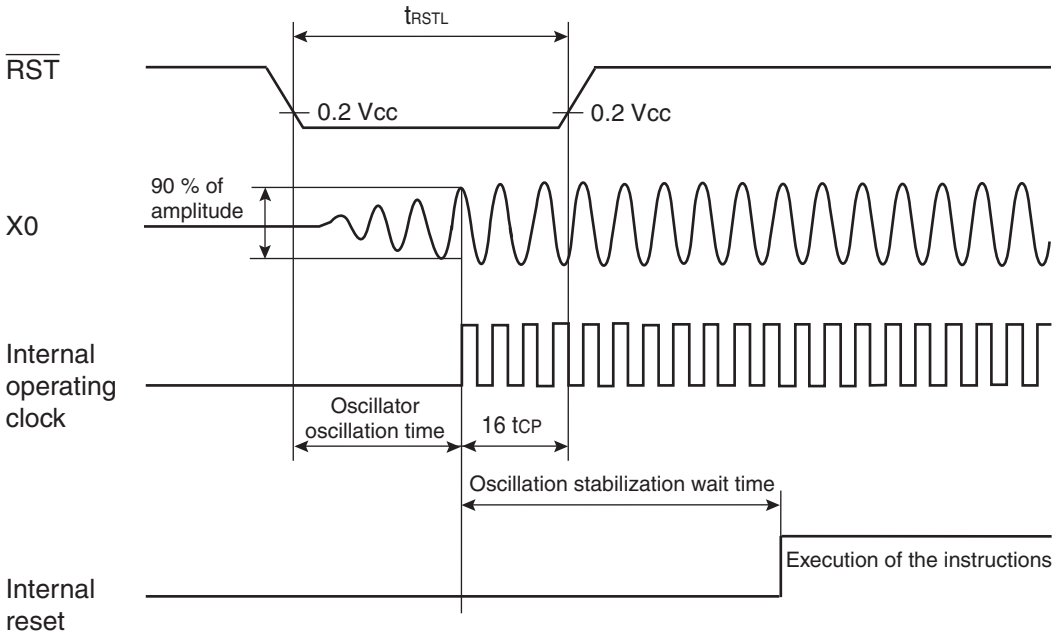
*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

Note : $t_{CP}$ is the internal operating clock cycle time. (Unit : ns)

• During normal operation




• In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



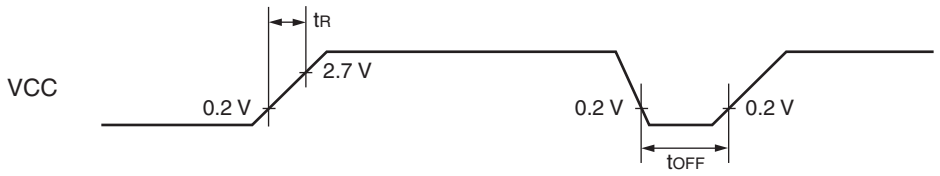



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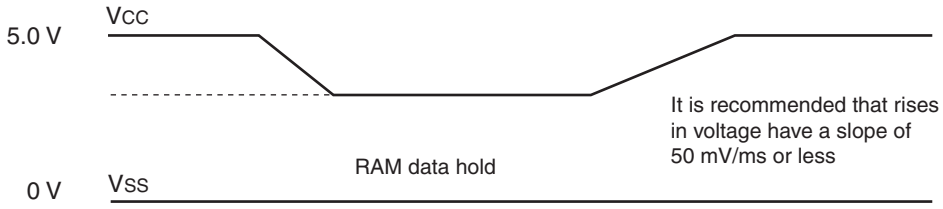
### (3) Power-on reset

($V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rise time | $t_R$ | VCC | — | 0.05 | 30 | ms | |
| Power off time | $t_{OFF}$ | | | 1 | — | ms | Waiting time until power-on |




Note : Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.






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### (4) UART0/1/2/3 (LIN/SCI)

- **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0**

($V_{CC}$ = 5.0 V±10 %, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

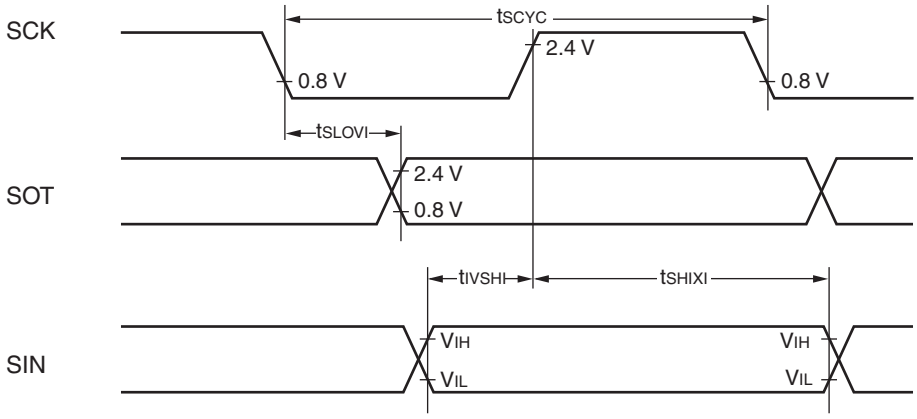
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pin $C_L$ = 80 pF + 1TTL | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | − 50 | + 50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXI}$ | | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK0 to SCK3 | External shift clock mode output pin $C_L$ = 80 pF + 1TTL | 3 $t_{CP}$ − $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | | | $t_{CP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXE}$ | | | $t_{CP}$ + 30 | — | ns |
| SCK ↓ time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK ↑ time | $t_R$ | | | — | 10 | ns |

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• $C_L$ is the load capacitance connected to the pin during testing.
• $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

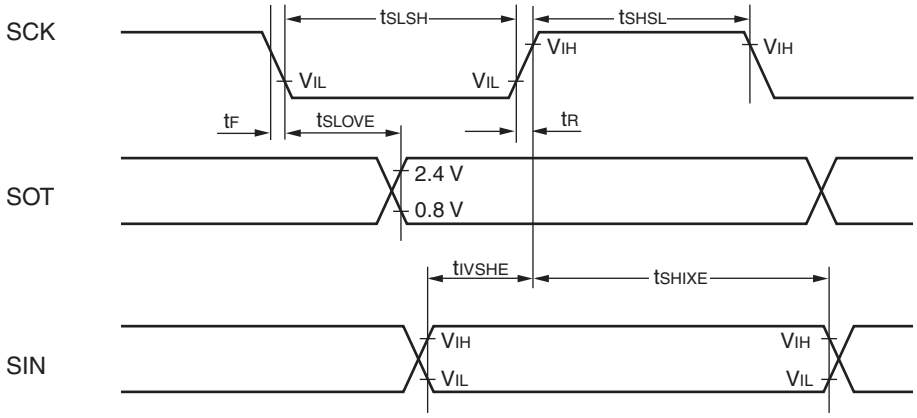


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- Internal shift clock mode




- External shift clock mode






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• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

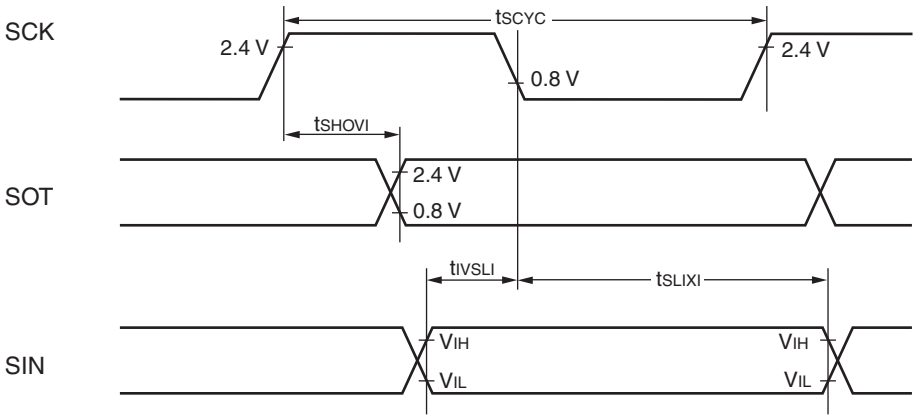
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pin $C_L$ = 80 pF + 1TTL | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | − 50 | + 50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → valid SIN hold time | $t_{SLIXI}$ | | | 0 | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0 to SCK3 | External shift clock mode output pin $C_L$ = 80 pF + 1TTL | 3 $t_{CP}$ − $t_R$ | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | | | $t_{CP}$ + 10 | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↓ → valid SIN hold time | $t_{SLIXE}$ | | | $t_{CP}$ + 30 | — | ns |
| SCK ↓ time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK ↑ time | $t_R$ | | | — | 10 | ns |

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- $C_L$ is the load capacitance connected to the pin during testing.
- $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

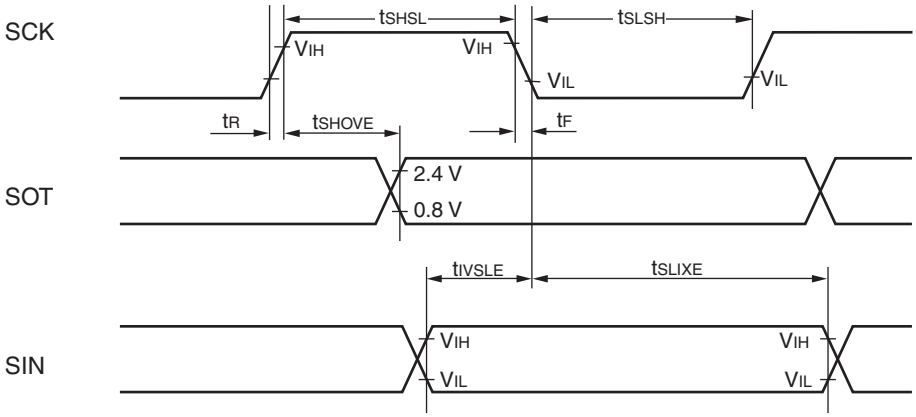


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- Internal shift clock mode




- External shift clock mode





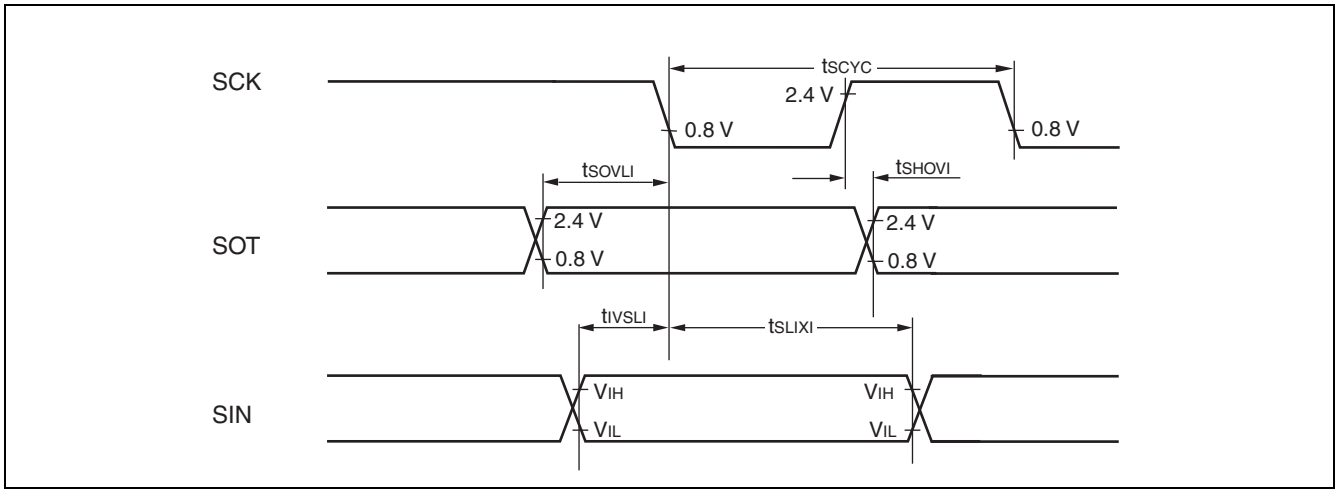

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• **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pin $C_L$ = 80 pF + 1TTL | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | – 50 | + 50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → valid SIN hold time | $t_{SLIXI}$ | | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• $C_L$ is the load capacitance connected to the pin during testing.
• $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.





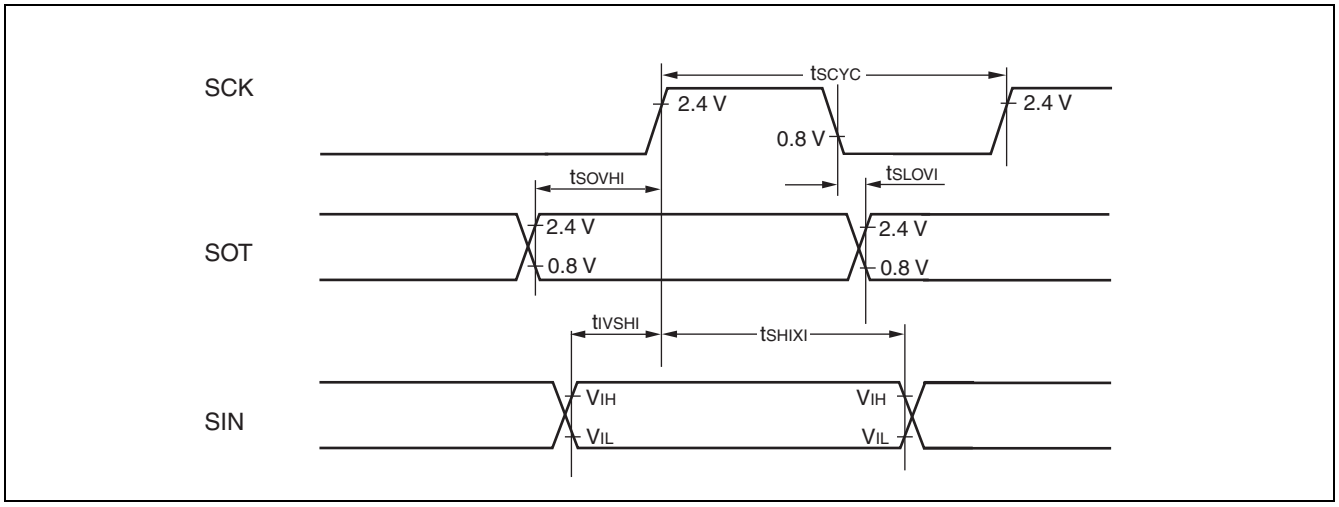

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• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pin $C_L$ = 80 pF + 1TTL | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | – 50 | + 50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXI}$ | | | 0 | — | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- $C_L$ is the load capacitance connected to the pin during testing.
- $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.






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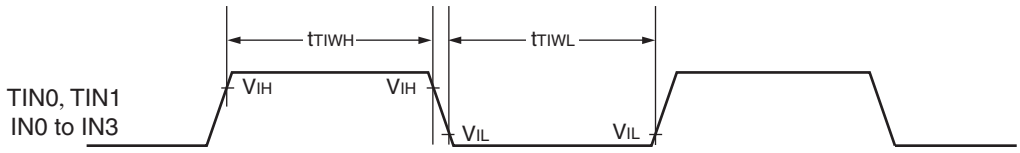
### (5) Timer input timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN0, TIN1,<br>IN0 to IN3 | — | 4 $t_{CP}$ | — | ns |

Note : $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Timer input timing






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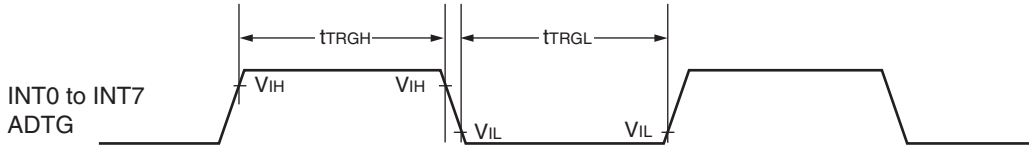
### (6) Trigger input timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | INT0 to INT7 | — | 200 | — | ns | During normal operation |
| | | ADTG | — | $t_{CP}$ + 200 | — | ns | |

Note : $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Trigger input timing



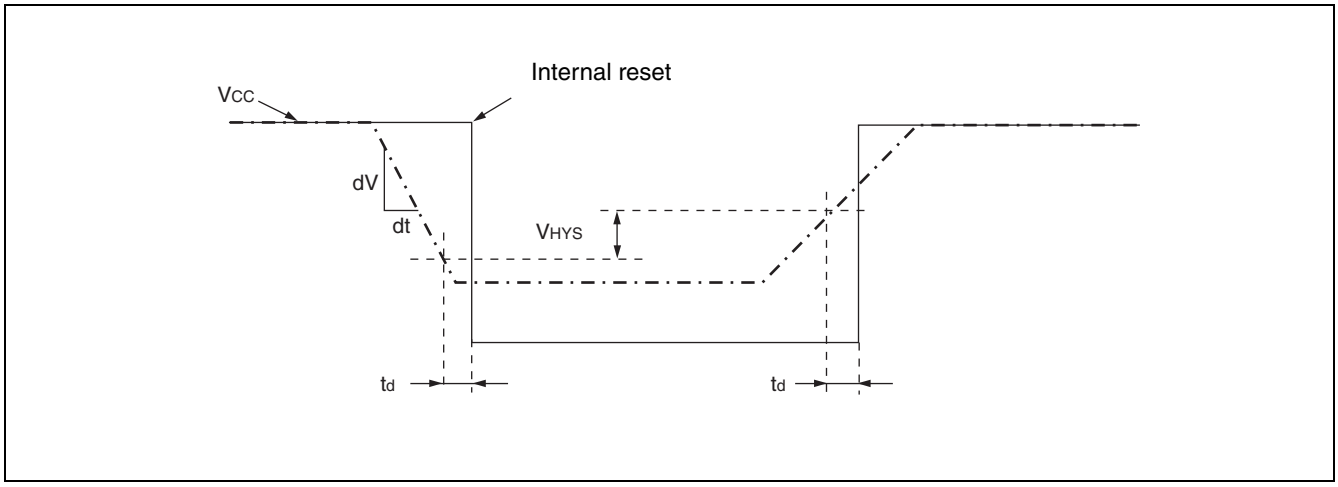



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### (7) Low voltage detection

($V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Detection voltage | $V_{DL}$ | VCC | — | 4.0 | 4.2 | 4.4 | V | Flash memory product, during voltage drop |
| | | | | 3.7 | 4.0 | 4.3 | V | Evaluation product, during voltage drop |
| Hysteresis width | $V_{HYS}$ | VCC | — | 190 | — | — | mV | Flash memory product, during voltage rise |
| | | | | 0.1 | — | — | V | Evaluation product, during voltage rise |
| Power supply voltage change rate | dV/dt | VCC | — | – 0.1 | — | + 0.1 | V/µs | Flash memory product, dV/dt at low voltage reset |
| | | | | –0.004 | — | + 0.004 | V/µs | Flash memory product, dV/dt at standard value of low voltage detection/release voltage |
| | | | | – 0.1 | — | + 0.02 | V/µs | Evaluation product |
| Detection delay time | td | — | — | — | — | 3.2 | µs | Flash memory product, when dV/dt ≤ 0.004 V/µs |
| | | | | — | — | 35 | µs | Evaluation product |






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## 5. A/D Converter

### (1) Electrical Characteristics

($V_{CC}$ = $AV_{CC}$ = AVRH = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | – 3.0 | — | + 3.0 | LSB | |
| Non-linear error | — | — | – 2.5 | — | + 2.5 | LSB | |
| Differential linear error | — | — | – 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | V | 1 LSB = (AVRH – $AV_{SS}$) / 1024 |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH – 3.5 LSB | AVRH – 1.5 LSB | AVRH + 0.5 LSB | V | |
| Sampling time | $t_{SMP}$ | — | 0.4 | — | 16500 | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 1.0 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| Compare time | $t_{CMP}$ | — | 0.66 | — | — | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 2.2 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| A/D conversion time | $t_{CNV}$ | — | 1.44 | — | — | µs | *1 |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | – 0.3 | — | + 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | 0 | — | AVRH | V | |
| Reference voltage | AV+ | AVRH | AVss + 2.7 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 2.3 | 6.0 | mA | |
| | $I_{AH}$ | | — | — | 5 | µA | *2 |
| Reference voltage supply current | $I_R$ | AVRH | — | 520 | 900 | µA | $V_{AVRH}$ = 5.0 V |
| | $I_{RH}$ | | — | — | 5 | µA | *2 |
| Inter-channel variation | — | AN0 to AN7 | — | — | 4 | LSB | |

*1 : The time per channel (4.5 V ≤ $AV_{CC}$ ≤ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when $V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

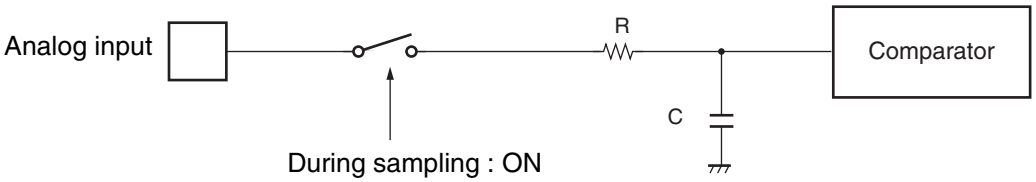


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• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.
If the sampling time is still not sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

• Analog input equivalent circuit




MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

| | R | C |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.6 kΩ (Max) | 8.5 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 12.1 kΩ (Max) | 8.5 pF (Max) |

MB90V920-101/102

| | | |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.0 kΩ (Max) | 14.4 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 8.2 kΩ (Max) | 14.4 pF (Max) |

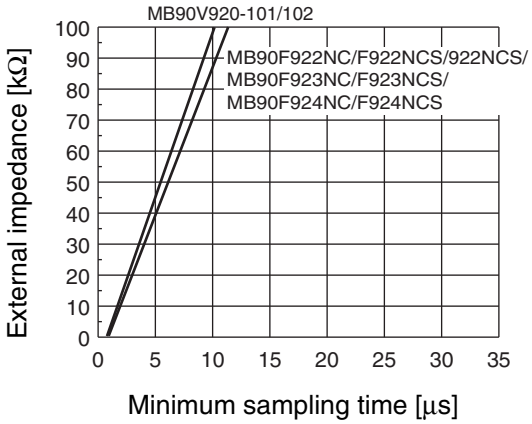
Note : The values are reference values.



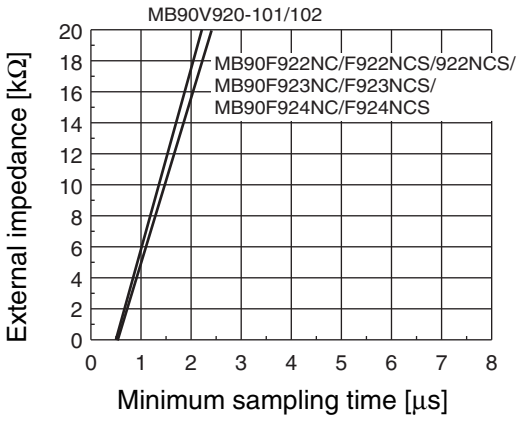
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- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

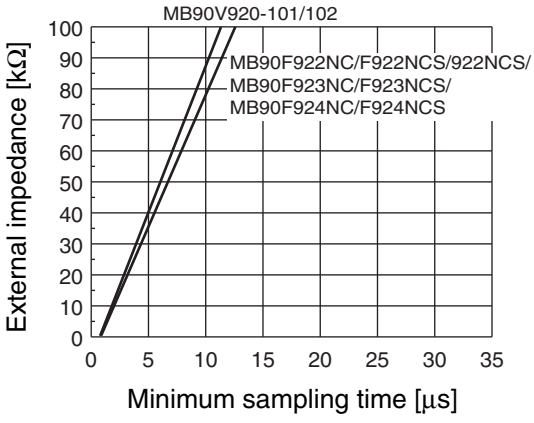



(External impedance = 0 kΩ to 20 kΩ)

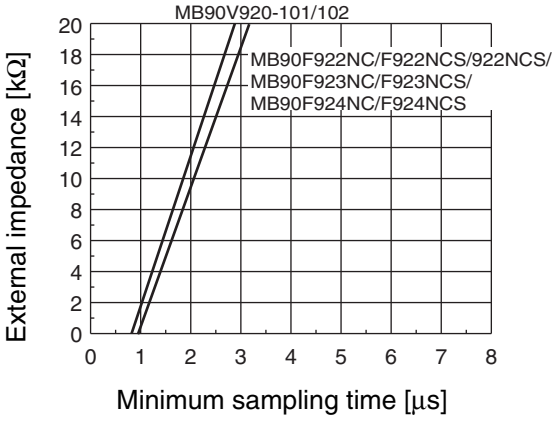



- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)




- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.



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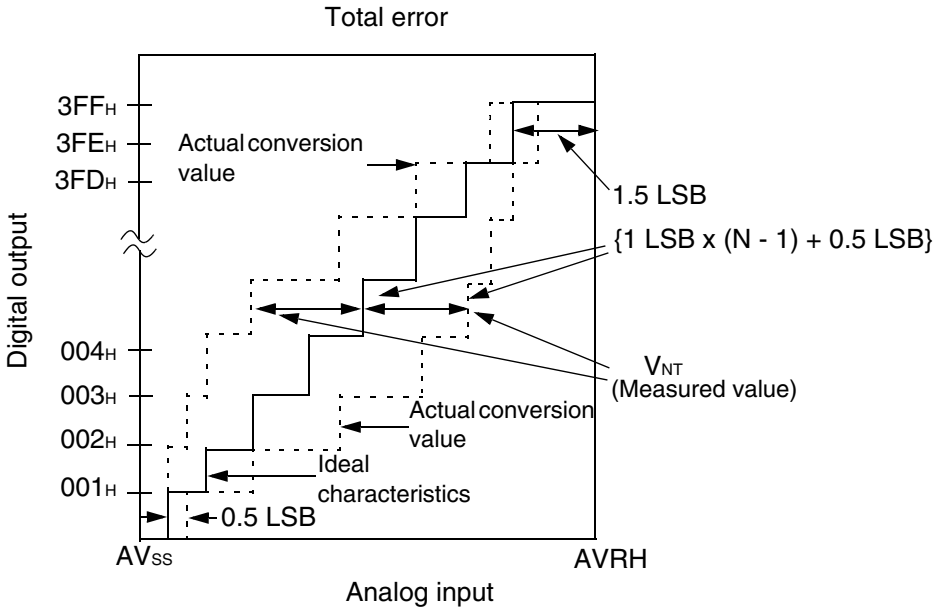
**(2) Definition of terms**

Resolution : Analog changes that are identifiable by the A/D converter.

Non-Linear error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ←→ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111") from actual conversion characteristics.

Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.

Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.




$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal)} = \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

$V_{OT}$ (Ideal) = AVss + 0.5 LSB [V]

$V_{FST}$ (Ideal) = AVRH − 1.5 LSB [V]

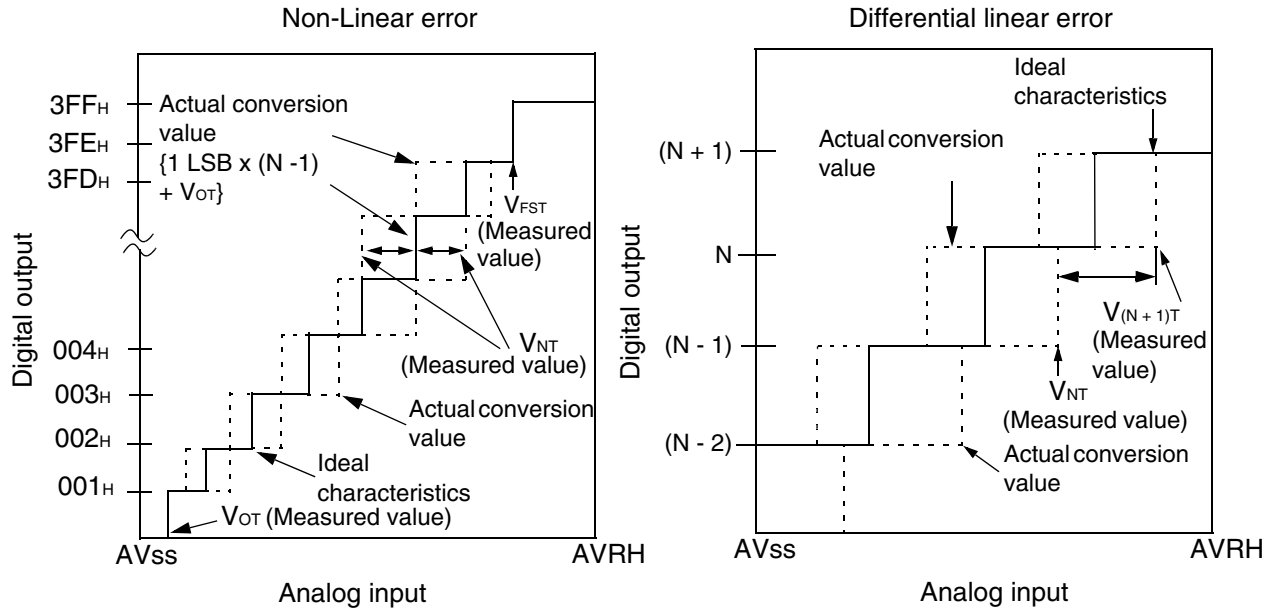
$V_{NT}$ : Voltage when the digital output changes from (N - 1) to N

*(Continued)*



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*(Continued)*




$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
$V_{OT}$ : Voltage when digital output changes from $000_H$ to $001_H$
$V_{FST}$ : Voltage when digital output changes from $3FE_H$ to $3FF_H$



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## 6. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | — | 0.9 | 3.6 | s | Excludes pre-programming before erase |
| Word (16-bit width) programming time | | — | 23 | 370 | µs | Excludes system-level overhead |
| Chip programming time | $T_A$ = + 25 °C,<br>$V_{CC}$ = 5.0 V | — | 3.4 | 55 | s | |
| Erase/program cycle | — | 10000 | — | — | cycle | |
| Flash memory data retention time | Average<br>$T_A$ = + 85 °C | 20 | — | — | year | * |

* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .



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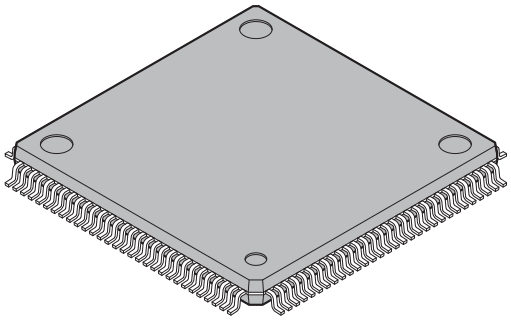
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F922NCPMC<br>MB90F922NCSPMC<br>MB90922NCSPMC<br>MB90F923NCPMC<br>MB90F923NCSPMC<br>MB90F924NCPMC<br>MB90F924NCSPMC | 120-pin plastic LQFP<br>(FPT-120P-M21) | |
| MB90V920-101CR<br>MB90V920-102CR | 299-pin ceramic PGA<br>(PGA-299C-A01) | For evaluation |



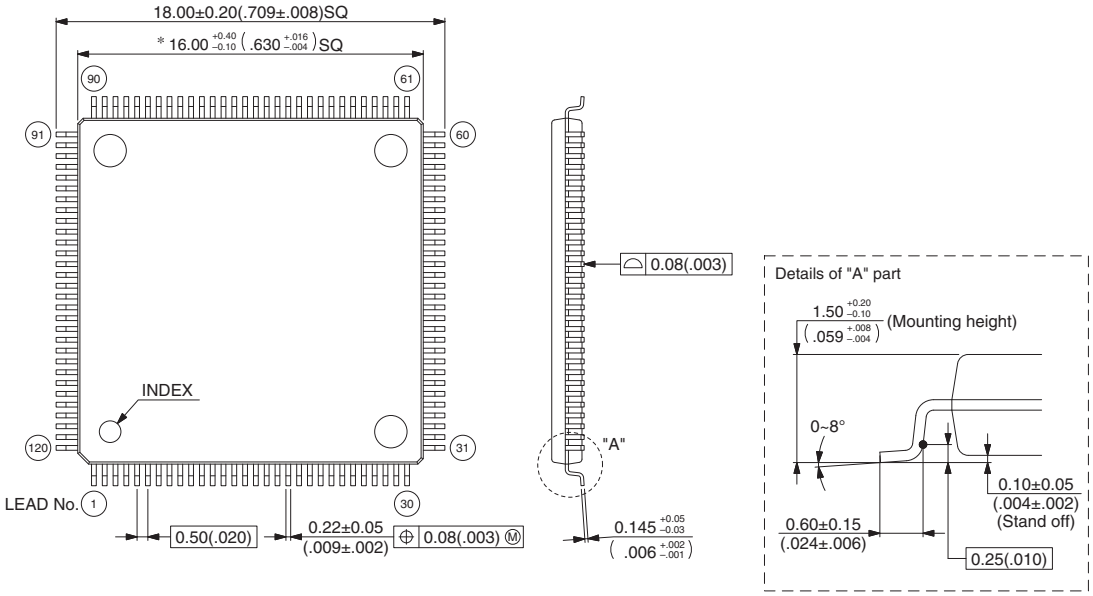
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## ■ PACKAGE DIMENSION

| 120-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 16.0 × 16.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.88 g |
| (FPT-120P-M21) | Code (Reference) | P-LFQFP120-16×16-0.50 |

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.




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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/



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## ■ MAJOR CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 12 | ■I/O CIRCUIT TYPE | Corrected the circuit type B. |
| 20 | ■ HANDLING DEVICES | Added the following items;<br>• Serial communication<br>• Characteristic difference between flash device and MASK ROM device |
| 31 | ■ I/O MAP | Corrected “Address: 003970$_H$”.<br>Clock supervisor control register → (Disabled) |
| 46 | ■ ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics | Added the item for “LCD output impedance”. |
| 68 | ■ ORDERING INFORMATION | Corrected the part numbers;<br>MB90V920-101 → MB90V920-101CR<br>MB90V920-102 → MB90V920-102CR |

The vertical lines marked in the left side of the page show the changes.



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# MEMO



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# MB90920 Series


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