ROHM SEMICONDUCTOR



STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCTNAME BU7961GUW

FUNCTION Serial Interface for Mobile Devices Application

MSDL3(Mobile Shrink Data Link 3) Serializer LSI

FEATURES
·Maximum transmission rate of highspeed differential interface MSDL3 is 900Mbps.
·Support LCD interface with 24bit parallel RGB video mode.
·Pixel clock frequency is 4~30MHz.

1. Absolute maximum

| Parameter | Symbol | Rated values | Unit | Remarks |
|---|---|---|---|---|
| Power supply voltage for IOVDD | IOVDD | -0.3 ~ +4.5 | V | |
| Power supply voltage for DVDD | DVDD | -0.3 ~ +2.5 | V | |
| Power supply voltage for MSVDD | MSVDD | -0.3 ~ +2.5 | V | |
| Input voltage | VIN | -0.3 ~ IOVDD+0.3 | V | I/O terminals of IOVDD line |
| | | -0.3 ~ +3.6 | V | XSD terminal |
| | | -0.3 ~ MSVDD+0.3 | V | I/O terminals of MSVDD line |
| Input current | IIN | -10 ~ +10 | mA | |
| Package power dissipation | Pd | 300 * | mW | Without board mounted |
| Preservation temperature | Tstg | -55 ~ +125 | °C | |

*When it uses by Ta=25°C or higher, reduce by 3.0 mW/°C (for a single package).

2. Operating Condition

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply voltage for IOVDD | VIOVDD | 1.65 | 1.80 | 3.60 | V | VDVDD=VMSVDD≤VIOVDD |
| Supply voltage for DVDD | VDVDD | 1.65 | 1.80 | 1.95 | V | |
| Supply voltage for MSVDD | VMSVDD | 1.65 | 1.80 | 1.95 | V | |
| PCLK frequency | fPCLK | 4.0 | - | 30.0 | MHz | |
| Operating temperature range | Topr | -30 | 25 | +85 | °C | |

These goods are specific machines. Because the exclusive goods which are specially designed for the device are considered. Whether that machine, device corresponds to strategic goods to decide as the foreign exchange and foreign trade control law. You must have it judged.
As for contents of mention of these materials. A service in the foreign exchange and foreign trade control law (Technology in the design, the manufacture and the use). Be careful of handling because it is likely to correspond.
This product is not designed against radioactive ray.



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3. ELECTRICAL CHARACTERISTICS

### 3.1 CMOS INOUT CHARACTERISTICS

Ta=25℃, DVDD=MSVDD=1.80V, IOVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions | |
|---|---|---|---|---|---|---|---|
| 'L' input voltage1 | VIL1 | DGND | - | 0.3*IOVDD | V | PCLK, PD[26:0], POL_PCLK, PLL_BW[1:0], LS0, RVS, TEST3 terminals | |
| 'H' input voltage1 | VIH1 | 0.7*IOVDD | - | IOVDD | V | | |
| 'L' input voltage2 | VIL2 | MSGND | - | 0.3*MSVDD | V | LS1 terminal | |
| 'H' input voltage2 | VIH2 | 0.7*MSVDD | - | MSVDD | V | | |
| 'H' input voltage3 | VIH3 | 0.7*IOVDD | - | 3.6 | V | XSD terminal | |
| 'L' output voltage1 | VOL1 | DGND | - | 0.3*IOVDD | V | IO=1mA | CKD terminal |
| 'H' output voltage1 | VOH1 | 0.7*IOVDD | - | IOVDD | V | IO=-1mA | |
| 'L' output voltage2 | VOL2 | MSGND | - | 0.3*MSVDD | V | IO=1mA | LS_EN terminal |
| 'H' output voltage2 | VOH2 | 0.7*MSVDD | - | MSVDD | V | IO=-1mA | |
| PCLK frequency1 | fPCLK1 | 4.0 | - | 15.0 | MHz | LS0=L | PCLK terminal |
| PCLK frequency2 | fPCLK2 | 8.0 | - | 30.0 | MHz | LS0=H | |
| PCLK duty cycle | DPCLKI | 33 | - | 67 | % | PCLK terminal | |
| Data setup to PCLK | tDSI | 5.0 | - | - | ns | PD[26:0] terminals | |
| Data hold to PCLK | tDHI | 5.0 | - | - | ns | | |

### 3.2 MSDL3 TX CHARACTERISTICS

Ta=25℃, DVDD=MSVDD=1.80V, IOVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Differential voltage range | Vdiff_tx | 100 | 150 | 200 | mVpp | |
| Common mode voltage range | Vcm_tx | 0.8 | 0.9 | 1.0 | V | |
| SubLVDS data rate | DR_tx | 120 | - | 450 | Mbps/ch | |

### 3.3 CURRENT COMSUMPTION

Ta=25℃, DVDD=MSVDD=1.80V, IOVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Shutdown current | Iop_sht_tx | - | 0.2 | 10.0 | μA | XSD=L, PCLK=L |
| Standby current | Iop_stb_tx | - | 0.2 | 10.0 | μA | XSD=H, PCLK=L |
| Active current of 1ch27bit format | Iop_act_tx1 | - | 14.0 | 18.5 | mA | LS[1:0]=LL, PLL_BW[1:0]=HL, fPCLK=15MHz, *1 |
| Active current of 2ch27bit format | Iop_act_tx2 | - | 19.7 | 25.7 | mA | LS[1:0]=LH, PLL_BW[1:0]=HL, fPCLK=30MHz, *1 |
| Active current of 1ch13bit format | Iop_act_tx3 | - | 16.3 | 21.3 | mA | LS[1:0]=HH, PLL_BW[1:0]=HL, fPCLK=30MHz, *2 |

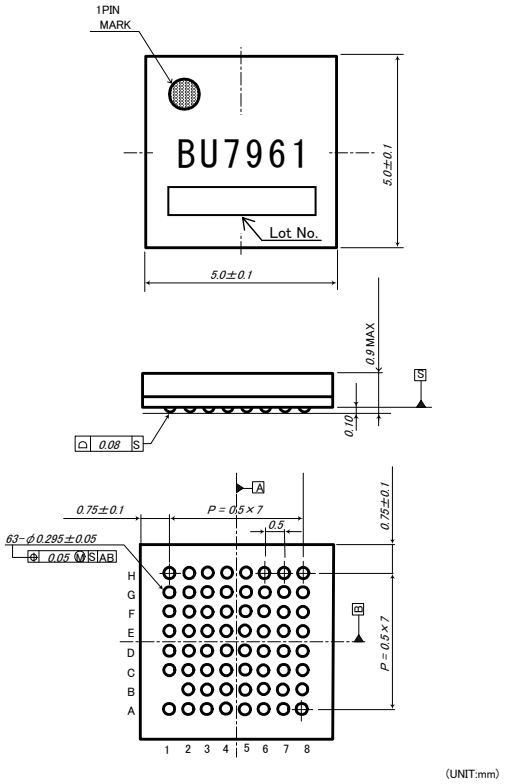
*1 : Total operating current(IDVDD+IMSVDD+IIOVDD) with PD[26:0] inputs toggling 0x2AAAAAA and 0x5555555.

*2 : Total operating current(IDVDD+IMSVDD+IIOVDD) with PD[26:15],PD[2] inputs toggling 0x0AAA and 0x1555.



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## 4. PACKAGE VIEW

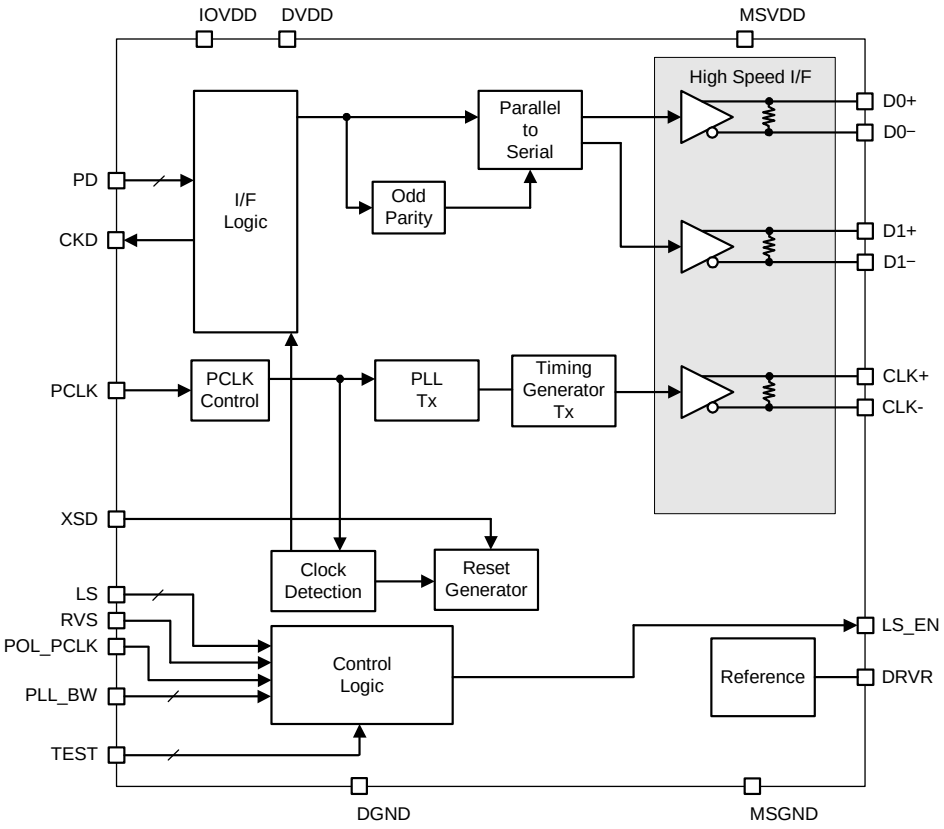



VBGA063W050

## 5. PIN LIST

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---|---|---|---|---|---|
| A1 | TEST0 | D1 | PD22 | G1 | CKD |
| A2 | PD18 | D2 | PD20 | G2 | RVS |
| A3 | PD16 | D3 | POL_PCLK | G3 | DRVR |
| A4 | PD15 | D4 | DGND | G4 | MSGND |
| A5 | PD13 | D5 | DGND | G5 | MSVDD |
| A6 | PD12 | D6 | IOVDD | G6 | LS1 |
| A7 | PD9 | D7 | PD3 | G7 | LS_EN |
| A8 | TEST2 | D8 | PD4 | G8 | XSD |
| B1 | | E1 | PD24 | H1 | TESTA |
| B2 | PCLK | E2 | PD23 | H2 | D1+ |
| B3 | PD17 | E3 | IOVDD | H3 | D1- |
| B4 | PD14 | E4 | DGND | H4 | CLK+ |
| B5 | PD11 | E5 | MSGND | H5 | CLK- |
| B6 | PD10 | E6 | PLL_BW0 | H6 | DO+ |
| B7 | PD8 | E7 | PD0 | H7 | D0- |
| B8 | PD7 | E8 | PD2 | H8 | TEST1 |
| C1 | PD21 | F1 | PD25 | | |
| C2 | PD19 | F2 | PD26 | | |
| C3 | DVDD | F3 | MSVDD | | |
| C4 | IOVDD | F4 | MSGND | | |
| C5 | TEST3 | F5 | MSVDD | | |
| C6 | DVDD | F6 | LS0 | | |
| C7 | PD6 | F7 | PLL_BW1 | | |
| C8 | PD5 | F8 | PD1 | | |

## 6. SYSTEM BLOCK DIAGRAM






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## 7. USAGE PRECAUTIONS

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operatingconditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals

In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.



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