HIGHLY INTEGRATED INTELLIGENT USB PD DECODER WITH EMBEDDED SR CONTROLLER

Description

The DIODES™ AP43671 is a highly integrated and intelligent USB Type-C power delivery (PD) controller with an embedded synchronous rectification (SR) controller. It is ideally targeted for cost-performance-sensitive USB Type-C adaptors and charger applications.

The device supports USB PD3. 0 V1.2, and Programmable Power Supply (PPS) and Qualcomm QC4/QC4+ protocols. Leveraging its embedded MCU and supporting circuitry, the AP43671 can accommodate popular quick-charging protocols for firmware stored in One-Time-Programmable (OTP) memory.

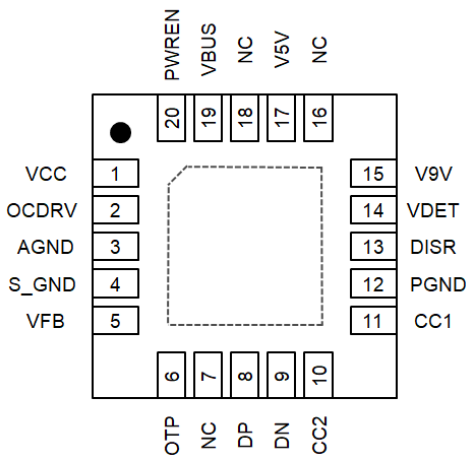
To enable optimal system BOM and performance implementation of quick chargers, the AP43671 embeds a multiple-mode adaptive SR controller where its key performance and safety parameters can be fine-tuned by a built-in MCU.

The AP43671 also adopts a relatively small current-sensing resistor (5mΩ) that is used to provide accurate current measurements without sacrificing power consumption.

The AP43671 provides robust protection schemes, which includes a CC1/CC2 short protection against VBUS (up to 24V) as well as built-in OVP/OCP/SCP/OTP features to provide necessary safety protection.

Pin Assignments

(Top View)



W-QFN4040-20 (Type A1)

Features

- Supports USB PD3.0 Programmable Power Supply (PPS)
- USB-IF PD3.0/PPS Certificated TID = 4999
- Compatible with QC4/QC4+ protocol
- MCU-based implementation for protocol decoding, application firmware, parameter fine-tuning and calibration.
- OTP (One-Time-Programmable) for main protocol and application firmware
- MTP (Multi-Time-Programmable) for system configuration options
- Built-in regulator for CV and CC control, no need for external CC/CV reference circuitry
- Ultra-low current consumption (550uA) at sleep mode
- Supports power-saving mode to enable low standby power of chargers
- Embed Synchronous Rectification (SR) Controller, which supports Adaptive Quasi-Resonant (QR) and Continuous Conduction Mode (CCM) for matching PWM controllers.
- Small current-sensing resistor (5 mΩ) for efficiency improvement
- Adaptive gate drive for external N-MOSFET output enable switch
- Supports e-marker cable detection and V_{CONN} power (20mA)
- Supports SCP/OTP/OVP/UVP with auto-restart
- CC1/CC2 pins shorted to VBUS protection up to 24V
- Minimum system BOM components for quick charger implementations.
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Battery chargers for smart phones, table PCs, and any USB Type-C PD-equipped mobile devices
- Wall and travel chargers for AC-DC adaptors (USB Type-C-equipped Notebook PCs)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

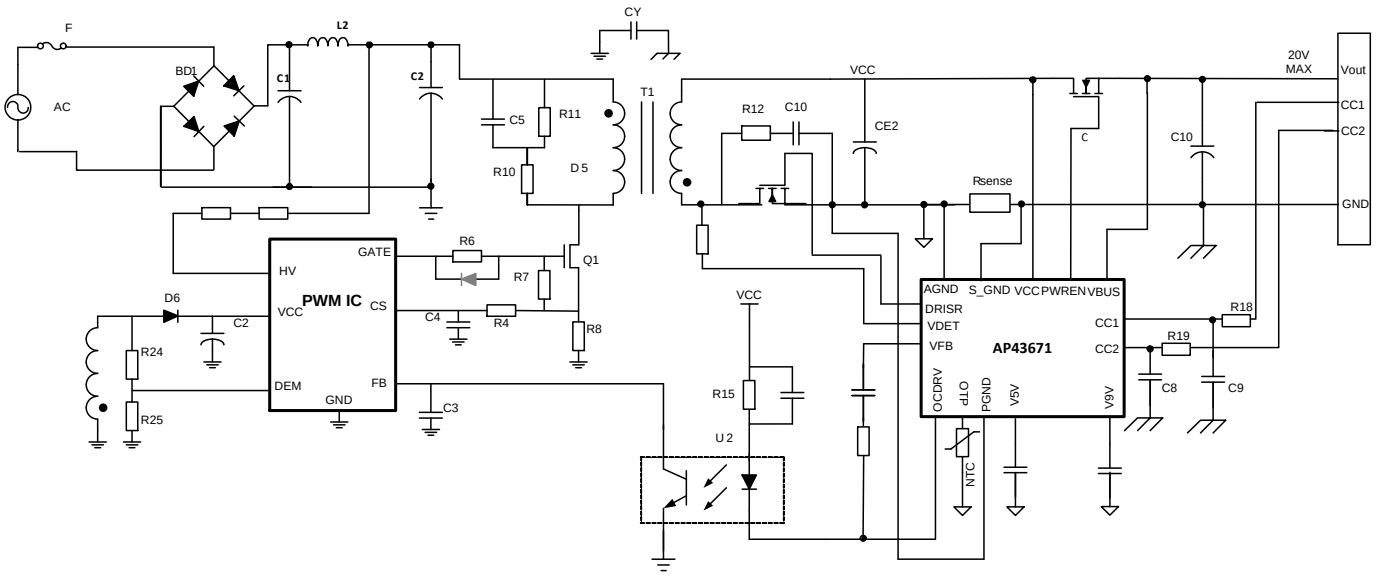


Figure 1. Typical Application Circuit of AP43671 for PD3.0 PPS Charger

Pin Descriptions

Pin Number	Pin Name	Function
1	VCC	The power supply of the IC, which also is input Current Sense Negative Node
2	OCDRV	CC/CV Output. Open Drain Output for Opto-Coupler.
3	AGND	Analog Ground
4	S_GND	System reference ground.
5	VFB	CV Input. Negative Node of CV OPAMP for Opto-Coupler.
6	OTP	Source Current to External NTC Sensor for overtemperature protection (OTP).
7	NC	No Connect (Keep floating)
8	DP	USB Type-C_DP
9	DN	USB Type-C_DN
10	CC2	USB Type-C_CC2
11	CC1	USB Type-C_CC1
12	PGND	Ground of SR controller
13	DISR	Gate Driver of SR MOS;
14	VDET	Sync signal of SR controller; connecting to SR MOS Drain node with a series resistor
15	V9V	Power for SR gate driver
16	NC	No Connect
17	V5V	LDO -5V Output
18	NC	No Connect
19	VBUS	Output Terminal for Discharge Path
20	PWREN	To drive external NMOS VBUS Switch

Functional Block Diagram

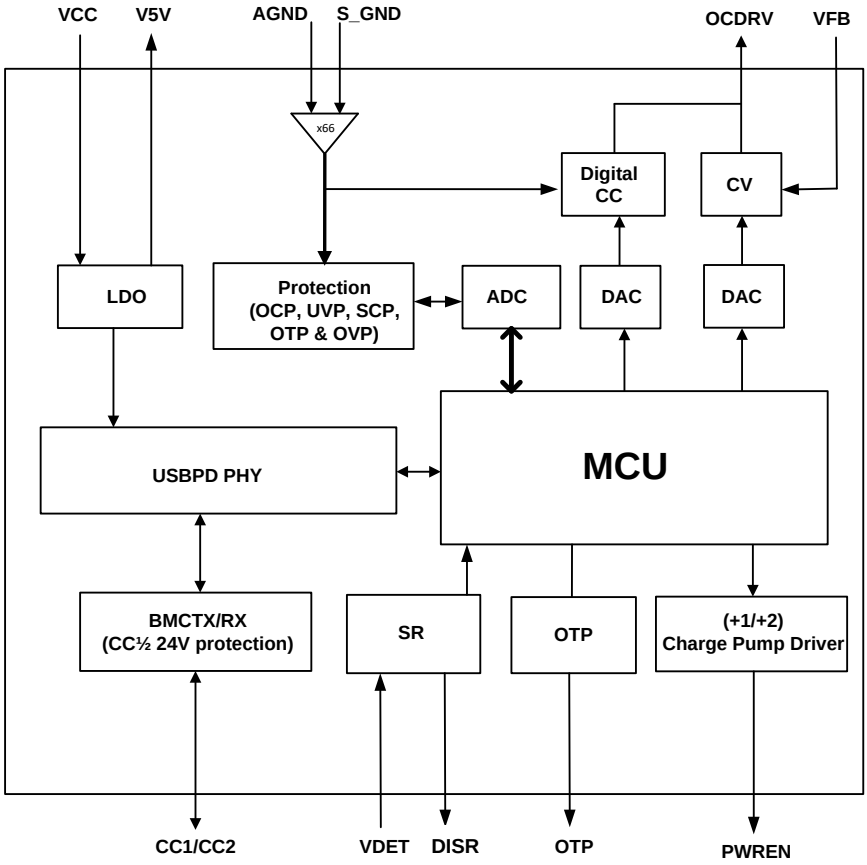


Figure 2. Functional Block Diagram of AP43671

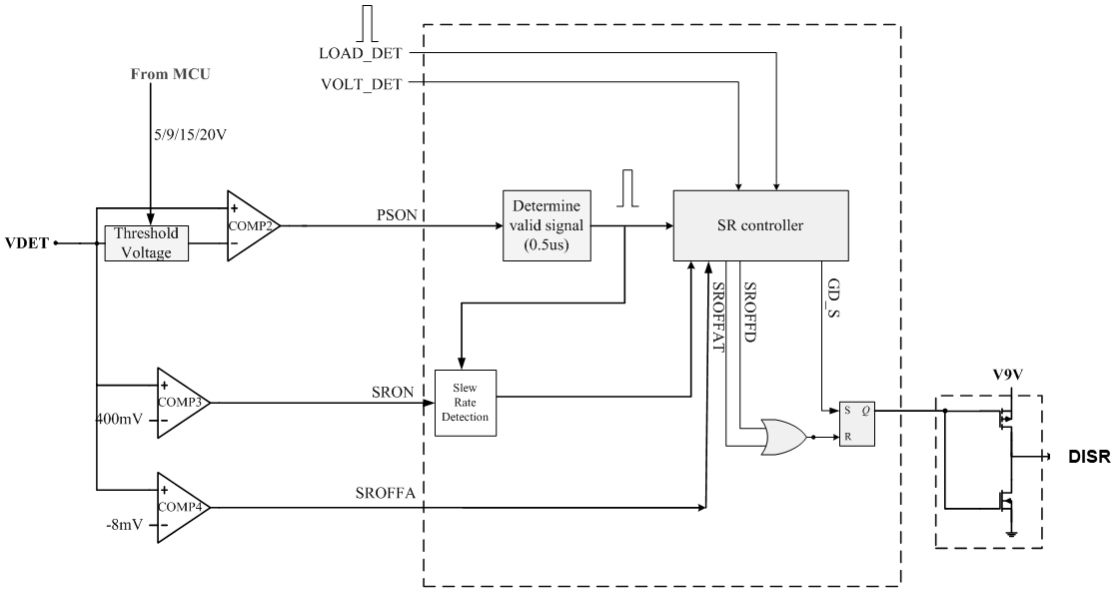


Figure 3. Functional Block Diagram of SR controller

Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{VCC} , V_{CC1}, V_{CC2}	Input Voltage at VCC, CC1, CC2 Pin	-0.3 to 24	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{VFB}, V_{OTP}	Input Voltage at VFB, OTP Pins	-0.3 to 7	V
V_{VBUS}, V_{PWREN}, V_{OCDRV}	Input Voltage at VBUS, PWREN, OCDRV Pins	-0.3 to 24	V
V_{V9V}	Input Voltage at V9V Pin	-0.3 to 7	V
V_{DISR}	Input Voltage at DISR Pin	-0.3 to 7	V
Others	Input Voltage at other Pin	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA} (QFN-20)	Thermal Resistance (Junction to Ambient) (Note 5)	134	°C/W
—	ESD (Human Body Model) Voltage on VBUS, VCC, OCDRV, PWREN, V5V, V9V, VFB, OTP, CC1, CC2 , VDET, DISR, S_GND Pins	2000	V
—	ESD (Human Body Model) Voltage on DP, DN Pins	6000	V
—	ESD (Charged Device Model)	750	V

Notes: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 cooling area.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Power Supply Voltage at VCC	3	21	V
T_{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V_{VCC_ST}	VCC Startup Voltage	—	2.65	2.85	3.05	V
V_{VCC_UVLO}	VCC Minimum Operating Voltage	—	2.5	2.7	2.9	V
V_{VCC_HYS}	VCC Hysteresis (V_{ST}-V_{UVLO})	—	—	0.15	—	V
$I_{VCC\_DEEP\ SLEEP}$	VCC Current in Deep Sleep Mode	CC1/2 Detach after 3 Seconds	—	750	—	μA
I_{VCC_OPR}	VCC Operating Supply Current	—	—	4.5	6	mA
PWREN (Note 10)						
V_{PWREN_L}	PWREN high voltage in low VCC input	V_{VCC}<4.5V	—	2*V_{V5V}+V_{VCC}-0.7	—	V
V_{PWREN_H}	PWREN high voltage in high VCC input	V_{VCC}=5V	—	V_{V5V}+V_{VCC}-0.7	—	V
VOLTAGE CONTROL LOOP SECTION						
V_{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9.0	9.27	V
V_{REF_CV12}	Reference Voltage for 12V CV Control	—	11.64	12.0	12.36	V
V_{CABLE}	Cable Compensation (Note 7)	—	24	30	36	mV/A
I_{OS}	Maximum OCDRV Pin Sink Current	V_{OUT} = 4V	10	16	—	mA
R_{OCDRV}	OCDRV Pin pull down resistor to GND	—	—	80	—	KΩ
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 8)	—	5.5	6	6.5	V
V_{OVP9V}	OVP_9V Enable Voltage (Note 8)	—	9.9	10.8	12.1	V
V_{OVP12V}	OVP_12V Enable Voltage (Note 8)	—	13.2	14.4	16.2	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 6)	—	—	90	—	ms
V_{UVP5V}	UVP_5V Enable Voltage (Note 8)	—	—	3.8	—	V
V_{UVP9V}	UVP_9V Enable Voltage (Note 8)	—	—	6.8	—	V
V_{UVP12V}	UVP_12V Enable Voltage (Note 8)	—	—	9.1	—	V
I_{OVD}	Overvoltage Discharge Current	—	—	240	—	mA
t_{OCP}	OCP Deglitch Time (Note 9)	—	—	30	—	ms
$t_{RESTART\_INTERVAL\_SCP}$	Restart Interval Time under SCP (Note 9)	—	1	—	2	s
$I_{OTP\_EXTERNAL}$	External OTP Current	—	—	100	—	μA

Notes:
6. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.
7. Cable compensation voltage can be adjusted by setting from 0 to $V_{CABLE * N, (N: 0 to 7)}$.
8. Programmable 120% OVP and 75% or 80% UVP setting.
9. Guaranteed by design.
10. Without resistor loading condition. The realistic measurement will be lower due to leakage current of prober.

Electrical Characteristics (continued) (@ T_A =+25°C, V_{VCC} = 15V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PROTECTION FUNCTION SECTION						
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 9)	—	—	3	—	s
t_{OV_DELAY}	Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 9)	—	—	—	50	μs
t_{UV_DELAY}	Delay from UVP Threshold Trip to NMOS Gate Turn-Off (Note 9)	—	—	—	50	μs
CC1/CC2, DP/DN PIN SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
I_{RD3A}	CC1/CC2 Current Source for 3A Advertisement	—	304	330	356	μA
V_{OVP_DN}	DN Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V_{OVP_DP}	DP Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V_{OVP_CC1}	CC1 Line Overvoltage Protection Threshold	—	—	7	—	V
V_{OVP_CC1}	CC2 Line Overvoltage Protection Threshold	—	—	7	—	V
SR SECTION						
V_{SROFFA}	VDET Negative Voltage Detection Threshold Voltage	Test mode	—	-10	—	mV
R_{DET}	Internal Resistor between VDET and GND	VCC=5V	—	1.6	—	kΩ
V_{DET_OVP}	VDET PIN OVP Threshold	—	—	4.8	—	V
V_{SR_Gate}	Gate Driver High Voltage	VCC=5V (External charge pump circuit active)		5		V
t_{R_Gate}	Gate Driver Rise Time	CL=6.5nF, VCC=5V, from 10% to 90%	—	50	—	ns
t_{F_Gate}	Gate Driver Fall Time	CL=6.5nF, VCC=5V, from 90% to 10%	—	30	—	ns
F_{CPCLK}	Charge Pump Clock Frequency	V5V=5V, measure VCP pin	—	187	—	KHz
t_{ON_min}	SR Gate-On Minimum On Time	Fs=100K	—	667	—	ns
t_{ON_DT}	SR Gate-On Dead Time	Fs=100K	—	200	—	ns
t_{OFF_DT}	SR Gate-Off Dead Time	Fs=100K	—	416	—	ns
$t_{d\_PSON\_min}$	Primary-Side Minimum On Time	—	500	—	—	ns

Note: 9. Guaranteed by design.

Performance Characteristics

System Power-On Sequence

When the external power source is provided, the AP43671 will wake up, and the USB PD controller and MCU will be initialized. All analog control blocks are ready and waiting for PD negotiation process. Meanwhile, the AP43671 monitors the voltage and current conditions to avoid abnormal conditions from occurring. Once any unacceptable conditions occur, the AP43671 will go into a protection procedure according to the types of abnormal conditions present.

Voltage Transition

According to USB PD's protocol, the PD device requests different power profiles. The AP43671's power control block will change the voltage and current values. The AP43671 provides corresponding Overvoltage Protection (OVP), Overcurrent Protection (OCP), and feedback system stability to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

The AP43671 provides zero-mismatch voltage methodology that is more flexible for customer system-design requirements. When UFP/DFP makes the acceptable power request deal, the AP43671 will change the VFB voltage according to the USB PD command. The voltage regulator control loop regulates the required VBUS voltage according to VFB voltage. In addition, the shunt regulator is built in to minimize the total external components and cost.

Protection

The AP43671 provides OVP/UVP/OCP/SCP/OTP functions and also supports Constant Current (CC) function. All of the protection thresholds depend on the requested power profile and provide the most reliable protection scheme.

The AP43671 provides OVP feature by turning off the power switch when VBUS is higher than OVP enable voltage. Meanwhile, it provides internal discharge path to reduce the overvoltage duration, and terminates discharge current as soon as VBUS reaches the target voltage. To avoid VBUS pin working abnormally, the AP43671 provides UVP function whenever VBUS drops to UVP enable voltage.

The AP43671 provides CC1/CC2 Overvoltage Protection (CC_OVP). There are two CC1/CC2 Overvoltage Protection (CC_OVP) mechanisms in the AP43671. First, the built-in switch-off circuit isolates the internal block with an external pin while the unpredictable high-voltage source shorts to the CC1/CC2 pin. Second, the AP43671 will turn off VBUS and resume to 5V if the CC1/CC2 voltage keeps higher than CC_OVP (7V) for more than 3ms, which will avoid the VBUS from shorting to the CC1/CC2 continuously.

Both methods guarantee USB PD system safety in case the Type-C plug or receptacle is damaged.

To ensure the safe operation of USB PD, the AP43671 provides programmable OCP function to make sure output current will not be higher than the allowed maximum current. Once OCP conditions occur, the AP43671 will shut down the USB PD system and send a "Hard Reset" to the Upstream-Facing Port (UFP) device.

CV/CC

The AP43671 supports Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and the output current by the control pin OCDRV. During the CV mode, the AP43671 operates in fixed PDO, and the output voltage will be regulated to the request voltage if the output current is below the allowed maximum current. Once the sink device draws more than I_{OCP}, overcurrent protection occurs. When the CC mode function is enabled, the output voltage drops, and the source current is limited within 150mA whenever output current exceeds the allowed maximum current. When the output voltage drops below UVP, constant current limit turns off VBUS and starts the error-recovery procedure. The AP43671 will reset if the voltage continues dropping to the UVLO threshold.

Synchronization Rectifier

In order to provide higher efficiency in the AC/DC converter system, the AP43671's built-in SR circuit replaces the schottky diode of the secondary side with a low Rds(on) MOSFET. It is suitable for low-side rectifying application systems. The AP43671 adopts proprietary SR control methodology that can work efficiently in either DCM or CCM mode. The AP43671 also has a built-in charge pump for low V_{OUT} applications.

The AP43671 adopts a prediction method for CCM mode and detection method for DCM mode with proprietary MCU flexible control scheme. To prevent large through-current due to abnormal primary and secondary MOS turn-on, there are some criterions to guarantee safe operation. Once the minimum primary turn-on time (td_PSON_min) and falling slew rate meets the AP43671's threshold value, the SR controller will then recognize it as a periodical SYNC signal and the SR Gate will turn on; otherwise, the SR Gate will be disabled for at least one PWM cycle. If any large dynamic voltage/current transient occurs, the SR Gate will be turned off to avoid through-current. This can be flexibly controlled by the MCU.

To minimize the power consumption at light-load condition, AP43671 disables the SR driver and enter sleep mode when cable detach. The controller monitors the switching frequency of PWM signal and exit the burst mode.

Application Circuit Case

A cost-effective 25W AC flyback adaptor schematic is shown in Figure 4 below, where the primary side uses the AP3304A (a multi-mode (QR+CCM) PWM controller) and the secondary side uses the AP43671 (a highly integrated PD controller embedded with a synchronous rectification (SR) controller). It is ideally targeted for cost-performance-sensitive USB Type-C adaptors and charger applications.

The AP3304A improves efficiency across all load levels with its multiple modes of operations, 60V processing of the VCC pin, and wide range of output applications. The device lowers BoM (bill of materials) quantity and simplifies system design for USB PD applications.

The AP43671 supports USB PD3.0 and Programmable Power Supply (PPS), and has passed the USB-IF certification. Its CC1/CC2 pins provide VBUS short protection up to 24V. Furthermore, its embedded synchronous rectification (SR) controller supports Adaptive Quasi-Resonant (QR) and Continuous Conduction Mode (CCM) for matching PWM controllers.

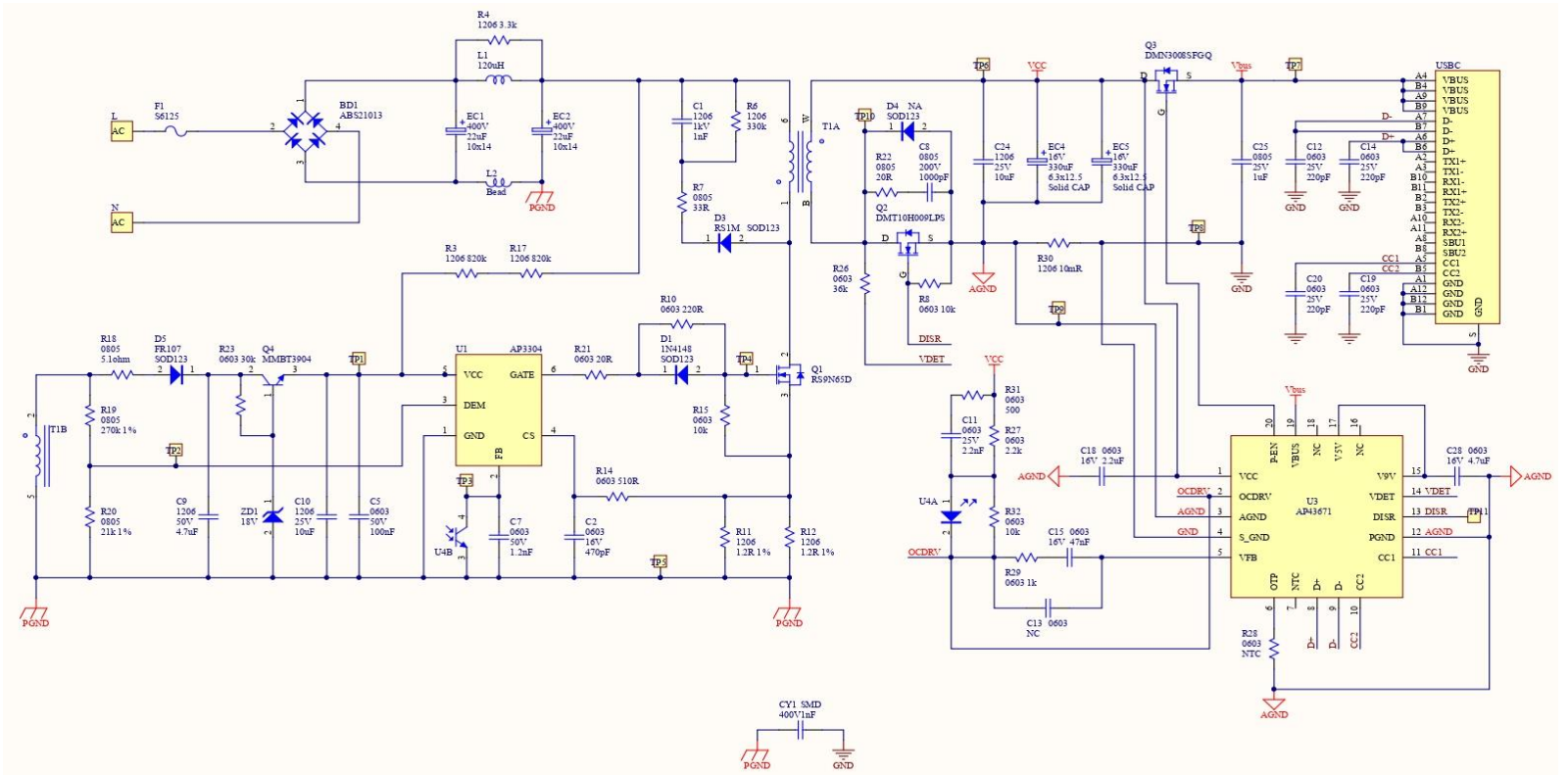


Figure 4. A Real 25W Flyback Adaptor based on AP43671 and AP3304A

Layout Guidelines

The AP43671 performance is dramatically affected by its PCB layout. Good engineering practice of layout techniques are required to minimize parasitic inductance and signal interference; and the overshoot voltages, ringing, oscillation, and EMC issues will reduce accordingly.

The most important guidelines for the AP43671 layout will include the current sense layout route, system ground path, and SR MOS distance from the SR controller, as shown in Figure 5.

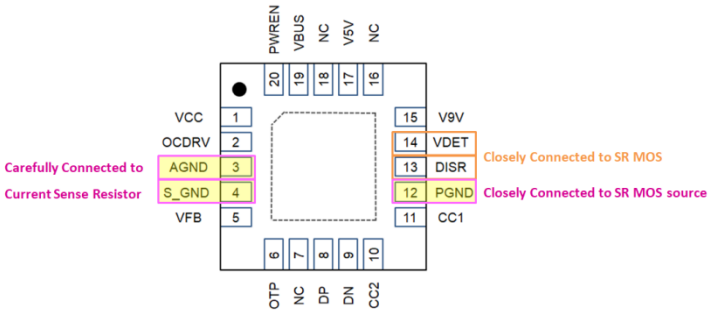


Figure 5. AP43671 layout key points

Current Sense Resistor

The four-point Kelvin connections are used for the current sense resistor.

The Kelvin sense traces should be connected to Pin3 (AGND) and Pin4 (S_GND) of the AP43671 in parallel and equal length, and reduce the distance if possible, as shown in Figure 6.

Be noted to reduce the PCB layout distance to the current sense resistor, which will reduce parasitic effect.

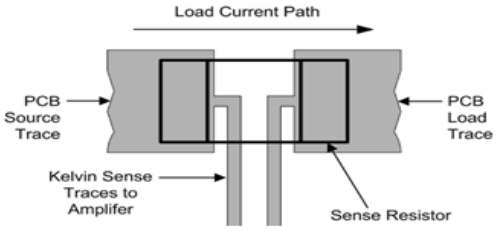


Figure 6. Be Symmetrical in Layout of Current Sensing Traces.

GND/PGND

To reduce impedance from Pin3 (AGND) / Pin12 (PGND) of the AP43671 to system AGND / GND, place the components according to the design priority and current direction.

According to the current direction, set the component in sequence.

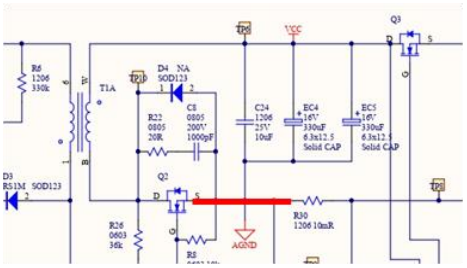


Figure 7. Be Short in Ground Path.

Layout Guidelines

VDET and DISR

Place the SR MOS and AP43671 as close as possible, as shown below Figure 8.

Resistor R26 needs close to PIN14 (VDET), a critical pin for SR controller, to reduce parasitic effect. It is suggested to use 100V/60V and a low Ron for SR MOS.

PIN13 (DISR) needs to reduce parasitic effect with PIN14 (VDET). The area of the PCB routing loop should not be too large, otherwise it will affect the turn-on of the SR controller.

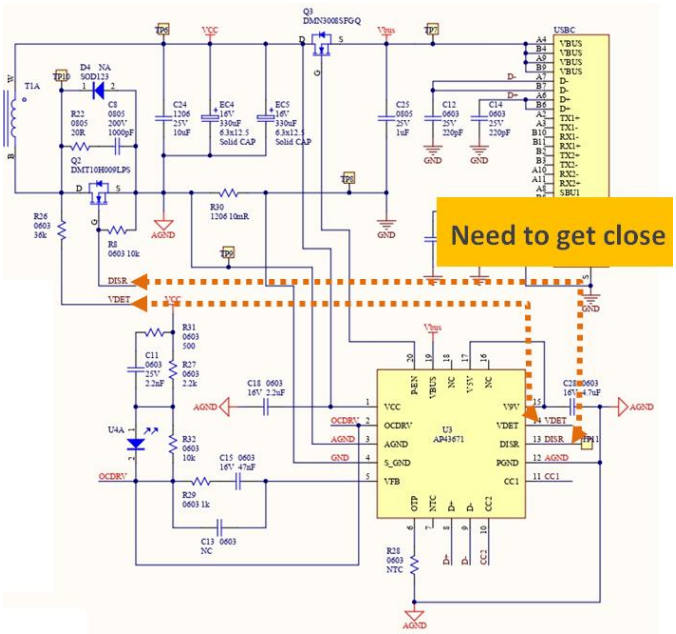


Figure 8. Be close in placement of AP43671 and SR MOS.

Decoupling Capacitor and GND

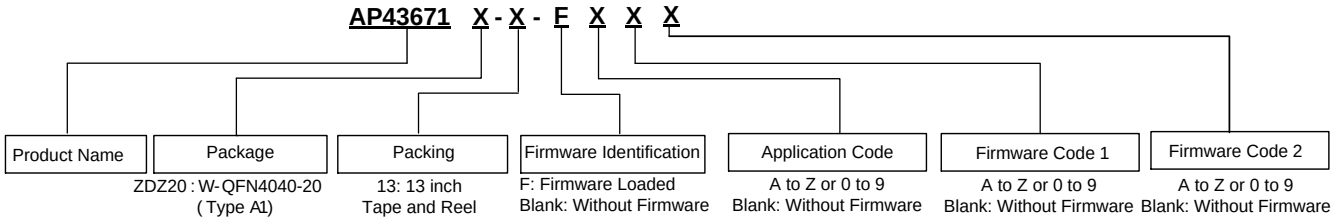
Keep the decoupling capacitor of V5V close enough to V5V (PIN17) of the AP43671.

PGND (PIN12) is suggested to return to SR MOS source directly and independently, and avoid the cross of any high-current point to reduce interference.

ESD Protection Placement

The GND for ESD protection devices are suggested to go back to USB Type-C GND connection of the PD module. In general, ESD protection devices are put on CC1/CC2 and DP/DN of the USB Type-C connector.

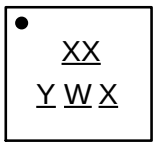
Ordering Information



Part Number	Package	Identification Code	7'Tape and Reel	
			Quantity	Part Number Suffix
AP43671ZDZ20-13	W-QFN4040-20 (Type A1)	B3	3000/Tape and Reel	-13

Marking Information

(Top View)

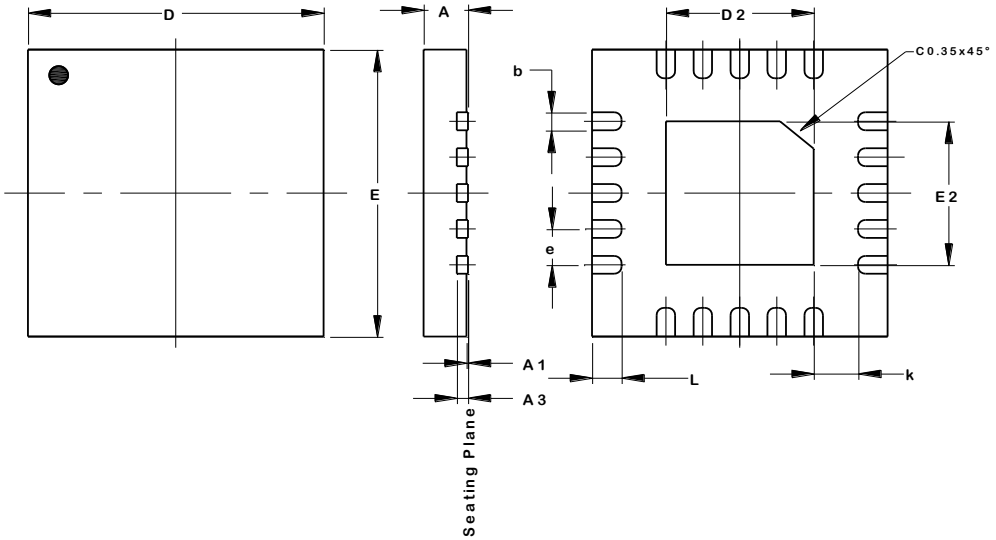


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-20 (Type A1)

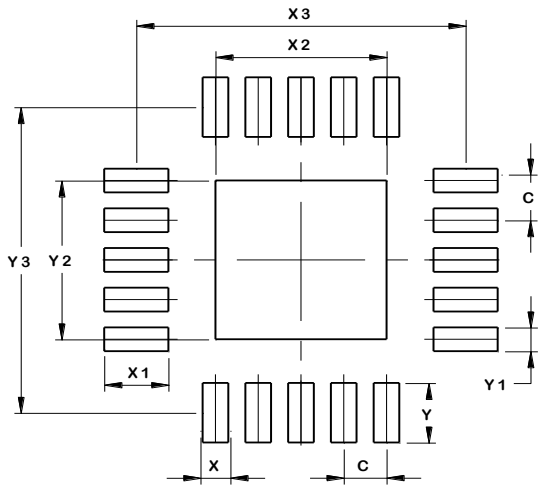


W-QFN4040-20 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.00 BSC		
D2	1.95	2.05	2.00
E	4.00 BSC		
E2	1.95	2.05	2.00
e	0.50 BSC		
k	0.20	--	--
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-20 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.000
X3	3.850
Y	0.750
Y1	0.300
Y2	2.000
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.0408 grams (Approximate)

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