REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Changes IAW NOR 5962-R087-93. – tjr	93-02-25	Monica L. Poelking
C	Add case outline Z. Update boilerplate to MIL-PRF-38535 requirements. – jak	01-08-27	Thomas M. Hess
D	Update boilerplate to MIL-PRF-38535 requirements. - LTG	08-04-16	Thomas M. Hess

Current CAGE CODE is 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Greg A. Pitz	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Daniel A. DiCenzo	
	APPROVED BY Nelson A. Hauck	MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-05-12	
	REVISION LEVEL D	SIZE A CAGE CODE **14933** **5962-87551** SHEET 1 OF 12

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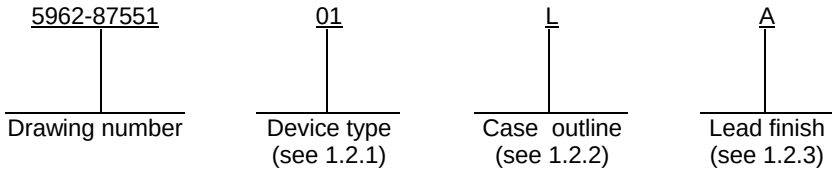
1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC241	Octal buffer/line driver with three-state outputs
02	54AC11241	Octal buffer/line driver with three-state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
R	GDIP1-T20 or CDIP4-T24	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
Z	GDFP1-G20	20	Flat pack with gull wing
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc 1/
DC Input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 1/
DC Output voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 1/
Clamp diode current ..... ±20 mA
DC output current (per pin) ..... ±50 mA
DC V_{CC} or GND current ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 2/

1/ Unless otherwise specified, all voltages are referenced to GND.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +3.0 V dc to +5.5 V dc 1/
Input voltage range (V_{IN}) ..... 0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... 0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times:
Device type 01;
Data inputs, V_{CC} = 3.6 V, V_{CC} = 5.5 V ..... 0 to 8 ns/V
Output enable inputs, V_{CC} = 3.6 V, V_{CC} = 5.5 V ..... 0 to 8 ns/V
Device type 02;
Data inputs, V_{CC} = 3.6 V, V_{CC} = 5.5 V ..... 0 to 8 ns/V
Output enable inputs, V_{CC} = 3.6 V, V_{CC} = 5.5 V ..... 0 to 5 ns/V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery backup systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq 70\%\ V_{CC}$, $V_{IL} \leq 30\%\ V_{CC}$, $V_{OH} \geq 70\%\ V_{CC}$ @ -20 μA, $V_{OL} \leq 30\%\ V_{CC}$ @ 20 μA.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH} 1/	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -50\ \mu A$	$V_{CC} = 3.0$ V	1, 2, 3	2.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 5.5$ V		5.4		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -4.0$ mA	$V_{CC} = 3.0$ V		2.4		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -24$ mA	$V_{CC} = 4.5$ V		3.7		
			$V_{CC} = 5.5$ V		4.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -50$ mA	$V_{CC} = 5.5$ V		3.85		
Low-level output voltage	V_{OL} 1/	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = 50\ \mu A$	$V_{CC} = 3.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 5.5$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = 12$ mA	$V_{CC} = 3.0$ V			0.5	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = 24$ mA	$V_{CC} = 4.5$ V			0.5	
			$V_{CC} = 5.5$ V			0.5	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = 50$ mA	$V_{CC} = 5.5$ V			1.65	
High-level input voltage	V_{IH} 2/		$V_{CC} = 3.0$ V	1, 2, 3	2.1		V
			$V_{CC} = 4.5$ V	1, 2, 3	3.15		
			$V_{CC} = 5.5$ V	1, 2, 3	3.85		
Low-level input voltage	V_{IL} 2/		$V_{CC} = 3.0$ V	1, 2, 3		0.9	V
			$V_{CC} = 4.5$ V	1, 2, 3		1.35	
			$V_{CC} = 5.5$ V	1, 2, 3		1.65	
Input leakage current	I_{IL}	$V_{IN} = 0.0$ V	$V_{CC} = 5.5$ V	1, 2, 3		-1.0	µA
	I_{IH}	$V_{IN} = 5.5$ V				1.0	
Quiescent current	I_{CCH}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5$ V		1, 2, 3		160	µA
	I_{CCL}					160	
	I_{CCZ}					160	
Off-state output leakage current	I_{OZH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $V_{CC} = 5.5$ V $V_{OUT} = V_{CC}$ or GND		1, 2, 3		10.0	µA
	I_{OZL}					-10.0	
Input capacitance	C_{IN}	See 4.3.1c		4		8.0	pF
Power dissipation capacitance	C_{PD} 3/	See 4.3.1c		4		60.0	pF
Functional tests		Tested at $V_{CC} = 4.5$ V and repeated at $V_{CC} = 5.5$ V, see 4.3.1d		7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, mAn to mYn	t_{PHL} 4/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	1.0	10.0	ns
				10, 11	1.0	11.5	
			V_{CC} = 4.5 V	9	1.0	8.0	
				10, 11	1.0	9.0	
	t_{PLH} 4/		V_{CC} = 3.0 V	9	1.0	10.5	
				10, 11	1.0	12.2	
			V_{CC} = 4.5 V	9	1.0	8.5	
				10, 11	1.0	9.5	
Output disable time, $\overline{OE1}$, OE2 to mYn	t_{PHZ} 4/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	1.0	12.0	ns
				10, 11	1.0	13.0	
			V_{CC} = 4.5 V	9	1.0	10.5	
				10, 11	1.0	11.5	
	t_{PLZ} 4/		V_{CC} = 3.0 V	9	1.0	12.0	
				10, 11	1.0	13.0	
			V_{CC} = 4.5 V	9	1.0	10.5	
				10, 11	1.0	11.5	
Output enable time, $\overline{OE1}$, OE2 to mYn	t_{PZH} 4/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	1.0	11.5	ns
				10, 11	1.0	13.8	
			V_{CC} = 4.5 V	9	1.0	9.0	
				10, 11	1.0	10.0	
	t_{PZL} 4/		V_{CC} = 3.0 V	9	1.0	11.5	
				10, 11	1.0	13.0	
			V_{CC} = 4.5 V	9	1.0	9.0	
				10, 11	1.0	10.0	

1/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V. V_{CC} = 5.5 V tests are guaranteed, if not tested. Limits shown apply to operation at V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ The V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}), determines the dynamic power consumption.

$P_D = (C_{PD} + C_L) V_{CC}2 f + I_{CC} V_{CC}$, and the dynamic current consumption (I_S) is, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}$.

4/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits are guaranteed for V_{CC} = 5.5 V by guardbanding V_{CC} = 4.5 V limits to 1.5 ns (minimum).

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Device types	01	02	
Case outlines	R, S, Z, and 2	L	3
Terminal number	Terminal symbol		
1	$\overline{OE1}$	1Y1	NC
2	1A1	2Y1	V_{CC}
3	4Y2	3Y1	4A1
4	2A1	4Y1	3A1
5	3Y2	GND	2A1
6	3A1	GND	1A1
7	2A2	GND	$\overline{OE1}$
8	4A1	GND	NC
9	1Y2	1Y2	1Y1
10	GND	2Y2	2Y1
11	1A2	3Y2	3Y1
12	4Y1	4Y2	4Y1
13	2A2	OE2	GND
14	3Y1	4A2	GND
15	3A2	3A2	NC
16	2Y1	2A2	GND
17	4A2	1A2	GND
18	1Y1	V_{CC}	1Y2
19	OE2	V_{CC}	2Y2
20	V_{CC}	4A1	3Y2
21		3A1	4Y2
22		2A1	NC
23		1A1	OE2
24		$\overline{OE1}$	4A2
25			3A2
26			2A2
27			1A2
28			V_{CC}

NC = No connection.

FIGURE 1. Terminal connections.

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Device types 01 and 02

Inputs			Outputs
$\overline{OE1}$	OE2	mAn	mYn
L	H	L	L
L	H	H	H
H	L	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 2. Truth table.

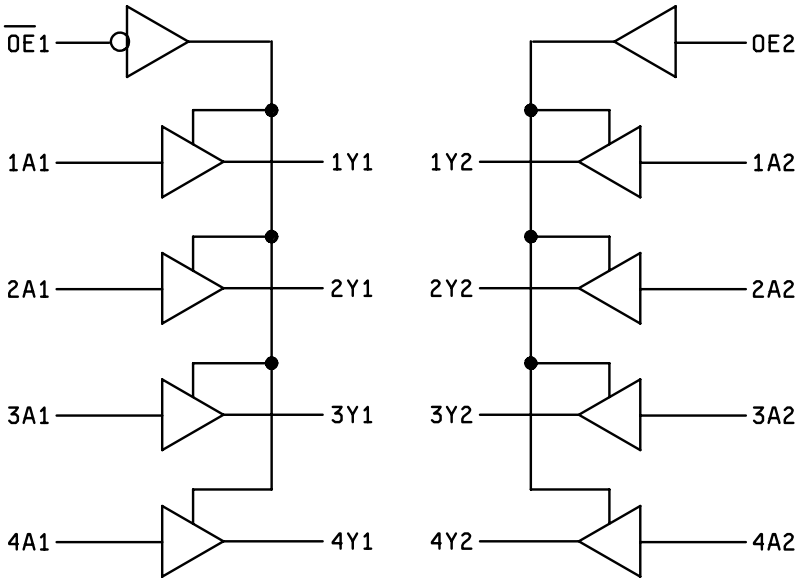

FIGURE 3. Logic diagram.

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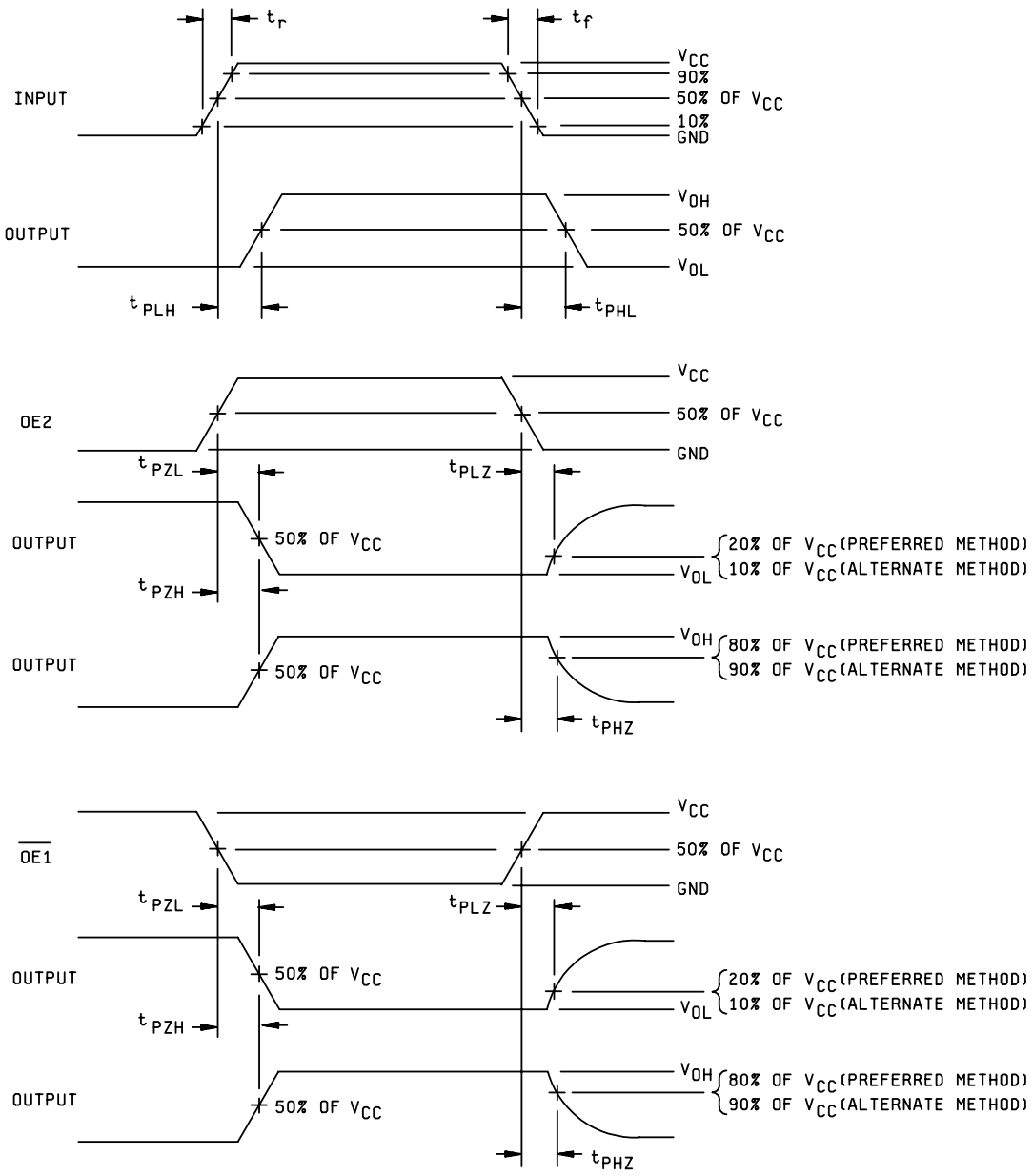

FIGURE 4. Switching waveforms and test circuit.

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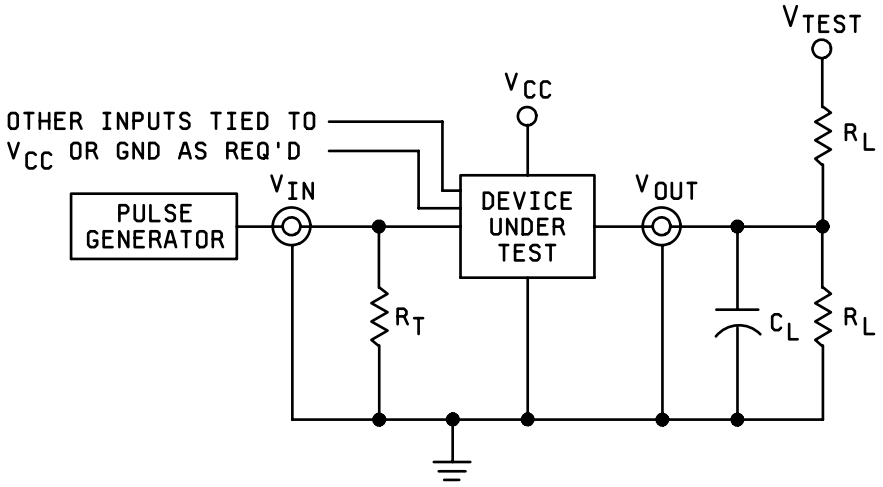

NOTES:
1. Preferred method:
   When measuring t_{PHZ} and t_{PZH}: V_{TEST} = GND
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PLH} and t_{PHL}: V_{TEST} = open
2. Alternate method:
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open
3. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance)
4. R_L = 500Ω or equivalent
5. R_T = 50Ω or equivalent
6. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; duty cycle = 50 percent. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 4. Switching waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-04-16

Approved sources of supply for SMD 5962-87551 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-87551012A	0C7V7	54AC241LMQB
5962-8755101RA	0C7V7	54AC241DMQB
5962-8755101SA	0C7V7	54AC241FMQB
5962-8755101ZA	0C7V7	54AC241WG-QML
5962-87551023A	3V146	54AC11241/B3A
5962-8755102LA	3V146	54AC11241/BLA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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