AN4562
Application note

STEVAL-ISA116V1: 5 W, 2 output wide range buck converter based on the VIPER26LD

Mirko Sciortino

Introduction

This application note describes a 2-output, 5 W power supply set in BUCK topology with the VIPER26, a new STMicroelectronics offline, high voltage converter specifically developed for non-isolated SMPS.

The device features an 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with adjustable set point, on-board soft-start, safe auto-restart after a fault condition and low standby power consumption.

The available protection includes thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. All protection is auto-restart mode.

Figure 1. STEVAL-ISA116V1 evaluation board

Contents

1 Adapter features

The electrical specifications of the board are listed in *Table 1*. The main output is 16 V/300 mA. A 5 V output able to supply up to 45 mA is obtained from the main output through a linear regulator.

Table 1. Electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[80 V_{AC}; 280 V_{AC}]
Output voltage 1	V_{OUT1}	16 V
Max output current 1	I_{OUT1}	0.27 A
Output voltage 1 (through LDO)	V_{OUT2}	5 V
Max output current	I_{OUT2}	0.045 A
Precision of output regulation	ΔV_{OUT1_LF}	± 5%
High frequency output voltage ripple	ΔV_{OUT1_HF}	50 mV
Max ambient operating temperature	T_{AMB}	60 ºC

2 Circuit description

The converter schematic is given in *Figure 2*. The input section includes a resistor R1 for inrush current limiting, a diode series D1 + D2 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V. The output voltage V_{OUT1} can therefore be set through the R4-R5 voltage divider between the output terminal and the FB pin, according to the formula:

Equation 1

$$V_{OUT1} = 3.3V \cdot \left(1 + \frac{R5}{R4}\right)$$

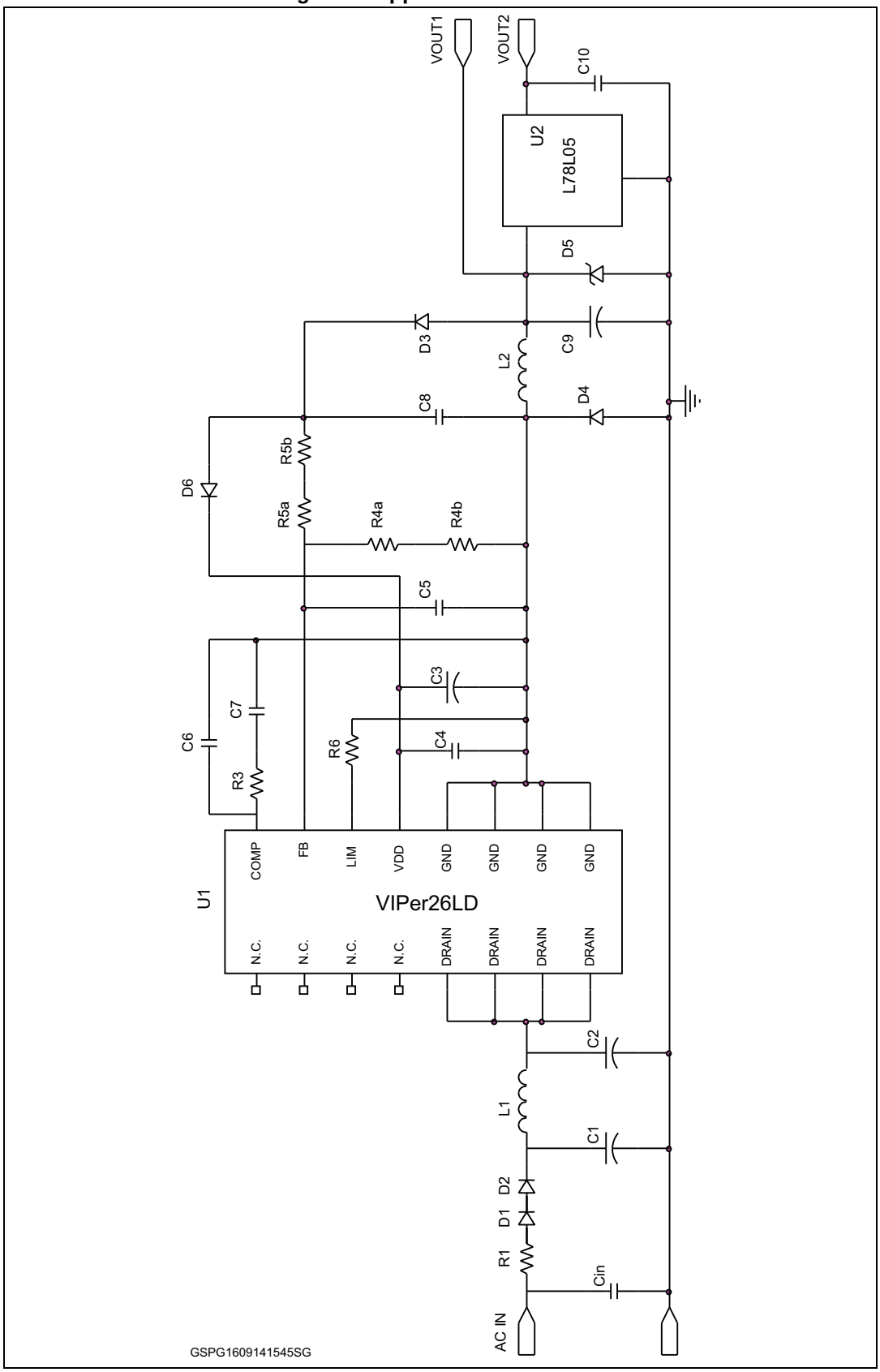
...where R4 is split into R4a and R4b and R5 into R5a and R5b to allow better tuning of the output voltage value.

The compensation network is connected between the COMP pin (error amplifier output) and the GND pin and consists of C6, R3 and C7.

The Zener diode D5 protects against overvoltage when the output load is disconnected.

At power-up, the DRAIN pin supplies the internal HV start-up current generator that charges the C3 capacitor up to V_{DDON} (13 V typical). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3 until V_{OUT1} reaches its steady state value. When this occurs, the IC is supplied from V_{OUT1} through the diode D6.

Figure 2. Application schematic



3 Bill of material (BOM)

Table 2. Bill of material

Name	Value	Description	Package	Manufacturer	RS code
Cin	100 nF	X2 capacitor, B32922 series	Through hole	Arcotronics	824-294
C1, C2	10 µF, 450 V	Electrolytic capacitor, NHG series	Through hole	Panasonic	365-4830
C3	1 µF, 35 V	Ceramic capacitor	SMD (0805)		
C4	100 nF, 50 V	Ceramic capacitor	SMD (0603)		
C5, C6	not mounted	Ceramic capacitor	SMD (0603)		
C7	1.5 nF, 50 V	Ceramic capacitor	SMD (0603)		
C8	1 µF, 100 V	Ceramic capacitor	SMD (0603)		
C9	330 µF, 25 V	Electrolytic capacitor ultra-low ESR, ZL series	Through hole	Rubycon	
C10	100 nF, 50 V	Ceramic capacitor	Through hole	Epcos	211-5378
R1	22 ohm	1 W resistor	SMD (case 2010)	Panasonic	572-823
R3	1 k	1/4 W resistor, 1%	SMD (0603)		
R4a	12k ohm	1/4 W resistor, 1%	SMD (0805)		
R4b	0 ohm	1/4 W resistor, 1%	SMD (0805)		
R5a	47 kohm	1/4 W resistor, 1%	SMD (0805)		
R5b	0 ohm	1/4 W resistor,1%	SMD (0805)		
R6	15 kohm	1/4 W resistor,1%	SMD (0805)		
D1, D2	GF1M	1000 V / 1 A diode	SMD (DO-214BA)	Vishay	629-1123
D3, D4	STTH1L06	Ultra-fast 600 V diode	SMD (SMB pack)	ST	
D5	18 V zener	not mounted	Through hole		
D6	LL4148	Diode	SMD (SOD-80)	Fairchild	670-8826
L1	1 mH	Axial inductor	Through hole	Epcos	191-0712
L2	0.82 mH	Power inductor	SMD	Coilcraft	
U1	VIPer26LD	Controlled switch	SMD (SO16N)	ST	
U2	L78L05	Voltage regulator	Through hole (TO-92)	ST	

4 Layout

Figure 3. Layout (top)

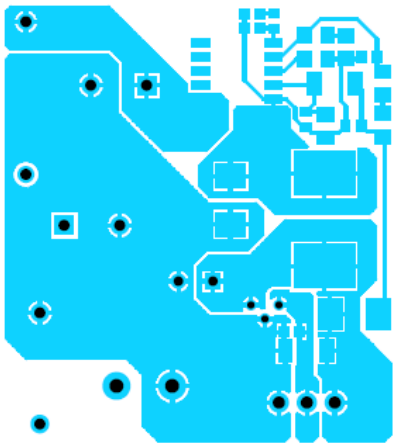


Figure 4. Layout (asytop)

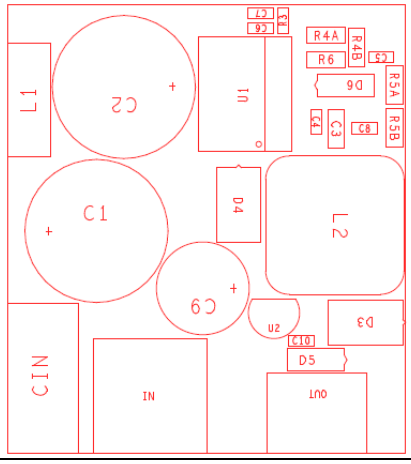


Figure 5. Layout (bottom)

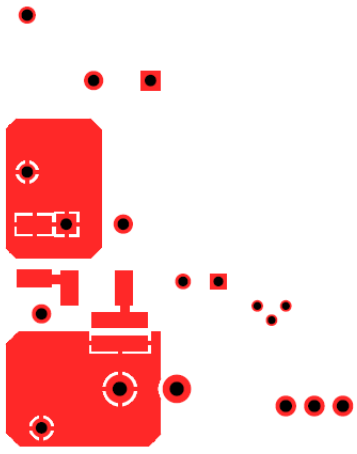
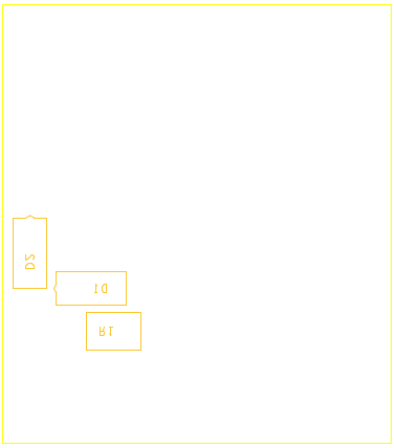


Figure 6. Layout (asybottom)



5 Testing the board

5.1 Typical waveforms

If the 5 V output is not loaded, the 16 V output can supply up to 320 mA. Since the efficiency standards are usually intended for single output converters, this setting is regarded as “full load” here and in *Section 6*.

The GND voltage and current waveforms under the full load condition are shown for the two nominal input voltages in *Figure 7* and *Figure 8*, and for the minimum and maximum input voltages in *Figure 9* and *Figure 10* respectively.

Figure 7. Waveforms at V_{IN} = 115 V_{AC}, full load

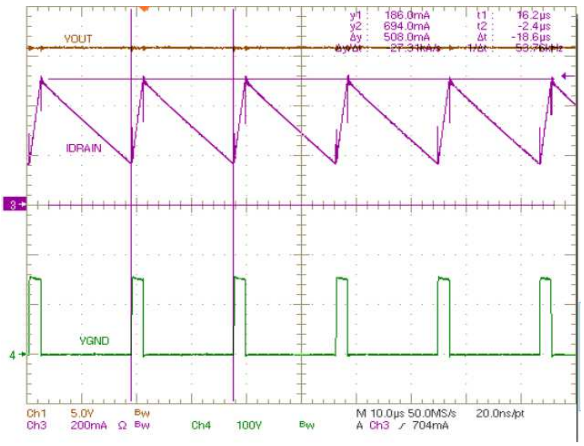


Figure 8. Waveforms at V_{IN} = 230V_{AC}, full load

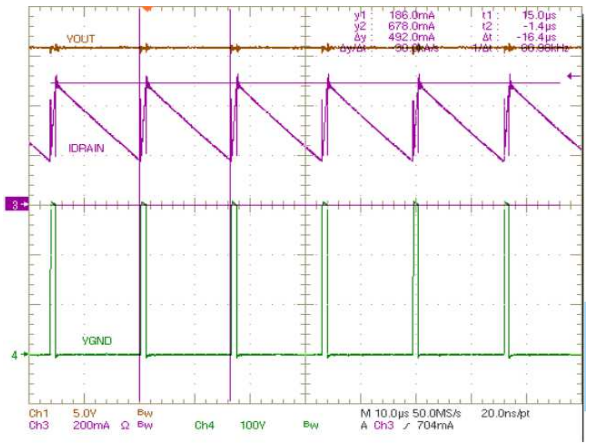


Figure 9. Waveforms at V_{IN} = 90 V_{AC}, full load

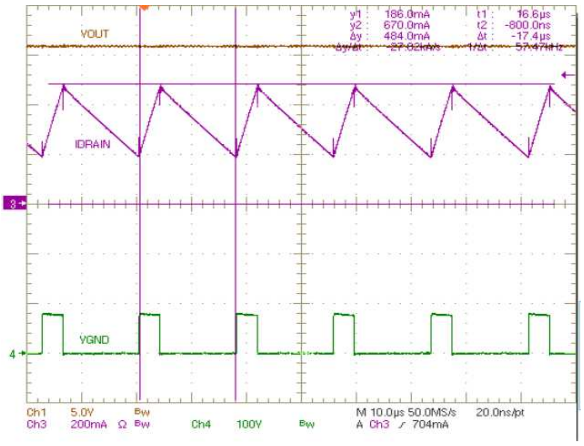
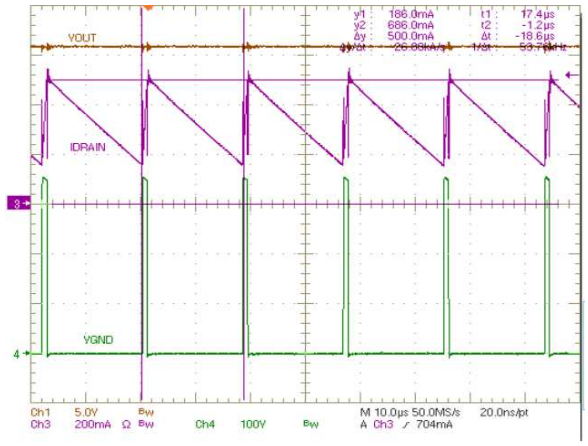


Figure 10. Waveforms at V_{IN} = 265 V_{AC}, full load



5.2 Line/load regulation and output voltage ripple

The output voltage of the board was measured under different line and load conditions, with the results given in the following figures.

Figure 11. Line regulation

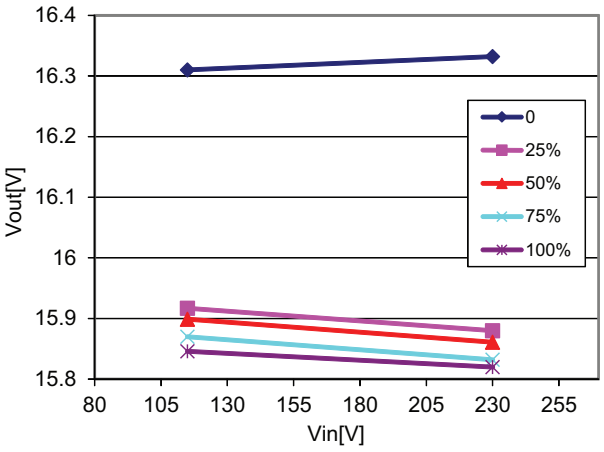
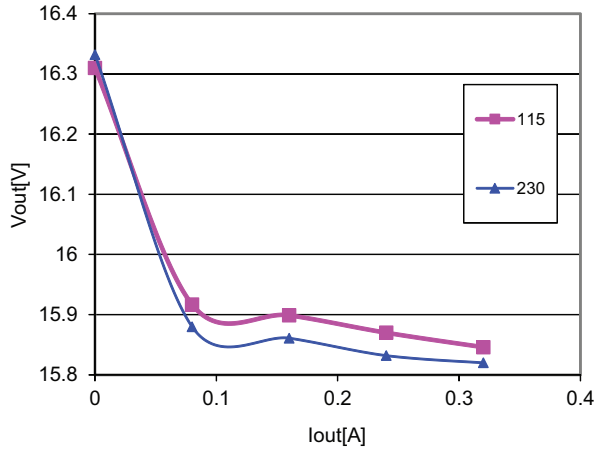


Figure 12. Load regulation



5.3 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

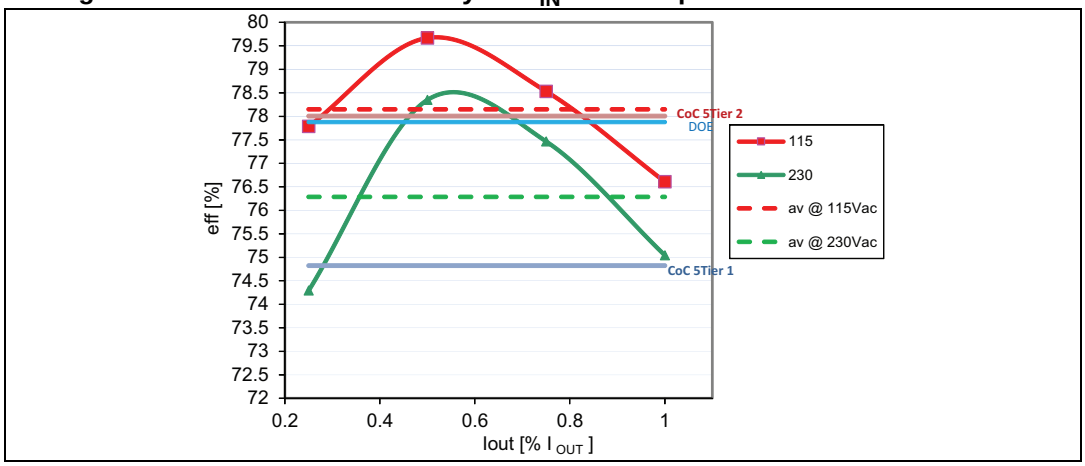
External power supplies (those housed separately to the end devices they are powering) must comply with the Code of Conduct, version 5 “active mode efficiency” criterion, which stipulates an active mode efficiency higher than 74.8% for a power throughput of 5.2 W (CoC5 tier1, January 2014). CoC5 tier2 will increase this to 78% in January 2016.

Another applicable standard is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 77.9%.

This evaluation board is compliant with all standards @115 V_{AC}, and with CoC5 Tier1 @ 230 V_{AC}, as can be seen in *Figure 13*, where the average efficiencies of the board at 115 V_{AC} (78.1%) and at 230 V_{AC} (76.3%) are plotted with dotted lines, together with the above mentioned limits. The efficiency at 25%, 50%, 75% and 100% load for both input voltages is also shown.[(a)]

a. the measurements performed in *Section 5.2* and *Section 5.4* are only indications as the above mentioned standards only apply to single output converters

Figure 13. Active mode efficiency vs V_{IN} and comparison with CoC5 and DOE



CoC5 also imposes a requirement on the active mode efficiency when the output load is 10% of the nominal output power. The table below comparing the requirement for an external power supply with a power throughput of 5.2 W and the performance of the evaluation demonstrates that the STEVAL-ISA116V1 is compliant with both Tier 1 and Tier 2 requirements.

Table 3. CoC5 requirement & performance at 10% output load

CoC5 minimum efficiency requirement in active mode at 10% of full load (for P_{OUT} = 5.2 W)		Evaluation board performance
Tier 1	Tier 2	
64.8%	68%	71.6%

5.4 Light load performances

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered. The compliance criteria are given in the table below:

Table 4. Energy consumption criteria for no load

Nameplate output power (Pno)	Maximum power in no load for AC-DC EPS	
	Tier 1	Tier 2
0.3W < Pno ≤ 49 W	0.15 W	0.075 W
50W < Pno < 250 W	0.25 W	0.15 W

The input power of the converter was measured under a no-load condition for different input voltages, with the results given in *Table 5*.

The board is compliant with the Tier1 requirement and also with the Tier 2 (at 115 V_{AC}) requirement. In the same table, the consumption of the demonstration board in other light load cases (P_{OUT} = 25 mW, P_{OUT} = 50 mW and P_{OUT} = 250 mW) is also shown.

Table 5. Light load consumption

V_{IN} [V_{AC}]	P_{IN} [mW]			
	@ P_{OUT} = 0	@ P_{OUT} = 25 mW	@ P_{OUT} = 50 mW	@ P_{OUT} = 250 mW
115	73	104	136	384
230	87	115	155	420

Depending on the equipment supplied, it is possible to measure the performance of a converter against several criteria. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The evaluation board satisfies this requirement, as shown in *Table 5*.

Another criterion is the measure of output power (or efficiency) when the input power is equal to one watt. This and some other conditions (P_{IN} = 250 mW and P_{IN} = 500 mW) are shown in the table below.

Table 6. Light load consumption

V_{IN} [V_{AC}]	P_{IN} [mW]		
	@ P_{IN} = 250 mW	@ P_{IN} = 500 mW	@ P_{IN} = 1 W
115	58.7	71.4	77.3
230	51.2	65.2	73.4

6 Functional check

6.1 Startup

The startup phase at maximum load at both nominal input voltages (115 V_{AC} and 230 V_{AC}) is shown in *Figure 14*, *Figure 15*, *Figure 16* and *Figure 17*.

Figure 14. Startup at V_{IN} =115 V_{AC}, full load

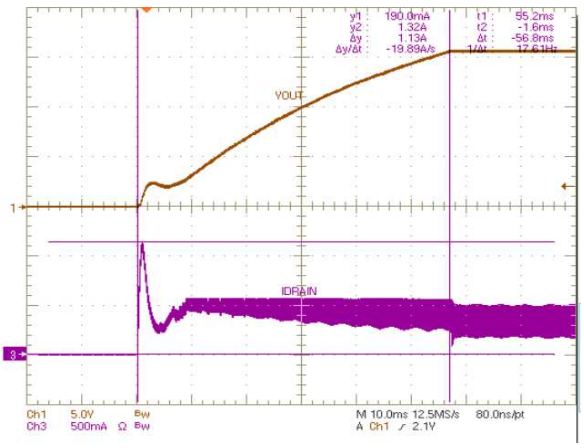


Figure 15. Startup at V_{IN} =115 V_{AC}, full load, zoom

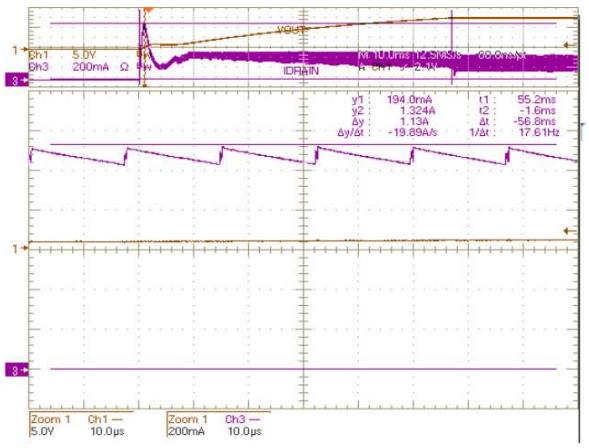


Figure 16. Startup at V_{IN} =230 V_{AC}, full load

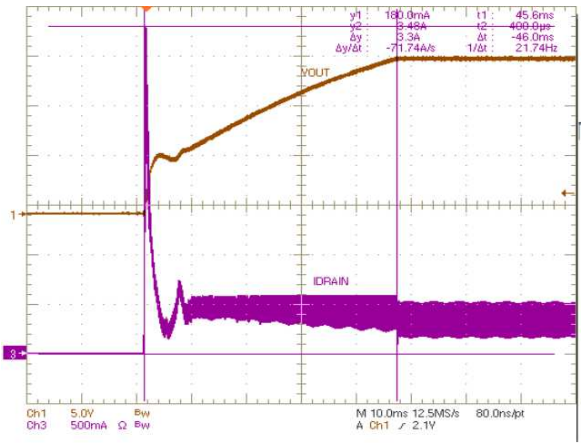
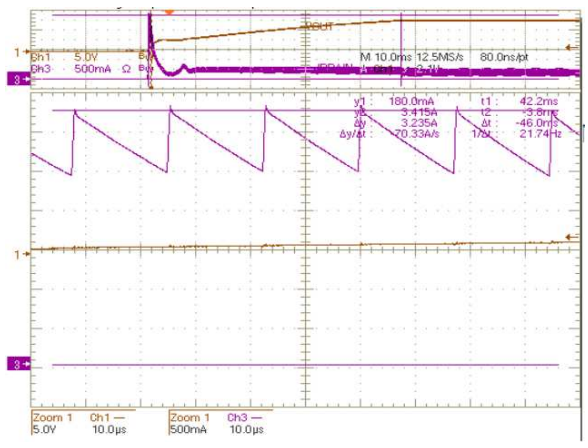


Figure 17. Startup at V_{IN} =230 V_{AC}, full load, zoom



6.2 Overload protection

In case of overload or short-circuit (see *Figure 18*), the drain current reaches the I_{DLIM} value (or the value set by the user connecting an appropriate resistor between LIM and GND pins, as explained in the VIPER26 datasheet). A counter increments for every cycle that this condition is met and, if it continues for the time t_{OVL} (set internally; typically 50 ms), the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (typically 1 s). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection continues indefinitely in the same way (*Figure 19*).

This ensures a low repetition rate of converter restart attempts, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

Once the short is removed, the IC resumes normal operation. If the short is removed before the protection is triggered, i.e., during t_{SS} or t_{OVL}, the counter decrements for each cycle down to zero.

If the short-circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before switching is resumed (*Figure 21*).

Figure 18. Output short-circuit applied: OLP tripping

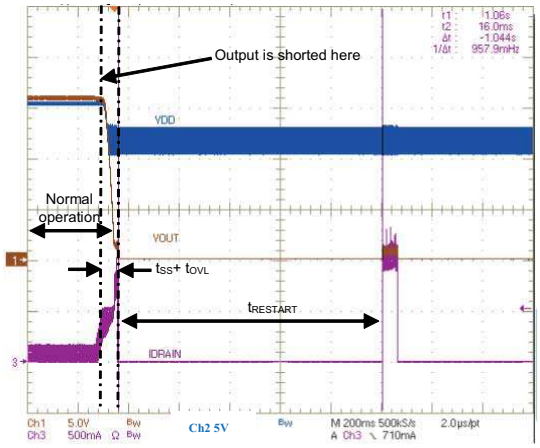


Figure 19. Output short circuit maintained: OLP steady- state

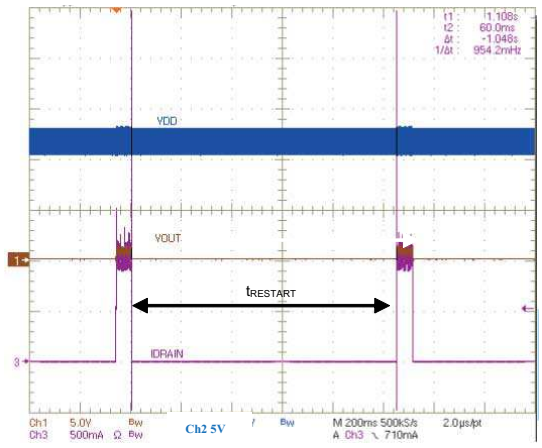


Figure 20. Output short circuit maintained: OLP steady- state (zoom)

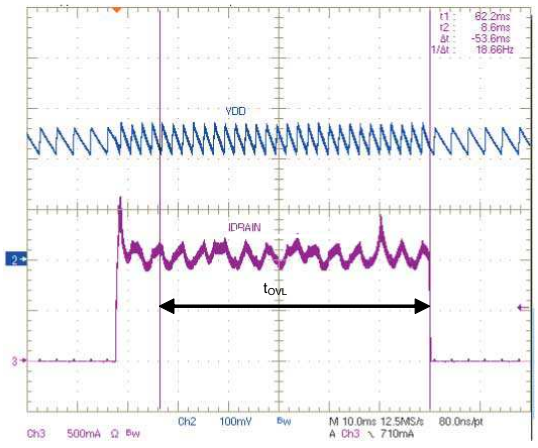
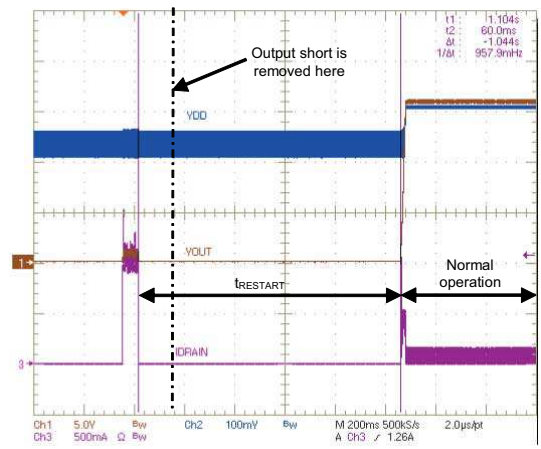


Figure 21. Output short-circuit removal and converter restart



6.3 Feedback loop failure protection

This protection is available whenever the IC is externally biased. When the loop is broken (R4 shorted or R5 open), the output voltage V_{OUT1} increases and the VIPER26 runs at its maximum current limitation. The V_{DD} pin voltage also increases as it is linked to V_{OUT1} through diode D6.

If the V_{DD} voltage reaches the $V_{DDclamp}$ threshold (23.5 V_{min}) in less than 50 ms, the IC is shut down by open loop failure protection (see *Figure 22* and *Figure 24*) or by OLP, as described in the previous section. Loop interruption was simulated by shorting the low side resistor of the output voltage divider, R4 = R4a1+R4b, but the same behavior can be induced by opening the high side resistor, R5 = R5a+R5b.

The protection functions in auto restart mode, where $t_{RESTART}$ = 1 s (*Figure 23*). Once the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval (*Figure 25*).

Figure 22. Feedback loop failure protection: tripping

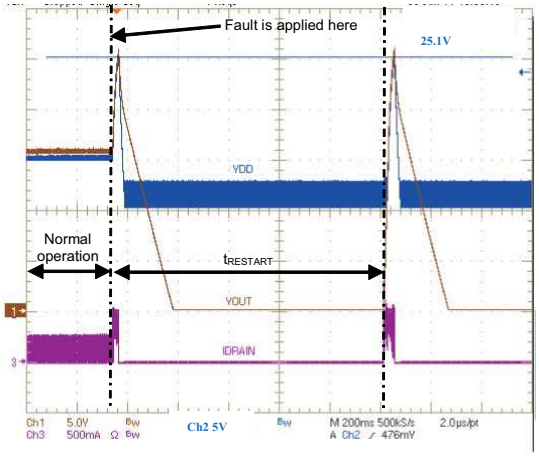


Figure 23. Feedback loop failure protection: steady state

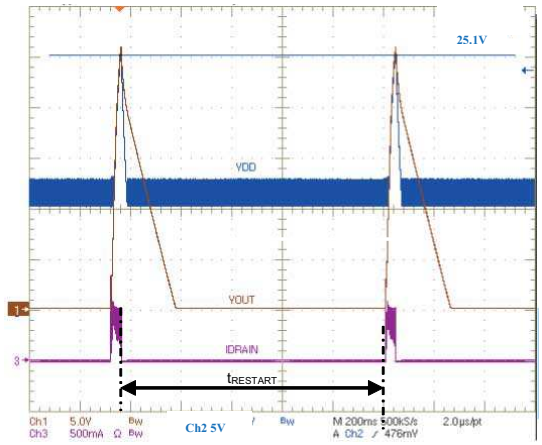


Figure 24. Feedback loop failure protection: steady state (zoom)

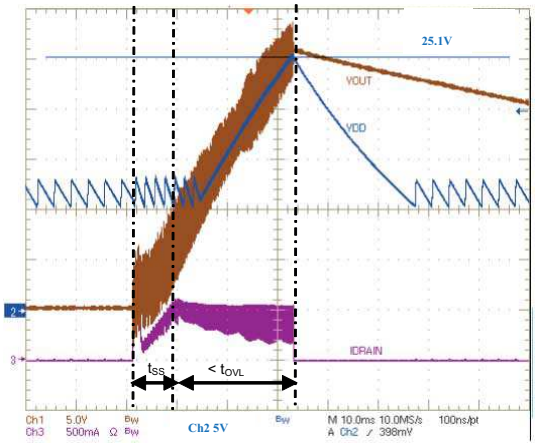
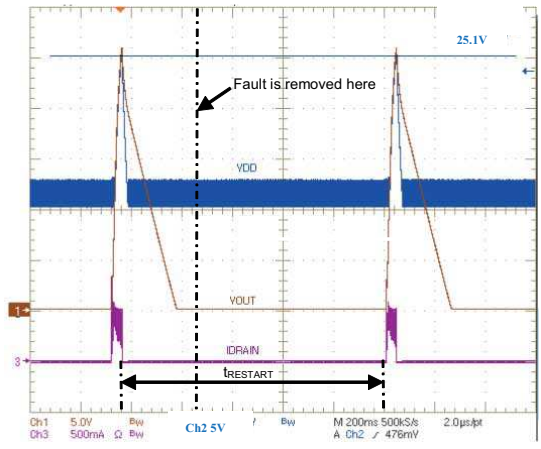


Figure 25. Feedback loop failure protection: converter restart

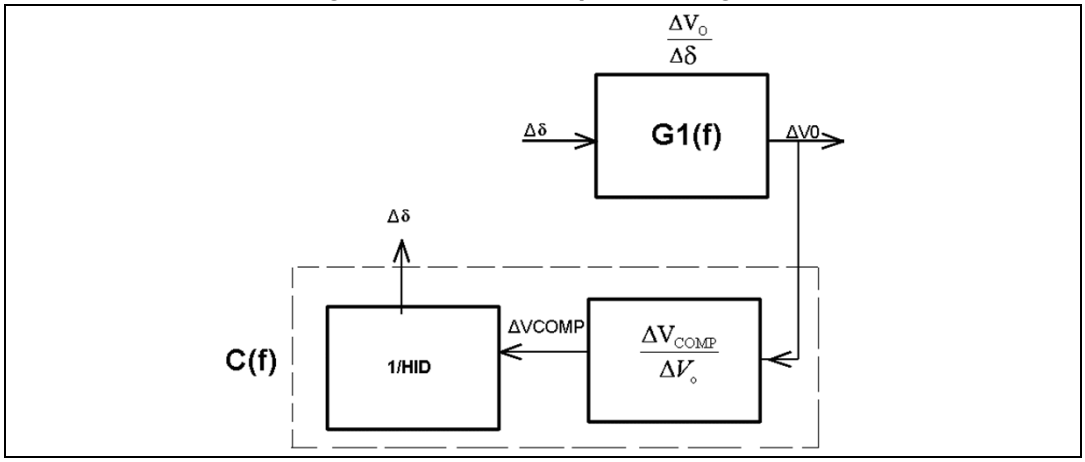


7 Feedback loop calculation guidelines

7.1 Transfer function

In the figure below, G1(f) represents the PWM modulator + power stage set, while C(f) is the controller or network which ensures the stability of the system.

Figure 26. Control loop block diagram



The mathematical expression of the power system G1(f) in DCM is the following:

Equation 2

$$G1(f) = \frac{\Delta V_{OUT}}{\Delta \partial} = G10 \cdot \frac{1 + \frac{j \cdot f}{f_Z}}{1 + \frac{j \cdot f}{f_P}}$$

where fz is the zero due to the ESR of the output capacitor:

Equation 3

$$f_Z = \frac{1}{2 \cdot \pi \cdot Cout \cdot ESR}$$

and fp is the pole due to the output load:

Equation 4

$$f_P = \frac{1 + \beta \cdot Rout}{2 \cdot \pi \cdot Cout \cdot (ESR + Rout + ESR \cdot \beta \cdot Rout)}$$

with:

Equation 5

$$\alpha = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)} \cdot \frac{Ipk}{2}$$

Equation 6

$$\beta = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)^2} \cdot \frac{Ipk}{2} \cdot \partial$$

Equation 7

$$G10 = \frac{\alpha \cdot Rout}{1 + \beta \cdot Rout} = \frac{(V_{OUT} + V\gamma) \cdot (V_{IN} + V\gamma) \cdot \frac{Ipk}{2} \cdot Rout}{(V_{OUT} + V\gamma)^2 + (V_{IN} + V\gamma) \cdot \frac{Ipk}{2} \partial \cdot Rout}$$

In the above formulas, Cout and ESR are the capacitance and the equivalent series resistance of the output capacitor respectively, Vγ is the forward drop of the free-wheeling diode, Rout = Vout/Iout is the output load, Ipk is the drain peak current at full load and δ = Ton*fsw is the duty cycle.

If the only compensation network between COMP and GND is an RC series as shown in *Figure 2* (C5 and C6 are not mounted), the mathematical expression for the compensator C(f) is:

Equation 8

$$C(s) = \frac{C_0}{H_{COMP}} \cdot \frac{(1 + \frac{j \cdot f}{fzc})}{j \cdot 2 \cdot \pi \cdot f}$$

where C_0 is given by:

Equation 9

$$C_0 = \frac{L \cdot fsw}{Vin - V_{OUT}} \cdot \left(\frac{-Gm}{C7}\right) \cdot \frac{R4}{R4 + R5}$$

and

Equation 10

$$fzc = \frac{1}{2 \cdot \pi \cdot R3 \cdot C7}$$

must be chosen in order to ensure the stability of the overall system.

The values $H_{COMP} = \delta V_{COMP}/\delta I_{COMP}$ and Gm (error amplifier transconductance) are specified in the VIPER26 datasheet.

7.2 Compensation procedure for a DCM BUCK

The first step is to choose the pole and zero of the compensator and the crossing frequency.

In this case, C(f) only has a zero (fzc) and a pole at the origin, thus a possible setting is:

fzc = n*fp
fcross = fcross_sel ≤ fsw/10

(n is chosen arbitrarily, a tentative value could be n = 25). After setting fcross, G1(fcross_sel) can be calculated from *Equation 2* and, since |C(fcross_sel)*G1(fcross_sel)|= 1, C_0 can be calculated as follows:

Equation 11

$$C_0 = \frac{\left| j \cdot 2 \cdot \pi \cdot fcross\_sel \right|}{\left| 1 + \frac{j \cdot fcross\_sel}{fzc} \right|} \cdot \frac{H_{COMP}}{\left| G1(fcross\_sel) \right|}$$

At this point, the bode diagram of G1(f)*C(f) can be plotted to check the phase margin for stability.

If the margin is not high enough, the procedure should be repeated with new choices for fzc and fcross_sel.

Once stability is achieved, the next step is to find the values of the schematic components, which can be calculated as follows.

From (*Equation 9*):

Equation 12

$$C7 = \frac{L \cdot fsw}{Vin - V_{OUT}} \cdot \left(\frac{\left| -Gm \right|}{C0} \right) \cdot \frac{R4}{R4 + R5}$$

and from (10):

Equation 13

$$R3 = \frac{1}{2 \cdot \pi \cdot fzc \cdot C7}$$

The quantities found in equations (*Equation 12*) and (*Equation 13*) are suggested values. Commercial values C7_act and R7_act are chosen, resulting in fzc_act.

Equation 14

$$fzc\_act = \frac{1}{2 \cdot \pi \cdot R3\_act \cdot C7\_act}$$

The value of C_0 is also recalculated from (*Equation 9*):

Equation 15

$$C_0\_act = \frac{L \cdot fsw}{Vin - V_{OUT}} \cdot \left(\frac{-Gm}{C7\_act} \right) \cdot \frac{R4\_act}{R4\_act + R5\_act}$$

and the compensator becomes:

Equation 16

$$\mathrm{C\_act(f)} = \frac{\mathrm{C_0\_act}}{H_{COMP}} \cdot \frac{(1 + \frac{f}{\mathrm{fzc\_act}})}{\mathrm{j} \cdot 2 \cdot \pi \cdot \mathrm{f}}$$

At this point, the bode diagram of G1(f)*C_act(f) should be plotted and the phase margin checked for stability.

8 Thermal measurements

A thermal analysis of the evaluation board under full load condition at T_{AMB} = 25 °C was performed using an IR camera. The results are shown in the following figures, where:

A = VIPer26LD; B = D4; C = L78L05; D = environment.

Figure 27. Thermal measurement @ V_{IN} = 115 V_{AC}, full load (I_{OUT1} = 270 mA, I_{OUT2} = 45 mA)

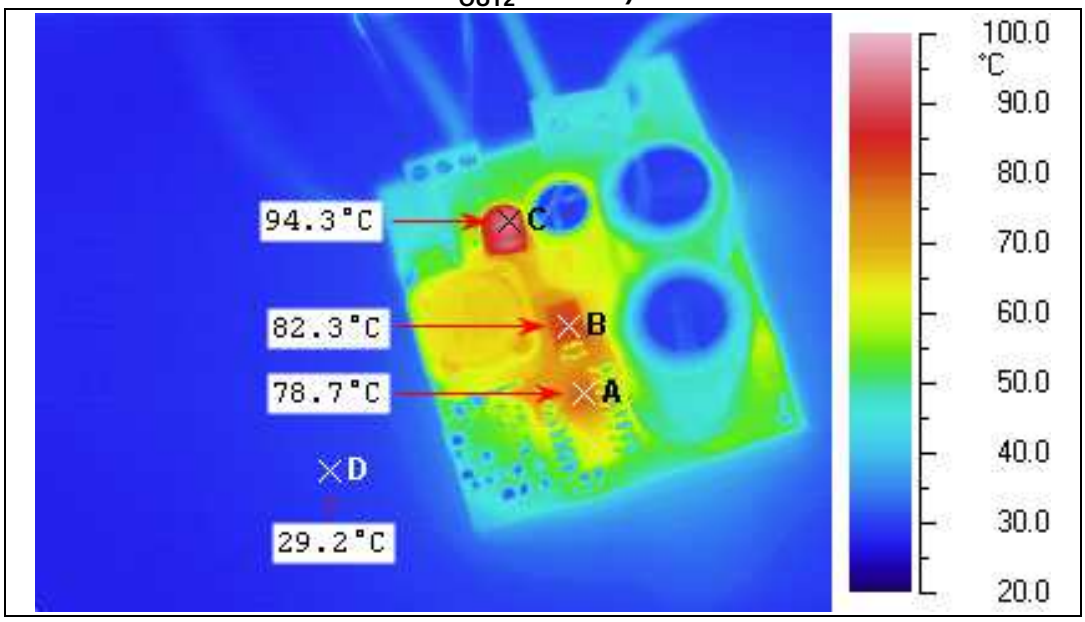
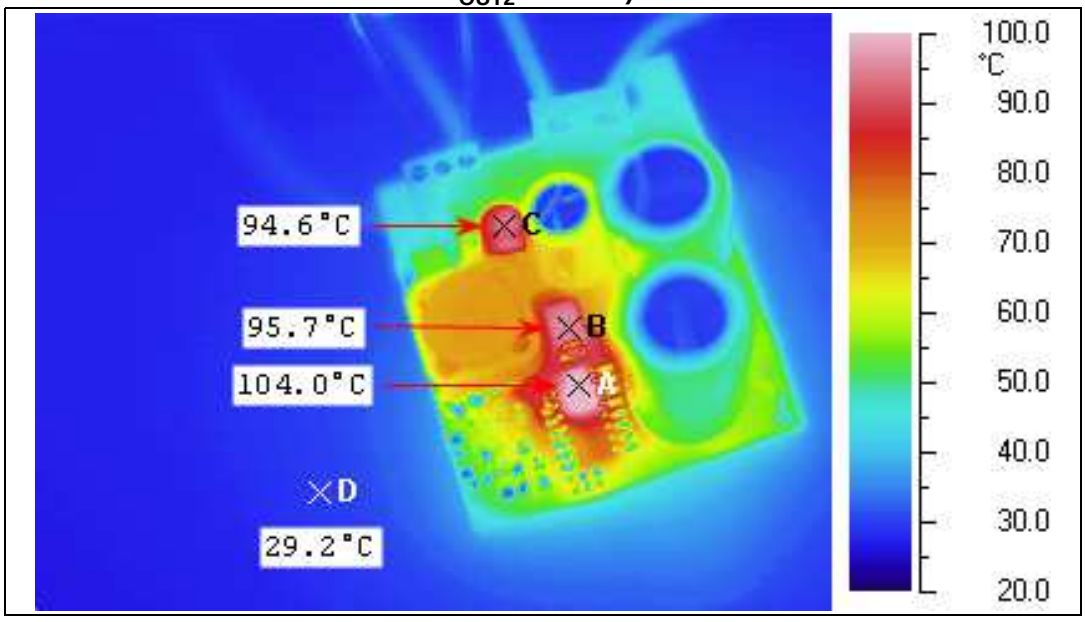


Figure 28. Thermal measurement @ V_{IN} = 230 V_{AC}, full load (I_{OUT1} = 270 mA, I_{OUT2} = 45 mA)



9 EMI measurements

A pre-compliance test against the EN55022 (Class B) European normative was performed using an EMC analyzer and an LISN. The average EMC measurements at 115 V_{AC}/full load and 230 V_{AC}/full load were taken and the results are shown in the following figures.

Figure 29. Average measurement at full load, 115 V_{AC}

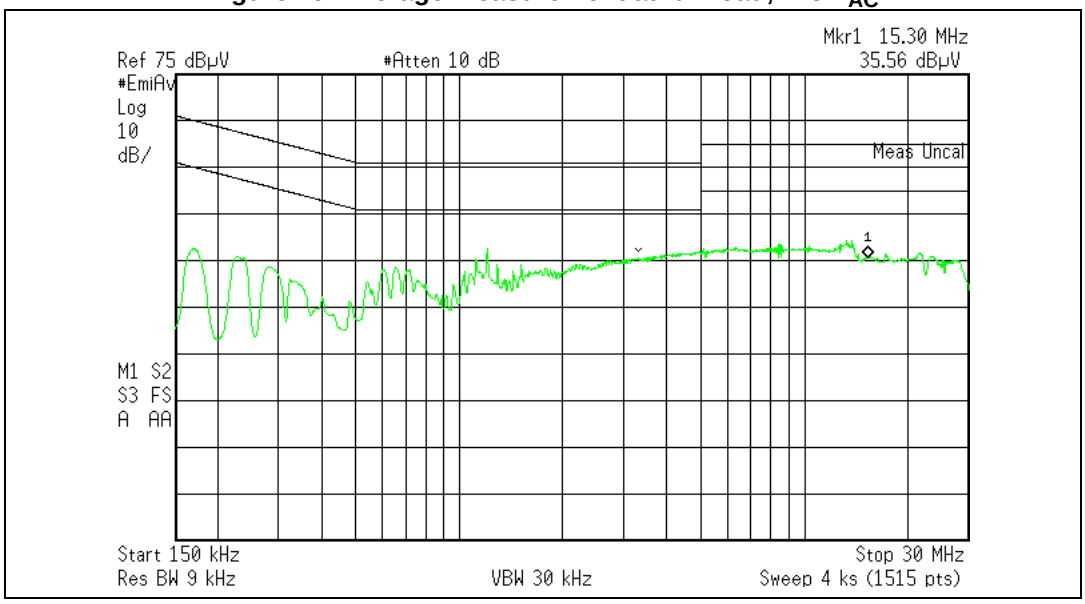
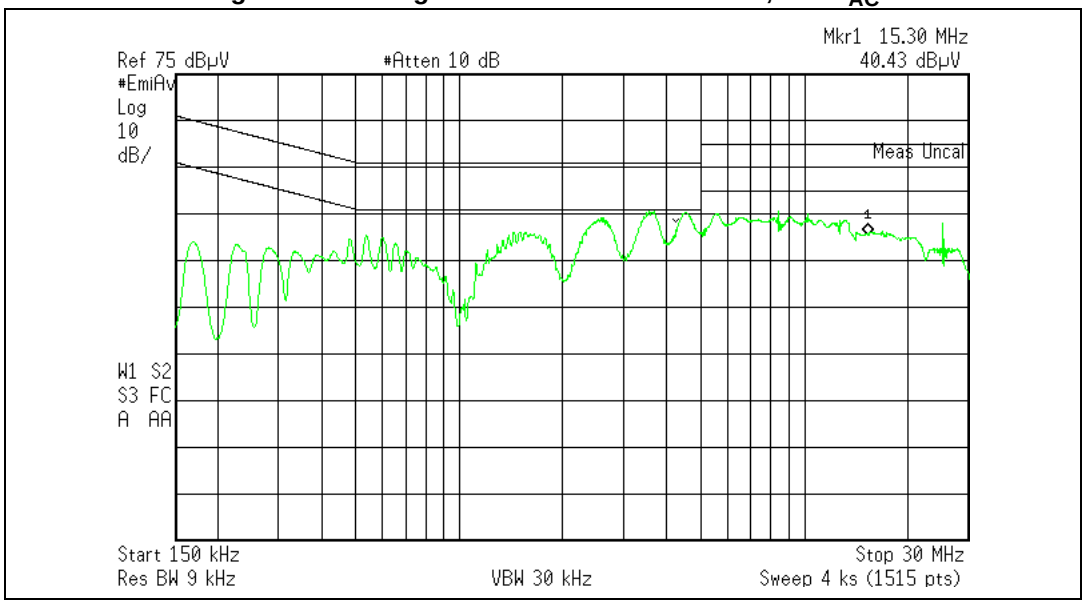


Figure 30. Average measurement at full load, 230 V_{AC}

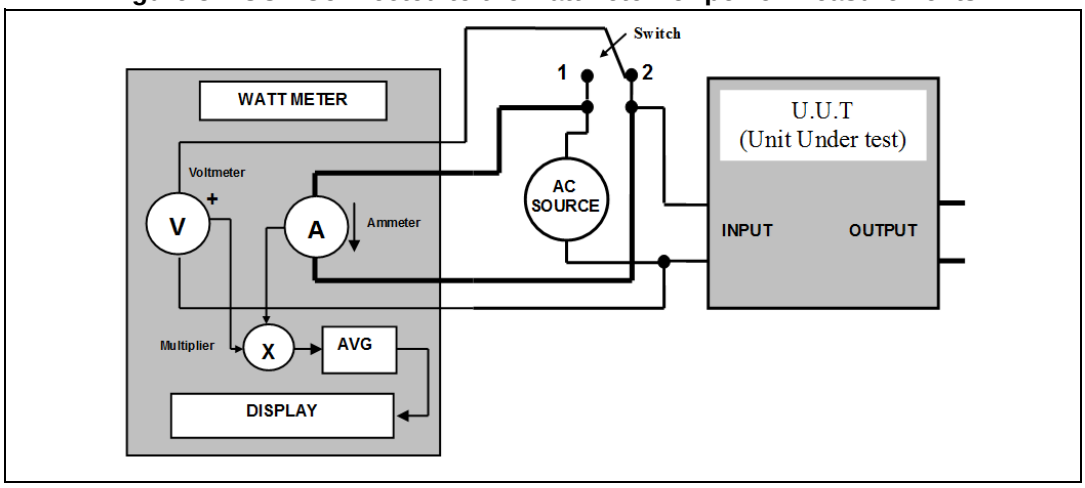


Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power was measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied to give the instantaneous measured power. The sampling frequency is in the 20 kHz range (or higher depending on the instrument used). The display returns the average over short intervals (typ. 1 sec) of the instantaneous power measurements.

Figure 31 shows the internal block diagram of the wattmeter and its connections with the UUT (unit under test) and the AC source.

Figure 31. UUT Connected to the wattmeter for power measurements



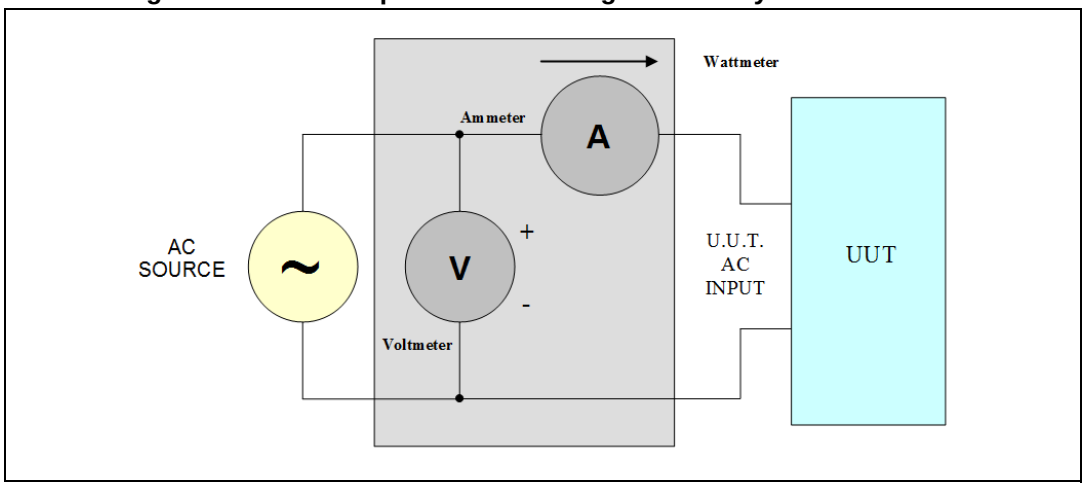
An electronic load is connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage is measured by a voltmeter. The output power is the product of the load current and output voltage. The ratio between this calculated output power and the input power measured by the wattmeter under different input/output conditions is the converter's efficiency.

A.1 Measuring input power

With reference to *Figure 31*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

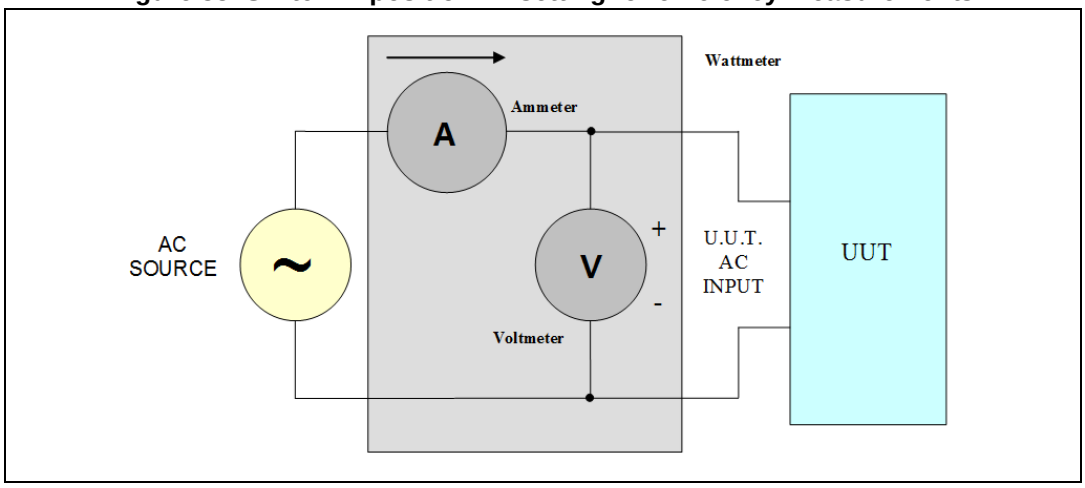
If the switch in *Figure 31* is in position 1 (see also the simplified scheme in *Figure 32*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which of course affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when measuring the input power of the UUT under a light load condition).

Figure 32. Switch in position 1 - setting for standby measurements



For a high UUT input current (i.e., for measurements under heavy load conditions), the voltage drop can be significant compared to the UUT real input voltage. In this case, the switch in *Figure 31* can be changed to position 2 (see simplified scheme in *Figure 33*), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 33. Switch in position 2 - setting for efficiency measurements



On the other hand, the position of *Figure 33* may introduce a significant error during light load measurements, where the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument with infinite input resistance) is not negligible. This is why it is preferable to use the settings in *Figure 32* for light load measurements and *Figure 33* for heavy load measurements.

If it is not clear which measurement scheme has the least effect on the result, try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT is considered stable and the measurements are recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both the AC input and DC output.

Some wattmeter models allow integration of the measured input power over a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is then calculated dividing by the same integration time.

10 References

- Code of Conduct on energy efficiency of external power supplies, version 5.
- VIPER26 datasheet

11 Revision history

Table 7. Document revision history

Date	Revision	Changes
04-Dec-2014	1	Initial release.