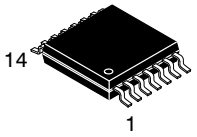
Quad 2-Input NAND Gate

MM74HCT00



TSSOP−14,
CASE 948G

General Description

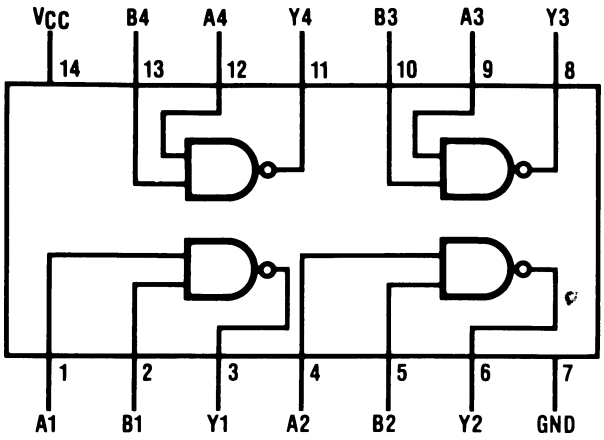
The MM74HCT00 is a NAND gates fabricated using advanced silicon−gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic and pin−out compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to VCC and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS Pin−out and Threshold Compatible
- Fast Switching: t_{PLH}, t_{PHL} = 14 ns (typ.)
- Low Power: 5 μW at DC
- High Fan Out, 10 LS−TTL Loads
- This Device is Pb−Free and Halide Free

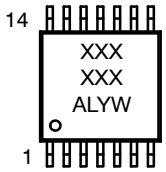
Connection Diagram



Top View

Figure 1. Pin Assignments for TSSOP

MARKING DIAGRAM

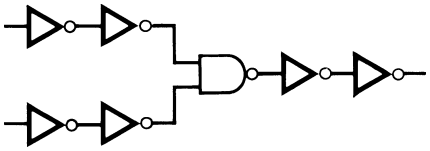


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

(Note: Microdot may be in either location)

LOGIC DIAGRAM

(1 of 4 gates)



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	−0.5 to +6.5	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per pin	±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10% (unless otherwise specified))

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		–	2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage		–	0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert$ = 4.0 mA, V_{CC} = 4.5 V	4.2	3.98	3.84	3.7	
		V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert$ = 4.8 mA, V_{CC} = 5.5 V	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH} $\lvert I_{OUT} \rvert$ = 20 μA	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\lvert I_{OUT} \rvert$ = 4.0 mA V_{CC} = 4.5 V	0.2	0.26	0.33	0.4	
		V_{IN} = V_{IH} $\lvert I_{OUT} \rvert$ = 4.8 mA V_{CC} = 5.5 V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}	–	±0.05	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	–	1.0	10	40	μA
		V_{IN} = 2.4 V or 0.5 V (Note 2)	–	1.2	1.4	1.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. This is measured per input with all other inputs held at V_{CC} or ground.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V, $t_r = t_f$ = 6 ns, C_L = 15 pF, T_A = 25°C (unless otherwise specified))

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	18	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, $t_r = t_f$ = 6 ns, C_L = 50 pF (unless otherwise specified))

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		18	23	29	35	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 3)	30	–	–	–	pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

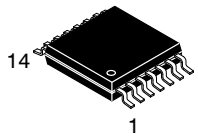
Device	Marking	Package	Shipping†
MM74HCT00MTCX	HCT 00A	TSSOP−14 WB, Case 948G (Pb−Free and Halide Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

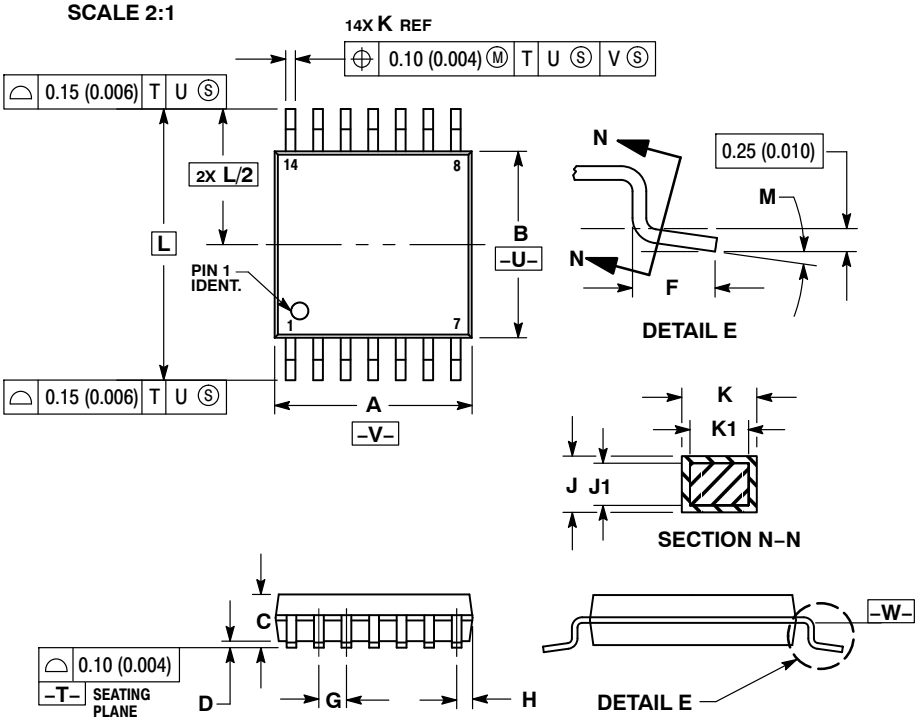
NOTE: All packages are lead free per JEDEC: J−STD−020B standard.

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



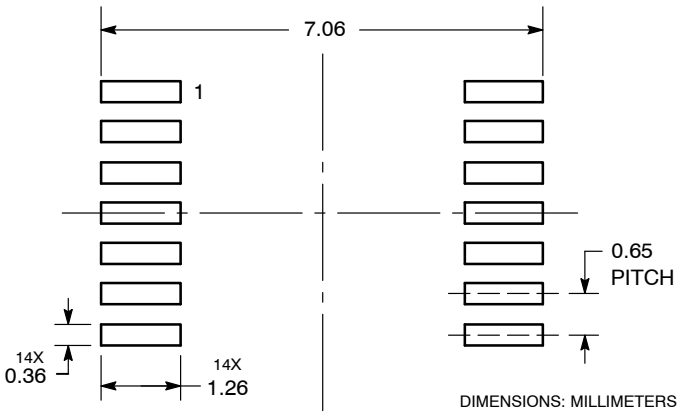
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

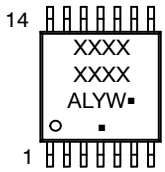
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSSOP−14 WB	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊