MOSFET – P-Channel, POWERTRENCH®

-12 V, -80 A, 3.9 mΩ

FDMC610P

General Description

This P−Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Features

- Max $r_{DS(on)} = 3.9\ m\Omega$ at $V_{GS} = -4.5\ V$, $I_D = -22\ A$
- Max $r_{DS(on)} = 6.4\ m\Omega$ at $V_{GS} = -2.5\ V$, $I_D = -16\ A$
- State−of−the−art Switching Performance
- Lower Output Capacitance, Gate Resistance, and Gate Charge Boost Efficiency
- Shielded Gate Technology Reduces Switch Node Ringing and Increases Immunity to EMI and Cross Conduction
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- High Side Switching for High End Computing
- High Power Density DC−DC Synchronous Buck Converter

MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

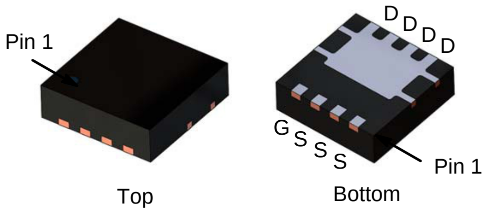
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	−12	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current − Continuous T_C = 25°C − Continuous (Note 1a) − Pulsed	 −80 −22 −200	A
P_D	Power Dissipation T_C = 25°C T_A = 25°C (Note 1a)	 48 2.4	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

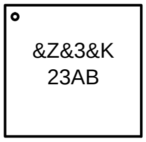
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case T_C = 25°C	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient T_A = 25°C (Note 1a)	53	

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
−12 V	3.9 mΩ @ −4.5 V	−80 A
	6.4 mΩ @ −2.5 V	



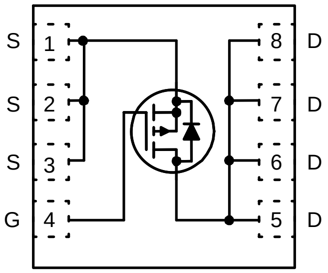
PQFN8 3.3X3.3, 0.65P
(Power 33)
CASE 483AK

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
23AB = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

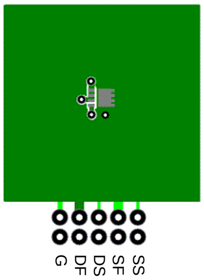
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu A$, $V_{GS} = 0$ V	−12	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu A$, referenced to 25°C	−	−13	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -9.6$ V, $V_{GS} = 0$ V	−	−	−1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8$ V, $V_{DS} = 0$ V	−	−	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu A$	−0.4	−0.7	−1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu A$, referenced to 25°C	−	3.1	−	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5$ V, $I_D = -22$ A	−	2.8	3.9	mΩ
		$V_{GS} = -2.5$ V, $I_D = -16$ A	−	3.7	6.4	
		$V_{GS} = -4.5$ V, $I_D = -22$ A, $T_J = 125$°C	−	3.6	5.4	
g_{FS}	Forward Transconductance	$V_{DD} = -5$ V, $I_D = -22$ A	−	16	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -6$ V, $V_{GS} = 0$ V, f = 1 MHz	−	0.89	1.25	nF
C_{oss}	Output Capacitance		−	1620	2270	pF
C_{rss}	Reverse Transfer Capacitance		−	1440	2015	pF
R_g	Gate Resistance		0.1	3.6	7.2	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	$V_{DD} = -6$ V, $I_D = -22$ A, $V_{GS} = -4.5$ V, $R_{GEN} = 6\ \Omega$	−	24	39	ns
t_r	Rise Time		−	37	60	ns
$t_{d(off)}$	Turn−Off Delay Time		−	193	309	ns
t_f	Fall Time		−	87	139	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{DD} = -6$ V, $I_D = -22$ A, $V_{GS} = -4.5$ V	−	71	99	nC
Q_{gs}	Gate to Source Charge		−	13	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	14	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -2$ A (Note 2)	−	−0.6	−1.2	V
		$V_{GS} = 0$ V, $I_S = -22$ A (Note 2)	−	−0.8	−1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -22$ A, di/dt = 100 A/μs	−	36	58	ns
Q_{rr}	Reverse Recovery Charge		−	19	33	nC

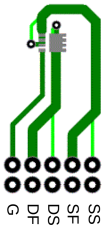
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

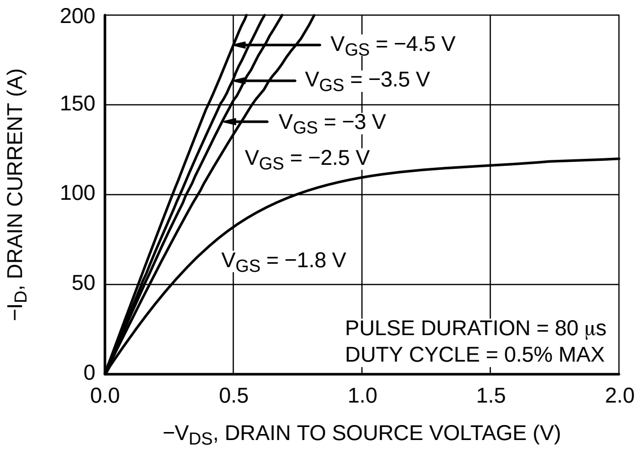


Figure 1. On Region Characteristics

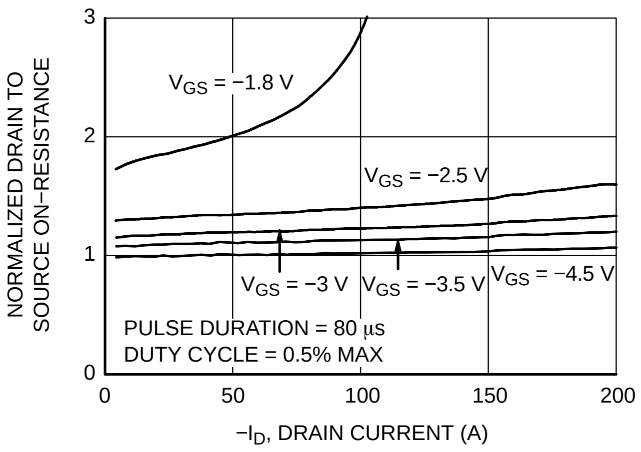


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

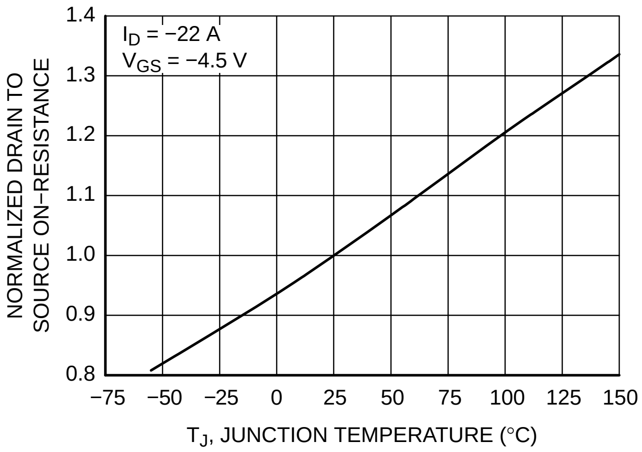


Figure 3. Normalized On Resistance vs. Junction Temperature

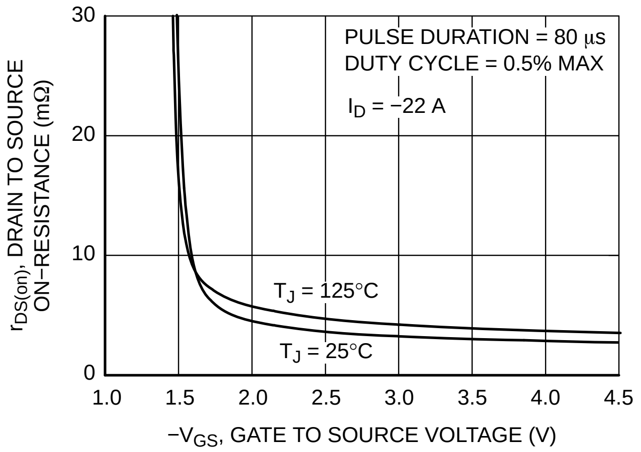


Figure 4. On−Resistance vs. Gate to Source Voltage

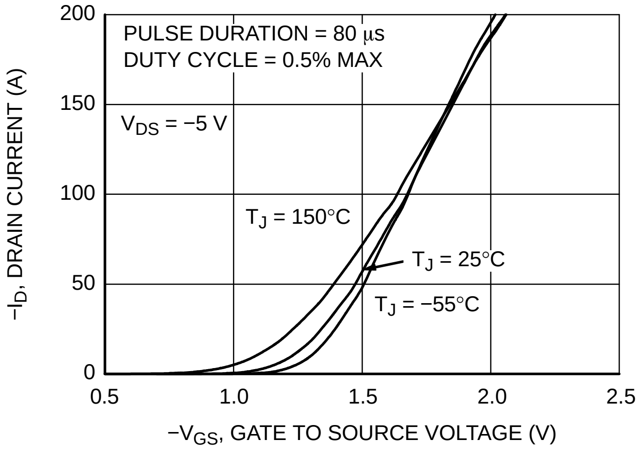


Figure 5. Transfer Characteristics

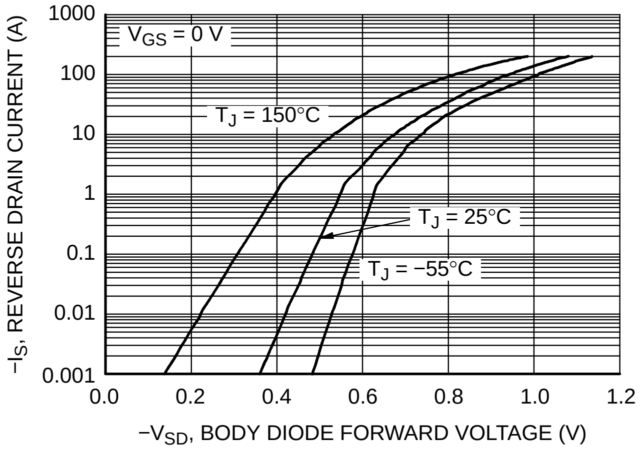


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

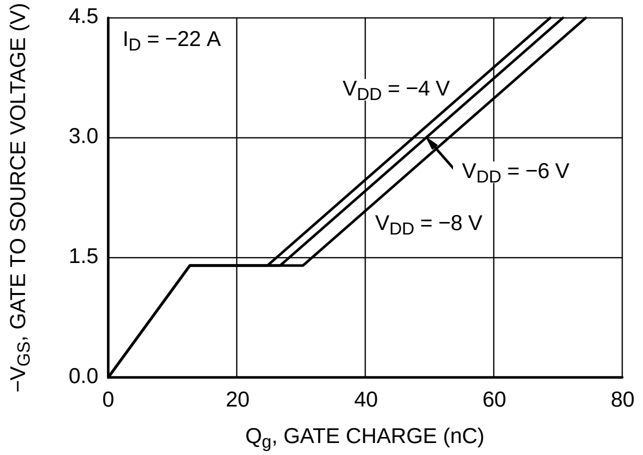


Figure 7. Gate Charge Characteristics

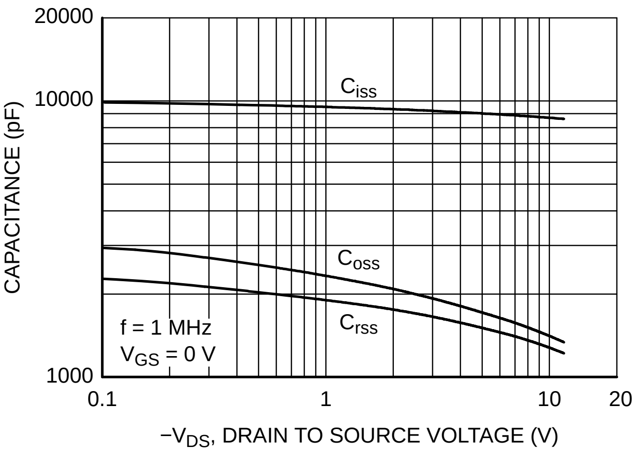


Figure 8. Capacitance vs. Drain to Source Voltage

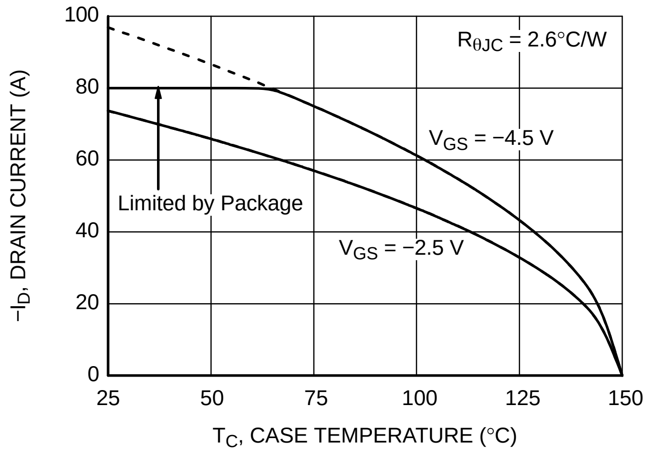


Figure 9. Maximum Continuous Drain Current vs. Case Temperature

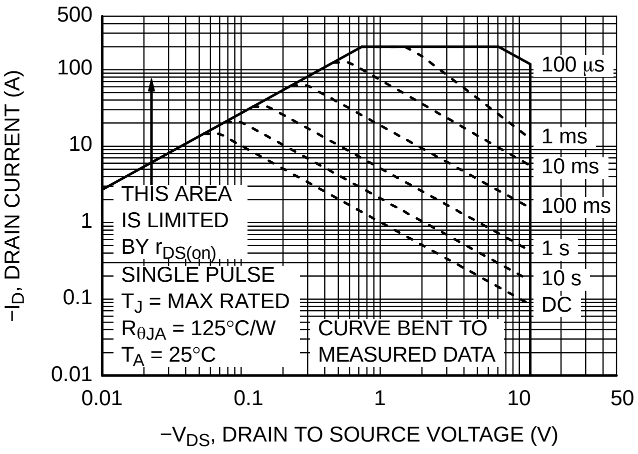


Figure 10. Forward Bias Safe Operating Area

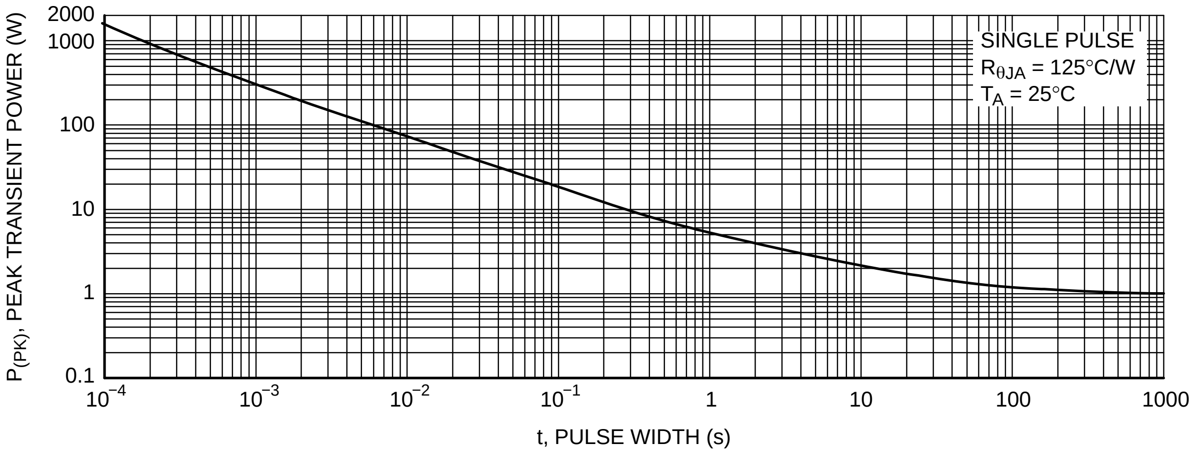


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

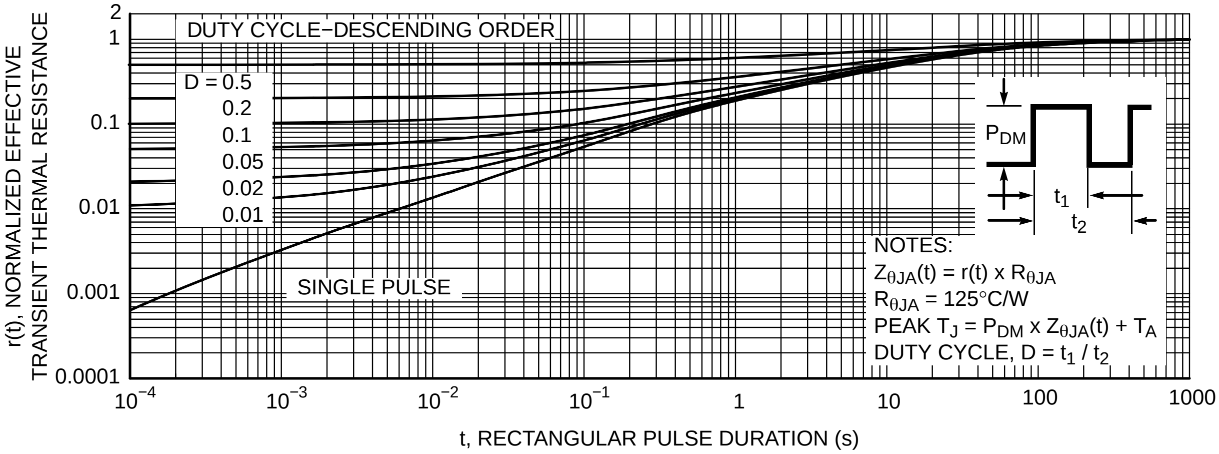


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC610P	23AB	PQFN8 3.3X3.3, 0.65P (Power 33) (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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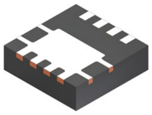
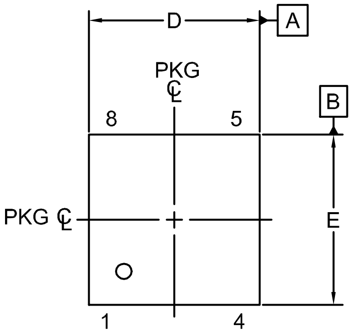
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

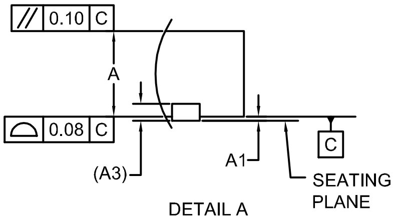


PQFN8 3.3X3.3, 0.65P
CASE 483AK
ISSUE B

DATE 12 OCT 2021



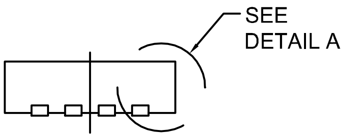
TOP VIEW



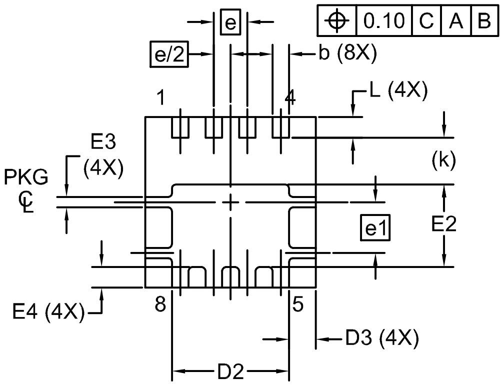
DETAIL A
SCALE: 2X

NOTES:

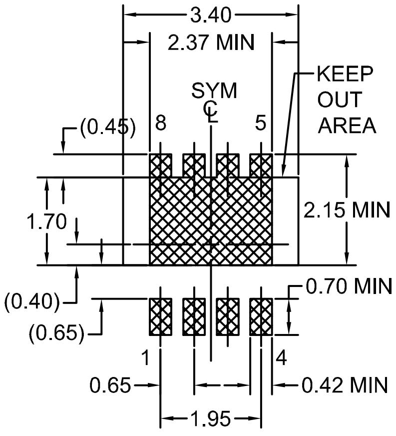
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



FRONT VIEW



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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