TO-247-4L
Half-Bridge Evaluation Board
Operation Manual

User's Guide

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＜High Voltage Safety Precautions＞

◇ Read all safety precautions before use

Please note that this document covers only the SiC MOSFET evaluation board (P02SCT3040KR-EVK-001) and its functions. For additional information, please refer to the Product Specification.

To ensure safe operation, please carefully read all precautions before handling the evaluation board



Depending on the configuration of the board and voltages used,

Potentially lethal voltages may be generated.

Therefore, please make sure to read and observe all safety precautions described in the red box below.

Before Use

[1] Verify that the parts/components are not damaged or missing (i.e. due to the drops).
[2] Check that there are no conductive foreign objects on the board.
[3] Be careful when performing soldering on the module and/or evaluation board to ensure that solder splash does not occur.
[4] Check that there is no condensation or water droplets on the circuit board.

During Use

[5] Be careful to not allow conductive objects to come into contact with the board.
[6] **Brief accidental contact or even bringing your hand close to the board may result in discharge and lead to severe injury or death.**

Therefore, DO NOT touch the board with your bare hands or bring them too close to the board.
In addition, as mentioned above please exercise extreme caution when using conductive tools such as tweezers and screwdrivers.

[7] If used under conditions beyond its rated voltage, it may cause defects such as short-circuit or, depending on the circumstances, explosion or other permanent damages.
[8] Be sure to wear insulated gloves when handling is required during operation.

After Use

[9] The ROHM Evaluation Board contains the circuits which store the high voltage. Since it stores the charges even after the connected power circuits are cut, please discharge the electricity after using it, and please deal with it after confirming such electric discharge.
[10] Protect against electric shocks by wearing insulated gloves when handling.

This evaluation board is intended for use only in research and development facilities and should by handled **only by qualified personnel familiar with all safety and operating procedures.**
We recommend carrying out operation in a safe environment that includes the use of high voltage signage at all entrances, safety interlocks, and protective glasses.

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SiC MOSFET Evaluation Board

TO-247-4L Half-Bridge Evaluation Board Operation Manual

For SiC MOSFET evaluation we are working with fast voltage and current slew rates, thus an appropriate evaluation environment is required. Unfortunately, it is almost impossible to get an evaluation board which fulfills all the required conditions when considering a device's new package.

Therefore, we have developed an evaluation board based on the most common circuit configuration known as a half-bridge circuit. In order to obtain appropriate evaluation conditions with simple preparation, this board is equipped with a driver circuit, an isolated power supply for the driver circuit, an over current protection circuit, Gate signal protection circuit and so forth.

In this application note the evaluation board operational guide for the TO-247-4L package will be explained. Additionally the detail information regarding topology, BOM, PCB layout, and electrical characteristics is described in the other application note. (TO-247-4L Half-bridge Evaluation Board Product Specification: No.62UG018E Rev.001)

1. Introduction

This board requires several external sources of power supply and input signals. In order to avoid any kind of malfunction or destruction, it is important to follow the power ON and power OFF sequences as shown in Figure 1.

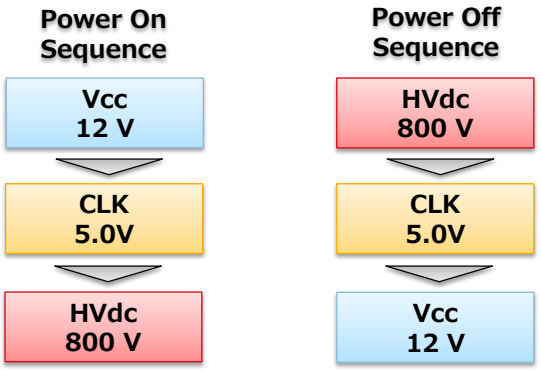


Figure 1. On/Off Sequences

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2. LED Indicators

In order to understand the operational condition of the board this evaluation board is equipped with several LED indicators. The location of the LEDs is shown in Figure 2, the indication details are described in Table 1 and LED status details for each occurred event are described in Table 2. Please note that if Alarm LED turns ON, the board goes into a Latch condition because of the external circuit fault. However, this board is equipped with a Reset button, push the button to clear the Latch condition.
After the abnormal condition is cleared, the board returns to a normal operating condition. The Latch is cleared by pushing the Reset button (non-lock type, push-button). Make sure to reset the OCP first if LS_FAULT and OCP LEDs turn ON at the same time.

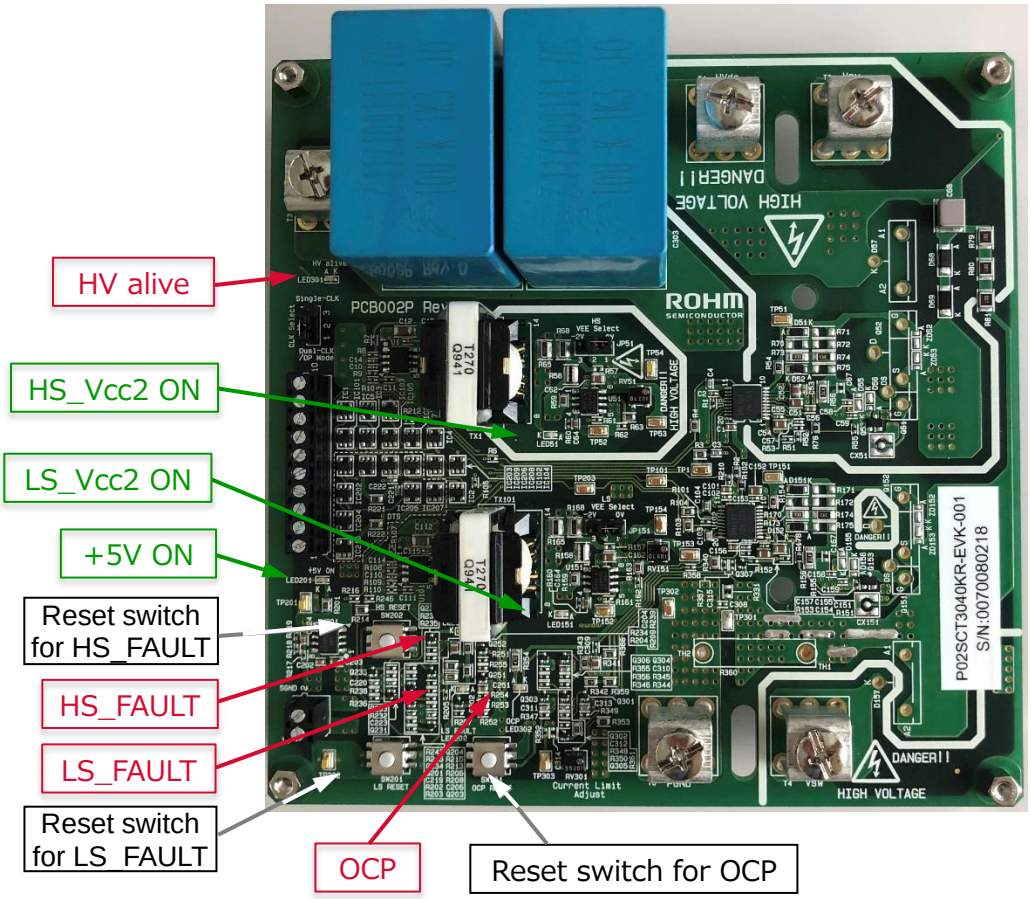


Figure 2. LEDs and Push-button switch Location

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Table 1. LED Indication

Indication	LED	Status	Details
HV alive	Red	ON	ON when HVdc is over 10V. This LED may still ON even if the HVdc is switched off. Do not touch the board if this LED is ON.
		OFF	HVdc is lower than 10V.
+5V_ON	Green	ON	ON during normal operation. Power supply for control (+12V) is applied.
		OFF	No power supply for control block.
HS_Vcc2_ON LS_Vcc2_ON	Green	ON	ON during normal operation. Isolated power supply for Gate drive is normally applied.
		OFF	No isolated power supply for Gate drive.
HS_FAULT LS_FAULT	Red	ON	ON when there is FLT signal output from driver IC.
		OFF	Normal operation.
OCP	Red	ON	Over current is detected at LS side MOSFT. LS_FAULT will also turn ON at the same time.
		OFF	Normal operation.

Table 2. FAULT LED Status Description

Status	LED Indication			Details
	HS_FAULT	LS_FAULT	OCP	
HS Side Failure	ON	--	--	● HS Gate-Source is shorted ● HS DESAT is detected ● HS Gate isolated power supply (Vcc2_HS) UVLO is detected ● INA_HS signal and OUT_HS signal are logically unmatched.
LS Side Failure	--	ON	--	● LS Gate-Source is shorted ● LS DESAT is detected ● LS Gate isolated power supply (Vcc2_LS) UVLO is detected ● INA_LS signal and OUT_LSI signal are logically unmatched. ● Need to supply drain current (more than 30usec and 30A) [NOTE1]
OCP	--	ON	ON	● LS OCP is detected (Only current flowing through Drain ➔ Source will be detected)

[NOTE1] Level shift amount of VTSIN signal from OCP circuit is determined by the resistor where is mounted at R359. (470Ω)
In case above 30A drain current supplies for low side MOSFET, GND level at OCP circuit becomes lower.
Then level shift amount of VTSIN signal from OCP circuit will be less than the detection level and LS_FAULT will turn on.
If pulse width more than 10usec is inputted, the resistance value at R359 has to be changed to 2.2kΩ

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3. OCP Setting

3.1 OCP Detection Signal

Over Current Protection (OCP) circuit detects the voltage drop across the current sense resistor mounted between LS MOSFET Source and PGND, inputs the OCP detection signal to VTSIN input (pin 01) of LS MOSFET driver IC (U102), generates the FLT signal at the input signal side, and makes all the CLK signals invalid including at the HS side.

OCP circuit is shown in Figure 3.

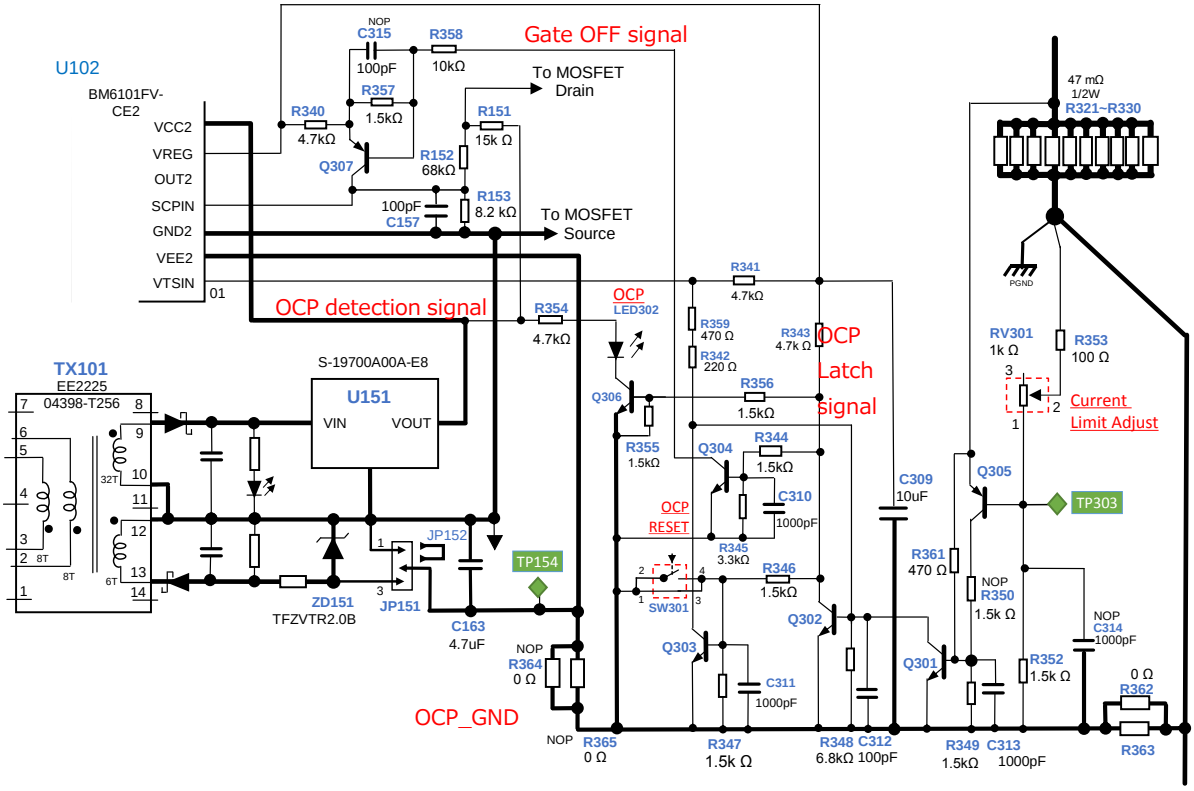


Figure 3. OCP Circuit

In order to minimize the power consumed by the current sense resistor, the OCP circuit is designed to be able to operate with negative bias drive, but VTSIN signal takes GND2 (pin 03) as a base, thus, it is not possible to input the OCP detection signal directly to VTSIN input in case of negative bias drive. Resistors (R341, R342, R359) for level-shifting are interconnected with OCP signal to the VTSIN pin, it is required to adjust this level-shifting circuit when changing the bias voltage. Resistor value for each bias voltage is shown in Table 3. Furthermore, OCP detected point can be adjusted during the negative bias, remove the resistor R361 to make it possible. Also R353 has to be changed in value at the same time due to a change of the OCP adjustable range.

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OCP circuit configuration consists of transistors for start-up (Q301, Q305), transistor for Latch (Q303), transistor for Gate OFF (Q304), and transistor for LED indication (Q306). Furthermore, the resistors R362/R363 and R364/R365 to select the OCP circuit GND are available. Table 4 shows the relation between the bias voltage and mounted resistors. Default setting is Zero bias.

Table 3. Level-shifting Resistor Adjustment

Bias Voltage	R341	R342	R359	R353	R361	Remarks
Zero bias	4.7k	220	470	100	470	No OCP Adjustment
-2V		220	2.2k	100	Not mounted	Adjust at RV301
-3.0V		470	3.3k	56		
-3.6V		220	4.7k	47		
-4.0V		220	5.6k	39		

Table 4. OCP GND Setting Based on Bias Voltage

Bias Voltage	R362	R363	R364	R365
Zero bias	0Ω	0Ω	Not mounted	Not mounted
Negative bias	Not mounted	Not mounted	0Ω	0Ω

In addition, to minimize the time taken from OCP circuit start-up until LS MOSFET turns OFF, the driver IC (U102) SCPIN voltage will be directly set high using the Gate OFF signal, MOSFET Gate signal can be cut off within 1us after the start-up of the SCP. However, when OCP circuit operates, the OCP Latch circuit will operate. OCP condition continues and turns ON the LED302 (red) even though the MOSFET Gate signal has been cut off. After the cause of the OCP occurrence is cleared, the Latch circuit can be reset by pushing the Reset switch (SW301).

Location of the OCP Reset switch and the resistors for the adjustment are shown in Figure 4.

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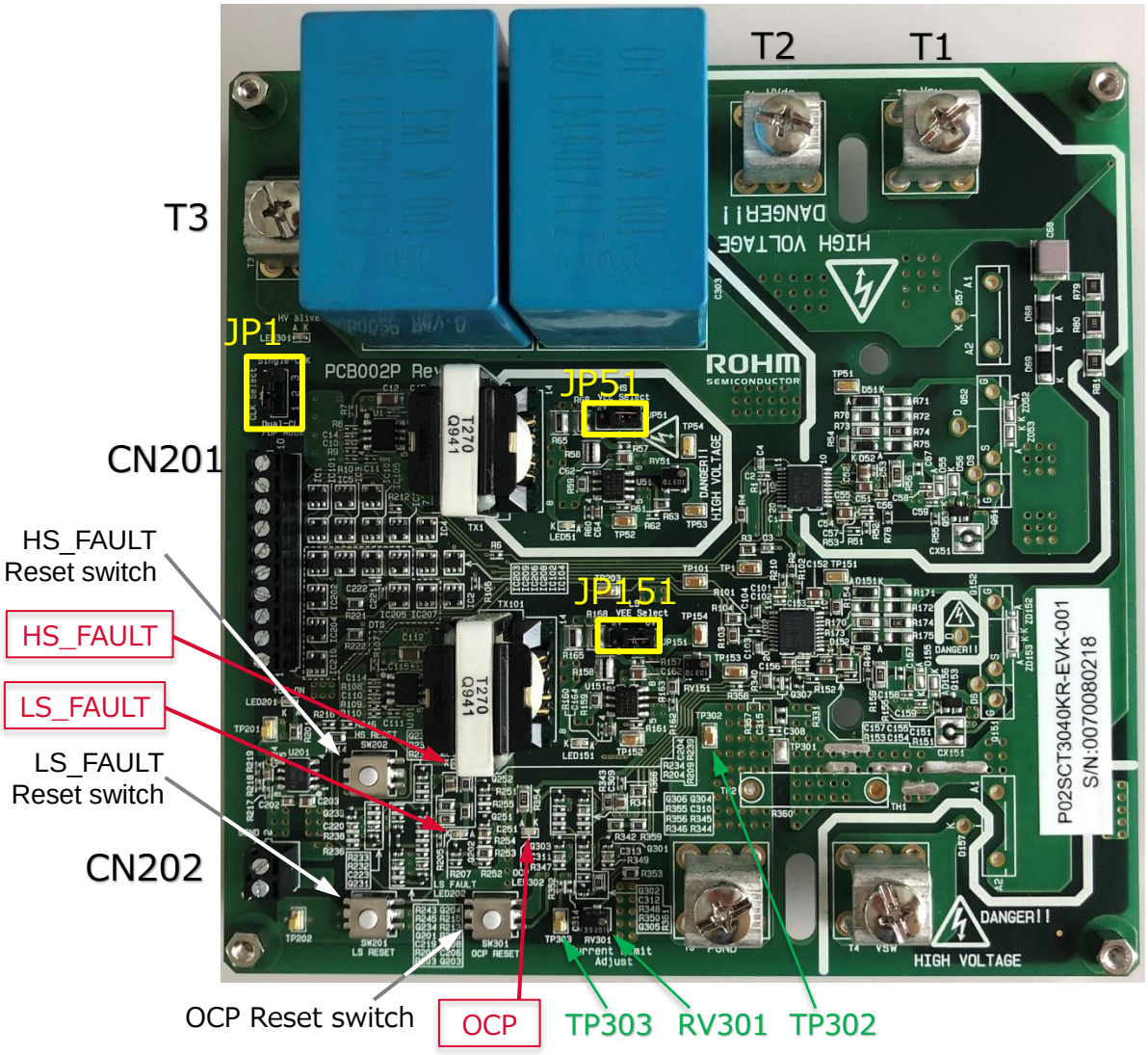


Figure 4. Connector and OCP Adjustment Circuit

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3.2 Setting at Zero Bias

OCP setting during zero bias is not possible. Thus, the OCP setting current I_{OCP} is estimated as below:

$$I_{OCP} = ((R361//R350)+R349)/R349*V_{BE_Q301}/0.0047 = 171A$$

3.3 Setting at Negative Bias

During negative bias, OCP point can be adjusted by adjusting the value of adjustable resistor RV301.

The procedure is as below:

- Connect a digital multi-meter between TP303 and TP302. (GND is at TP302 side)
- Turn RV301 in the clockwise direction while reading the voltage value (V_{BEMIN}) in which turns ON the LED for OCP. The LED turns ON when the voltage is around -0.65V.
- Turn RV301 in the counter-clockwise direction several times, push the OCP Reset button to turn OFF the OCP LED.
- Adjust the RV301. Based on TP303 voltage V_{TP303}, I_{OCP} is set as follows:

$$V_{TP303} = V_{BEMIN} + I_{OCP}*0.0047$$

I_{OCP} becomes smaller by turning the RV301 in the clockwise direction.

Table 5. OCP Setting Voltage Example

I_{OCP}	V_{TP303}
50 Amps	- 0.415 V
70 Amps	- 0.320 V
90 Amps	- 0.230 V
110 Amps	- 0.130 V
130 Amps	- 0.030 V

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The OCP start-up sequence example at negative bias is shown in Figure 5.

■ OCP setting: 53A (Voltage between TP 303-TP302: 0.4V)

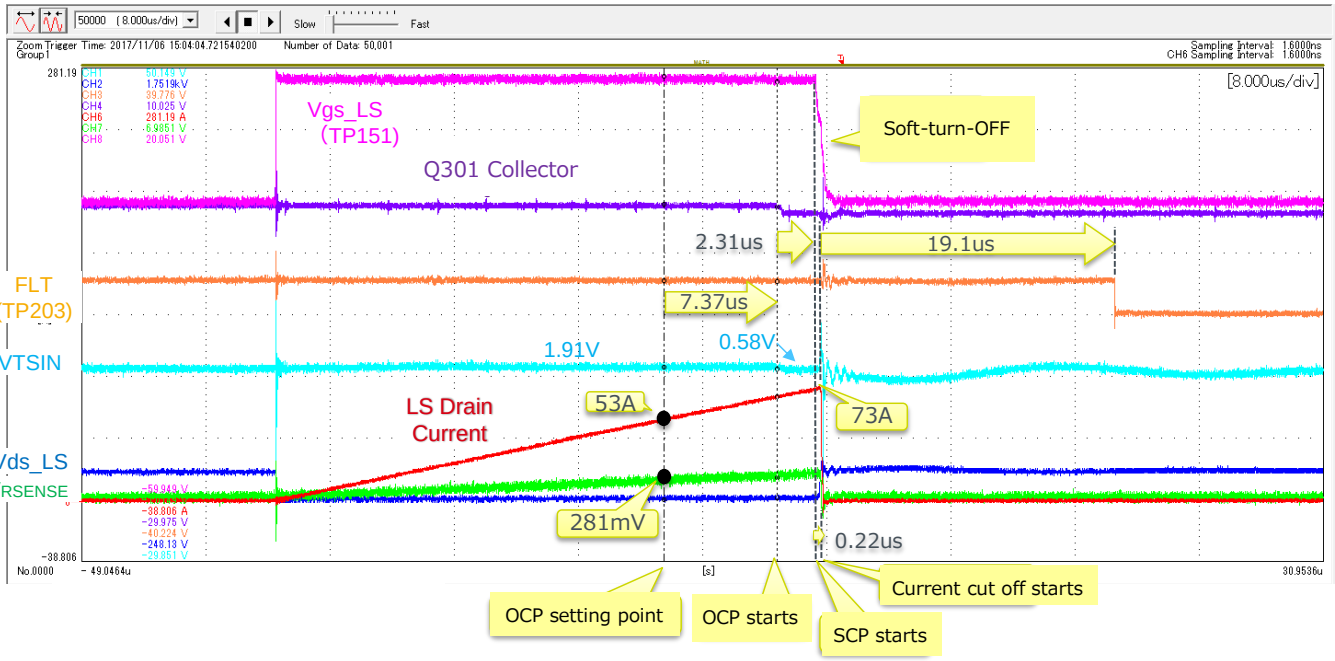


Figure 5. OCP start-up sequence

The setting value of V_{TP303} is -0.4V, thus the OCP setting point is 53A. Drain current increases when drive voltage 18V is applied to the Gate voltage Vgs_LS. Since the same current is flowing to the current sense resistor, the drain current also increases proportionally with the voltage V_{SENSE} occurs between both ends of the resistor. It becomes the OCP setting point if the V_{SENSE} voltage reaches 281mV, and turns ON Q305, but it takes around 7.37us to turn ON the Q301. This is because the base voltage of Q301 is supplied with R349 and R350 divided voltage, if the negative bias voltage is low, the time taken to reach the voltage which turns ON the Q301 V_{BE} becomes longer.

Next, when the Q301 is turned ON (around 2.31us after the OCP circuit started up) operation to turn OFF the LS side Gate signal starts when SCP circuit of the driver IC is activated. Here, the operation is based on soft-turn-off, thus, overshoot of the MOSFET Drain voltage can be suppressed. Approximately 19us after the SCP is activated, FLT signal at the input side starts and turns ON the LS_FAULT LED (red).

As explained above, since there is some delay time between overcurrent detection and when the Gate drive stops, the current will keep increasing for some time, thus, it is important to consider the actual delay time on the actual board.

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4. Connector Pin Assignments

Connectors' pin assignment is shown in Figure 6.

Each signal and power supply pin description are described in Table 6 and Table 7.

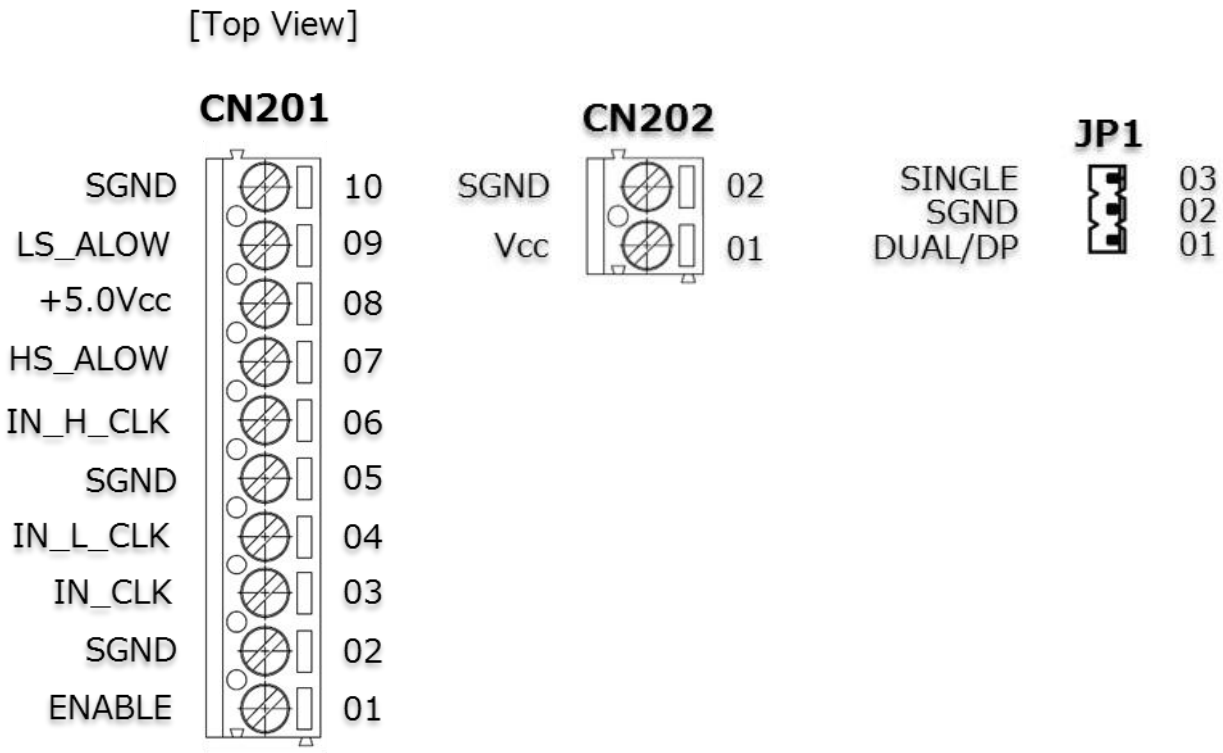


Figure 6. Connector Pin Assignment

Table 6. Power Supply Pin Description

Power Supply Pin	Signal	Description
T1	HVdc	High voltage input pin. It functions as the Input pin in Buck or Inverter topology, but functions as the Output pin in Boost topology.
T2 T4	Vsw	HS MOSFET Power Source pin and LS MOSFET Drain pin It is connected inside the board, thus cutting off this connection is not possible.
T3 T5	PGND	Power GND pin It is connected with input signal side SGND. Cutting off this connection is possible.

Table 7. Signal Description

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Connector	Pin	Symbol	I/O	Details
CN201	01	ENABLE	I	Driver ICs U2 and U102 shared Enable pin (individual control is not required) Active (Driver IC operates) when this signal is Low. It is being pulled up with 2.2kΩ resistor at +5V when OPEN.
	02	SGND	--	Input signal side GND. It can be completely separated from DUT side GND.
	03	IN_CLK	I	ON/OFF signal for HS and LS MOSEFT. High: HS MOSFET turns ON, LS MOSFET turns OFF. Low: HS MOSFET turns OFF, LS MOSFET turns ON. Only valid when connector「JP1」is set to "Single-CLK Mode" side. It is being pulled down with 2.2kΩ resistor when OPEN.
	04	IN_L_CLK	I	ON/OFF signal for LS MOSFET. ON when this signal is High. Only valid when connector「JP1」is set to "Dual-CLK/DP Mode" side. It is being pulled down with 2.2kΩ resistor when OPEN.
	05	SGND	--	Input signal side GND.
	06	IN_H_CLK	I	ON/OFF signal for HS MOSFET. ON when this signal is High. Only valid when connector「JP1」is set to "Dual-CLK/DP Mode" side. It is being pulled down with 2.2kΩ resistor when OPEN.
	07	HS_ALOW	I	Logic invert signal for "IN_H_CLK". HS MOSFET is ON when this signal is High, and "IN_H_CLK" signal is Low It is being pulled down with 2.2kΩ resistor when OPEN.
	08	+5Vcc	--	Output pin for control block power supply (+5V). Maximum output is 20mA. Used for input signal pull-up.
	09	LS_ALOW	I	Logic invert signal for "IN_L_CLK". LS MOSFET is ON when this signal is High, and "IN_L_CLK" signal is Low. It is being pulled down with 2.2kΩ resistor when OPEN.
	10	SGND	--	Input signal side GND.
CN202	01	Vcc	--	Power supply pin for driver IC and internal control block. Voltage for Gate drive is generated internally from this power supply.
	02	SGND	--	Input signal side GND.
JP1	01	DUAL/DP	I	Signal to set to "Dual-CLK/DP Mode". "IN_x_CLK" signal becomes valid when this pin is Low. It is being pulled up to +5Vcc with 2.2kΩ resistor when OPEN.
	02	SGND	--	Input signal side GND.
	03	SINGLE	I	Signal to set to "Single-CLK Mode". "IN_CLK" signal becomes valid when "DUAL/DP" signal is other than Low. OPEN condition when it is OPEN.

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5. CLK Select Function (JP201 Setting)

It is important to prevent simultaneous activation of the HS and LS Gates of the MOSFETs when using a half-bridge configuration. For this evaluation board, selection between Single-CLK Mode that allows driving with a single external signal while preventing the HS and LS simultaneous ON condition, or Dual/DP-CLK Mode that allows ON/OFF driving individually is possible. The selection can be done by using the JP201 jumper.

- When Single-CLK Mode is selected, only "IN_CLK" signal is valid.
- When Dual/DP-CLK Mode is selected, "IN_H_CLK" signal for driving the HS side and "IN_L_CLK" signal for driving the LS side is valid. Even though HS and LS simultaneous ON prevention circuit is included during this mode, there is no dead time period.
- Select DUAL/DP-CLK Mode when performing double-pulse test, drive either HS or LS.

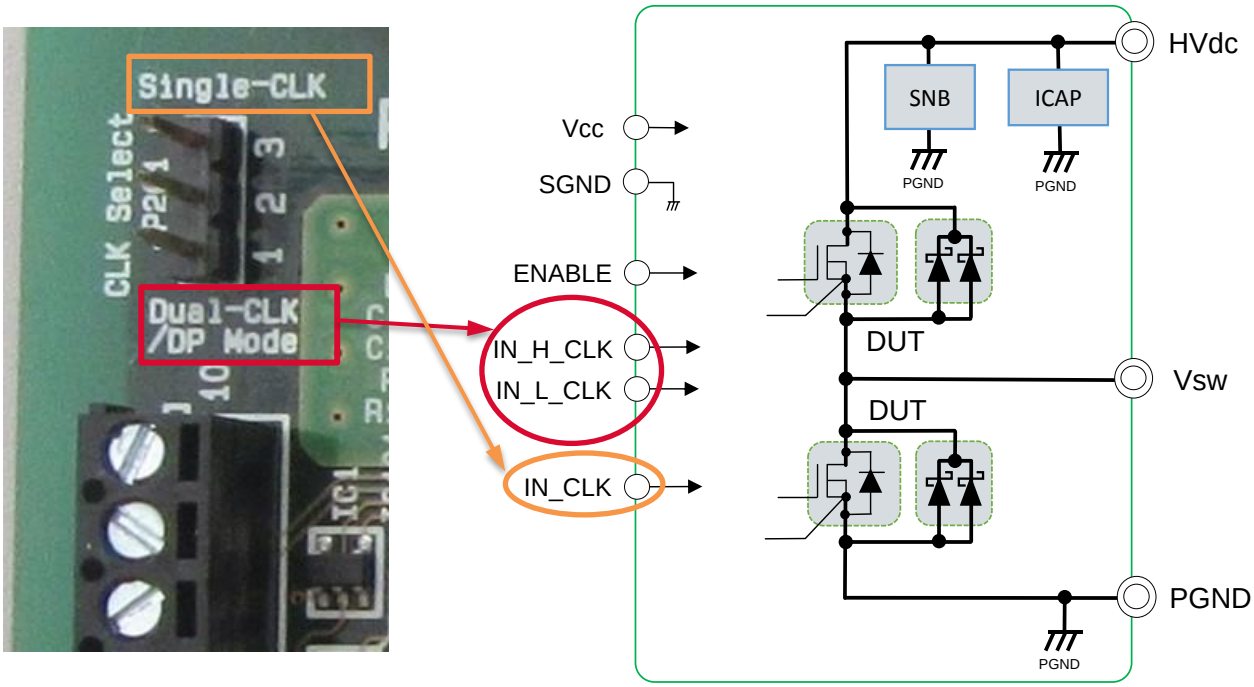
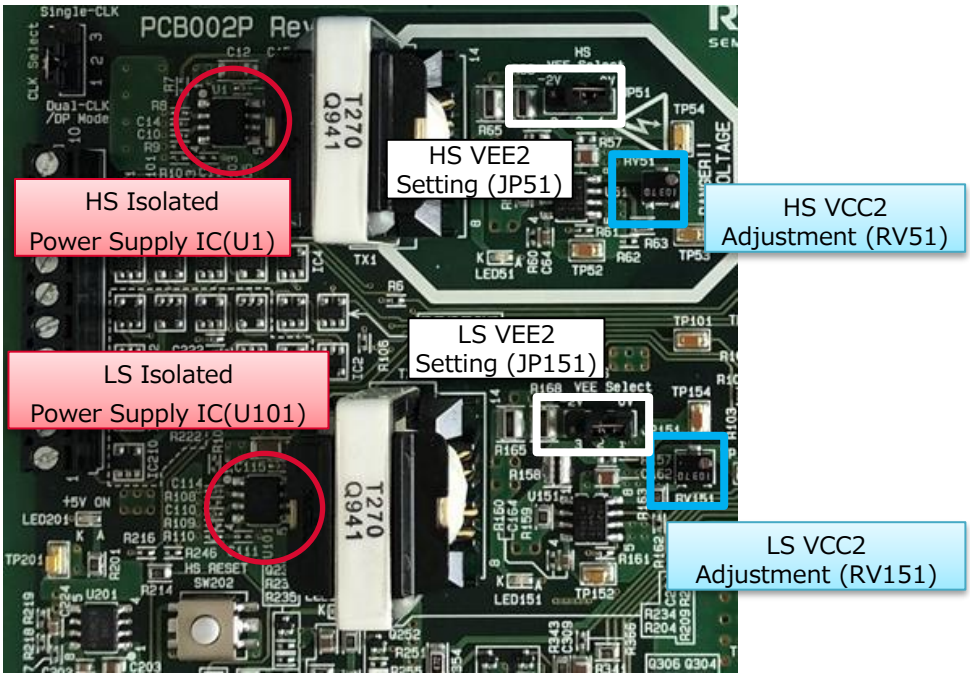


Figure 7. CLK Select Function

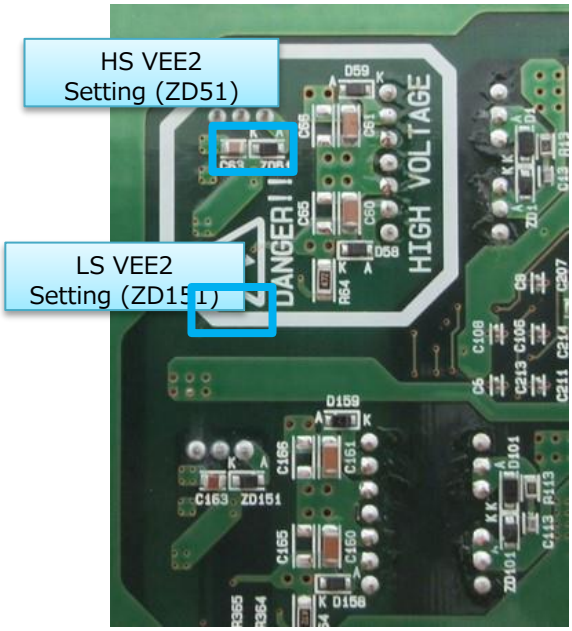
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6. Gate Drive Voltage Setting

Gate drive voltage is supplied by the isolated type Flyback power supply mounted on the board. ROHM's optocoupler-less control IC (BD7F200EFJ) is used for this Flyback power supply. In addition, transformers to output positive/negative drive voltage for each LS and HS are included. On-board power supply layout is shown in Figure 8.



a) TOP VIEW



b) BOTTOM VIEW

Figure 8. Gate Power Supply

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6. 1 Positive Bias (VCC2) Adjustment

Isolated Flyback power supply transformers (TX1, TX101) are used to generate both positive and negative voltages. The MOSFET drive voltage (positive bias) VCC2 is generated through a LDO Regulator from the transformer's positive output. The LDO Output voltage is adjustable by adjusting the RV51 and RV151 resistor values. Turning the adjustable resistor in the clockwise direction increases the output voltage. Please note that the setting range is from 10.35V to 20.56V, but the UVLO of the VCC2 operates at 11.5V (typical), therefore pay attention when reducing the voltage.

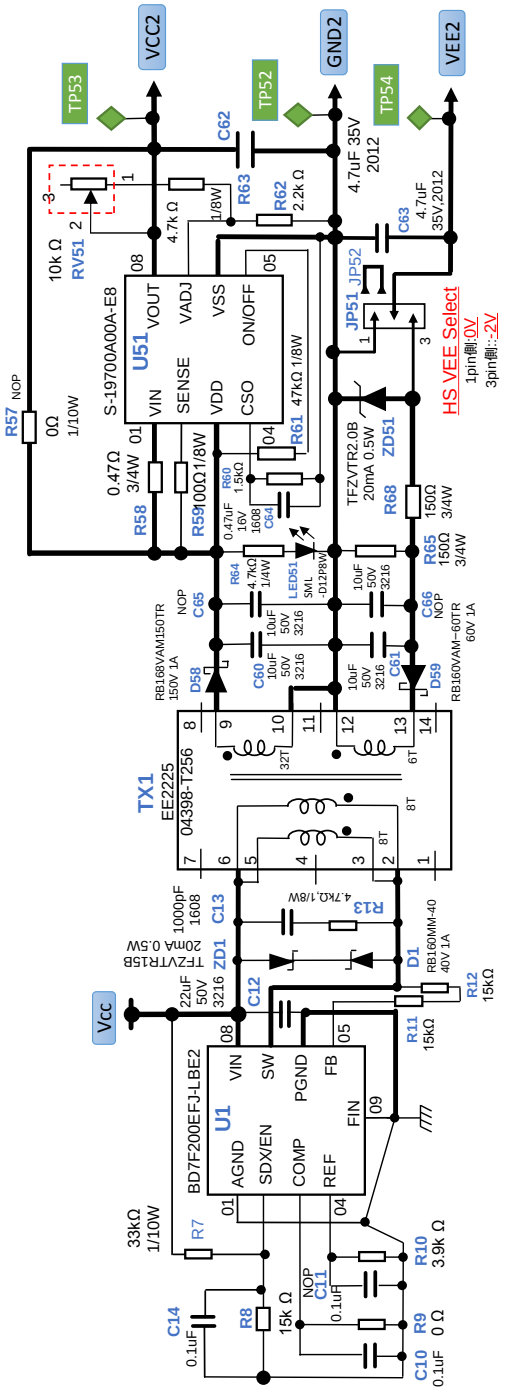


Figure 9. Gate Drive Power Supply Circuit (HS side)

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Moreover, the output of the transformers can also be used without the LDO. It can be done by mounting 0Ω resistors at R57 and R157 and removing the R61 and R161 resistors. In this case, LDO output is OFF and transformers' output is directly output to VCC2. Please note that the transformers' output is around 23.3V.

6. 2 Negative Bias (VEE2) Adjustment

Bias voltage during MOSFET OFF (negative bias VEE2) is stabilized at -2V from the negative voltage of TX1 and TX101 transformers by using ZD51 and ZD151 Zener diodes (ROHM: TFZVTR2.0B). VEE2 is supplied through JP51 and JP151 negative bias setting pins. Zero bias and -2V bias can be selected and the setting is shown in Table 8.

Table 8. Negative Bias (VEE2) Setting

Connector	Pin No.	Symbol	Details
JP51	01	HS_GND2	HS MOSFET Driver Source pin。
	02	HS_VEE2	HS negative bias supply pin (VEE2). Do not make it OPEN.
	03	HS_N2V	HS negative bias power supply pin. Default setting is -2V, generated at ZD51. Max -4.3V setting is possible.
JP151	01	LS_GND2	LS MOSFET Driver Source pin.
	02	LS_VEE2	LS negative bias supply pin (VEE2). Do not make it OPEN.
	03	LS_N2V	LS negative bias power supply pin. Default setting is -2V, generated at ZD151. Max -4.3V setting is possible.

In addition, the setting of negative bias can be done by changing the ZD51 and ZD151, but the negative output of the transformers is around -4.3V, thus the adjustment can only be done within 0V~-4.3V range. Furthermore, the negative voltage also can be supplied directly from the transformers by shorting the R68 and R168 resistors and removing ZD51 and ZD151 diodes. Arbitrary negative voltage setting using ROHM Zener diodes is shown in Table 9.

Table 9. Zener Diodes and Resistors for Negative Bias Voltage Adjustment

Setting Voltage	ZD51, ZD151	R68, R168
-2.4V	TFZVTR2.4B	120 ohm
-3.0V	TFZVTR3.0B	82 ohm
-3.6V	TFZVTR3.6B	47 ohm
-4.0V	Not Mounted	0 ohm

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7. Gate Resistor Adjustment

MOSFET switching speed can be adjusted by using the Gate resistors. In addition, the speed for HS and LS can be set individually.

Turn ON: HS (R70, R71, R72, D51)
LS (R170, R171, R172, D151)
Turn OFF: HS (R73, R74, R75, D52)
LS (R173, R174, R175, D152)

The circuit configuration allows the adjustment of the device characteristics switching speed.

The drive circuit mounting condition is shown in Figure 10, and the circuit diagram is shown in Figure 11.

The MOSFET is driven by ROHM's MOSFET driver IC (BM6101FV-C) output signal through the Gate resistors. It is better to shorten the wiring of the driver circuit pattern as it's inductance affects the surge voltage characteristics of the Gate-Source signal. However, this evaluation board allows the individual setting of Gate resistors at turn ON and turn OFF to support various driving conditions.

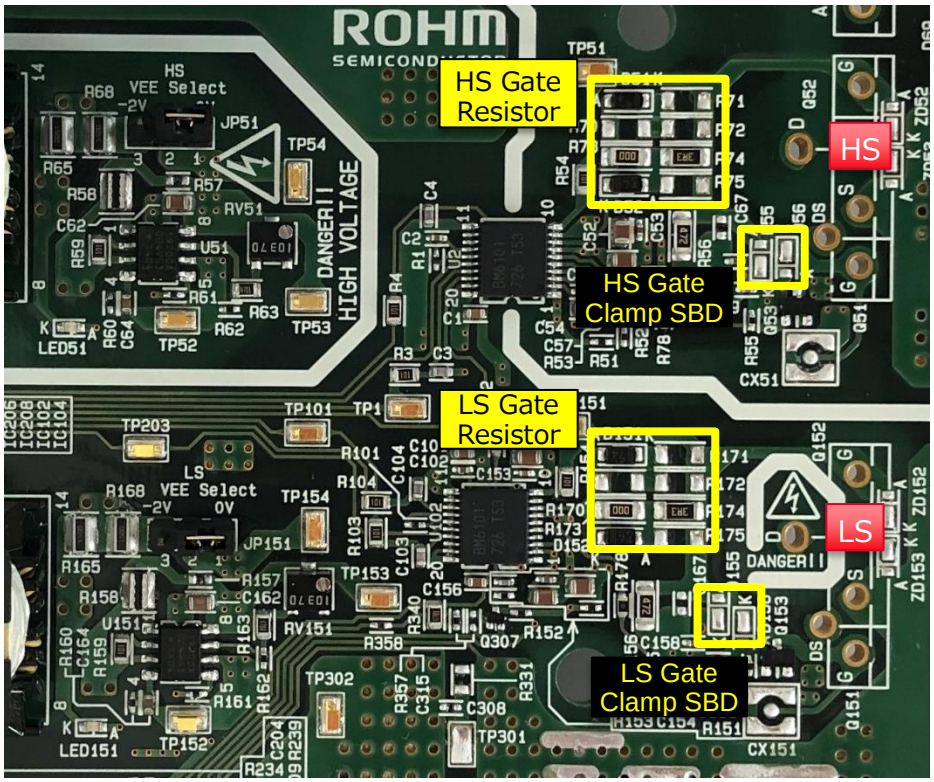


Figure 10. Gate Drive Circuit Mount Condition

When turn ON and turn OFF switching speed of the MOSFET is set individually, the drive signal is sent to the MOSFET through D51 and D151 diodes for turn ON, and through D52 and D152 diodes for turn OFF. Here, R70, R73, R170 and R173 resistors are not mounted, switching speed is set by R71, R72, R171 and R172 resistors.

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Furthermore, switching speed adjustment can also be done by using either D51 (D151) or D52 (D152). For example, to set the turn ON slower, use D52 (D152) for diodes, and R73 (R173), R74 (R174), R75 (R175) for resistors. Here, the total gate Resistances are R73 (R173) + R74 (R174) // R75 (R175) for the turn ON, and R74 (R174) // R75 (R175) for the turn OFF. Turn ON switching speed can set slower by adjusting the R73 (R173) resistors' value. In case of setting the turn OFF slower, use D51 (D151) for diodes, and use the same setting method as explained for turn ON. Default setting for this board is adjusted by R74 (R174), hence, the same speed for turn ON and OFF.

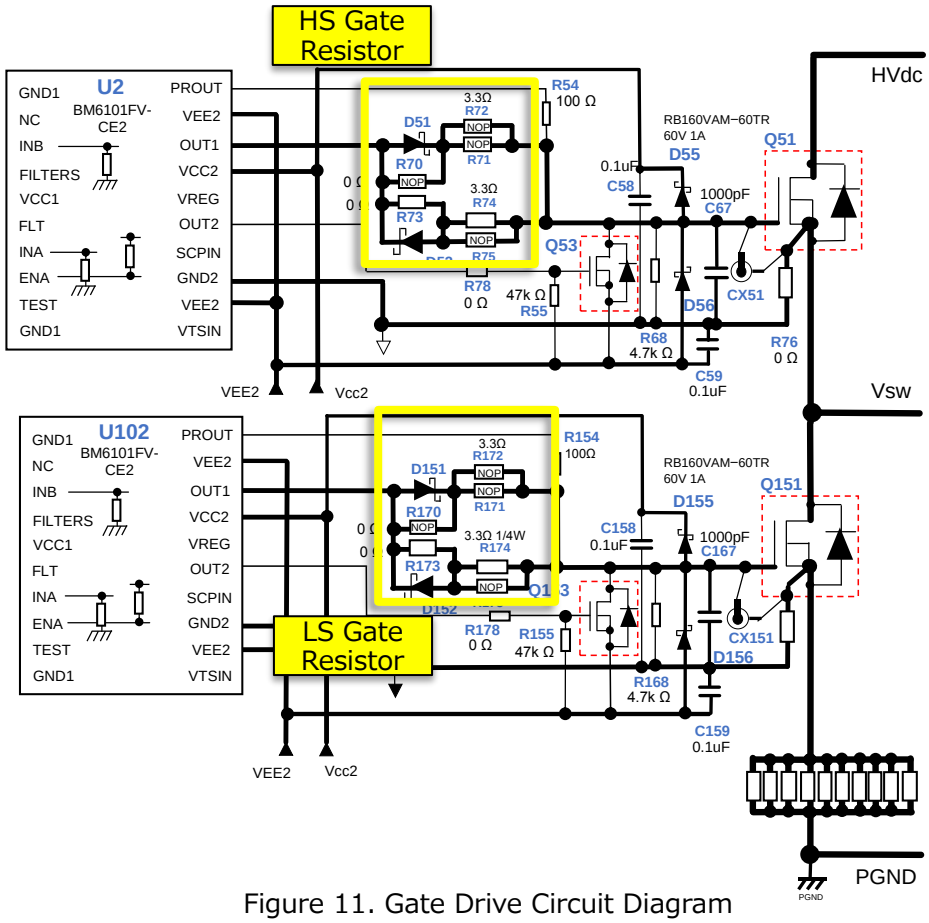


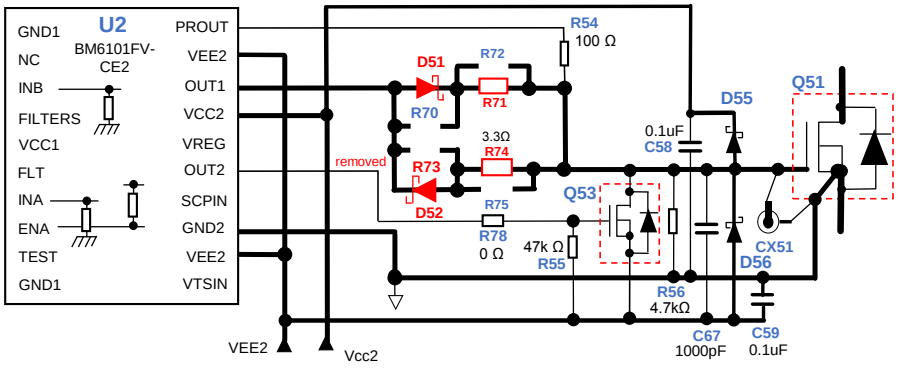
Figure 11. Gate Drive Circuit Diagram

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A specific example of the adjustment is shown in Table 10. However, there are also adjustments other than the example shown in the Table 10.

Table 10. Gate Drive Speed Adjustment

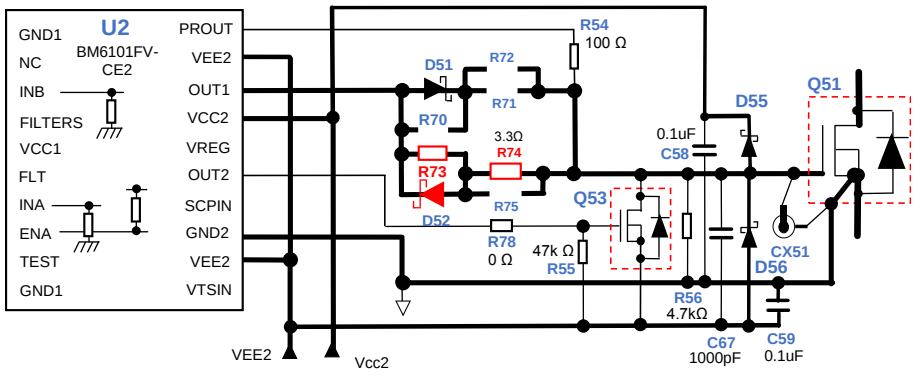
Turn ON Turn OFF Setting	Gate Drive Circuit Resistor and Diode (Mount/No Mount)								Gate Resistor Setting Value (HS)	
	D51 / D151	R70 / R170	R71 / R171	R72 / R172	D52 / D152	R73 / R173	R74 / R174	R75 / R175	Turn ON	Turn OFF
Individual Adjustment	Mount	No mount	Mount	Mount	Mount	No mount	Mount	Mount	R71//R72	R74//R75
Slower Turn ON Faster Turn OFF		No mount	No mount	No Mount		Mount	Mount	Mount	R73 + R74//R75	R74//R75
Faster Turn ON Slower Turn OFF		Mount	Mount	Mount		No mount	No mount	No mount	R71//R72	R70 + R71//R72
Same for Turn ON/OFF		No mount	No mount	No mount		Mount 0 ohm	Mount	Mount	R74//R75	
		Mount 0 ohm	Mount	Mount		No mount	No mount	No mount	R71//R72	
Default setting (Same ON/OFF)	Mount	No mount	No mount	No mount	Mount	0 ohm	3.3 ohm	No mount	3.3 ohm	3.3 ohm



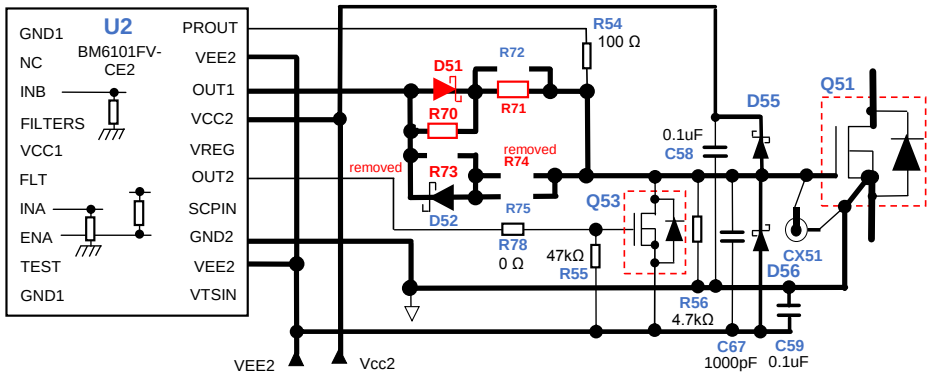
a) Individual Adjustment for both Turn-On and Turn Off

Figure 12. Gate Resistor Setting Example

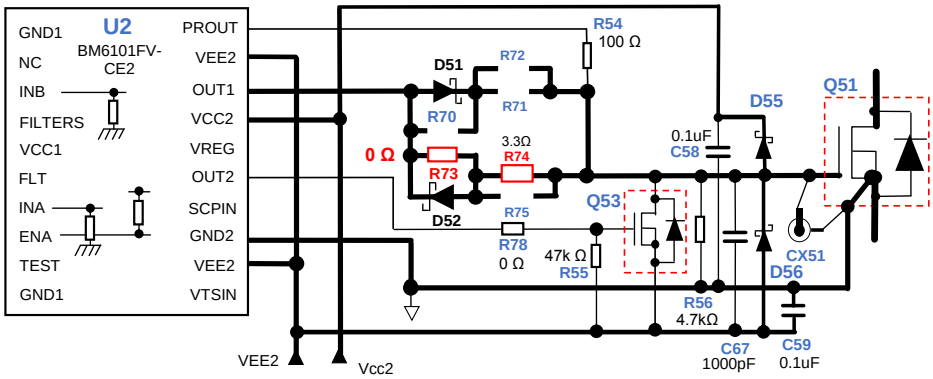
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b) Slower Turn-On, Faster Turn-Off



c) Faster Turn-On, Slower Turn-Off



d) The same Turn-On and Off（Default）

Figure 12. Gate Resistor Setting Example

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8. Dead Time Adjustment

Although HS and LS ON/OFF by IN_CLK signal is possible when「Single-CLK」Mode is selected from CLK Select function, it is important to prevent simultaneous turn ON of HS and LS. Therefore, a dead time in which both the HS and LS are OFF needs to be included.

This evaluation board includes a dead time generator circuit, and it can be set using resistors R221 and R222. The default setting for this board is 470Ω, setting the dead time to be around 300ns. The allowable minimum setting for this resistor is 220Ω, giving a dead time of around 270ns.

Resistors R221 and R222 must be set with the same value and the value has to be set by verifying there is NO shoot-through current caused by a simultaneous ON condition. Setting resistors mounting location is shown in Figure 13 and relation between setting resistor and dead time period is shown in Figure 14.

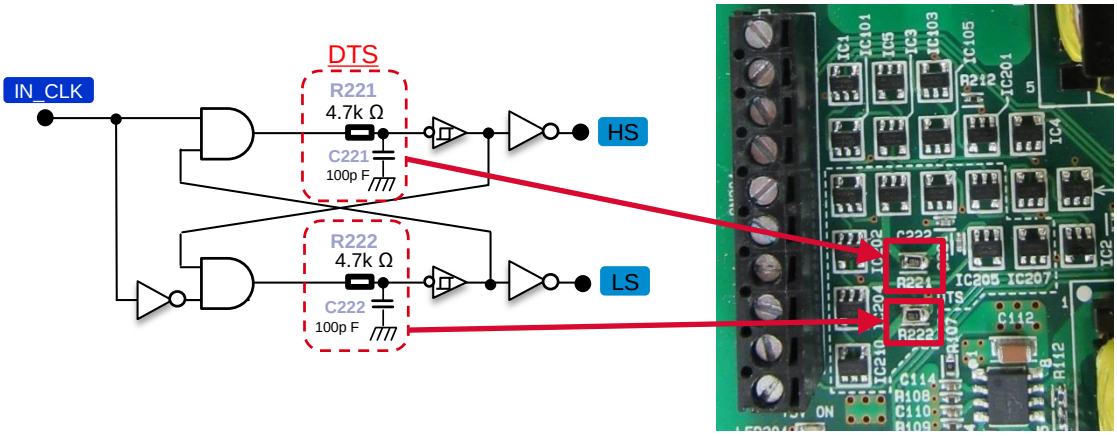


Figure 13. Dead Time Setting Resistor

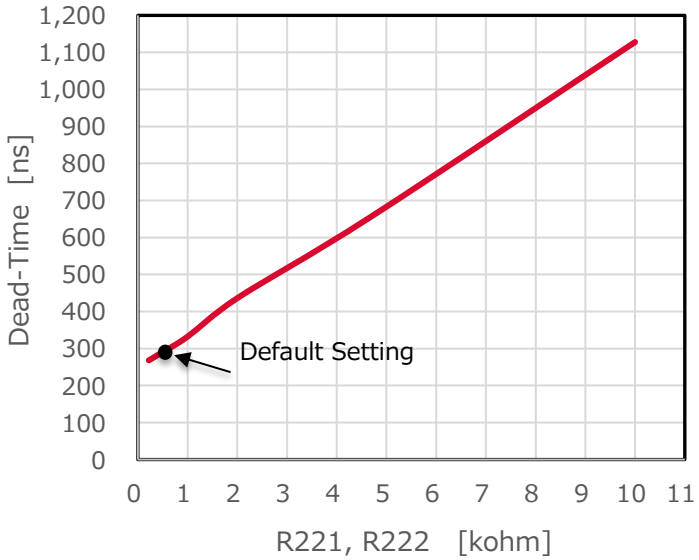


Figure 14. Dead-Time Characteristics by R221/R222 Setting

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9. Device Current Measurement

There are two through-holes (no plating) for each HS and LS on this evaluation board to allow the current flowing to each device to be easily measured using a Rogowski current probe. It is possible to measure the current at the Drain pin for the HS and at the Power Source pin for the LS. The image of the through-holes as well as the probing method are shown in Figure 15:

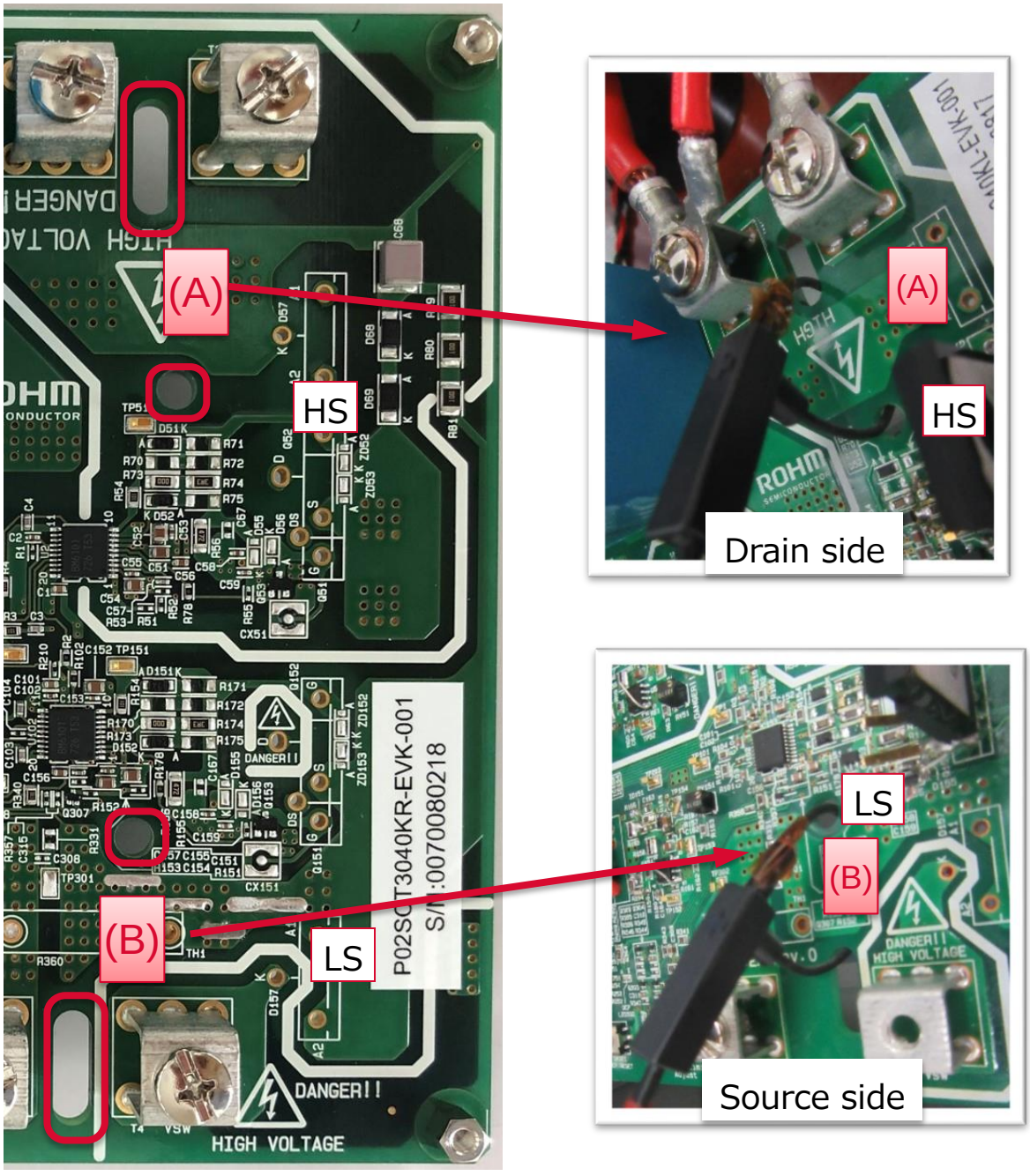


Figure 15. Measurement Using Rogowski Current Probe

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Rogowski current probes have various loop diameters, the suitable diameter for this evaluation board is shown in Figure 1, 25mm~30mm for the circle diameter, and less than 3mm for the wire diameter. The dimension of the through-holes is shown in Figure 17.



Figure 16. Rogowski Current Probe Suitable Loop Size

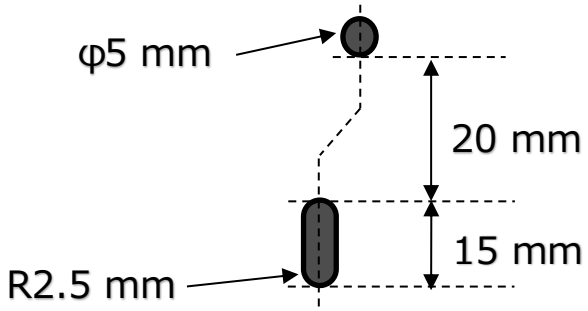


Figure 17. Through-holes for Rogowski Current Probe Dimension

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10. DUT Selection

Although this evaluation board is designed based on TO-247-4L package as the DUT, TO-247N(3L) package can also be mounted as the DUT with evaluation environment under the same conditions.

Shared drive circuit (HS) is shown in Figure 18. Q51 is for TO-247-4L and Q52 is for TO-247N. Each pin is connected, but the Q52 Gate circuit return line (return loop to GND2) is separated by R77 resistor (R177 for LS) to avoid the merging of Power Source pin and return line when 4L DUT is mounted. R77 (R177) are not mounted on this board as default, mount these resistors to perform the evaluation on 3L DUT.

The mounting location and lead forming image are shown in Figure 19. Drain pin and Source (Power Source) pin are the same connection for both packages.

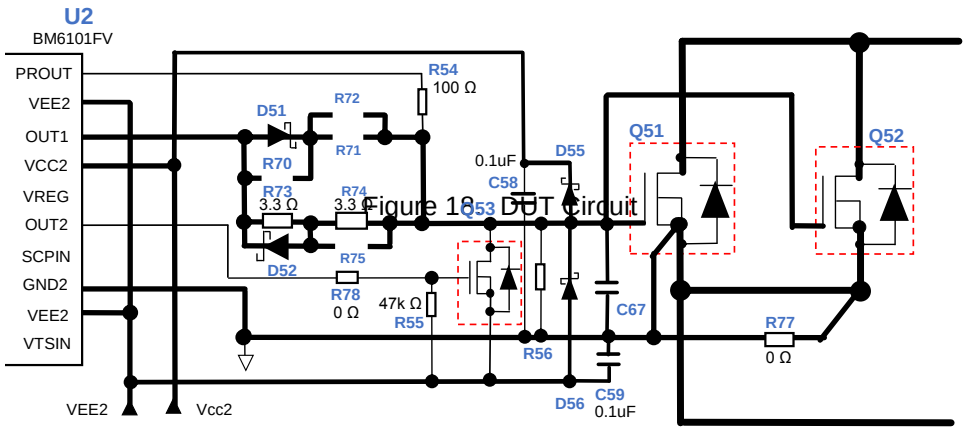


Figure 18. DUT Circuit

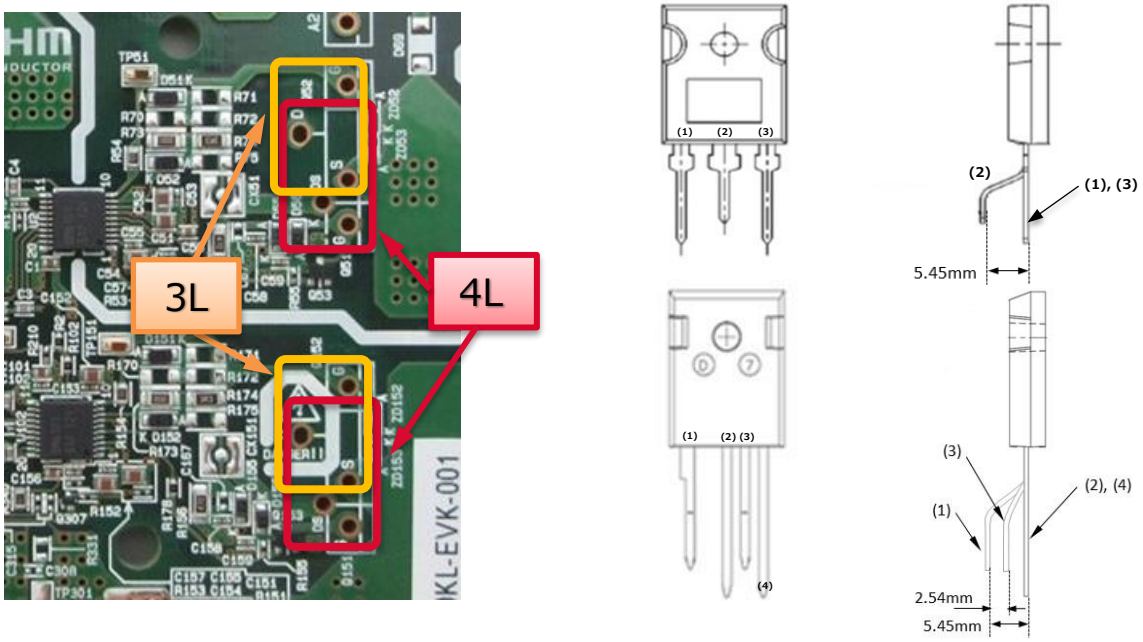


Figure 19. 4L and 3L Mounting and Lead Forming

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11. Heatsink Installation

When performing power conversion of several kW such as efficiency measurement based on a power supply topology, the device power consumption itself may reach several W, which will require a heatsink. The layout allows the using of a single heatsink for the cooling purpose even for the commutation devices. An insulator will be required under each device. The installation image is shown in Figure 20.

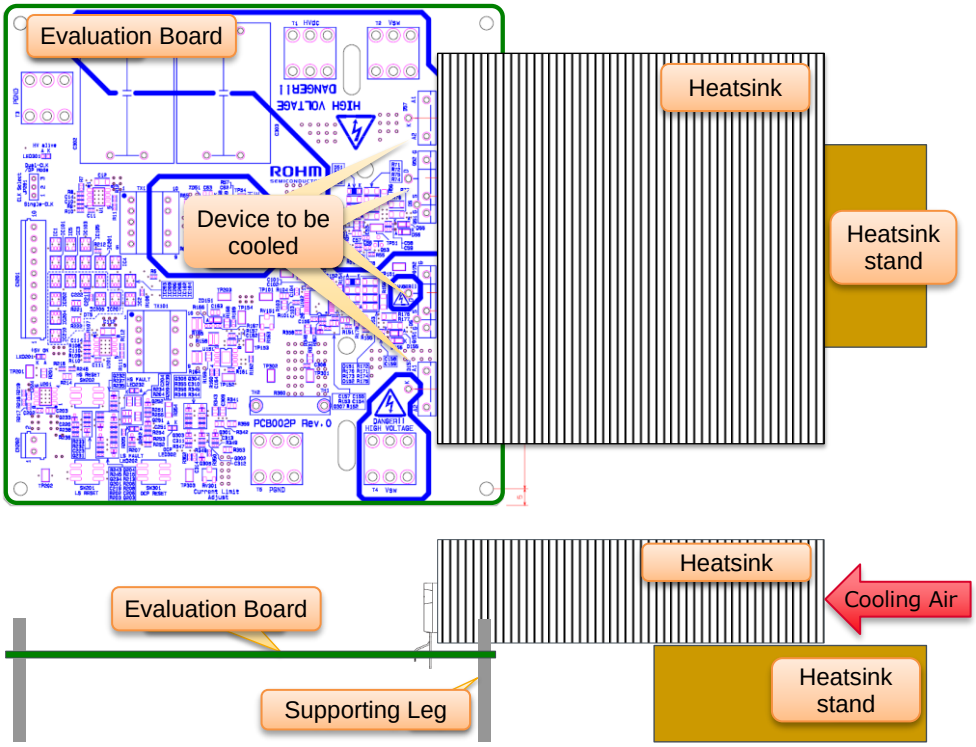


Figure 20. Heatsink Installation

The example of heatsink installation is shown in Figure 21.
SANKYO THERMO-TECH has the equivalent Heat sink, thermal resistance is 0.79℃/W.

Part number: 90BS125

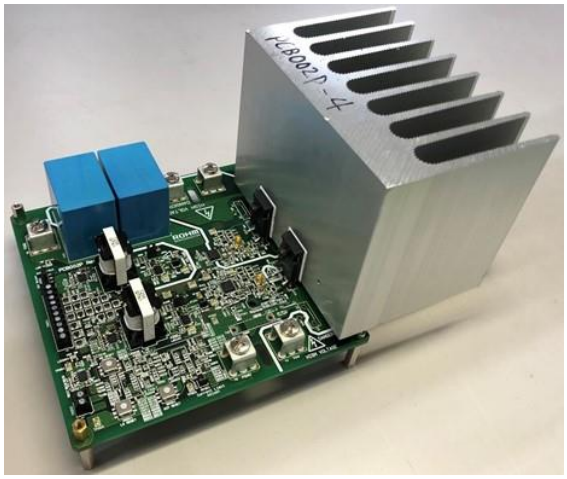


Figure 21. Heatsink Installation Example

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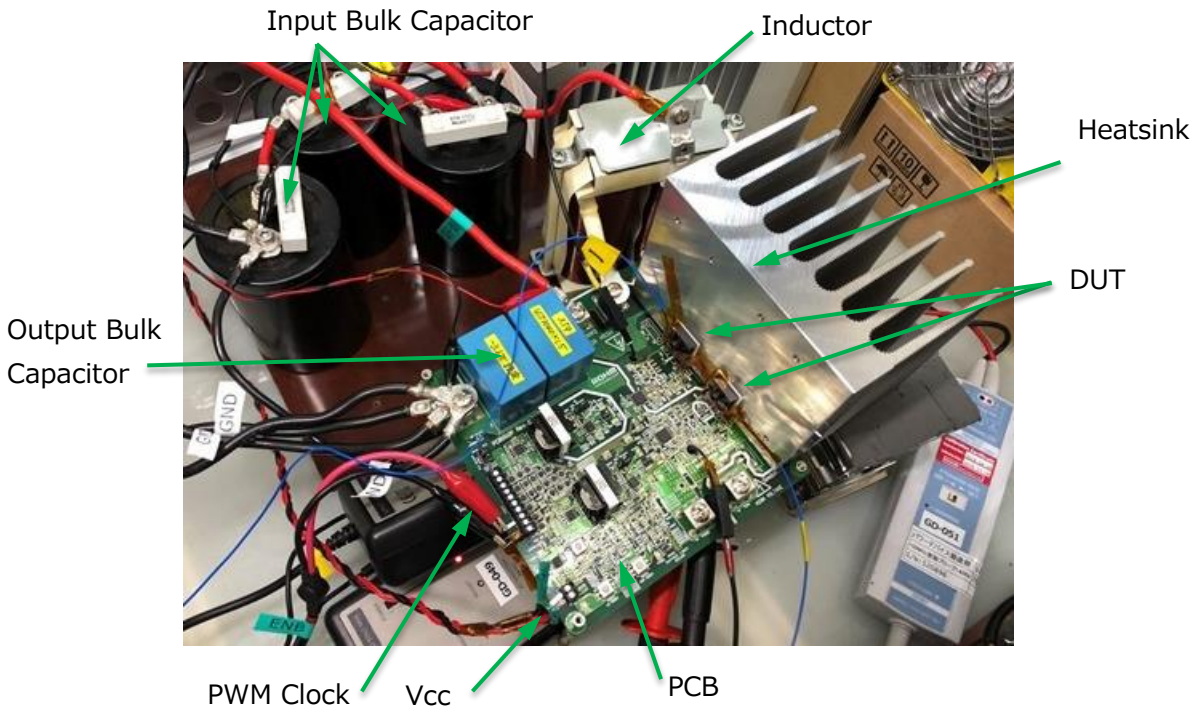


Figure 22. Heat Sink Installation

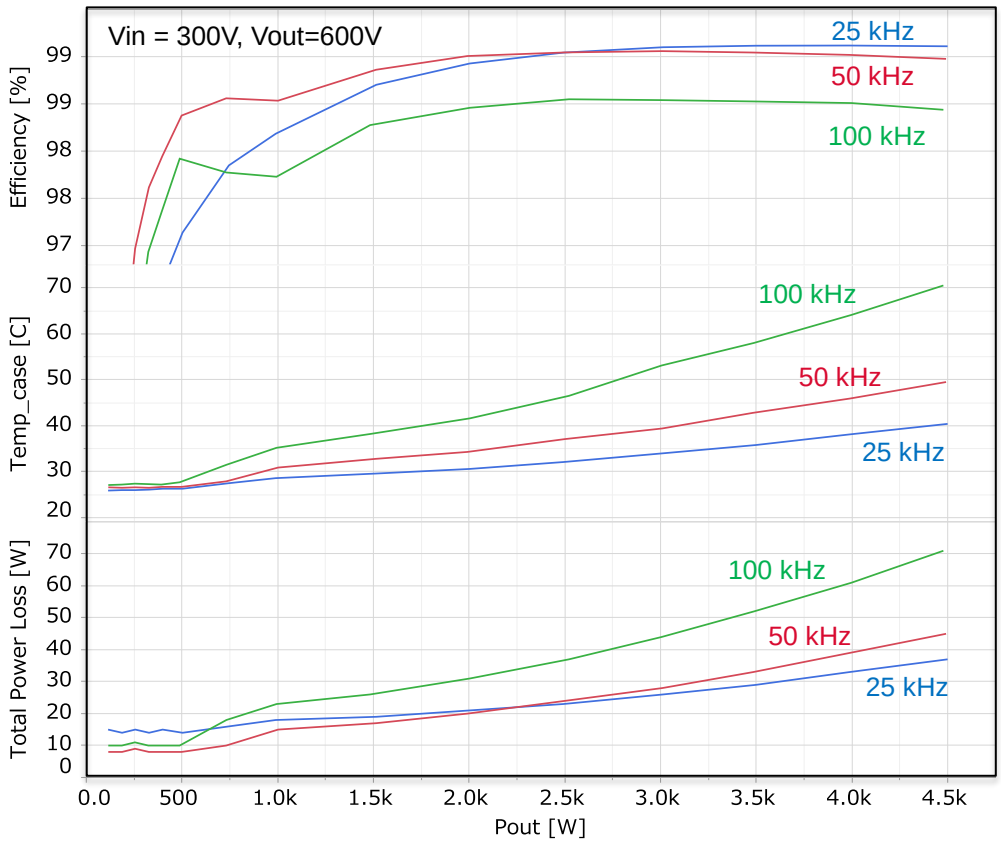


Figure 23. Device Surface Temperature
（SCT3040KL, BOOST, Rg=3.3Ω）

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12. Evaluation Board Connection Example

12.1 Double-pulse Test for HS MOSFET

The connection of the double-pulse test for HS MOSFET is shown in Figure 24.

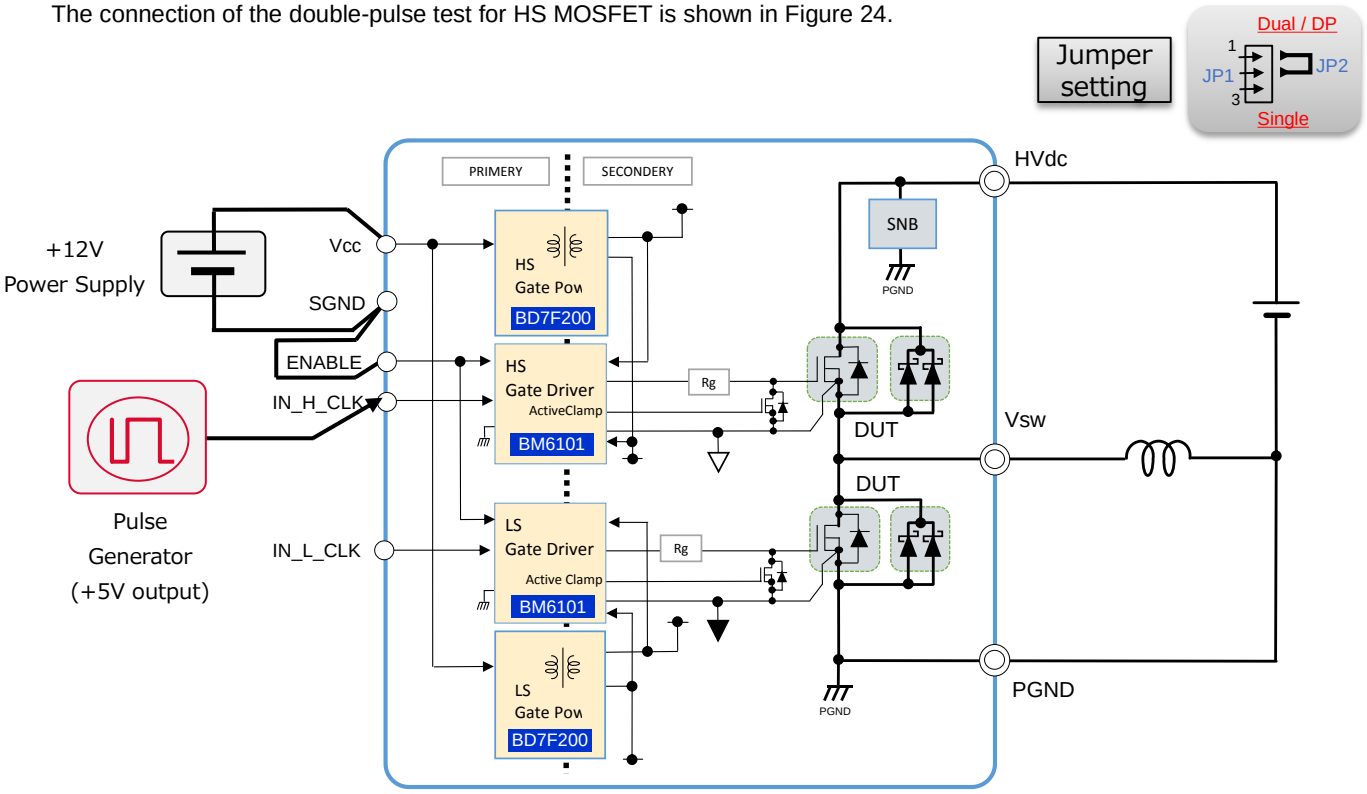


Figure 24. HS Double-pulse Test

Connect the HS_ALOW (CN201/7pin) signal to +5Vcc (CN201 8pin) if the pulse generator Single-shot Mode is at Active Low. Although OCP circuit is not valid, but the DESAT circuit will operate and function as the short protection. Input the CLK signal from the pulse generator to IN_H_CLK pin (CN201/6pin). Connect the 12V power supply to Vcc pin (CN202) and high voltage HVdc power supply to HVdc pin (T1). Preliminary setting has to be done for JP1 only.

① JP1 setting: Set to "Dual/DP" side

② Directly connect the ENABLE signal to SGND

Operation procedure is as follows:

③ Input the power supplies by following this sequence: +12V→HVdc

④ Input the pulse signal from the pulse generator

Peak current (IDP) flowing through the inductor (L) can be estimated using the equation below:

IDP ≒ HVdc/L*TDP_TTL [A]

HVdc: Applied voltage [V]

L: Inductor value [uH]

TDP_TTL: Double-pulse signal total time [us]

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Usually, double-pulse signal is a single-shot, please insure adequate inductor current IDP reset time between pulses if a periodic pulse is applied. As the reset voltage is equal to freewheeling diode forward voltage VF, the reset time can be calculated using the equation below:

Trst = IDP*L/Vf [us]

Secure the reset time Trst to have around 2 times longer than the calculated value. Even though a heatsink is not necessary during the double-pulse test, please pay attention as the freewheeling diode temperature may increase when performing the test repeatedly.

12.2 LS MOSFET Double-pulse Test

The connection of the double-pulse test for LS MOSFET is shown in Figure 25.

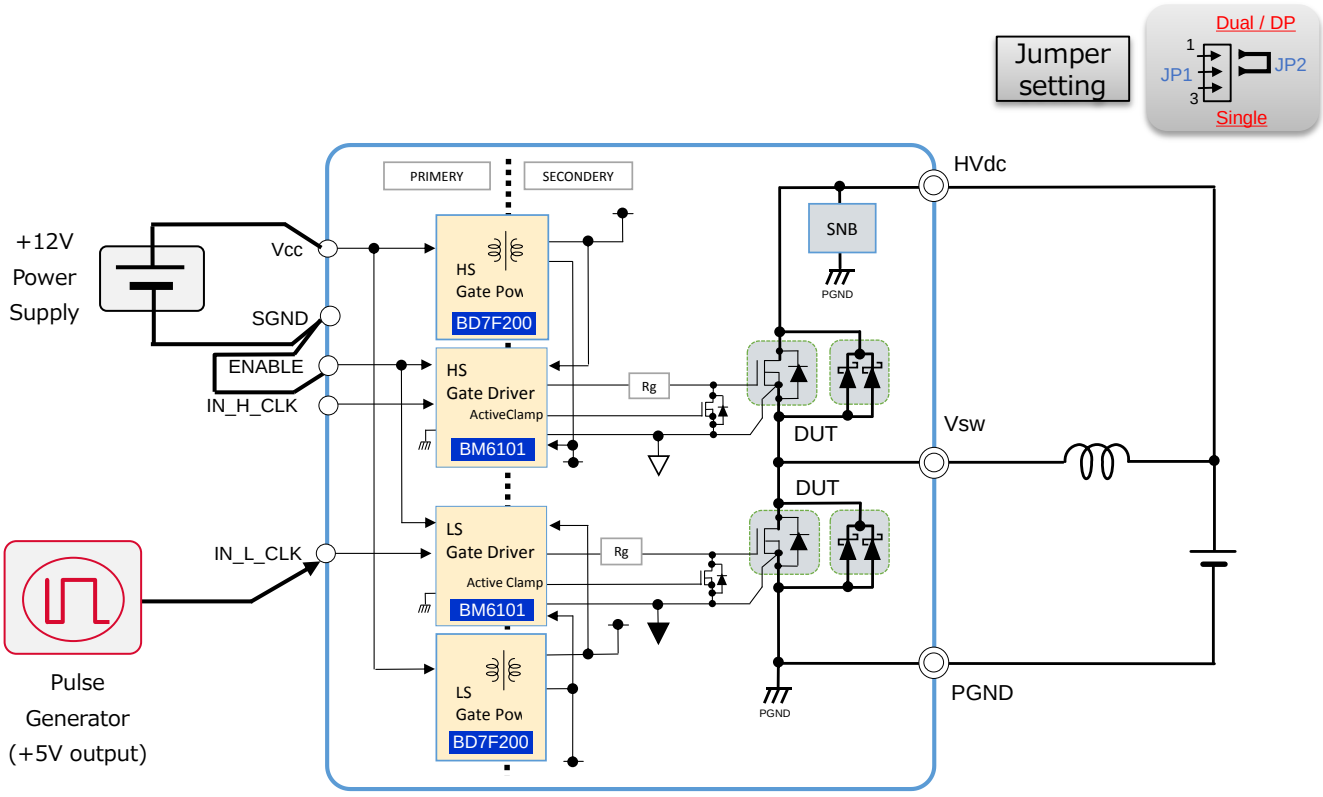


Figure 25. LS Double-pulse Test

Connect the LS_ALOW (CN201/9pin) signal to +5Vcc (CN201 8pin) if the pulse generator Single-shot Mode is at Active Low. Set the OCP point in advance as the OCP circuit is valid.

Input the CLK signal from the pulse generator to IN_L_CLK pin (CN201/4pin), then follow the same procedure as HS.

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12.3 Boost Topology Power Supply Circuit

The connection of the boost operation by switching the LS MOSFET is shown in Figure 26.

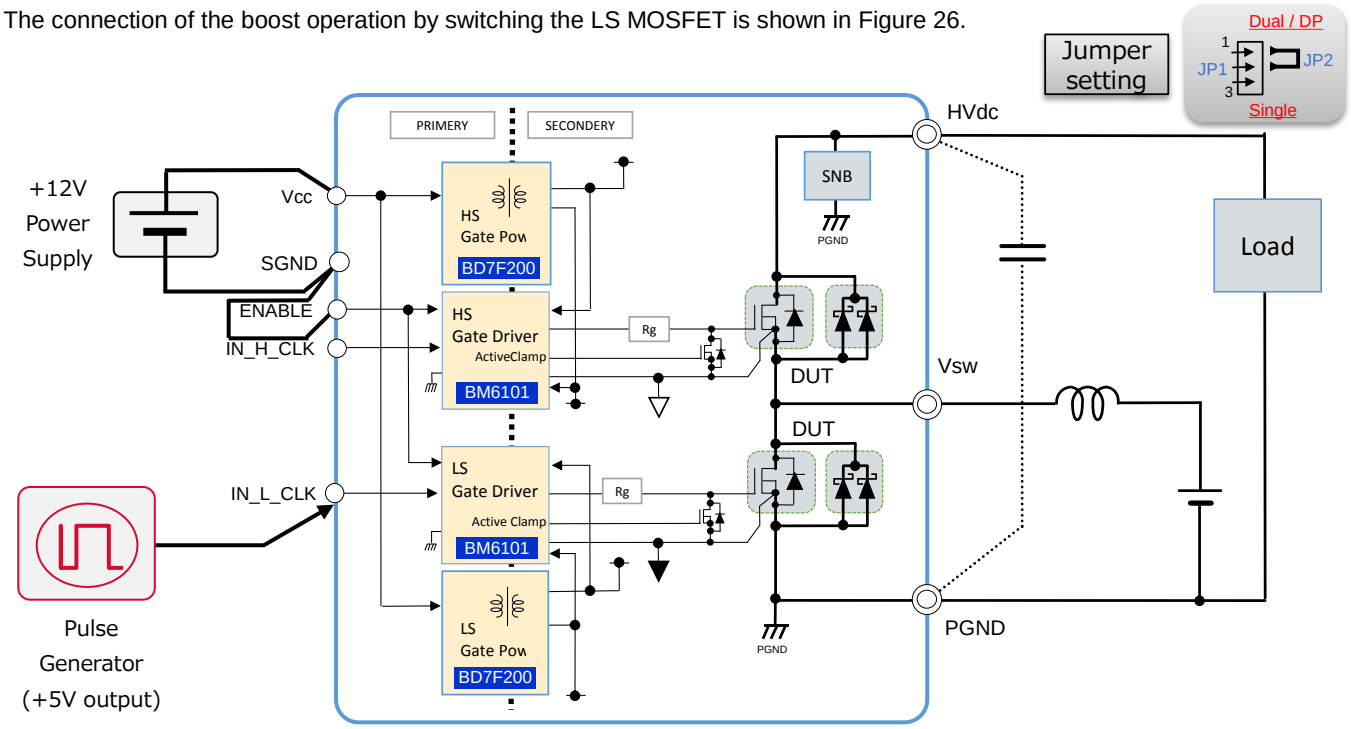


Figure 26. Boost Topology Power Supply Circuit Operation Test

Set the OCP point in advance as the OCP circuit is valid.

Connect the CLK signal from a pulse generator to IN_L_CLK pin (CN201 4pin). Then, connect the 12V power supply (for control block) to Vcc pin (CN202), load inductor to Vsw pin (T2), electronic load to HVdc pin (T1), as shown in Figure 26. The HVdc side becomes the output, as the output capacitor is already mounted on the PCB, basically it is not necessary to add an input capacitor externally. However, if the oscillating frequency is low, it is recommended to add an appropriate value of external input capacitor. In that case, ensure the capacitor has an adequate rated voltage.

Preliminary setting has to be done for JP1 only.

① JP1 Setting: Set to "Dual/DP" side

② Directly connect ENABLE signal to SGND

Operation procedure is as follows:

③ Input the +12V power supply

④ Set the switching frequency, duty ratio at the pulse generator, then input the CLK signal

⑤ Input the HVdc power supply

⑥ Adjust the output current at the electronic load equipment

At CCM mode in which the inductor current is continuous, the output voltage is approximately defined as below:

Vout=Vin/(1-Duty)

When the current is discontinuous (output current is small) the output voltage increases without being proportional to the duty ratio (output voltage changes depending on the load current). Here, as it is an open loop control, and the pulse is not thinning-out, the output voltage becomes multiple times larger than the input voltage. Please make sure to gradually increase the input voltage while monitoring the output voltage.

Pay attention to the heat generation when increasing the load current, use a sufficient cooling heat sink if necessary.

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12.4 2 Level Inverter Circuit

2 level inverter circuit based on half bridge configuration is shown in figure 27.

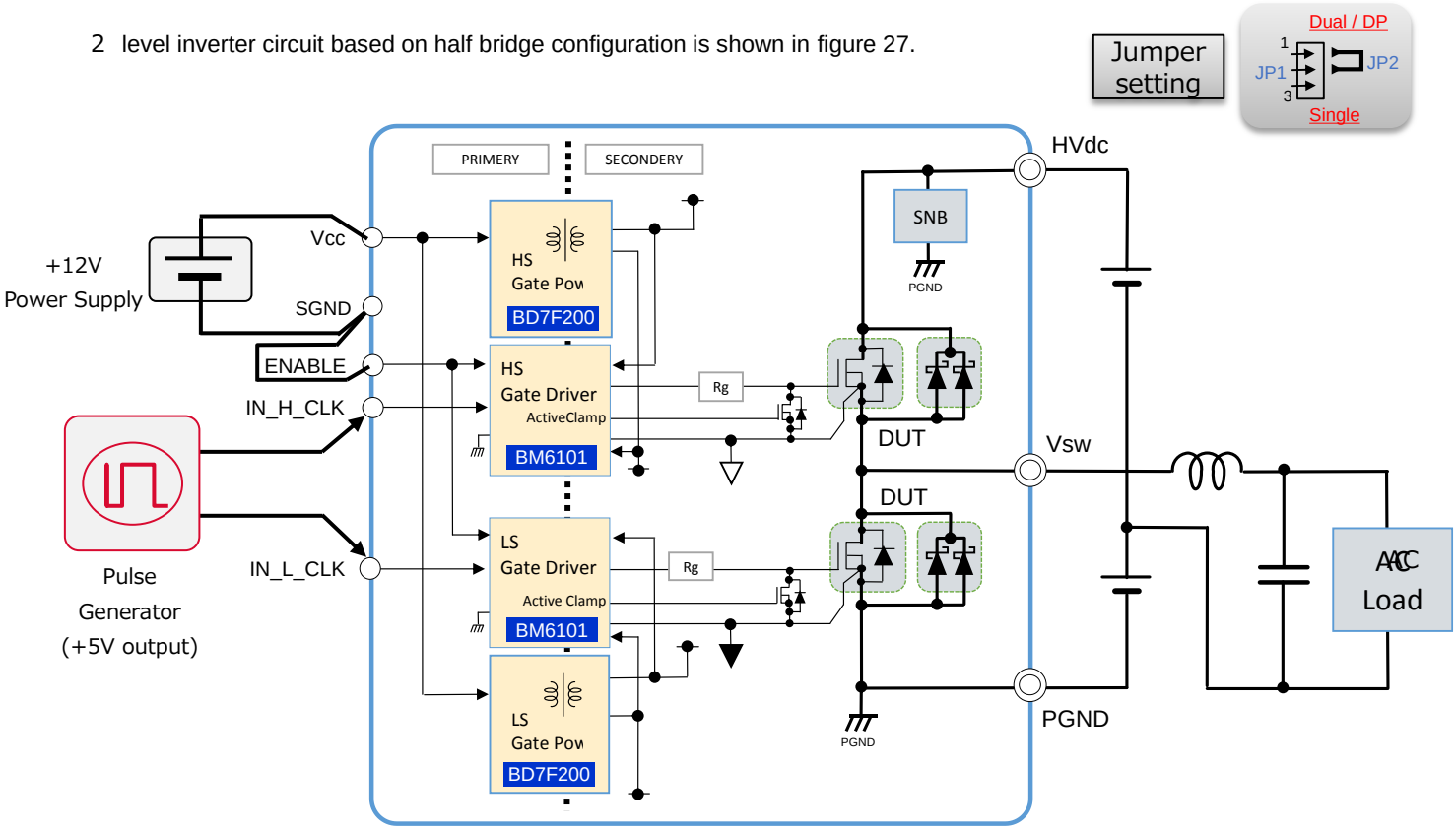


Figure 27. 2 Level Inverter Circuit Operation Test

Set the OCP point in advance as the OCP circuit is valid.

Connect the CLK signal from a pulse generator to IN_L_CLK pin (CN201 4pin). Then, connect the 12V power supply (for control block) to Vcc pin (CN202), and load inductor to Vsw pin (T 2). Prepare two HVdc power supplies with the same voltage, and connect them in series, connect the high side to HVdc pin (T1), and low side to the PGND pin (T3). Connect the smoothing capacitor and AC load to one side of the load inductor and connect its return line between the two serial connected HVdc power supplies.

The switching operation is at HS when AC output is (+) side, at LS when AC output is (−) side. The sine wave voltage is obtained by controlling the CLK signal Duty.

Preliminary setting has to be done for JP1 only.

① JP1 setting: Set to "Dual/DP" side

② Directly connect ENABLE signal to SGND

Operation procedure is as follow:

③ Input the +12V power supply

④ Set the switching frequency, duty ratio at the pulse generator, then input the CLK signal.

⑤ Input the HVdc power supply

⑥ Adjust the output current at AC load equipment

Pay attention to the heat generation when increasing the load current, use a sufficient cooling heat sink if necessary.

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12.5 Synchronous Buck Topology Power Supply Circuit

The connection of the buck operation using the HS MOSFET is shown in Figure 28.

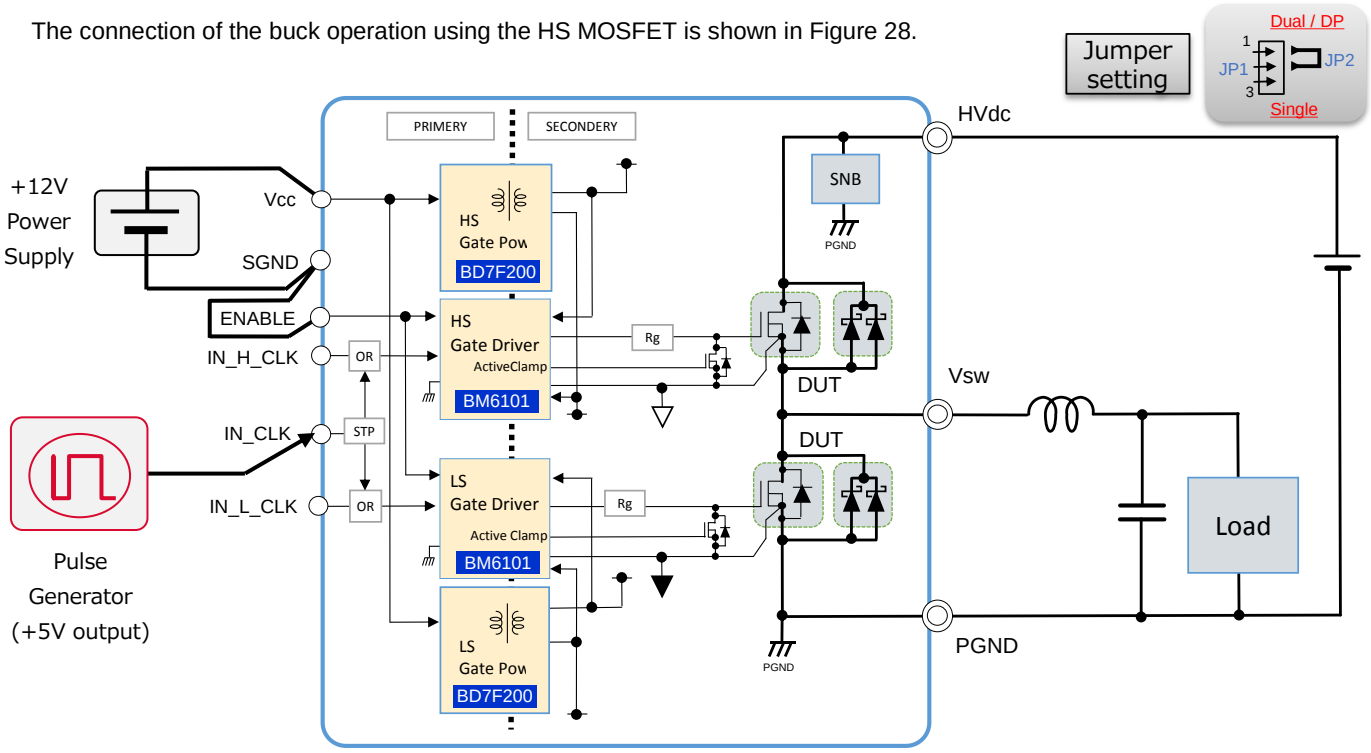


Figure 28. Synchronous Buck Topology Power Supply Operation Test

Since the OCP circuit is not valid, attention need to be paid. However, the DESAT circuit will operate and function for the short protection.

Connect the CLK signal from a pulse generator to IN_CLK pin (CN201 3pin). Then, connect the 12V power supply (for control block) to (CN202), high voltage HVdc power supply to HVdc pin (T1), load inductor to Vsw pin (T2), as the connection shown in Figure 28

Connect the smoothing capacitor and current load to one side of the load inductor. HVdc side becomes the input. As the input capacitor is already mounted on the PCB, basically it is not necessary to add an input capacitor externally. However, if the oscillating frequency is low, it is recommended to add an appropriate value of external input capacitor. In that case, ensure the capacitor has an adequate rated voltage.

Preliminary setting has to be done for JP1 only.

① JP1 Setting: Set to "single-CLK" side

② Directly connect ENABLE signal to SGND

Operation procedure is as follows:

③ Input the +12V power supply

④ Set the switching frequency, duty ratio at the pulse generator, then input the CLK signal

⑤ Input the HVdc power supply

⑥ Adjust the output current at the electronic load equipment

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At the CCM Mode in which the inductor current is continuous, the output voltage is approximately defined as below:

Vout=Duty*Vin

On the other hand, at the DCM Mode, output voltage becomes equal to the input voltage because it is an open loop control, and the pulse is not thinning-out, the output voltage is equal to the input voltage. Therefore, please make sure that the electronic load equipment has an adequate rated voltage, etc.

As the STP (Shoot Through Prevention) is used to prevent the Simultaneous ON of HS and LS MOSFET, user can start performing the operation immediately by only deciding the CLK signal frequency and duty ratio to be used. The dead time of the STP circuit can be adjusted by changing the resistors (R221/R222) value. Please refer to Chapter 8 for the details.

Pay attention to the heat generation when increasing the load current, use a sufficient cooling heat sink if necessary.

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13. Snubber Circuit

This evaluation board is equipped with non-discharge type RCD Snubber circuit layout for MOSFET turn OFF surge suppression, the circuit is shown in Figure 29.

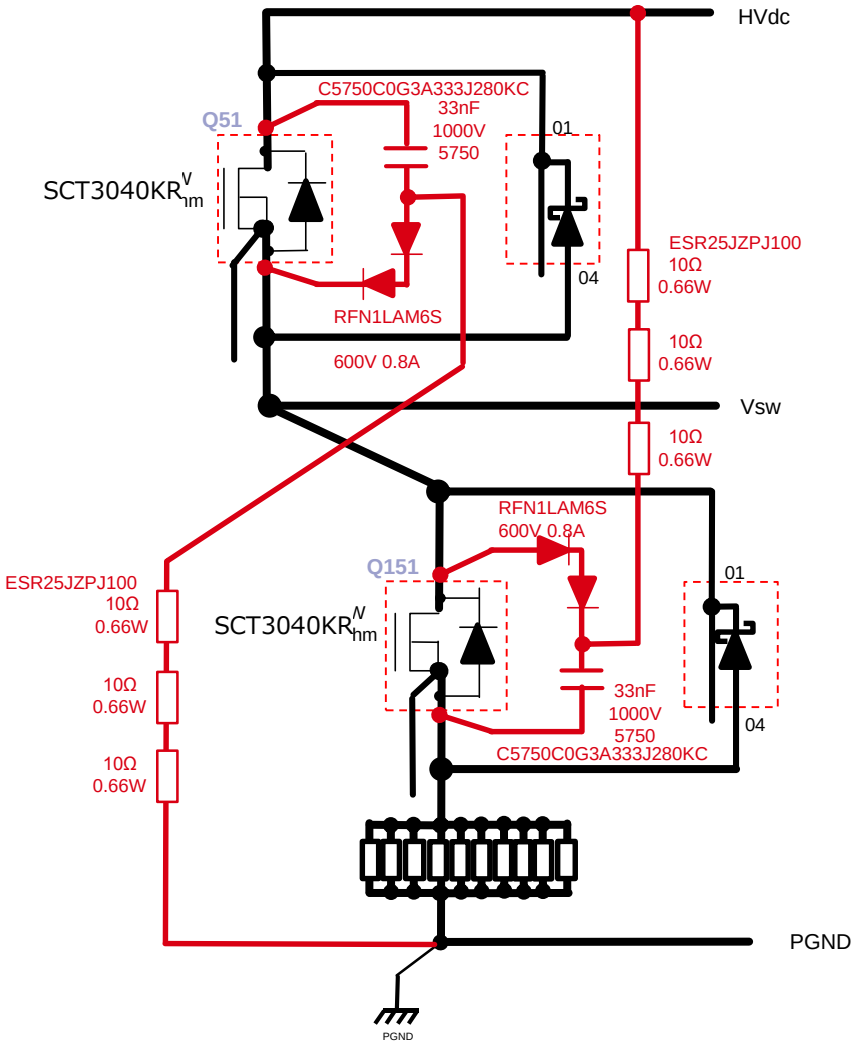


Figure 29. Non-discharge RCD Snubber Circuit

The resistor inside the non-discharge type Snubber circuit will only consume the power of the surge which exceeds the high voltage input HVdc, thus this circuit is suitable for high frequency switching circuit. However, the pattern layout is difficult, therefore, the board is recommended to have at least 4 layers.

All the power consumption of the Snubber circuit resistor P_{SNB} is consumed by the R_{SNB}, and this P_{SNB} can be calculated using following equation:

$$P_{SNB} = \frac{L_{TRACE} \times {I_{MAIN}}^2 \times f_{sw}}{2}$$

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Here, the L_{TRACE} is the wiring inductance of the main circuit to the bulk (DC link) capacitor, I_{MAIN} is the drain current during MOSFET turn OFF, and f_{SW} is the switching frequency of the MOSFET.

On the other hand, the Snubber circuit capacitance, C_{SNB} is the energy stored in the inductance and can be calculated using the equation below:

$$C_{SNB} = \frac{L_{TRACE} \times {I_{MAIN}}^2}{(V_{SURGE} - HV_{dc})^2}$$

Here, HV_{dc} is the high voltage input, and V_{SURGE} is the maximum value of the surge voltage.

Finally, the R_{SNB} is obtained by using the following equation:

$$R_{SNB} < \frac{-1}{C_{SNB} \times \ln[(V_{SURGE} - V_{SNB})/(V_{SURGE})]} \times \frac{1}{f_{sw}}$$

This maximizes the effect of absorbing the surge by discharging all the energy absorbed by CSNB during one cycle of the MOSFET.

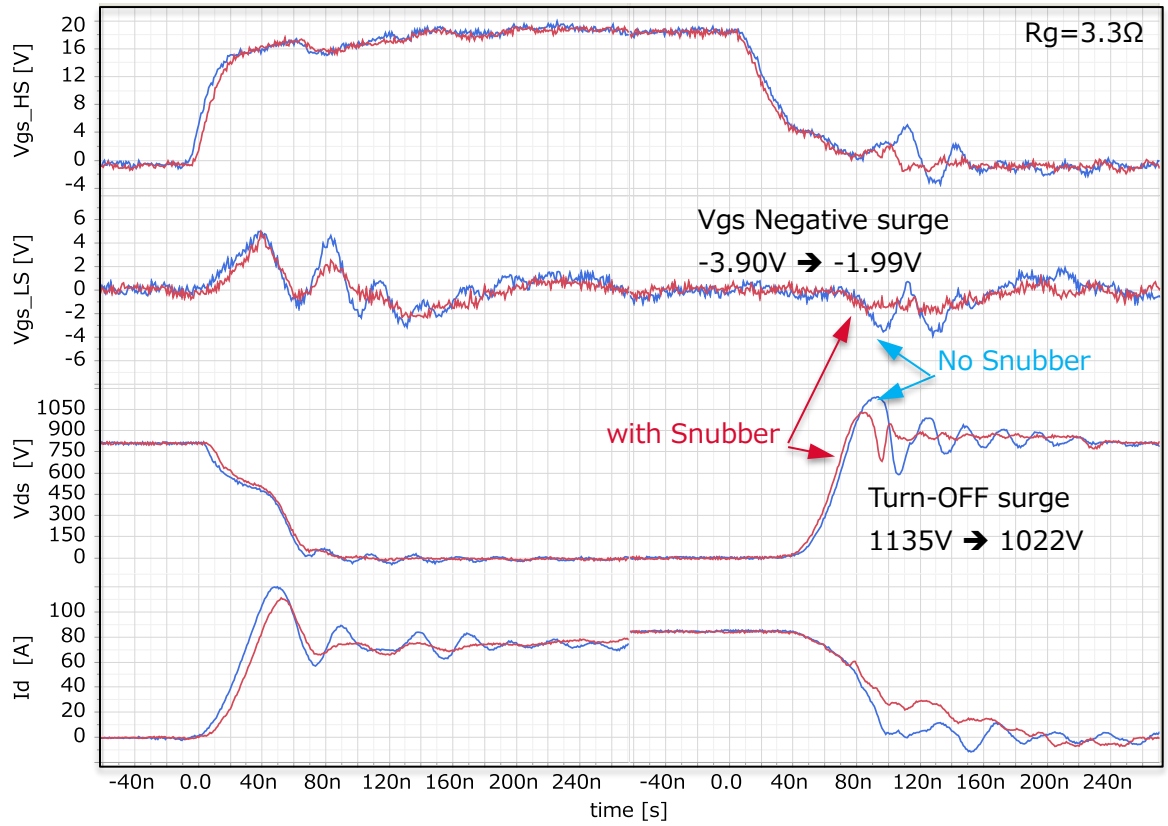


Figure 30. Snubber Circuit Effect (SCT3040LR)

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14. Gate-Source Signal Protection Circuit

This evaluation board is equipped with protection circuits to absorb the surge occurring at the MOSFET Gate-Source pin. The clamp circuit has three functions and four countermeasure circuits as shown in Table 11. It is important to suppress the surge voltage by implementing these protection circuits as the Gate-Source voltage is greatly affected by the changes of Vds and Id during the switching operation. Please note that the Gate-Source voltage behavior is explained in a separate application note ("Gate-Source Voltage Behavior in Bridge Configuration (No.60AN135E Rev.001)), it is recommended to refer this application note.

The circuit diagram is shown in Figure 31.

Table 11. Clamp Circuit and Operation Details

Item	Clamp Circuit	Circuit Symbol	Operation Details	Initial Setting
(I)	Positive Surge Clamp	D55, C58	The positive side surge that occurs when the Vds change of the MOSFET is completed. It may exceed the Vgs maximum rating during turn ON, therefore, D55 will clamp it to Vcc2. C58 is a bypass capacitor, place its layout close to D55.	No Mount
(II)	Negative Surge Clamp	D56, C59	When Vds turns ON at the turn OFF of the opposite MOSFET in a bridge configuration, a negative surge occurs, and it may exceed the Vgs negative side maximum rating, therefore, D56 will clamp it to VEE2. C59 is a bypass capacitor, place its layout close to D56.	No Mount
(III)	Self-turn ON Surge Clamp	Q53	When the opposite side of the MOSFET in a bridge configuration turns ON, Vgs gets raised up by the Vds rise, the other MOSFET turns ON (so-called self-turn ON) when the Vgs exceeded the threshold voltage. The Vgs rising can be reduced by clamping it with Q53 (impedance smaller than Gate drive resistor R74). This countermeasure circuit requires the control signal which generally included inside the drive IC side. The Q53 is called a miller clamp MOSFET.	Mount
(IV)		C67	As the Crss/Ciss ratio of the MOSFET increases, Vgs tends to get raised up easily (as the charging current is proportional to Crss). The Crss/Ciss ratio can be reduced by adding a capacitor in parallel to Ciss. It prevents the voltage to exceed the Vth. As the added capacitance is bigger, the voltage increase becomes less, but more drive capability is required and switching loss becomes higher, so please add the capacitance by considering the heat dissipation.	No Mount

It is necessary to make these clamp circuits' pattern inductances to be as small as possible since the Vgs surge voltage occurs in several ns, therefore design the layout to be as close as possible to the MOSFET.

Among ROHM SiC MOSFETs, the third generation SCT3xxxx Series has a narrow Gate-Source voltage rating thus, it is recommended to have these clamp circuits. The Vgs surge voltage can be more effectively suppressed by implementing several of them on the board, but the priority of the layout to be close to the MOSFET is as follows:

(III)Active Clamp MOSFET ➔ (II)Negative Surge Clamp Circuit ➔ (I)Positive Surge Clamp Circuit ➔ (IV)Additional GS Capacitance (Csg)

Figure 32 shows the protection circuit mounting location.

In addition, the waveform examples with/without the protection circuit are shown in Figure 33～34. However, the actual operation is not only depending on the device itself, but the board where it is mounted also affects the operation greatly, therefore verification on the actual board is necessary.

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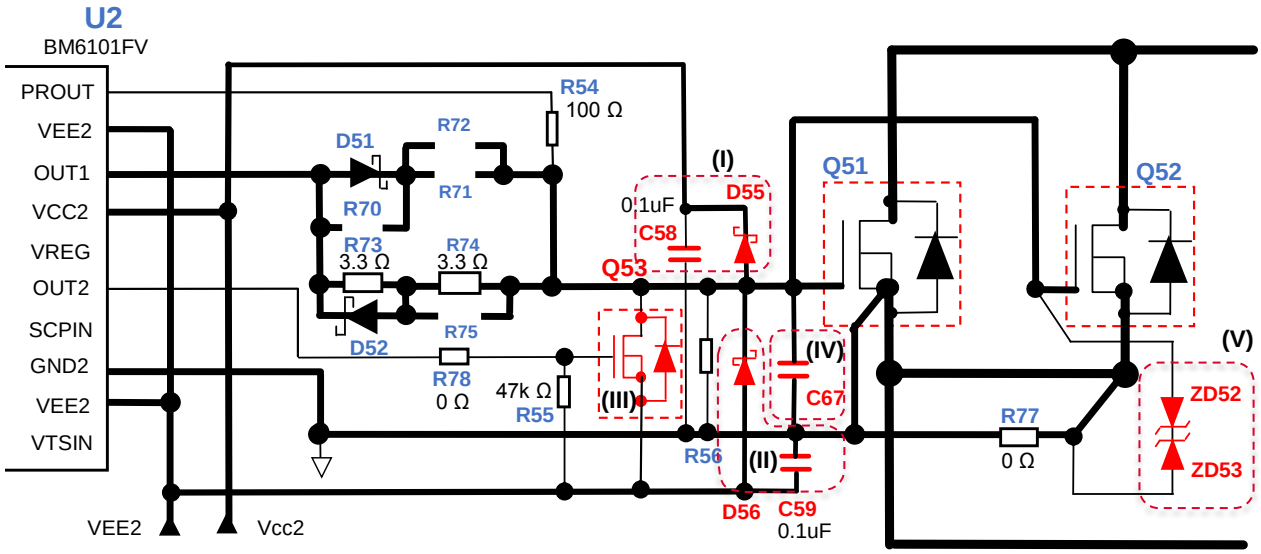


Figure 31. Gate Source Signal Protection Circuit

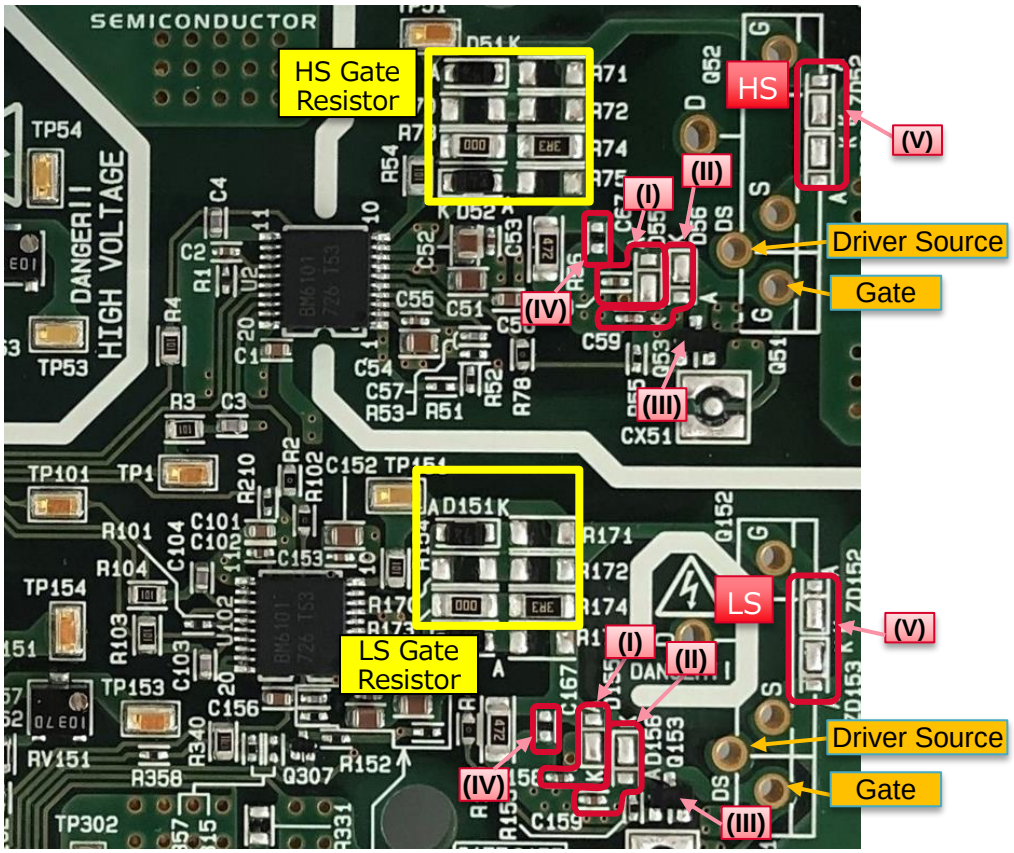


Figure 32. Gate Source Voltage Protection Circuit Mounting Location

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■ Waveform example when clamp-SBD is used

Figure 33 shows the Vgs surge suppression effect at double pulse test when clamp SBD is used. SCT3040KR MOSFETs are connected in a half-bridge configuration and switching is done on the high side MOSFET. The external Gate resistor is 10Ω. From top, the first waveform is the high side MOSFET Vgs, the second waveform is the commutation side (low side) Vgs, the third waveform is the high side Vds, and the last waveform is the high side Id. From red line waveform, we can notice that there is not a single Vgs protection circuit being applied as the self-turn on during turn on and the negative surge during turn off is very severe.

On the other hand, with only clamp SBD is applied to the circuit (green line), we can notice that the negative surge disappeared. However, this clamp SBD does not effective in reducing the positive surge, and does not stop the self-turn on. There is only one way to reduce the positive surge or stop the self-turn on which is by using Active MOSFET.

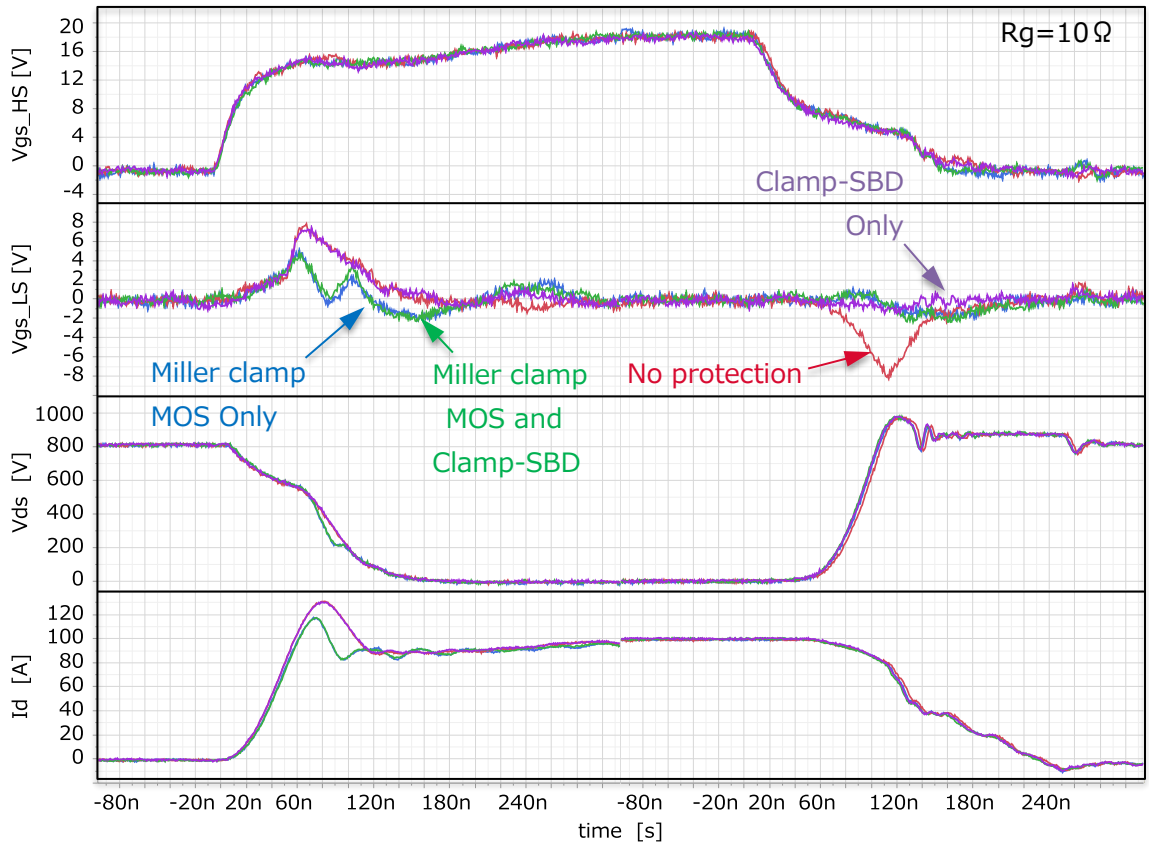


Figure 33. Vgs Protection Circuit Effect (SCT3040KR)

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■Waveform comparison by using different Cgs capacitances（**Without protection circuit**）

Figure 34 shows the measurement result and the effect of using Cgs on the self-turn on and surge voltage.

From the waveforms, we can see that the self-turn on can be prevented by adding the Cgs. However, we also understand that the Cgs does not give a significant effect on the negative surge at turn off. Furthermore, switching loss increases when Cgs is added, thus it is necessary to measure the heat dissipation on the device at actual application board when selecting the Cgs value.

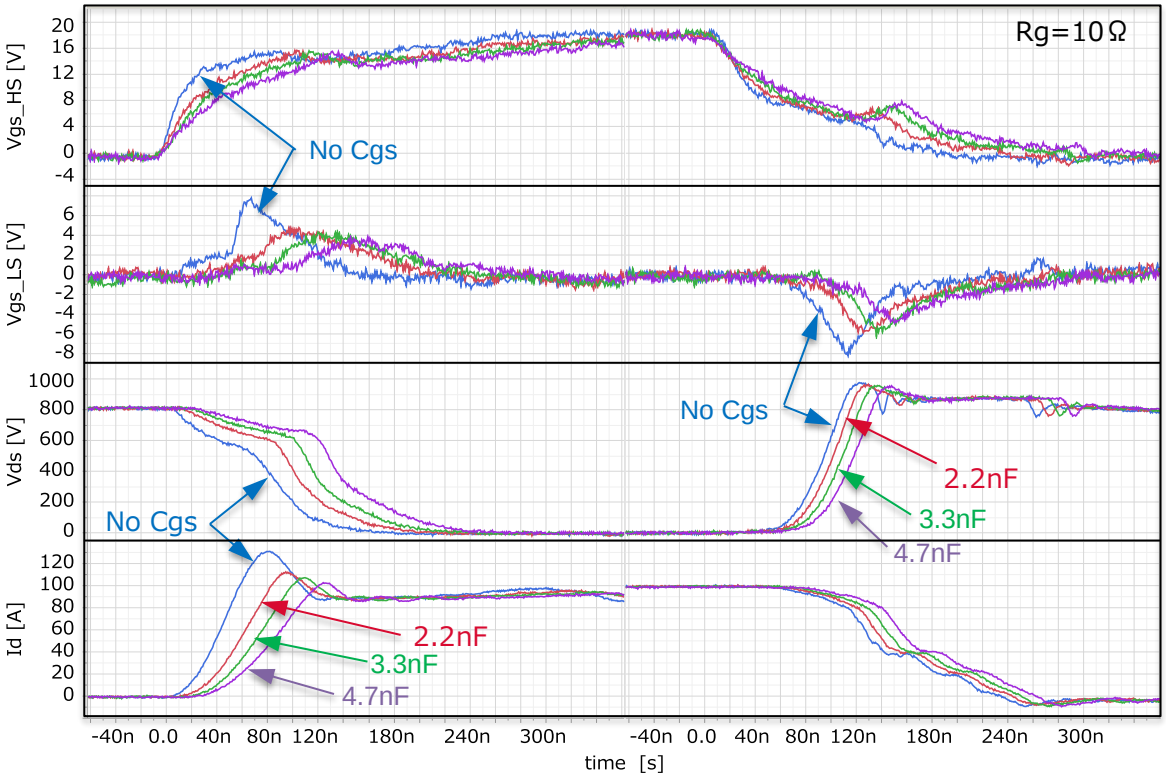


Figure 34. Cgs comparison（SCT3040KR, without protection circuit）

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■Waveform comparison by using different Cgs capacitances（**With protection circuits**）

Finally, the measured waveforms when all the Vgs protection circuits are applied are shown in Figure 35. All the abnormalities during turn on and turn off disappeared, therefore, Cgs is not needed.

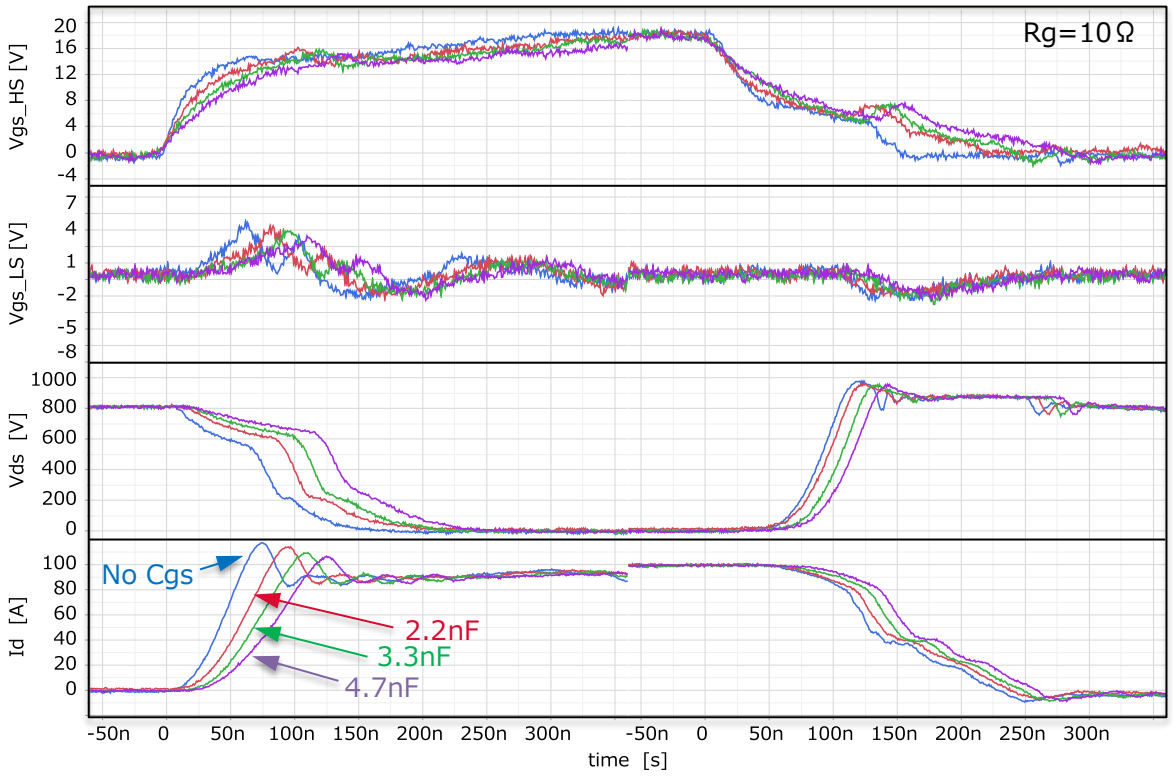


Figure 35. Cgs comparison（SCT3040KR, with protection circuits）

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15. Precautions when measuring the Gate-Source signal

Drain current di/dt of the MOSFETs with driver source pin is in several A/ns level. Thus, the generation of radiation noise is quite big. Therefore, pay attention to the connection of the voltage probes when measuring comparatively low voltage signals. Figure 36 shows the influence of the voltage probe connection on the measured waveforms.

The comparison is done between two types of connections when connecting an isolated probe, one is when there is a "Big Loop Sensing" where there is space created between the (+) and (-) of the clips, and the other one is when the sensing wire is directly soldered to the device's package root with a 100Ω damping resistor. This 100Ω damping resistor removes the voltage oscillation caused by the sensing wire inductance and does not affect the actual measurement waveforms.

The commutation side Vgs (Vgs_LS) surge polarity is different depending on measurement method. Originally, at turn on, the commutation side current decreases, Vf of the body diode decreases and Coss and Crss are charged. Since this charged current is flowing from drain pin to gate pin, positive surge should occur in Vgs. However, in "Big Loop Sensing", a large surge is generated on the negative side. This happens as the di/dt of the current flowing on the PCB creates the radiation noise, and the error in measurement occurs when there is space between the probe connections.

Therefore, consider that the commutation side of Vgs positive surge can be correctly measured by soldering the sensing wire directly to the device's package root in order to minimize the connection space. However, connection space also exists between PCB and the device leads, that creates the radiation noise. Therefore, even a measurement by using a 50Ω coaxial cable with BNC connector directly mounted on the PCB can still cause a measurement error.

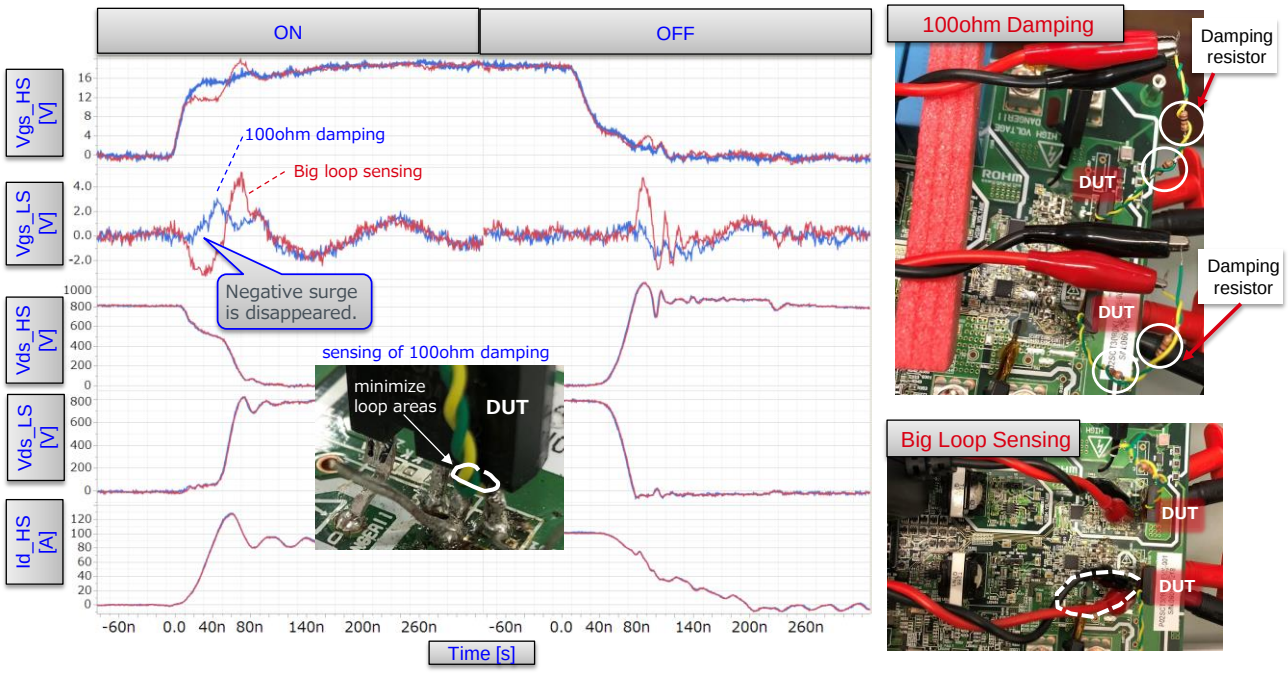


Figure 36. Probe connection and measured waveforms
(SCT3040KR with Vgs protection circuits)

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