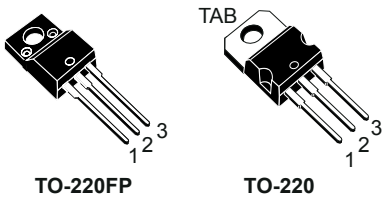
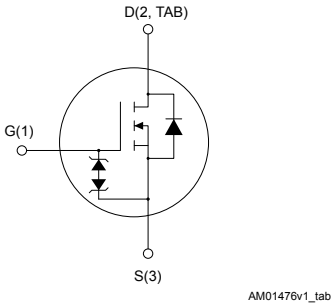
N-channel 600 V, 1.06 Ω typ., 4.5 A MDmesh M2 Power MOSFET in a TO-220FP and TO-220 packages



TO-220FP TO-220



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF6N60M2	600 V	1.2 Ω	4.5 A
STP6N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.

Product status links
STF6N60M2
STP6N60M2

Product summary	
Order code	**STF6N60M2**
Marking	6N60M2
Package	TO-220FP
Packing	Tube
Order code	**STP6N60M2**
Marking	6N60M2
Package	TO-220
Packing	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	4.5		A
I_D	Drain current (continuous) at T_C = 100 °C	2.9		A
I_{DM}(1)	Drain current (pulsed)	18		A
P_{TOT}	Total power dissipation at T_C = 25 °C	20	60	W
dv/dt(2)	Peak diode recovery voltage slope	15		V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	-	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 4.5 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DD} = 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	6.25	2.08	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	86	mJ

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)	-	-	100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.25 A	-	1.06	1.2	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	232	-	pF
C_{oss}	Output capacitance		-	14	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	71	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 4.5 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	8	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	4	-	nC
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6.5	-	Ω

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1.65 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	9.5	-	ns
t_r	Rise time		-	7.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	22.5	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	4.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	18	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	274	-	ns
Q_{rr}	Reverse recovery charge		-	1.47	-	µC
I_{RRM}	Reverse recovery current		-	10.7	-	A
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	376	-	ns
Q_{rr}	Reverse recovery charge		-	1.96	-	µC
I_{RRM}	Reverse recovery current		-	10.5	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

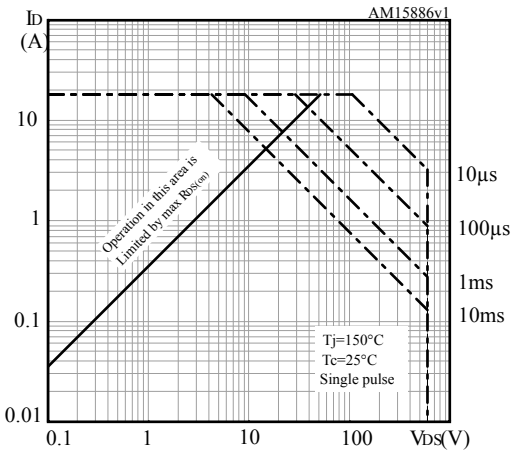


Figure 2. Normalized transient thermal impedance for TO-220FP

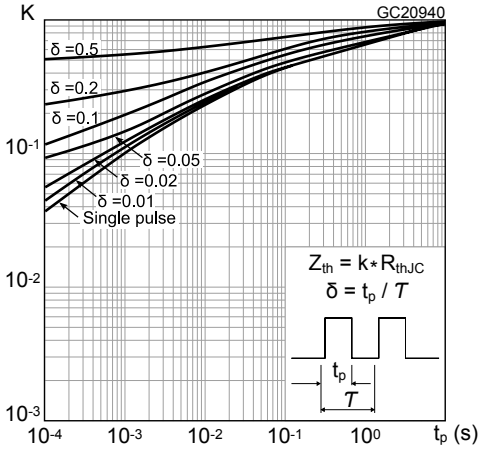


Figure 3. Safe operating area for TO-220

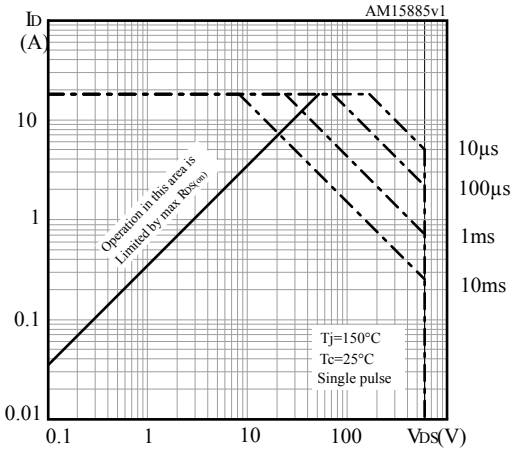


Figure 4. Normalized transient thermal impedance for TO-220

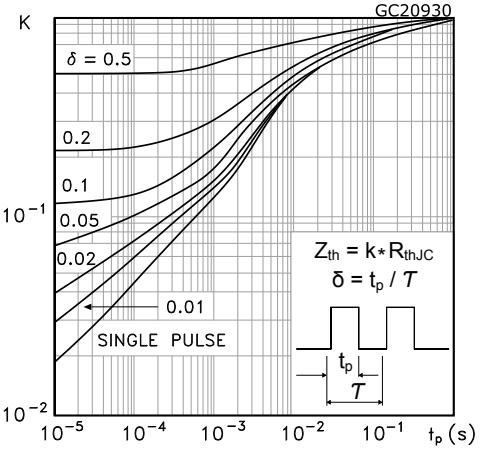


Figure 5. Typical output characteristics

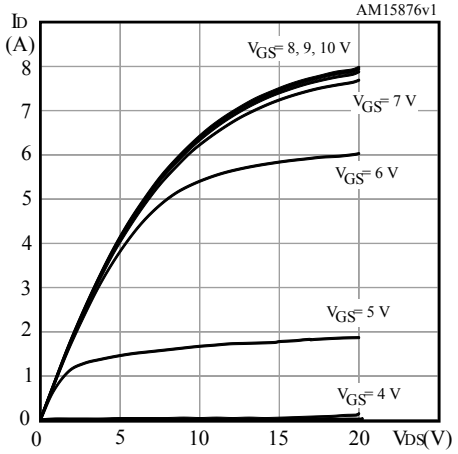
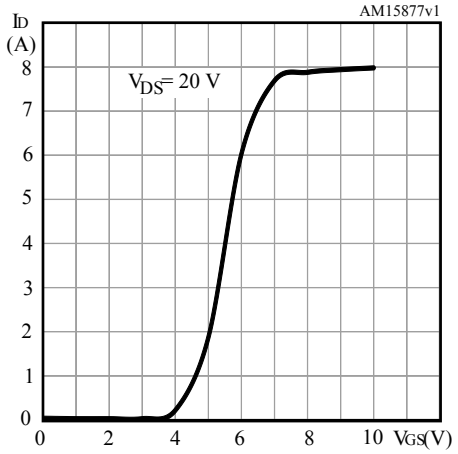


Figure 6. Typical transfer characteristics



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Figure 7. Typical gate charge characteristics

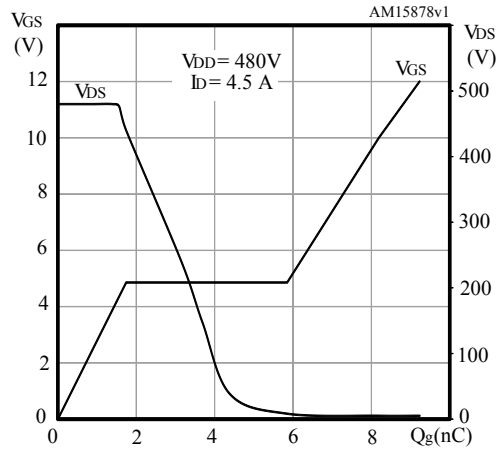


Figure 8. Typical capacitance characteristics

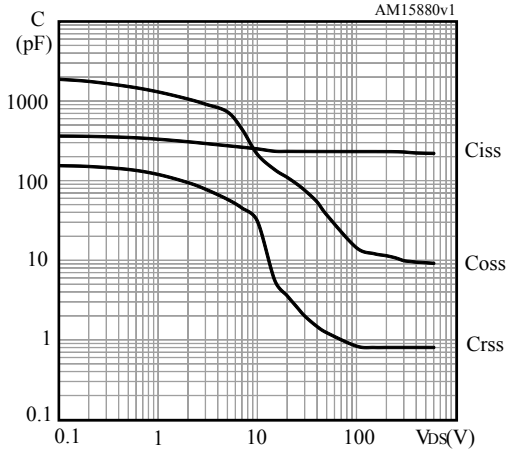


Figure 9. Typical drain-source on-resistance

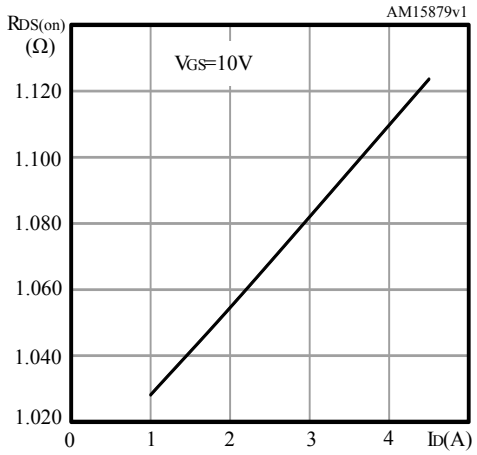


Figure 10. Normalized breakdown voltage vs temperature

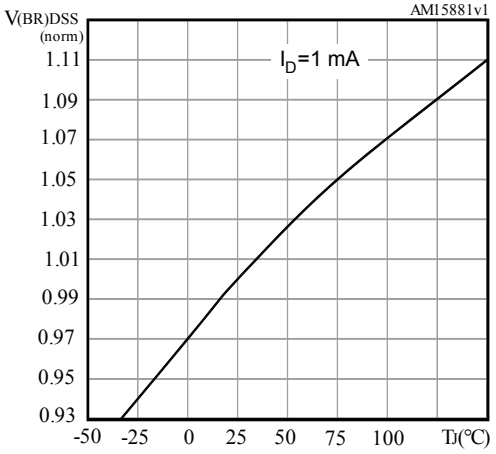


Figure 11. Normalized gate threshold vs temperature

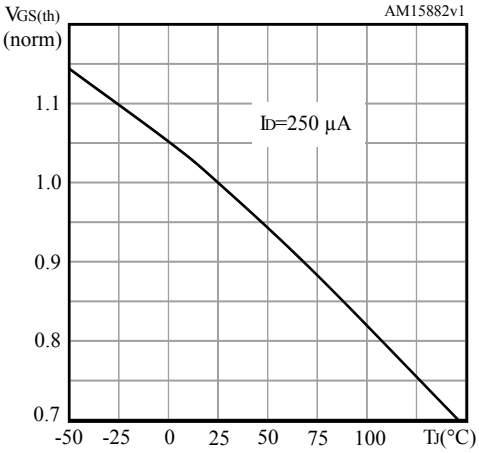
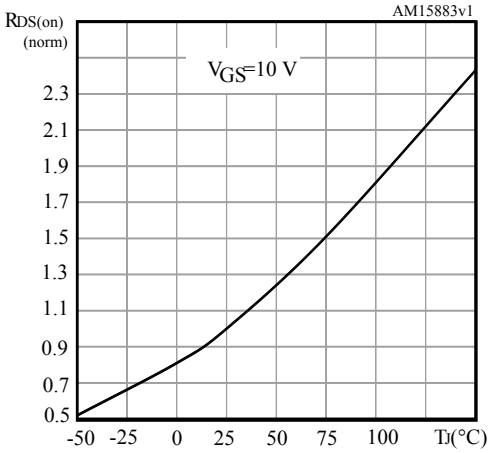
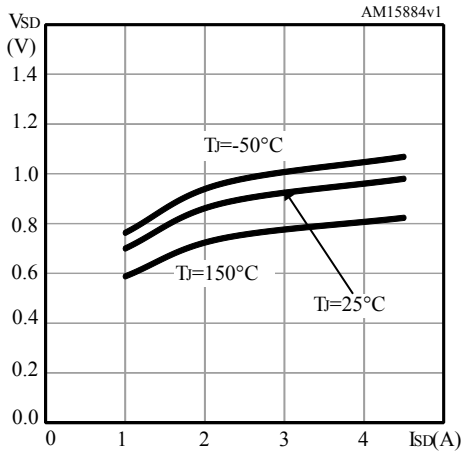


Figure 12. Normalized on-resistance vs temperature



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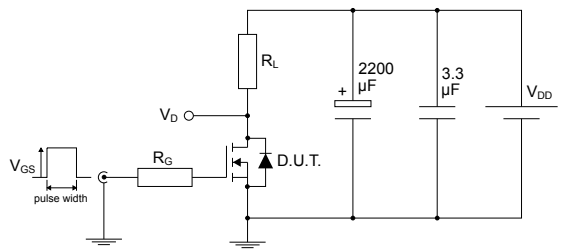
Figure 13. Typical reverse diode forward characteristics



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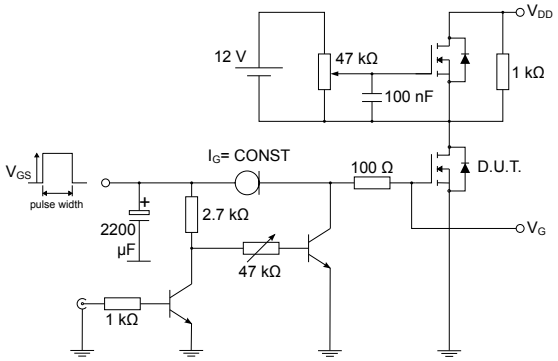
3 Test circuits

Figure 14. Test circuit for resistive load switching times



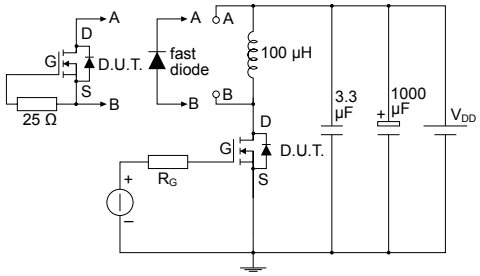
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Figure 15. Test circuit for gate charge behavior



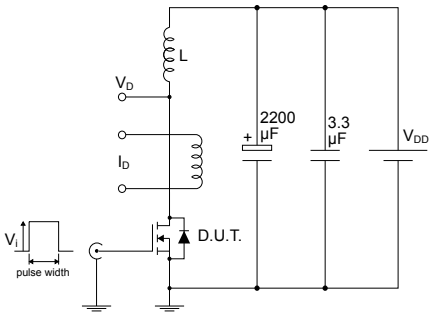
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Figure 16. Test circuit for inductive load switching and diode recovery times



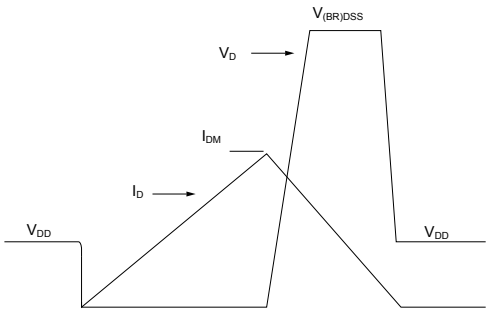
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Figure 17. Unclamped inductive load test circuit



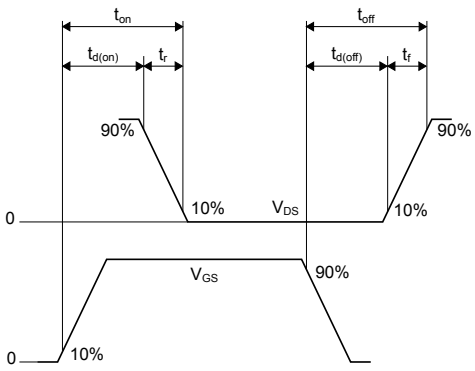
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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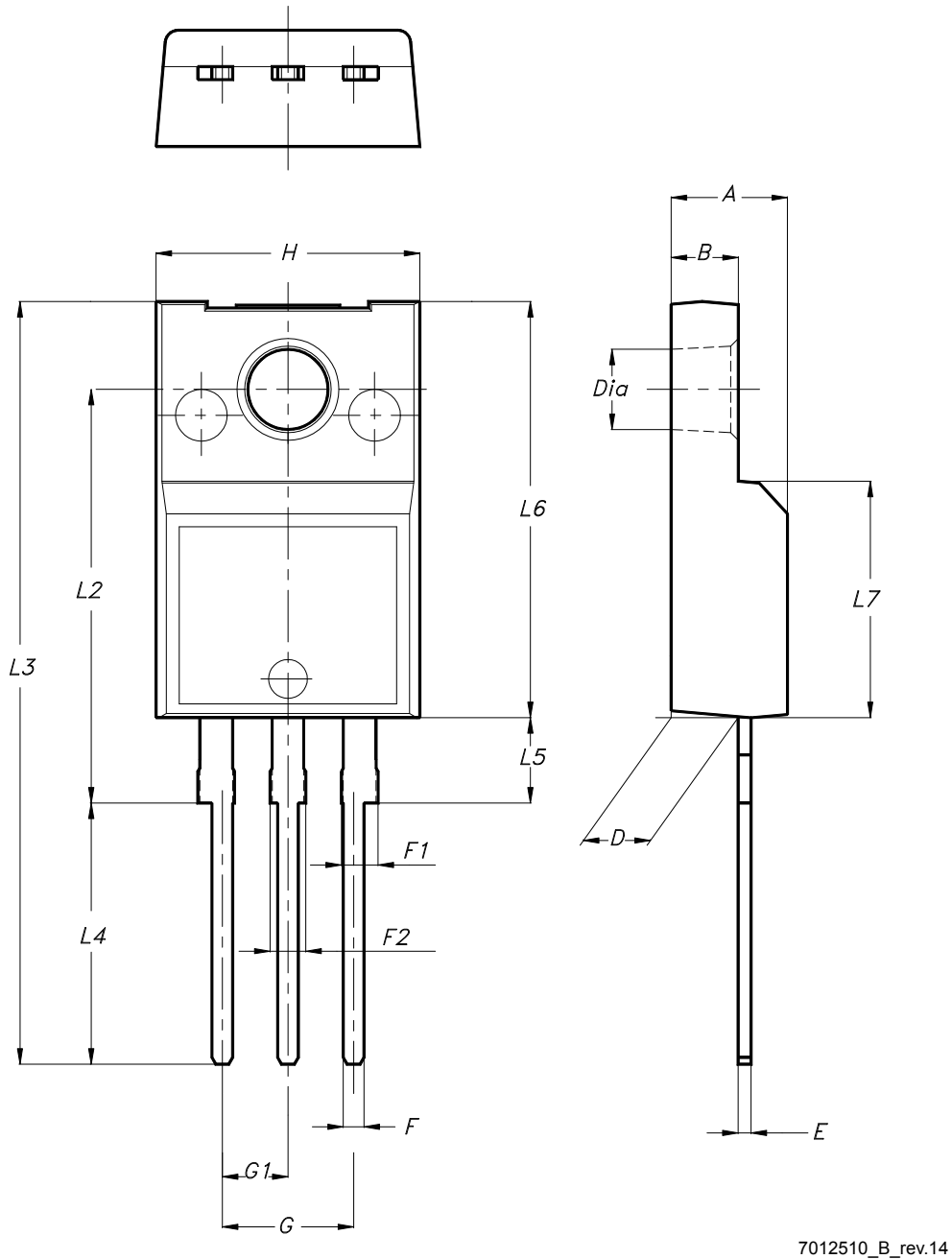
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 20. TO-220FP type B package outline



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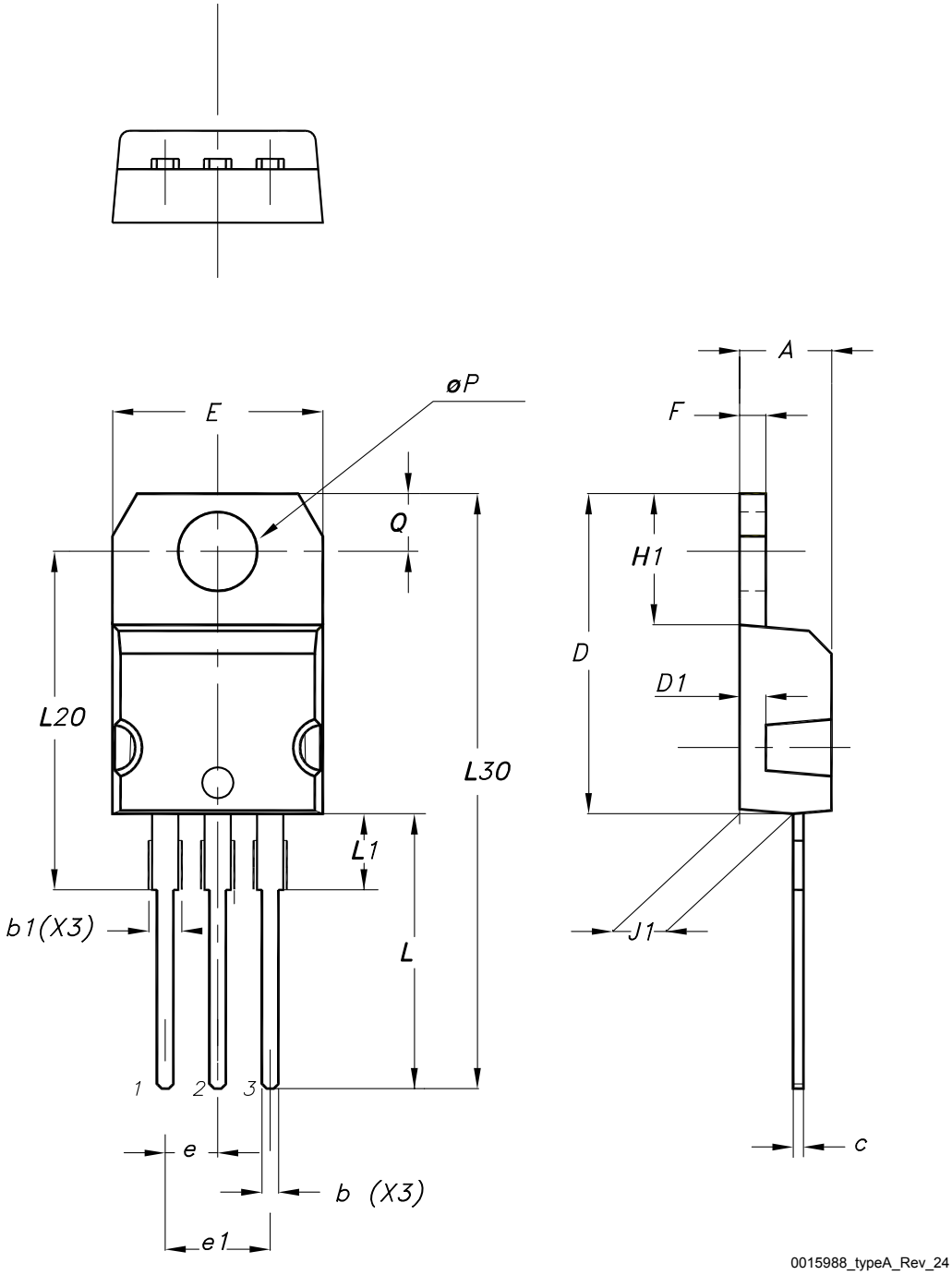
Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

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4.2 TO-220 type A package information

Figure 21. **TO-220 type A package outline**



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Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

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Revision history

Table 10. **Document revision history**

Date	Revision	Changes
11-Jun-2013	1	First release.
01-Oct-2015	2	Updated title, features and description. Updated *Table 2.: Absolute maximum ratings* and *Table 8.: Source drain diode*. Updated *4.3: IPAK(TO-251) package information*. Minor text changes.
04-Dec-2025	3	Removed order code STU6N60M2. Updated Section 4: Package information. Minor text changes.

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