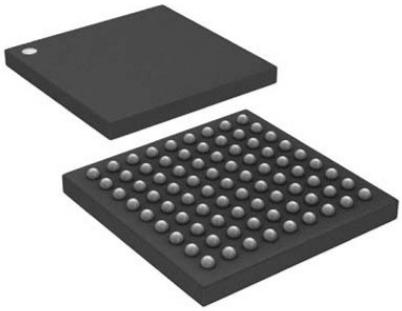
STA8135GA

Data brief

Teseo V family automotive triple-band multi-constellation GNSS precise engine receiver



TFBGA160 7x11x1.2 mm
0.65 mm ball pitch

Product status link
STA8135GA

Product summary
Order code
STA8135GATR
Temperature range
-40 °C to +105 °C
Package
LFBGA160 7x11x1.2 mm
Packing
Tray, Tape and Reel

Features

- AEC-Q100 qualification ongoing
- STMicroelectronics 5th generation positioning receiver with 80 tracking channels and 4 fast acquisition channels compatible with 6 constellations: GPS, Galileo, GLONASS, BeiDou, QZSS, NAVIC (former IRNSS)
- Triple band L1, L2, L5, E6 single package solution
- SBAS systems: WAAS, EGNOS, MSAS, GAGAN, BeiDou
- Code phase, carrier phase, doppler frequency measurement
- Antenna sensing
- PPS output
- Notch filter for anti-jamming
- ARM® Cortex® M7 core:
  - Maximum clock frequency 314 MHz
  - 16 KB I-cache and 16 KB D-cache
  - 64 KB I-TCM and 384 KB D-TCM, core clock speed
  - Nested vector interrupt controller
  - JTAG debugging capability
  - 256 Kbyte system RAM
- 32 channels DMA
- Memory interfaces:
  - SFC (Octal/Quad serial flash controller, SDR)
  - SD multimedia card
- Serial interfaces:
  - 3 x UART
  - Synchronous serial port (SPI supported)
  - I^2C
  - 2 x multi mode serial interfaces
  - 2 x CAN controllers
- Core peripherals:
  - 2 x multi timer units
  - Watchdog timer
  - 1 x extended function timers
  - 32 kHz oscillator real time clock
  - AES decipher hardware accelerator

- Power management unit, with separate power supply domain and on-chip LDO and high voltage/low voltage monitors:
  - Backup voltage domain 1.7 to 3.6 V with LDO for always-on core supply and HV/LV detectors, and dedicated IO-ring0
  - Main voltage domain 1.7 to 3.6 V with LDO for switchable logic domain and HV/LV detectors for 85 °C maximum ambient temperature operations or 1.2 V ± 5% external voltage supply for 105 °C maximum ambient temperature operations
  - Separate RF domain with dedicated LDO
  - IO-ring1 1.8 or 3.3 V capable, and dedicated 1.8 V LDO
  - IO-ring2 3.3 V ± 10% capable
  - Fail safe GPIOs available
- Secure-Digital Multimedia Memory Card interfaces (SDMMC)
- USB2.0 full speed (12 Mb/s) with integrated physical layer transceiver
- ESD: 2 kV (HBM) and 500 V (CDM)
- Automotive grade 105 °C option

Description

STA8135GA is part of the Teseo V family.

STA8135GA is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5 and E6 frequency bands.

1 Overview

The STA8135GA is part of the Teseo V family: it's a MultiChipModule (MCM) combining in a single package both STA8100GA and STA5635A.

It is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5 and E6 frequency bands.

The STA8135GA is able to manage most of the GNSS bands (L1, L2, L5, E6) allowing even to receive simultaneously three frequencies L1/L2/L5 or L1/L5/E6 in a single package without the need of any external RF front-end.

It provides to the main host via serial interface the precise raw measurements of all the visible GNSS satellites to let run any possible precise position algorithm. STA8135GA provides also an autonomous precision positioning calculation to main host using all the satellites constellations.

The STA8135GA is compliant with ST Automotive Grade qualification which includes in addition to AEC-Q100 requirements a set of production flow methodologies targeting zero defect per million.

The STA8135GA, fulfilling high quality and service level requirements of the Automotive market, is the ideal solution for in-dash navigation, smart antenna, car to car, V2X, OEM telematics, marine, drone, lawnmower and many other applications requiring a precise position.

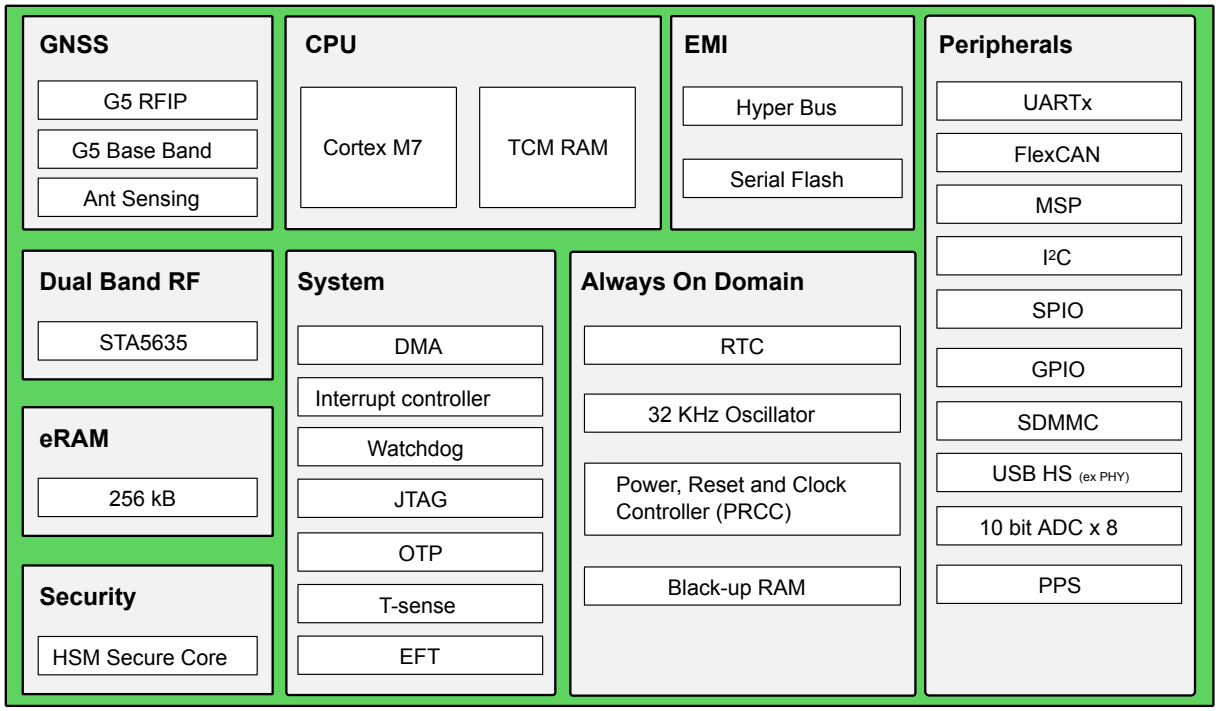
It embeds separated LDOs to supply, the analog parts, the digital core and the IO ring of the device facilitating requirements to external power supply.

The chip is manufactured in CMOS technology and housed in a TFBGA package 160 balls 11x7 mm body size 0.65 mm pitch.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. **STA8135GA block diagram**



2.2 Package

TFBGA 160 balls with 7x11x1.2 mm body size and 0.65 mm ball pitch.

2.3 Ball list

Figure 2. **Device ballout**

Note: Balls all have alternate functionalities, which can be selected by relevant registers.

Table 1. **Power supply pins**

Symbol	I/Ovoltage	I/O	Description	Ball
VRF_IN	1.70 to 3.6 V	PWR	LDO RF power input - IO ring RF	M10
VRF_OUT	1.2 V	PWR	LDO RF power output	N10
VCC_LNA	1.2 V	PWR	LNA power input	T10
VCC_PLL	1.2 V	PWR	RF VCC power input	T8
VBK_IN(1)	1.62 to 3.6 V	PWR	LDO Backup power input - IO ring 0	R6
VBK_OUT	1.2 V	PWR	LDO Backup power output	N5

Symbol	I/Ovoltage	I/O	Description	Ball
VCORE_IN	1.70 to 3.6 V	PWR	LDO Core power input	F3, P3
VDD_EXT_REG	1.2 V	PWR	LDO Core power output	F1, N4, N7, R2, R3
VIO2_IN	3 to 3.6 V	PWR	LDO IO ring 2 power input - IO ring 2	G1, H1, J10
VIO1_EXT	1.70 or 3.6 V	PWR	LDO IO ring 1 power output - IO ring 1 input	M3, N3, P2, T2
GND_PMU	GND	GND	Main voltage regulator ground	G2
GND_BKP_PMU	GND	GND	Backup voltage regulator ground	P5
GND_TSENS	GND	GND	Temperature sense block ground	D10
GND_RF	GND	GND	RF ground	P9, R9, M8, N8, P8, R8
GND	GND	GND	Ground	F8, M7, N6, M4, E3, E4, T3, F2
LDO_1V1_OUT_0	1.1 V	PWR	LDO 1.1V OUT_0	A1
PLL_VCCp_0	1.2 V	PWR	RF VCC_0 power input	A3
LDO_RF_OUT_1V1_0	1.2 V	PWR	LDO RF_0 power output	A4
LDO_IN_3V3_1V8_0	1.70 or 3.6 V	PWR	LDO RF_0 power input - IO ring RF	A5
RFA_IF_VCC_0	1.2 V	PWR	RFA_IF_VCC_0	A7
LNA_VCC_0	1.2 V	PWR	LNA_VCC_0	A9
RF_GND_0	GND	PWR	RF_GND_0	A10, B5, B6, B7, B8, B9, C10, C7
GND_0	GNS	PWR	GND_0	B4, C4, D3, D5
LDO_1V8_OUT_0	1.8 V	PWR	LDO_1V8_OUT_0	B1
LDOS_VCC_0	1.10 to 1.8 V	PWR	LDO_0 power input	C1
VCORE_OUT_2V5	2.5 V	PWR	VCORE_OUT_2V5	F5
VDD_SQI	-	PWR	VDD_SQI	R4

1. *Backup power shall be applied at the same time or before VCORE_IN, not after.*

Table 2. Main function pins

Symbol	I/Ovoltage(1)	I/O	Description	Ball	Reset state
EXT_REG_SEL	VCORE_IN	I	LDO Core Disable. When High the LDO CORE is off. Core issupplied by an external power source.	C3	NA
TEST	IOring2	I	TEST -JTAG enable. In mission/application mode this pin must be connected to GND.	D4	Hi-Z/PD
RTC_XTI	VBK_IN/IOring0	I	If 32 kHz oscillator enabled then input of the 32 kHz oscillator amplifier circuit. Else CMOS input as electrical characteristic table. Both cases, it is the reference for real time clock counter circuitry.	T5	NA
RTC_XTO	VBK_IN/IOring0	O	Output of the oscillator amplifier circuit.	T6	NA
RESETn	VBK_IN/IOring0	I	Reset input with Schmitt-Trigger characteristics and noise.	R5	Hi-Z/PD
WAKEUP	VBK_IN/IOring0	I	When high, the device will wakeup and exit from Standby mode. It has higher priority compared to Standby_in pin. Wakeup from Standby mode.	P6	Hi-Z
STANDBY_IN(2)	VBK_IN/IOring0	I	When low, the chip is forced in Standby mode.	R7	Hi-Z
STANDBY_OUT	VBK_IN	O	When low, it indicates device is in Standby mode.	P7	Hi-Z

1. *In Standby mode, if VIO1 and VIO2 are powered, GPIOs have no driving capabilities and no PD/PU is active.*
2. *If VCORE_IN is removed before STANDBY_IN has switched from high to low, STANDBY_OUT remains high level, even if device enters in Standby mode.*

Table 3. RF front-end pins

Symbol	I/O voltage	I/O	Description	Ball
ANTSens2/AIN1	IO ring RF	I	Antenna sensing - TPIF_P	M9
ANTSens1/AIN0	IO ring RF	I	Antenna sensing - TPIF_N	N9
LNA_IN	LNA VCC	I	LNA input	T9
LNA_OUT	LNA VCC	O	LNA output	R10
RFA_IN	VRFOUT	I	RFA input	P10
TCXO_IN	PLL VCC	I	TCXO input	T7
XTAL_IN_0	PLL VCC	I	TCXO_0 input	A2
RFA_IN_0	VRFOUT	I	RFA_0 input	A6
LNA_OUT_0	LNA_VCC_0	O	LNA_0 output	A8
LNA_IN_0	LNA_VCC_0	I	LNA_0 input	B10
TP_N_SENSE2_0	IO ring RF	I	Antenna sensing - TPIF_P_0	B2
TP_P_SENSE1_0	IO ring RF	I	Antenna sensing - TPIF_N_0	B3
CHIP_EN_0	IO ring RF	-	Chip_En_0	C2
TCXO_CLK_0	PLL_VCCp_0	I	TCXO_CLK_0 input	D1

Table 4. SQI Memory interface (power fail safe IOs)

Symbol	I/O voltage	I/O	Description	Ball	Reset state
SFC_CLK	IO ring1	O	Serial flash controller clock	R1	Hi-Z/PD
SFC_CSN	IO ring1	O	Serial flash controller chip select	J6	Hi-Z/PD
SFC_SIO0	IO ring1	I/O	Serial flash controller data IO 0	P1	Hi-Z/PD
SFC_SIO1	IO ring1	I/O	Serial flash controller data IO 1	M2	Hi-Z/PD
SFC_SIO2	IO ring1	I/O	Serial flash controller data IO 2	M1	Hi-Z/PD
SFC_SIO3	IO ring1	I/O	Serial flash controller data IO 3	T4	Hi-Z/PD

Table 5. External RF interface (power fail safe IOs)

Symbol	I/Ovoltage(1)	I/O	Description	Ball
ISIG1	IOring1 (FS)	I	Ex RF interface I-Sign1	H6
IMAG1	IO ring1 (FS)	I	Ex RF interface I-Mag1	K6
QSIG1	IO ring1 (FS)	I	Ex RF interface Q-Sign1	J2
QMAG1	IO ring1 (FS)	I	Ex RF interface Q-Mag1	L6
ISIG2	IOring1 (FS)	I	Ex RF interface I-Sign2	F6
IMAG2	IO ring1 (FS)	I	Ex RF interface I-Mag2	J3
QSIG2	IO ring1 (FS)	I	Ex RF interface Q-Sign2	K4
QMAG2	IO ring1 (FS)	I	Ex RF interface Q-Mag2	E6

1. *(FS) Fail Safe IO*

Table 6. Communication interface pins

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO6	IO ring2 (FS)	I/O	Default	GPIO6	-	D2	PD

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO6	IO ring2 (FS)	I	ALT A	CAN0_RX	CAN Receiver	D2	-
		O	ALT B	-	-		-
		I/O	ALT C	I2C_SDA	I_2C Data		-
GPIO5	IO ring2 (FS)	I/O	Default	GPIO5	-	G3	PD
		O	ALT A	CAN0_TX	CAN Transmitter		-
		I	ALT B	SFC_DQS	Serial Flash Controller DQS		-
		I/O	ALT C	I2C_CLK	I^2C Cock		-
PPS_OUT	IO ring2 (FS)	I/O	Default	GPIO32	-	E8	PD
		O	ALT A	-	-		-
		O	ALT B	UART0_TX	UART0 Transmitter		-
		O	ALT C	PPS_OUT	-		-
MSP1_clk_out	IO ring1 (FS)	I/O	Default	GPIO91	-	L3	PD
		O	ALT A	MSP1_clk_out	MSP1 Master Clock		-
		I	ALT B	SPI_CK	-		-
		O	ALT C	CLKOUT	Clock Output		-
MSP1_CS	IO ring1 (FS)	I/O	Default	GPIO90	-	M5	PD
		I/O	ALT A	MSP1_CS	MSP1 Master Chip Select		-
		I	ALT B	SPI_CS	-		-
		I	ALT C	UART2_RX	UART2 Receiver		-
MSP1_Din	IOring1 (FS)	I/O	Default	GPIO94	-	L4	PD
		I	ALT A	MSP1_Din	MSP1 Data Input		-
		I	ALT B	SPI_SI	SPI ChipSelect		-
		O	ALT C	OCTOSPI_CLKn	OctoSPI Clock Inverted		-
MSP1_Dout	IO ring1 (FS)	I/O	Default	GPIO95	-	L5	PD
		O	ALT A	MSP1_Dout	MSP1 Data Output		-
		O	ALT B	SPI_SO	SPI Data Output		-
		O	ALT C	UART2 TX	UART2 Transmitter		-
JTAG-TRSTn	IOring2 (FS)	I/O	Default	JTAG-TRSTn	JTAG Reset	D7	PD
		O	ALT A	-	-		-
		I	ALT B	-	-		-
		I	ALT C	Timer_OCMPA	Timer AInput		-
JTAG-TCK	IOring2 (FS)	I/O	Default	JTAG-TCK	JTAG Clock	C8	PD
		I	ALT A	SPI_CK	SPI Slave Clock		-
		O	ALT B	MSP0_clk_out	MSP0 Master Clock		-
		I	ALT C	Timer_ICAPA1	Timer AInput		-
JTAG-TMS	IOring2 (FS)	I/O	Default	JTAG-TMS	JTAG TMS	D6	PU
		I	ALT A	SPI_CS	SPI Slave Chip Select		-
		O	ALT B	MSP0_Din	MSP0 Data Input		-
		O	ALT C	UART0_RTS	UART0 RTS		-
JTAG-TDI	IOring2 (FS)	I/O	Default	JTAG-TDI	JTAG Data Input	D8	PU

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
JTAG-TDI	IOring2 (FS)	I	ALT A	SPI_SI	SPI Data Input	D8	-
		I/O	ALT B	MSP0_Dout	MSP0 Data Output		-
		O	ALT C	UART0_CTS	UART0 CLR		-
JTAG-TDO	IOring2 (FS)	I/O	Default	JTAG-TDO	JTAG Data Output	E6	PD
		O	ALT A	SPI_SO	SPI Data Output		-
		O	ALT B	MSP0_CS	MSP0 Chip Select		-
		I	ALT C	PPS_IN	PPS Input		-
UART1_RX	IO ring2	I/O	Default	USB_DM	USB Minus	J7	PD
		I	ALT A	UART1_RX	UART1 Receiver		-
		I/O	ALT B	I2C_SDA	I^2C Data		-
		I	ALT C	CAN1_RX	CAN1 Receiver		-
UART1_TX	IO ring2	I/O	Default	USB_DP	USB Positive	J6	PD
		O	ALT A	UART1_TX	UART1 Transmitter		-
		I/O	ALT B	I2C_CLK	I^2C Clock		-
UART2_RX	IO ring2 (FS)	I/O	Default	GPIO89	-	E1	PD
		I	ALT A	UART2_RX	UART2 Receiver		-
		I/O	ALT B	-	-		-
		O	ALT C	-	-		-
UART2_TX	IO ring2 (FS)	I/O	Default	GPIO88	-	E2	PD
		O	ALT A	UART2_TX	UART2 Transmitter		-
		I/O	ALT B	-	-		-
		O	ALT C	-	-		-
GPIO67	IOring2	I/O	Default	GPIO67	-	C9	PD
		O	ALT A	-	-		-
		I/O	ALT B	UART0_RX	-		-
		I	ALT C	PPS_IN	-		-
GPIO8	IO Ring 2	I/O	Default	GPIO 8	-	C5	PD
		I	ALT A	MII_TX_EN	-		-
		O	ALT B	i_g5rf_MONITOR_LDO_sig	-		-
		O	ALT C	I_sign2	-		-
GPIO7	IO Ring 2	I/O	Default	GPIO 7	-	C6	PD
		O	ALT A	MII_TX_CLK	-		-
		O	ALT B	i_g5rf_MONITOR_PLL_sig	-		-
		O	ALT C	I_sign	-		-
GPIO1	IO Ring 2	I/O	Default	GPIO 1	-	C8	PD
		O	ALT A	SPI_CK	-		-
		O	ALT B	MSP0_clk_out	-		-
		O	ALT C	Timer_ICAPA1	-		-
GPIO2	IO Ring 2	I/O	Default	GPIO 2	-	D6	PD
		O	ALT A	SPI_CS	-		-
		I	ALT B	MSP0_Din	-		-

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO2	IO Ring 2	I	ALT C	UART0_RTS	-	D6	-
GPIO0	IO Ring 2	I/O	Default	GPIO 0	-	D7	PD
		O	ALT A	PPS_OUT	-		-
		O	ALT B	BLANK_INT	-		-
		O	ALT C	Timer_OCMPA	-		-
GPIO3	IO Ring 2	I/O	Default	GPIO 3	-	D8	PD
		I	ALT A	SPI_SI	-		-
		O	ALT B	MSP0_Dout	-		-
		O	ALT C	UART0_CTS	-		-
GPIO33	IO Ring 2	I/O	Default	GPIO 33	-	D9	PD
		O	ALT A	SPI_CS	-		-
		O	ALT B	Timer_OCMPB1	-		-
		O	ALT C	OCTOSPI_CEN1	-		-
GPIO34	IO Ring 2	I/O	Default	GPIO 34	-	F9	PD
		O	ALT A	SPI_CK	-		-
		-	ALT B	-	-		-
		O	ALT C	OCTOSPI_CEN1	-		-
GPIO35	IO Ring 2	I/O	Default	GPIO 35	-	E10	PD
		O	ALT A	SPI_DO	-		-
		O	ALT B	Timer_OCMPA1	-		-
		-	ALT C	-	-		-
GPIO36	IO Ring 2	I/O	Default	GPIO 36	-	E9	PD
		I	ALT A	SPI_SI	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO43	IO Ring 2	I/O	Default	GPIO 43	-	E5	PD
		O	ALT A	Timer_ICAPA	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO4	IO Ring 2	I/O	Default	GPIO 4	-	E7	PD
		O	ALT A	SPI_SO	-		-
		O	ALT B	MSP0_CS	-		-
		I	ALT C	PPS_IN	-		-
GPIO92	IO Ring 2	I/O	Default	GPIO 92	-	F10	PD
		I	ALT A	MSP1_clk_in	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO77	IO Ring 2	I/O	Default	GPIO 77	-	F4	PD
		I	ALT A	CAN1 RX	-		-
		-	ALT B	MII_PTP_AUX_TS_TRIG0	-		-
		-	ALT C	-	-		-

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO48	IO Ring 2	I/O	Default	GPIO 48	-	F7	PD
		O	ALT A	MSP0_clk_out	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO76	IO Ring 2	I/O	Default	GPIO 76	-	G4	PD
		O	ALT A	CAN1 TX	-		-
		-	ALT B	MII_MDC_O	-		-
		-	ALT C	-	-		-
GPIO47	IO Ring 2	I/O	Default	GPIO 47	-	G5	PD
		O	ALT A	MSP0_CS	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO51	IO Ring 2	I/O	Default	GPIO 51	-	G6	PD
		I	ALT A	MSP0_Din	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO52	IO Ring 2	I/O	Default	GPIO 52	-	G7	PD
		O	ALT A	MSP0_Dout	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO86	IO Ring 2	I/O	Default	GPIO 86	-	H2	PD
		O	ALT A	UART1 TX	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO87	IO Ring 2	I/O	Default	GPIO 87	-	H3	PD
		I	ALT A	UART1 RX	-		-
		-	ALT B	MII_PTP_AUX_TS_TRIG1	-		-
		-	ALT C	-	-		-
GPIO78	IO Ring 2	I/O	Default	GPIO 78	-	H4	PD
		O	ALT A	MMC CLK	-		-
		I	ALT B	TCXO_CLK	-		-
		)	ALT C	CLK64FO	-		-
GPIO50	IO Ring 2	I/O	Default	GPIO 50	-	H5	PD
		O	ALT A	MSP0_L/R	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO37	IO Ring 2	I/O	Default	GPIO 37	-	J1	PD
		I	ALT A	UART0_RX	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO42	IO Ring 2	I/O	Default	GPIO 42	-	K1	PD

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO42	IO Ring 2	O	ALT A	UART0_DTR	-	K1	-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO38	IO Ring 2	I/O	Default	GPIO 38	-	K2	PD
		O	ALT A	UART0_TX	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO44	IO Ring 2	I/O	Default	GPIO 44	-	K3	PD
		O	ALT A	Timer_OCMPA	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO49	IO Ring 2	I/O	Default	GPIO 49	-	K5	PD
		O	ALT A	MSP0_clk_in	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
USB_DM	IO Ring 2	I/O	Default	USB_DM	-	K8	PD
		-	ALT A		-		-
		-	ALT B		-		-
		-	ALT C		-		-
USB_DP	IO Ring 2	I/O	Default	USB_DP	-	K9	PD
		-	ALT A		-		-
		-	ALT B		-		-
		-	ALT C		-		-
GPIO23	IO Ring 2	I/O	Default	GPIO 23	-	L1	PD
		O	ALT A	SFC_SIO1	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO1	-		-
GPIO24	IO Ring 2	I/O	Default	GPIO 24	-	L2	PD
		O	ALT A	SFC_SIO2	-		-
		-	ALT B	GPIO 24	-		-
		I/O	ALT C	OCTOSPI_SIO2	-		-
GPIO26	IO Ring 2	I/O	Default	GPIO 26	-	M1	PD
		O	ALT A	SFC_SIO4	-		-
		-	ALT B	MMC CLK	-		-
		I/O	ALT C	OCTOSPI_SIO4	-		-
GPIO27	IO Ring 2	I/O	Default	GPIO 27	-	M2	PD
		O	ALT A	SFC_SIO5	-		-
		-	ALT B	MMC CMD	-		-
		I/O	ALT C	OCTOSPI_SIO5	-		-
GPIO22	IO Ring 2	I/O	Default	GPIO 22	-	N1	PD
		O	ALT A	SFC_SIO0	-		-

Symbol after bootstrap	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO22	IO Ring 2	-	ALT B	-	-	N1	-
		-	ALT C	OCTOSPI_SIO0	-		-
GPIO25	IO Ring 2	I/O	Default	GPIO 25	-	N2	PD
		O	ALT A	SFC_SIO3	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO3	-		-
GPIO61	IO Ring 2	I/O	Default	GPIO 61	-	P4	PD
		O	ALT A	SFC_CSN	-		-
		-	ALT B	-	-		-
		O	ALT C	OCTOSPI_RWDS	-		-
GPIO62	IO Ring 2	I/O	Default	GPIO 62	-	T1	PD
		O	ALT A	SFC_CLK	-		-
		I/O	ALT B	GPIO 62	-		-
		O	ALT C	OCTOSPI_CLK	-		-

1. *(FS) Fail Safe IO*

Table 7. OCTA SPI Memory interface (power fail safe IOs)

Symbol	I/O voltage	I/O	Description	Ball	Reset
OCTOSPI_RWDS	IO ring1	O	-	H7	Hi-Z/PD
OCTOSPI_CEN0	IO ring1	O	OCTO SPI flash controller chip select	J4	Hi-Z/PD
OCTOSPI_CEN1	IO ring1	O	OCTO SPI flash controller chip select	J5	Hi-Z/PD
OCTOSPI_SIO0	IO ring1	I/O	OCTO SPI flash controller data IO 0	J9	Hi-Z/PD
OCTOSPI_SIO1	IO ring1	I/O	OCTO SPI flash controller data IO 1	K7	Hi-Z/PD
OCTOSPI_SIO2	IO ring1	I/O	OCTO SPI flash controller data IO 2	J7	Hi-Z/PD
OCTOSPI_SIO3	IO ring1	I/O	OCTO SPI flash controller data IO 3	J8	Hi-Z/PD
OCTOSPI_SIO4	IO ring1	I/O	OCTO SPI flash controller data IO 4	H9	Hi-Z/PD
OCTOSPI_SIO5	IO ring1	I/O	OCTO SPI flash controller data IO 5	H8	Hi-Z/PD

Table 8. ADC

Symbol	I/O voltage	I/O	Description	Ball	Reset
ADC6	-	I	ADC channel 6	K10	-
ADC0	-	I	ADC channel 0	L10	-
GND_ADC	-	GND	ADC ground	L7	-
ADC4	-	I	ADC channel 4	L8	-
ADC2	-	I	ADC channel 2	L9	-
VADC_IN	-	I	ADC voltage	M6	-

3 General description

3.1 Multi-constellation and multi-band

The constellations that STA8135GA supports are the following ones:

- GPS (L1 C/A, L2C, and L5)
- GLONASS (L1OF, L2OF)
- BeiDou (B1C, B1I, B2a, B2I)
- GALILEO (E1, E5a, E5b, E6)
- QZSS (L1 C/A, L2C, L5)
- NAVIC - former IRNSS (L5)

Carrier phase raw measurements are also provided.

STA8135GA supports a wide range of combinations of such signals and bands without the need of external RF front end. The most important GNSS user cases that can be supported by STA8135GA are listed in the below table. Each of those cases would require a dedicated firmware.

Table 9. GNSS user cases

Constellation	GPS/QZSS			Glonass		BeiDou			Galileo				NAVIC	SBAS
Frequency	L1 C/A	L2C	L5	L1OF	L2OF	B1I	B2I	B2A	E1	E5b	E5A	E6	L5	L1 C/A
Case 0	X	X	-	X	X	X	-	-	X	-	-	-	-	X
Case 1	X	X	-	X	-	X	X	-	X	-	-	-	-	X
Case 2	X	X	-	X	-	X	-	-	X	X	-	-	-	X
Case 3	X	-	X	X	-	X	-	X	X	-	-	-	-	X
Case 4	X	-	X	X	-	X	-	-	X	-	X	-	-	X
Case 5	X	-	X	X	-	X	-	-	X	-	-	-	X	X
Case 6	X	-	X	-	-	-	-	-	X	-	X	X	-	X
Case 7	X	-	X	-	-	X	-	X	X	-	-	-	X	X
Case 8	X	-	X	-	-	X	-	-	X	-	X	-	-	X
Case 9	X	X	X	-	-	X	X	X	-	-	-	-	-	X
Case 10	X	X	X	-	-	-	-	-	X	X	X	-	-	X

Note: Maximum 72 satellites tracked simultaneously.

3.2 RF front end (G5RF)

The integrated RF front-end is able to support different bands (L1, L2, L5, and E6) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.

The RF_IF chain is followed by a 3-bit ADC able to convert the IF signal to Sign (SIGN) and Magnitude (MAG1, MAG0) bit. The MAG bit is internally integrated in order to control the variable gain amplifiers.

The embedded fractional PLL allows supporting a wide range of reference clocks (10 to 55 MHz).

3.3 Multi-band multi-constellation base band (G5BB) processor

STA8135GA integrates G5BB proprietary IP, which is the STMicroelectronics latest generation high-sensitivity baseband processor fully compliant with all different constellations and bands: GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS systems.

3.4 MCU sub system

The Cortex® M7 core masters the system resources (memories, registers, and external memory controllers) through the AXI, AHB and APB interconnects present in the SOC.

3.4.1 Caches

The size of instruction and data cache used for ARM® sub-system in STA8135GA is 16 KB each.

3.4.2 TCM

ARM® Cortex® M7 has TCM Control Unit (TCU) with TCM interfaces and an AHB slave (AHBS) interface for system access to TCMs. These TCM memories are integrated outside the ARM® sub-system. STA8135GA has 64 KB ITCM memory and 384 KB of DTCM memory.

In the DTCM memory 160 KB is dedicated for ARM® usage and remaining 224 KB DTCM is shared between the ARM® sub-system and G5BB module.

ARM® provides access to TCM memories through an AHB slave interface. This AHBS interface is connected to the AMBA infrastructure in STA8135GA so that DMA present on the bus can access the TCM memories MCU.

3.4.3 Nested Vector Interrupt Controller (NVIC)

This Nested Vectored Interrupt Controller (NVIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. ARM® Cortex® M7 has NVIC module for handling the interrupts. The NVIC supports 128 interrupts with 16 levels of priority, which can be changed dynamically. The software can control each request line to generate software interrupts.

3.4.4 AXI bus

AXI Bus matrix handles major high bandwidth transactions for STA8135GA. It connects the SRAM, boot ROM and external memory controllers, which provide access to the external Flash. ARM® acts as a master on this bus with the highest priority.

3.5 APB peripherals

3.5.1 APB bridge 2 peripherals

AHB to APB Bridge 2 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix 0.

The peripherals connected to APB 2 are: UART2, MSP1, GPIO PORT 2, MTU1.

3.5.2 APB bridge 1 peripherals

AHB to APB bridge 1 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 1 are UART1, EFT0, EFT1, GPIO PORT 0 and 1, MTU0, OTP, SSP, Thermal sensor, Watchdog timer.

3.5.3 APB bridge 0 peripherals

AHB to APB bridge 0 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 0 are the ones on the always on domain: PRCC always ON, RTC.

3.5.4 AHB slave devices

There are some AHB slave devices which are connected to AHB bus matrix 0.

3.6 eSRAM

256 KB of embedded RAM are available on top of the TCM RAM.

The eSRAM is directly connected to the MCU through the AXI bus. It can be used for data and instruction.

3.7 Serial Flash Memory Controller (SFC)

The Serial Flash Memory Controller supports single, quad and octal memories. It can be used for in place execution thanks to direct memory mapping.

3.8 SSP

STA8135GA has one Synchronous Serial Ports (SSPs). The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:

- Serial peripheral interface bus standards
- Synchronous serial protocol bus standards
- Micro-wire interface bus standards
- Unidirectional interface

In both master and slave configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and pre-scaler
- Programmable clock phase and polarity in SPI mode
- Support for direct memory access (DMA)

3.9 UART

The UARTx performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) to receive. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to sixteen words per transfer.

3.10 Watchdog Timer (WDT)

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (Irq_wdt), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. The WDT is counting down at a fixed frequency of 32.768 kHz.

The watchdog timer peripheral can be used as free-running timer or as watchdog to resolve processor malfunctions due to hardware or software failures.

Feature set overview:

- 16-bit down counter
- 8-bit clock pre-scaler
- Safe reload sequence
- Free-running timer mode
- End of counting interrupt generation

3.11 GPIO

There are 34 GPIOs in this device.

The GPIO block provides programmable inputs or outputs. Each input or output can be controlled in two modes:

- Software mode through an APB bus interface
- Alternate function mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

A de-bouncing logic can be enabled for each GPIO to filter glitches on IOs before going to the Interrupt generation and CPU read value.

All GPIOs are fail safe to avoid leakage consumption in any condition even when the ring is off and the external line is logic level high.

3.12 Multi Timer Unit (MTU)

Multi Timer Unit consists of eight timers. Each timer is clocked by MXTAL frequency divided by 8 (which means 2.4 MHz with a 19.2 MHz crystal) or REFCLK (32.768 kHz) inputs.

3.12.1 MTU feature overview

- The Multi Timer Unit provides access to four interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs) allowing up to four counts to be performed in parallel.
- The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.
- In each FRC the 32-bit counter is split up into two 16-bit counters.

3.13 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 256 bytes SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake up the system when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features:

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer + fractional part) to the 47-bit counter

Once set by the MCU this bit is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.14 MSP

STA8135GA has one Multi mode Serial Port (MSP).

The following section describes the functionalities of the MSP unit.

The Multi mode Serial Port (MSP) is a synchronous transmitter serial interface.

The MSP provides:

- Element (data) sizes of 8, 10, 12, 14, 16, 20, 24, and 32 bits, LSB or MSB first
- Programmable frequency shift clock for data transfer
- Direct interface to SPI compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), 32 bits wide, 8 locations deep

3.15 Direct Memory Access (DMA)

The DMAC is an Advanced Microcontroller Bus Architecture (AMBA) compliant System-on-Chip (SoC) peripheral. The DMAC is an AMBA AHB module, and connects to the Advanced High-performance Bus (AHB).

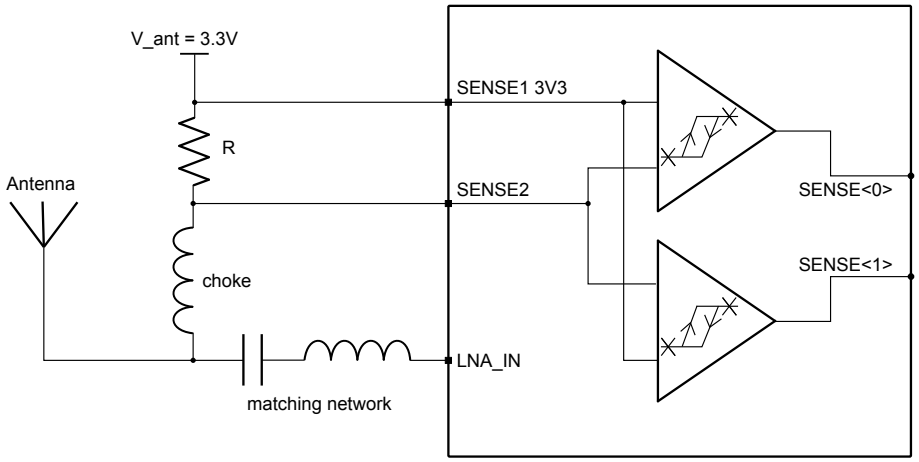
Module key features:

- Eight DMA channels. Each channel can support an unidirectional transfer.
- The DMAC provides 32 peripheral DMA request lines.
- Single DMA and burst DMA request signals.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA support through the use of linked lists.
- Hardware DMA channel priority. DMA channel 0 has the highest priority and channel 31 has the lowest priority.
- If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface to the DMA control registers.
- Two AHB bus masters for transferring data.
- Programmable DMA burst size.
- Working on AHB clock.

3.16 Antenna sensing

The following figures show how the antenna sensing circuit works. SENSE1 and SENSE2 input voltage range must be between VRF_IN and GND.

Figure 3. Antenna sensing configuration when antenna is supplied with 3.3 V



Antenna sensing detection in STA8135GA uses two comparators with hysteresis. If the antenna is supplied with a voltage of 3.3 V the antenna sensing can be connected as showed in the picture.

In the following tables are showed thresholds when current is rising and when is falling with R = 1.4 Ω and V_ant = 3.3 V.

Table 10. Antenna sensing current - power rising

Current from antenna (when current is rising)	SENSE <1>	SENSE <0>
I < 24 mA	0	0
24 ≤ I ≤ 62 mA	0	1
I > 62 mA	1	1

Table 11. **Antenna sensing current - power falling**

Current sunk from antenna (when current is falling)	SENSE <1>	SENSE <0>
I > 53 mA	1	1
16 ≤ I ≤ 53 mA	0	1
I < 16 mA	0	0

3.17 Temperature sensor

Thermal sensor provides digital measurement of junction temperature. Temperature measurement range is -40 to 125 °C. It uses integrated bandgap reference and 8-bit ADC.

The temperature sensor provides two threshold registers. Writing in these registers and enabling the threshold mode compare the temperature recorded with the threshold value. If the temperature is higher than the upper threshold register or lower than the lower threshold register, it generates an interrupt if enabled.

Table 12. **Temperature sensor**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Tsens	Sensitivity	-	-	-	1	°C
Tacc(1)	Accuracy	Calibration performed at 125 °C	± 3(2)	-	± 10	°C

1. *Best accuracy is at calibrated temperature.*
2. *Limited by manufacturing calibration environment.*

3.18 Serial boot pins

UART2-TX (Boot0) pin is used to select the boot configuration of Cortex® M7. The ROM code starts the boot process which then polls the PRCC register (UART2-TX) which has already latched the UART2-TX pin (C8 ball) status after latch reset.

Based on this register value the code is loaded from one of the two options as given in the table below:

Table 13. **Boot peripheral selection**

Pin	ROM action
UART2-TX = 0	Boot from flash memory - SFC controller
UART2-TX = 1	Boot from peripheral - UART

3.19 Reset

After a reset, the Cortex® M7 is woken-up by the ROM code.

The PRCC module is used to sequence through all the steps needed to properly reset the device and prepare it to fetch the first instruction of the user application code.

STA8135GA has the following reset options:

- Pad reset: SoC will have active low chip reset (RESET) pad. Low (zero) status on this pad will keep device in the reset. Assertion of this pin low should be minimum of 5 ms.
- Power on reset: The power on reset circuitry is embedded in the main voltage regulator built on HV supply (VCORE_IN) of regulator. It ensures all voltage monitors are under reset state until VCORE_IN (or VDD_EXT_REG) minimum voltage is reached.
- Hardware resets: The internal voltage regulator embeds multiple LVD (Low Voltage Detector) and HVD (High Voltage Detector) which are used in the reset sequence.
- Soft reset: Different peripherals present on STA8135GA can be reset independently through registers present inside PRCC module.

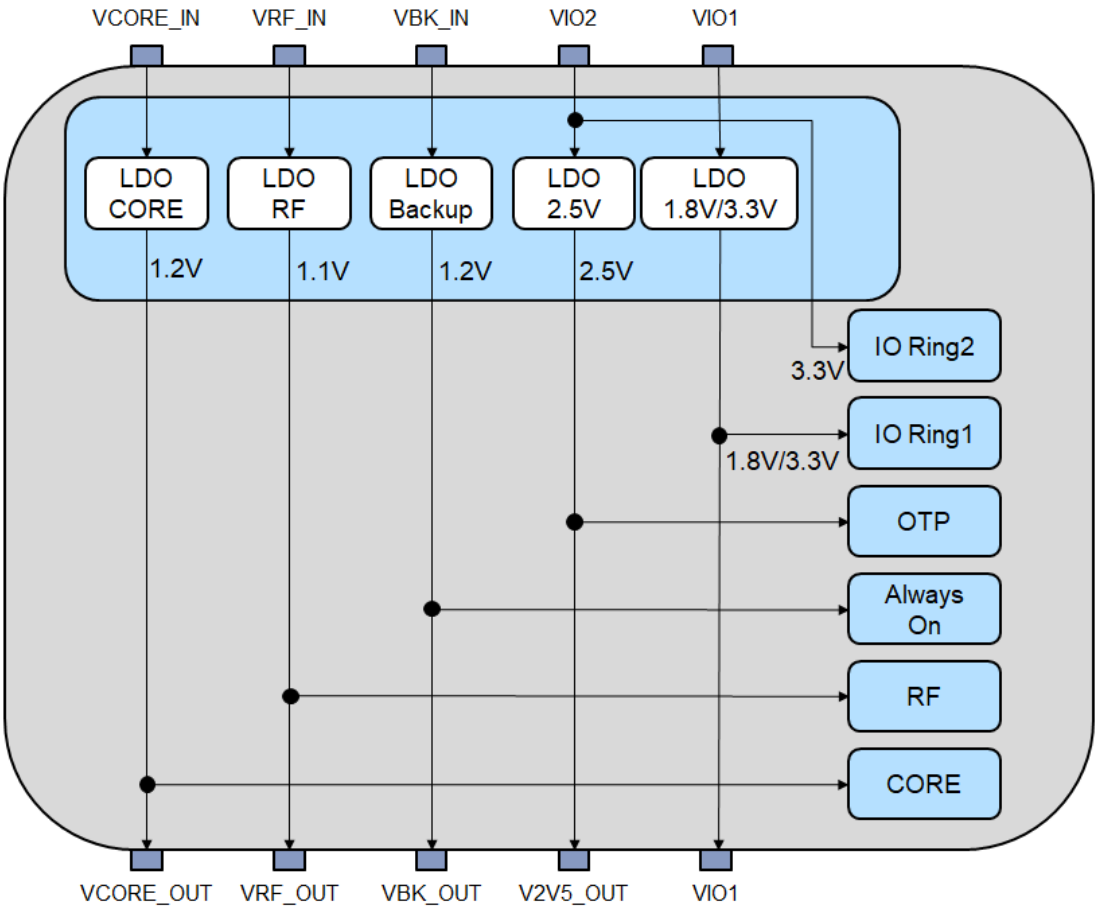
3.20 Power Management Unit (PMU)

STA8135GA embeds 5 voltage regulators (LDO):

Table 14. LDO on-chip regulators

LDO	Supply regions	Input voltage	Typical output voltage at 25 °C
CORE LDO	Core	VCORE_IN = 1.62 – 3.6 V	1.2 V
LDO2v5	Safmem, temp sensor	VIO_IN = 3.3 V	2.5 V
IO LDO	IOring 1	VIO_IN = 3.3 V	1.8 V
BACKUP LDO	Always on	VBK_IN = 1.62 – 3.6 V	1.2 V
RFLDO	RF	VRF_IN = 1.62 – 3.6 V	1.1 V

Figure 4. LDO on-chip regulators dependencies



3.20.1 Power Regions

STA8135GA has six major power regions. The modules present inside each power region are given below.

- Always on backup region: 1.2 V
  - prcc_backup
  - RTC
  - Backup RAM 256 bytes
- Switchable region: 1.2 V
  - ARM® core
  - Other digital IPs
- RF: 1.1 V
- OTP: 2.5 V
- IO ring1: 1.8 V or 3.3 V
- IO ring2: 3.3 V

By default IO ring1 is at 1.8 V supplied by internal LDO IO. If IO ring1 has to be at 3.3 V then external supply must be applied on VIO1 at 3.3 V.

The switchable power region can be supplied by an external voltage regulator directly at pin VDD_EXT_REG. The integrated LDO CORE has to be switched off by forcing EXT_REG_SEL to high voltage.

The usage of the external regulator to supply the switchable power region is mandatory in applications that require to sustain 105 °C.

3.21 I²C high speed controller

One I²C high speed controller interface is capable of master/slave modes in multi-master environment. It is DMA capable and multiple baud rates are supported: 100/400/1000/3400 Kbits/s.

3.22 Full speed USB 2.0

It supports 12 Mbps (full speed) and 1.5 Mbps (low speed) serial data transmission according to USB 2.0 OTG controller specification.

3.23 SDMMC (Secure Digital Multi Media Card Controller)

The SDMMC card host interface provides an interface between the APB peripheral bus and Multi Media cards (MMC), SD memory cards, SDIO cards, and CE-ATA devices.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TFBGA160 (7x11x1.2 mm) package information

Figure 5. **TFBGA160 (7x11x1.2 mm) package outline**

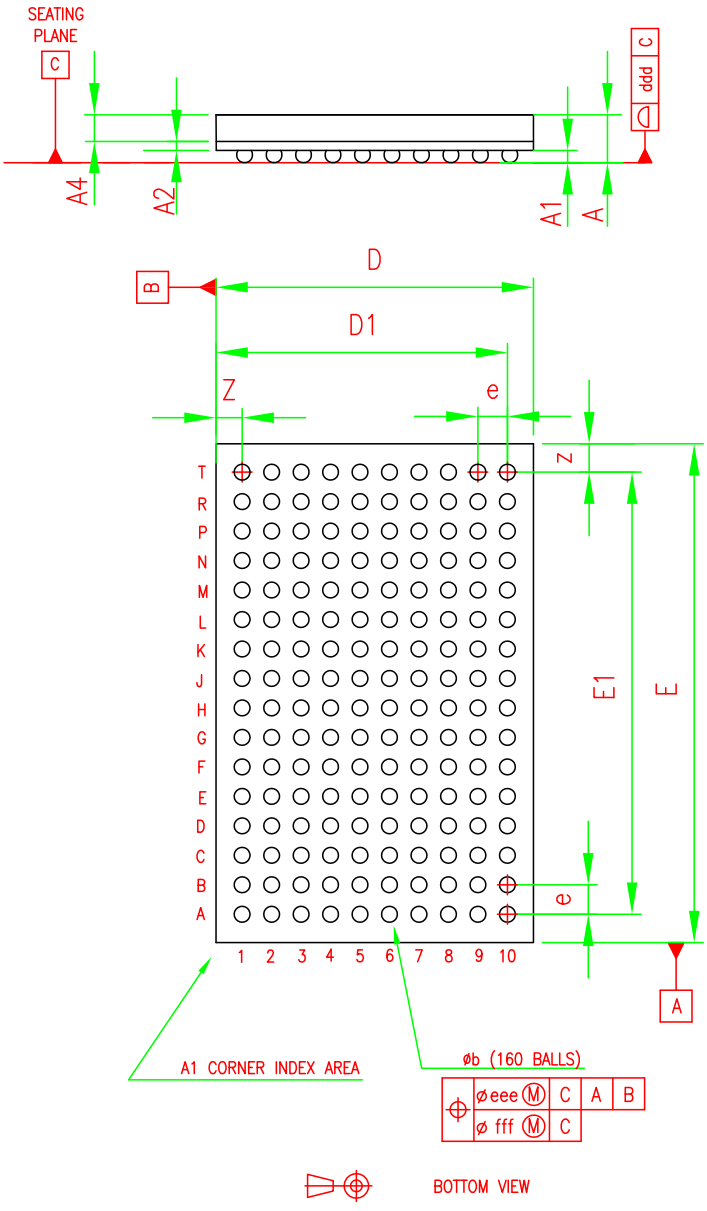


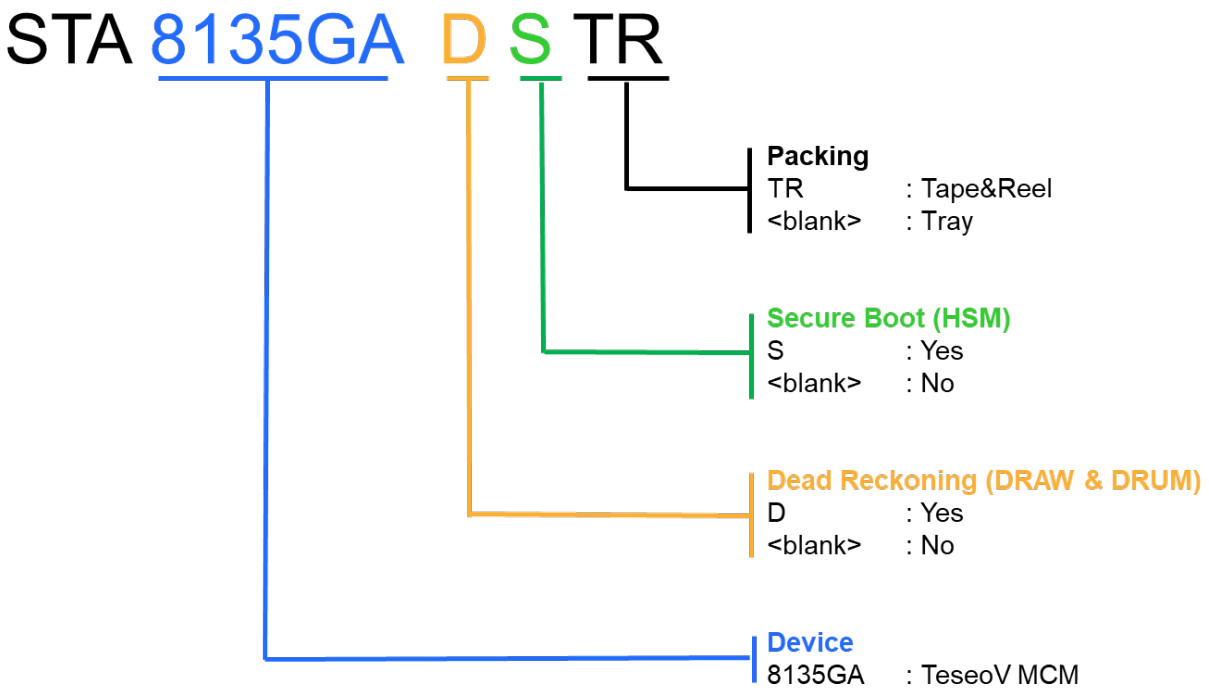
Table 15. TFBGA160 (7x11x1.2 mm) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A(1)	-	-	1.20
A1	0.20	-	-
A2	-	0.27	-
A4	-	0.585	-
b(2)	0.30	0.35	0.40
D	6.85	7.00	7.15
D1	-	5.85	-
E	10.85	11.00	11.15
E1	-	9.75	-
e	-	0.65	-
Z	-	0.625	-
ddd	-	-	0.10
eee(3)	-	-	0.15
fff(4)	-	-	0.08

1. *TFBGA stands for Thin Profile Fine Pitch Ball Grid Array.*
   - *Thin Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.*
   - *The maximum total package height is calculated by the following methodology:*
     A Max. = A1 Typ + A3 Typ + A4 Typ + √ (A1²+A3²+A4² tolerance values).
   - *Thin profile: 1.00 mm < A ≤ 1.20 mm / Fine pitch: e < 1.00 mm pitch.*
2. *The typical ball diameter before mounting is 0.35 mm.*
3. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

5 Ordering information

Figure 6. **Ordering information**



Revision history

Table 16. **Document revision history**

Date	Version	Changes
13-Oct-2021	1	Initial release.

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