Arria® 10 IDK OpenCL™ BSP

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OpenCL

PRODUCT OVERVIEW

OpenCL™ (Open Computing Language) is an open royalty-free standard for general purpose parallel programming across CPUs, GPUs and other processors, giving software developers portable and efficient access to the power of these heterogeneous processing platforms.

OpenCL™ abstracts the hardware layer from the programmer and allows him, even with little or no FPGA development skills , a quick and easy way to run his algorithms on a 100% FPGA accelerator target.

Based on Intel® SDK for OpenCL™, and optimized for REFLEX CES Arria 10 hardware, our BSPs are aligned with the "instant" philosophy of the DevKit family, gives the user the immediate ability to run OpenCL™ designs on the REFLEX CES Accelerator boards and is a quick way of implementing complex parallel algorithms targeted on REFLEX CES Arria® 10 FPGA accelerators.

Learn more about the OpenCL™ expertise in REFLEX CES

DIAGRAMS TECH SPEC DELIVERABLES

Tech spec

The REFLEX CES accelerator boards are based on Arria® 10-based with working PCI Express (PCIe) and memory interfaces

The REFLEX CES OpenCL™ BSP included all hardware interfaces implementations (10GMAC, DDR, QDR, PCIe,...) allowing the user to focus on functional OpenCL™ software only.

General BSP features:

- The FPGA architecture, including clocking, global routing, and I/Os
- Optimized performances
- Timing closure
- QSYS-based HDL design
- Tcl scripting
- PCIe
- DDR4/DDR3/QDRII+ external memory

Features of the Arria® 10 reference platform:

- OpenCL™ Host
- The host that connects to the accelerator board REFLEX CES uses PCIe Gen3 x8 (FPGA Gen3 x8 hard IP core and DMA engine.)
- OpenCL™ Global Memory (DDR, QDR, heterogeneous DDR+QDR)
- The hardware provides one or two banks of DDR4/DDR3 SDRAM, depends on the REFLEX CES Arri®a 10 board selected.
- FPGA Programming via one of the following methods:
  - Partial Reconfiguration (PR) over PCIe.
  - External cable and the Arria® 10 GX/SX FPGA Development Kit's on-board USB Download Cable II interface.

Prerequisites for the Intel FPGA SDK for OpenCL™

To install the Intel FPGA SDK for OpenCL™ and create an OpenCL™ application for REFLEX CES accelerator board, your system must meet certain hardware, target platform, and operating system requirements.

Hardware Requirements

Accelerator boards requirements:

- REFLEX CES Accelerator board
- Refer to the OpenCL™ BSP documentation
- For PCI Express accelerator boards, the host machine motherboard must have an available PCIe port slot that is at least the same width (that is, the same number of PCIe lanes) as the board.
- The host system must be running one of the following supported operating systems: For a list of supported Windows and Linux operating systems, refer to the Operating System Support page on the Intel website.

Development system requirements:

- You must have administrator privileges on the development system to install the necessary packages and drivers.
- The development system has at least 85 GBytes (GB) of free disk space for software installation.
- The development system has at least 64 GBytes of RAM.

Please refer to the REFLEX CES OpenCL™ portable station is a highly integrated and easy portable station, designed to maximize the ease-of-use for every customer. The best to design quickly your OpenCL™ design without worrying about the material.

OpenCL™ portable station is designed to provide to the user a pre-installed and ready-to-use OpenCL™ environment integrated with one REFLEX CES Accelerator board.

Software Prerequisites

Develop your host application using one of the following Intel FPGA SDK for OpenCL™ and Quartus Prime software-compatible C compiler or software development environment:

- For Windows systems, use Microsoft Visual Studio version 2010 Professional.
- For Linux systems, use the C compiler included with the GCC.

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Arria® 10 GX FMC PCIe board

INTEL COTS BOARDS

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