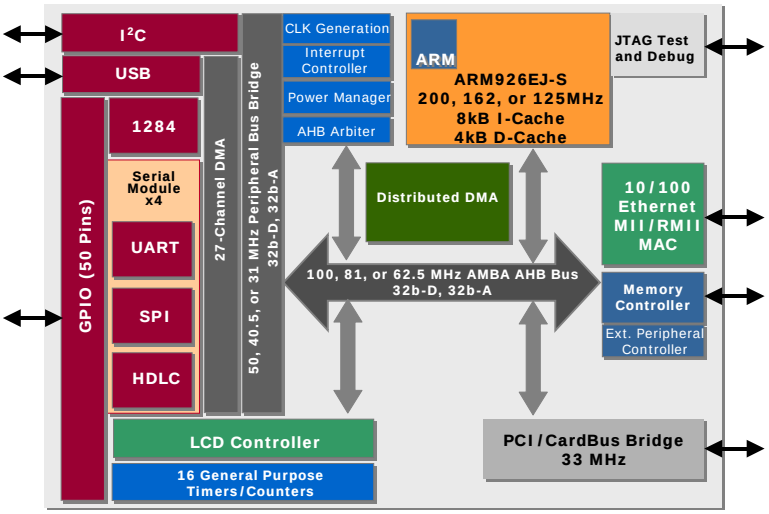
NS9750B-0 Datasheet

The Digi NS9750 is a single chip 0.13µm CMOS network-attached processor. The CPU is the ARM926EJ-S core with MMU, DSP extensions, Jazelle Java accelerator, and 8 kB of instruction cache and 4 kB of data cache in a Harvard architecture. NS9750 runs up to 200 MHz, with a 100 MHz system and memory bus and 50 MHz peripheral bus. NS9750 operates at a 1.5V core and 3.3V I/O ring voltages.



With its extensive set of I/O interfaces, Ethernet high-speed performance and processing capacity, NS9750 is the most capable of highly integrated 32-bit network-attached processors available. NS9750 is designed specifically for use in high-performance intelligent networked devices and Internet appliances including high-performance/low-latency remote I/O, intelligent networked information displays, and streaming and surveillance cameras. The NS9750 is a member of the award-winning NET+ARM family of system-on-chip (SOC) solutions for embedded systems.

NS9750 offers a connection to an external bus expansion module as well as a glueless connection to SDRAM, PC100 DIMM, Flash, EEPROM, and SRAM memories, and an external bus expansion module. It includes a versatile embedded LCD controller supporting up to 16M color TFT or 3375 color STN. NS9750 features a PCI/CardBus port as well as a USB port for applications requiring WLAN, external storage, or external sensors, imagers, or scanners. Four multi-function serial ports, an I^2C port, and 1284 parallel port provide a standard glueless interface to a variety of external peripherals. NS9750

features up to 50 general purpose I/O (GPIO) pins and highly-configurable power management with sleep mode.

NET+ARM processors are the foundation for the NET+Works® family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, operating systems, networking software, development tools, APIs, and complete development boards.

Using NS9750 and associated Net+Works packages allows system designers to achieve dramatic time-to-market reductions with pre-integrated and tested NET+ARM hardware, NET+Works software, and tools. Product unit costs are reduced dramatically with complete system-on-chip, including Ethernet, display support, a robust peripheral set, and the processing headroom to meet the most demanding applications. Customers save engineering resources, as no network development is required. Companies will reduce their design risk with a fully integrated and tested solution.

A complete NET+Works development package includes ThreadX™ picokernel RTOS, Green Hills™ MULTI® 2000 IDE or Microcross GNU X-Tools™, drivers, networking protocols and services with APIs, NET+ARM-based development board, Digi-supplied utilities, Integrated File System, JTAG In Circuit Emulator (ICE), and support for Boundary Scan Description Language (BSDL). One year software maintenance and technical support is available.

Contents

NS9750 Features

32-bit ARM926EJ-S RISC processor

- 125 to 200 MHz
- 5-stage pipeline with interlocking
- Harvard architecture
- 8 kB instruction cache and 4 kB data cache
- 32-bit ARM and 16-bit Thumb instruction sets. Can be mixed for performance/code density tradeoffs
- MMU to support virtual memory-based OSs such as Linux, WinCE/Pocket PC, VxWorks, others
- DSP instruction extensions, improved divide, single cycle MAC
- ARM Jazelle, 1200CM (coffee marks) Java accelerator
- EmbeddedICE-RT debug unit
- JTAG boundary scan, BSDL support

External system bus interface

- 32-bit data, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- 4 static and 4 dynamic memory chip selects
- 0–63 wait states per chip select
- Self-refresh during system sleep mode
- Automatic dynamic bus sizing to 8 bits, 16 bits, 32 bits
- Burst mode support with automatic data width adjustment
- Two external DMA channels for external peripheral support

System Boot

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

High performance 10/100 Ethernet MAC

- 10/100 Mbps MII/RMII PHY interfaces
- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kB RX FIFO
- 256 byte TX FIFO with on-chip buffer descriptor ring
  - Eliminates underruns and decreases bus traffic
- Separate TX and RX DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

PCI/CardBus port

- PCI v2.2, 32-bit bus, up to 33 MHz bus speed
- Programmable to:
  - PCI device mode
  - PCI host mode:

    Supports up to 3 external PCI devices

    Embedded PCI arbiter or external arbiter
- CardBus host mode

Flexible LCD controller

- Supports most commercially available displays:
  - Active Matrix color TFT displays — Up to 24bpp direct 8:8:8 RGB; 16M colors
  - Single and dual panel color STN displays — Up to 16bpp 4:4:4 RGB; 3375 colors
  - Single and dual-panel monochrome STN displays — 1, 2, 4bpp palettized gray scale
- Formats image data and generates timing control signals
- Internal programmable palette LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

USB ports

- USB v.2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Configurable to device or OHCI host
  - USB host is bus master
  - USB device supports one bidirectional control endpoint and 11 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel; 13 channels total
- 20 byte RX FIFO and 20 byte TX FIFO

Serial ports

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 6.25 Mbps: synchronous mode
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for RX clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte TX FIFO and 32 byte RX FIFO per module

I^2C port

- I^2C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I^2C bus arbitration

1284 parallel peripheral port

- All standard modes: ECP, byte, nibble, compatibility (also known as SPP or “Centronix”)
- RLE (run length encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

High performance multiple-master/distributed DMA system

- Intelligent bus bandwidth allocation (patent pending)
- System bus and peripheral bus

System bus:

- Every system bus peripheral is a bus master with a dedicated DMA engine

Peripheral bus:

- One 13-channel DMA engine supports USB device
  - 2 DMA channels support control endpoint
  - 11 DMA channels support 11 endpoints

- One 12-channel DMA engine supports:
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)

External peripheral:

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

Power management (patent pending)

- Power save during normal operation
  - Disables unused modules
- Power save during sleep mode
  - Sets memory controller to refresh
  - Disables all modules except selected wakeup modules
  - Wakeup on valid packets or characters

Vector interrupt controller

- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

General purpose timers/counters

- 16 independent 16-bit or 32-bit programmable timers or counters
  - Each with an I/O pin
- Mode selectable into:
  - Internal timer mode
  - External gated timer mode
  - External event counter
- Can be concatenated
- Resolution to measure minute-range events
- Source clock selectable: internal clock or external pulse event
- Each can be individually enabled/disabled

System timers

- Watchdog timer
- System bus monitor timer
- System bus arbiter timer
- Peripheral bus monitor timer

General purpose I/O

- 50 programmable GPIO pins (muxed with other functions)
- Software-readable powerup status registers for every pin for customer-defined bootstrapping

External interrupts

- 4 external programmable interrupts
  - Rising or falling edge-sensitive
  - Low level- or high level-sensitive

Clock generator

- Low cost external crystal
- On-chip phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate PLL for USB

Operating grades/Ambient temperatures

- 200 MHz: 0 – 70° C
- 162 MHz: -40 – +85° C
- 125 MHz: 0 – 70° C

System-level interfaces

Figure 1 shows the NS9750 system-level hardware interfaces, which are detailed after the figure.

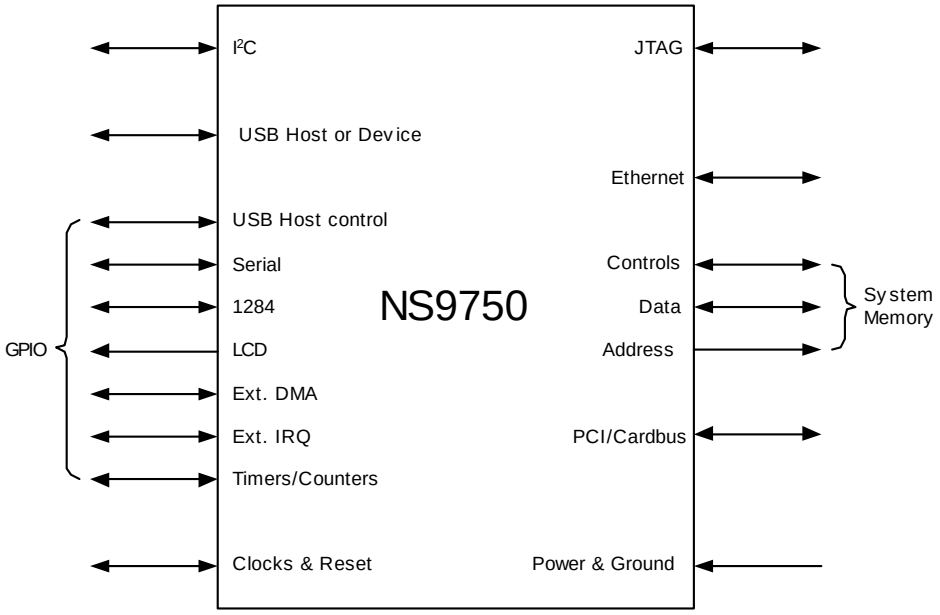


Figure 1: System-level hardware interfaces

NS9750 interfaces

- Ethernet MII/RMII interface to an external PHY
- System Memory interface
  - Glueless connection to SDRAM
  - Glueless connection to buffered PC100 DIMM
  - Glueless connection to SRAM
  - Glueless connection to Flash memory or ROM
- PCI muxed with CardBus interface
- USB host or device interface
- I^2C interface
- 50 GPIO pins muxed with:
  - Four 8-pin-each serial ports, each programmable to UART or SPI
  - 1284 port
  - Up to 24-bit TFT or STN color and monochrome LCD controller
  - Two external DMA channels
  - Four external interrupt pins programmed to rising or falling edge, or to high or low level
  - Sixteen 16-bit or 32-bit programmable timers or counters
  - Two control signals to support USB host
- JTAG development interface
- Clock interfaces for crystal or external oscillator
  - System clock
  - USB clock
- Clock interface for optional LCD external oscillator
- Power and ground

System configuration

The PLL and other system settings can be configured at powerup before the CPU boots. External pins configure the necessary control register bits at powerup. External pulldown resistors can be used to configure the PLL and system configuration registers depending on the application. The recommended value is 2.2k ohm to 2.4k ohm.

Table 1 indicates how each bit is used to configure the powerup settings, where 1 indicates the internal pullup resistor and 0 indicates an external pulldown resistor. Table 2 shows `PLL ND[4:0]` multiplier values.

Pin name	Configuration bits
rtck	**PCI arbiter configuration** 0 External PCI arbiter 1 Internal PCI arbiter
boot_strap[0]	**Chip select 1 byte_lane_enable_n/write_enable_n configuration bootstrap select** 0 write_enable_n for byte-wide devices (default) 1 byte_lane_enable_n (2.4K pulldown added)
boot_strap[4:3]	**Chip select 1 data width bootstrap select** 00 16 bits 01 8 bits 11 32 bits
boot_strap[2]	**Memory interface read mode bootstrap select** **Note:** An external pulldown resistor must be used to select command delayed mode. Clock delayed mode is reserved for future use. 0 Command delayed mode Commands are launched on a 90-degree phase-shifted AHB clock, and AHB clock is routed to the external dynamic memory. 1 Clock delayed mode Reserved for future use.
boot_strap[1]	**CardBus mode bootstrap select** 0 CardBus mode 1 PCI mode
gpio[49]	**Chip select polarity** 0 Active high 1 Active low
gpio[44]	**Endian mode** 0 Big Endian 1 Little Endian
reset_done	**Bootup mode** 0 Boot from SDRAM using serial SPI EEPROM 1 Boot from flash/ROM

Table 1: Configuration pins— Bootstrap initialization

Pin name	Configuration bits
gpio[19]	**PLL BP (PLL bypass)** 0 PLL bypassed 1 PLL not bypassed
gpio[17], gpio[12], gpio[10], gpio [8], gpio[4]	**PLL ND[4:0] (PLL multiplier, ND + 1)** See Table 2: PLL ND[4:0].
gpio[2], gpio[0]	**PLL FS[1:0] (PLL frequency select)** **FS** **Divide by** 00 1 01 2 10 4 11 8

Table 1: Configuration pins— Bootstrap initialization

Register configuration: gpio 17, 12, 10, 8, 4	Multiplier
1 1 0 1 0	32
0 0 1 0 0	31
1 1 0 0 0	30
1 1 0 0 1	29
1 1 1 1 0	28
1 1 1 1 1	27
1 1 1 0 0	26
1 1 1 0 1	25
1 0 0 1 0	24
1 0 0 1 1	23
1 0 0 0 0	22
1 0 0 0 1	21
1 0 1 1 0	20
1 0 1 1 1	19
1 0 1 0 0	18
1 0 1 0 1	17
0 1 0 1 0	16
0 1 0 1 1	15

Table 2: PLL ND[4:0]

Register configuration: gpio 17, 12, 10, 8, 4	Multiplier
0 1 0 0 0	14
0 1 0 0 1	13
0 1 1 1 0	12
0 1 1 1 1	11
0 1 1 0 0	10
0 1 1 0 1	9
0 0 0 1 0	8
0 0 0 1 1	7
0 0 0 0 0	6
0 0 0 0 1	5
0 0 1 1 0	4
0 0 1 1 1	3
0 0 1 0 0	2
0 0 1 0 1	1

Table 2: PLL ND[4:0]

There are 32 additional GPIO pins that are used to create a general purpose, user-defined ID register. These are external signals that are registered at powerup.

gpio[41]	gpio[40]	gpio[39]	gpio[38]
gpio[37]	gpio[36]	gpio[35]	gpio[34]
gpio[33]	gpio[32]	gpio[31]	gpio[30]
gpio[29]	gpio[28]	gpio[27]	gpio[26]
gpio[25]	gpio[23]	gpio[22]	gpio[21]
gpio[18]	gpio[16]	gpio[15]	gpio[14]
gpio[13]	gpio[11]	gpio[9]	gpio[7]
gpio[6]	gpio[5]	gpio[3]	gpio[1]

Read these signals for general purpose status information.

System boot

There are two ways to boot the NS9750 system (see Figure 2):

- From a fast Flash over the system memory bus
- From an inexpensive, but slower, serial EEPROM through SPI port B

Both boot methods are glueless. The bootstrap pin, RESET_DONEn, is used to indicate where to boot on a system powerup. Flash boot can be done from 8-bit, 16-bit, or 32-bit ROM or Flash.

Serial EEPROM boot is supported by NS9750 hardware. A configuration header in the EEPROM specifies total number of words to be fetched from EEPROM, as well as a system memory configuration and a memory controller configuration. The boot engine configures the memory controller and system memory, fetches data from low-cost serial EEPROM, and writes the data to external system memory, holding the CPU in reset.

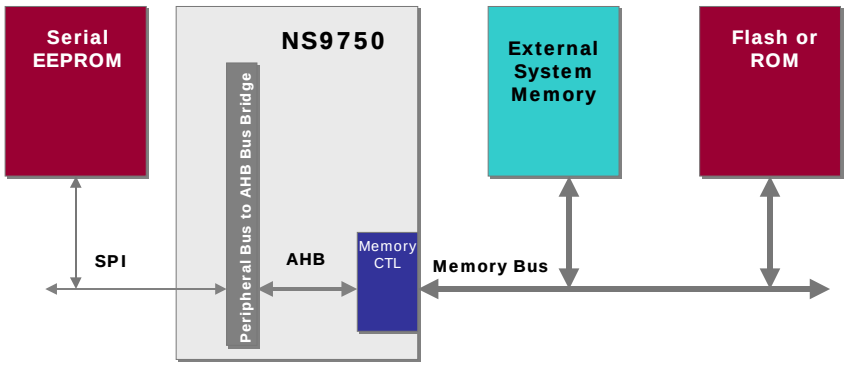


Figure 2: Two methods of booting NS9750 system

Reset

Master reset using an external reset pin resets NS9750. Only the AHB bus error status registers retain their values; software read resets these error status registers. The input reset pin can be driven by a system reset circuit or a simple power-on reset circuit.

RESET_DONE as an input

Used at bootup only:

- When set to 0, the system boots from SDRAM through the serial SPI EEPROM.
- When set to 1, the system boots from Flash/ROM. This is the default.

RESET_DONE as an output

Sets to 1, per Step 6 in the boot sequence:

If the system is booting from serial EEPROM through the SPI port, the boot program must be loaded into the SDRAM before the CPU is released from reset. The memory controller is powered up with `dy_cs_n[0]` enabled with a default set of SDRAM configurations. The default address range for `dy_cs_n[0]` is from `0x0000 0000`. The other chip selects are disabled.

Boot sequence

1. When the system reset turns to inactive, the reset signal to the CPU is still held active.
2. An I/O module on the peripheral bus (BBus) reads from a serial ROM device that contains the memory controller settings and the boot program.
3. The BBus-to-AHB bridge requests and gets the system bus.
4. The memory controller settings are read from the serial EEPROM and used to initialize the memory controller.
5. The BBus-to-AHB bridge loads the boot program into the SDRAM, starting at address 0.
6. The reset signal going to the CPU is released once the boot program is loaded. `RESET_DONE` is now set to 1.
7. The CPU begins to execute code from address `0x0000 0000`.

Figure 3 shows a sample reset circuit.

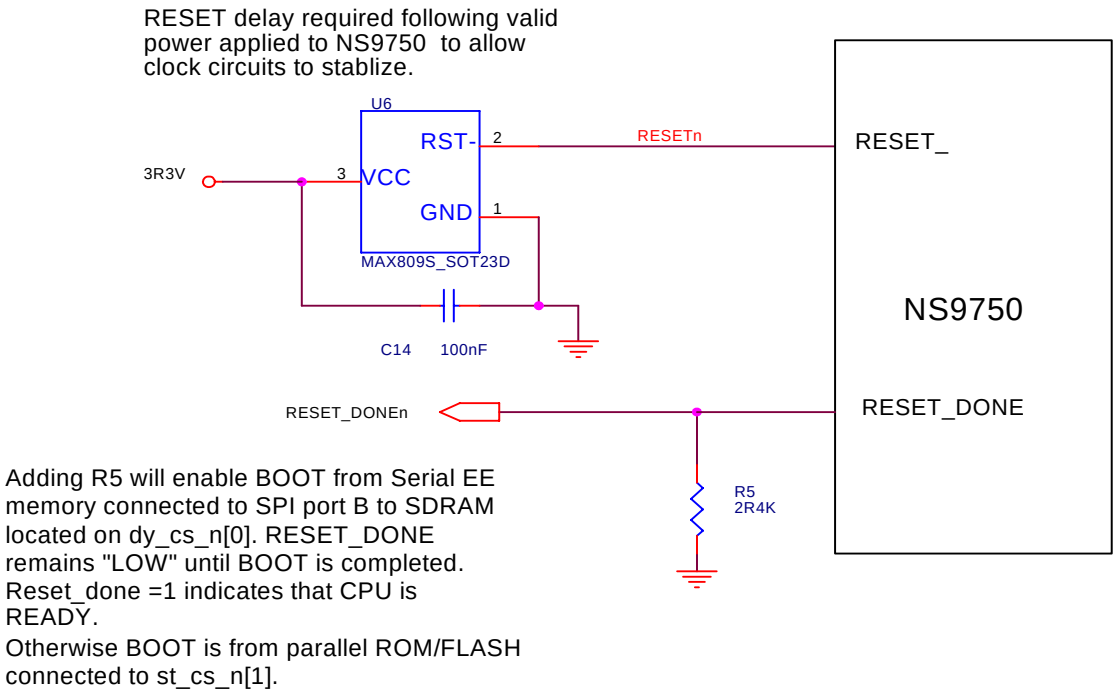


Figure 3: Sample reset circuit

You can use one of four software resets to reset the NS9750. Select the reset by setting the appropriate bit in the appropriate register:

- Watchdog timer can issue reset upon Watchdog timer expiration.
- AHB bus arbiter can issue reset upon AHB bus arbiter timer expiration.
- AHB bus monitor can issue reset upon AHB bus monitor timer expiration.
- Software reset can reset individual internal modules or all modules (except memory and CPU).

Hardware reset duration is 4ms for PLL to stabilize. Software reset duration depends on speed grade, as shown in Table 3.

Speed grade	CPU clock cycles	Duration
200 MHz	128	640 ns
162 MHz	128	790 ns
125 MHz	128	1024 ns

Table 3: Software reset duration

The minimum reset pulse width is 10 crystal clocks.

System Clock

The system clock is provided to NS9750 by either a crystal or an external oscillator; Table 4 shows sample clock frequency settings for each chip speed grade.

Speed	cpu_clk	hclk (main bus)	bbus_clk
200 MHz	200 (199.0656)	99.5328	49.7664
162 MHz	162.2016	81.1008	40.5504
125 MHz	125.3376	62.6688	31.3344

Table 4: Sample clock frequency settings with 29.4912 MHz crystal

If an oscillator is used, it must be connected to the `x1_sys_osc` input (C8 pin) on the NS9750. If a crystal is used, it must be connected with a circuit such as the one shown in Figure 4.

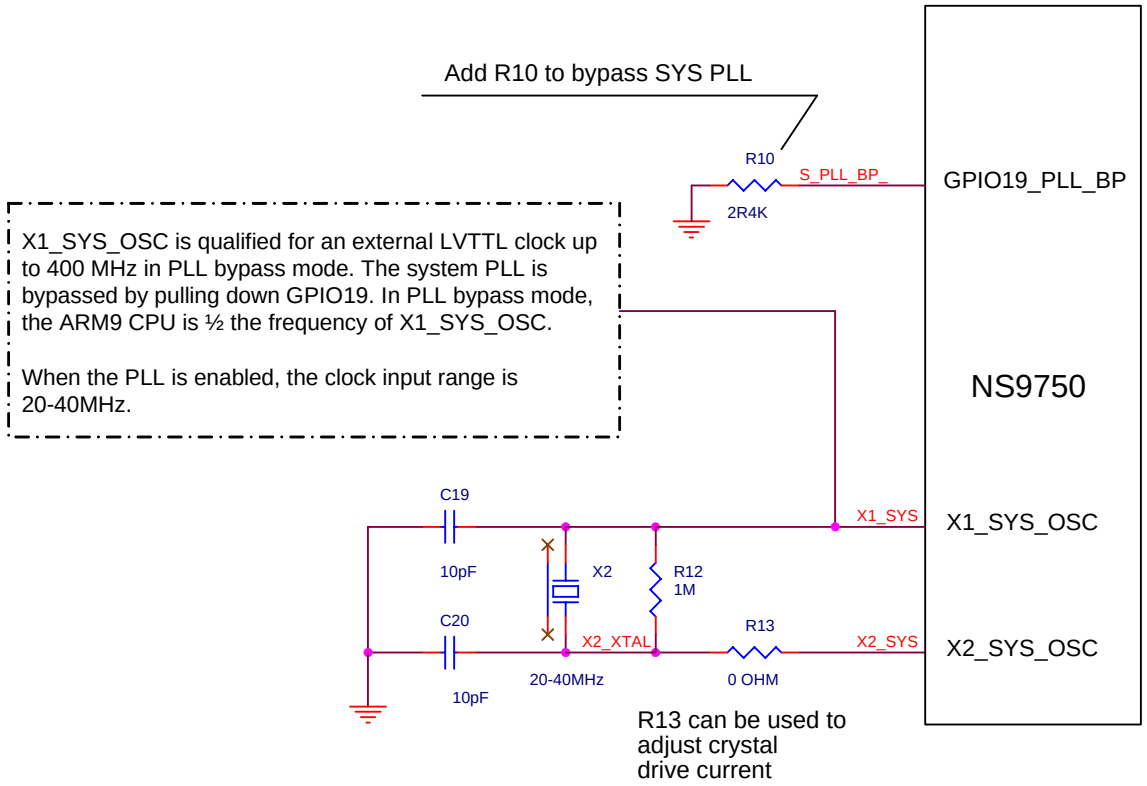


Figure 4: NS9750 system clock

The PLL parameters are initialized on powerup reset and can be changed by software from f_{max} to 1/2 f_{max}. For a 200 MHz grade, then, the CPU may change from 200 MHz to 100 MHz, the AHB system bus may change from 100 MHz to 50 MHz, and the peripheral BBus may change from 50 MHz

to 25 MHz. If changed by software, the system resets automatically after the PLL stabilizes (approximately 4 ms).

The system clock provides clocks for CPU, AHB system bus, peripheral BBus, PCI/CardBus, LCD, timers, memory controller, and BBus modules (serial modules and 1284 parallel port).

The Ethernet MAC uses external clocks from a MII PHY or a RMII PHY. For a MII PHY, these clocks are input signals: `rx_clk` on pin T3 for receive clock and `tx_clk` on pin V3 for transmit clock. For a RMII, there is only one clock, and it connects to the `rx_clk` on pin T3. In this case, the transmit clock `tx_clk`, pin V3, should be tied low.

PCI/CardBus, LCD controller, serial modules (UART, SPI), and 1284 port can optionally use external clock signals.

USB clock

USB is clocked by a separate PLL driven by an external 48 MHz crystal, or it can be driven directly by an external 48 MHz oscillator. Figure 5 shows a USB circuit.

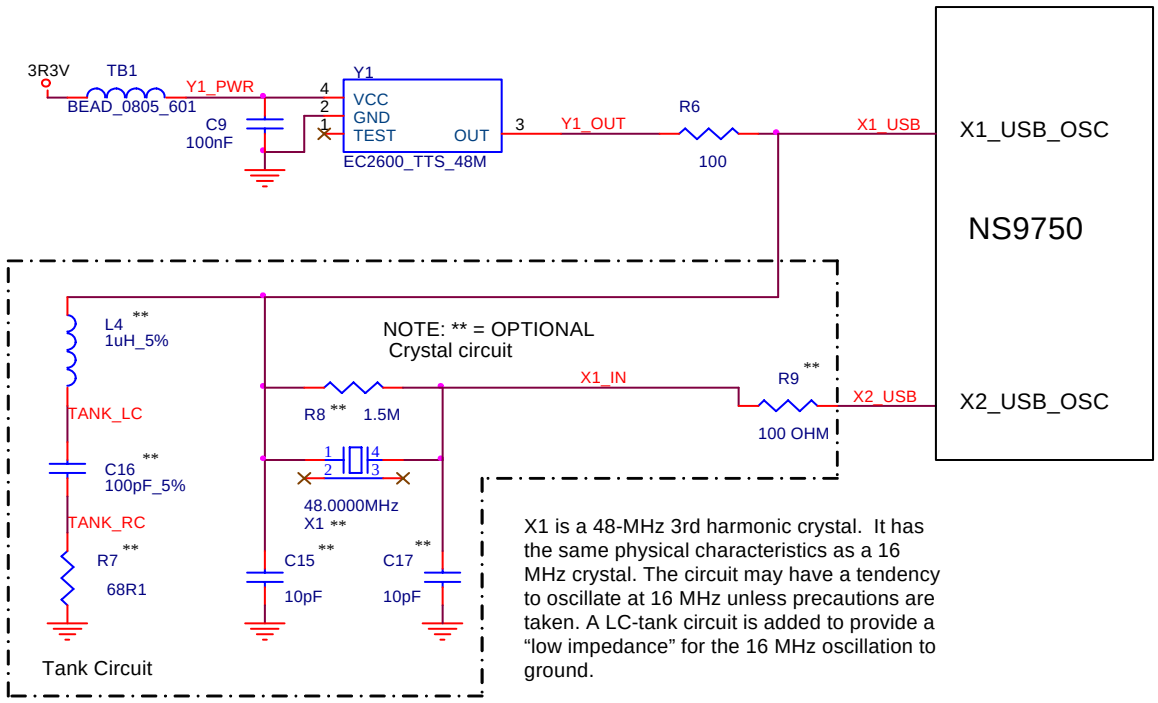


Figure 5: USB clock

NS9750 pinout and signal descriptions

Each pinout table applies to a specific interface, and contains the following information:

Heading	Description
Pin #	The pin number assignment for a specific I/O signal.
Signal Name	The pin name for each I/O signal.Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers. _n in the signal name indicates that this signal is active *low*.
U/D	U or D indicates whether the pin is a pullup resistor or a pulldown resistor: ■ **U** — Pullup (input current source) ■ **D** — Pulldown (input current sink) If no value appears, that pin is neither a pullup nor pulldown resistor.
I/O	The type of signal — input, output, or input/output.
OD (mA)	The output drive strength of an output buffer. The NS9750 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

More detailed signal descriptions are provided for selected modules.

System Memory interface

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
A21	addr[0]		8	O	Address bus signal
B20	addr[1]		8	O	Address bus signal
C19	addr[2]		8	O	Address bus signal
A20	addr[3]		8	O	Address bus signal
B19	addr[4]		8	O	Address bus signal
C18	addr[5]		8	O	Address bus signal
A19	addr[6]		8	O	Address bus signal
A17	addr[7]		8	O	Address bus signal
C16	addr[8]		8	O	Address bus signal
B16	addr[9]		8	O	Address bus signal
A16	addr[10]		8	O	Address bus signal
D15	addr[11]		8	O	Address bus signal

Table 5: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
C15	addr[12]		8	O	Address bus signal
B15	addr[13]		8	O	Address bus signal
A15	addr[14]		8	O	Address bus signal
C14	addr[15]		8	O	Address bus signal
B14	addr[16]		8	O	Address bus signal
A14	addr[17]		8	O	Address bus signal
A13	addr[18]		8	O	Address bus signal
B13	addr[19]		8	O	Address bus signal
C13	addr[20]		8	O	Address bus signal
A12	addr[21]		8	O	Address bus signal
B12	addr[22]		8	O	Address bus signal
C12	addr[23]		8	O	Address bus signal
D12	addr[24]		8	O	Address bus signal
A11	addr[25]		8	O	Address bus signal
B11	addr[26]		8	O	Address bus signal
C11	addr[27]		8	O	Address bus signal
G2	clk_en[0]		8	O	SDRAM clock enable
H3	clk_en[1]		8	O	SDRAM clock enable
G1	clk_en[2]		8	O	SDRAM clock enable
H2	clk_en[3]		8	O	SDRAM clock enable
A10	clk_out[0]		8	O	SDRAM reference clock. Connect to clk_in[0] using series termination.
A9	clk_out[1]		8	O	SDRAM clock
A5	clk_out[2]		8	O	SDRAM clock
A4	clk_out[3]		8	O	SDRAM clock
G26	data[0]		8	I/O	Data bus signal
H24	data[1]		8	I/O	Data bus signal
G25	data[2]		8	I/O	Data bus signal
F26	data[3]		8	I/O	Data bus signal
G24	data[4]		8	I/O	Data bus signal
F25	data[5]		8	I/O	Data bus signal
E26	data[6]		8	I/O	Data bus signal

Table 5: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
F24	data[7]		8	I/O	Data bus signal
E25	data[8]		8	I/O	Data bus signal
D26	data[9]		8	I/O	Data bus signal
F23	data[10]		8	I/O	Data bus signal
E24	data[11]		8	I/O	Data bus signal
D25	data[12]		8	I/O	Data bus signal
C26	data[13]		8	I/O	Data bus signal
E23	data[14]		8	I/O	Data bus signal
D24	data[15]		8	I/O	Data bus signal
C25	data[16]		8	I/O	Data bus signal
B26	data[17]		8	I/O	Data bus signal
D22	data[18]		8	I/O	Data bus signal
C23	data[19]		8	I/O	Data bus signal
B24	data[20]		8	I/O	Data bus signal
A25	data[21]		8	I/O	Data bus signal
C22	data[22]		8	I/O	Data bus signal
D21	data[23]		8	I/O	Data bus signal
B23	data[24]		8	I/O	Data bus signal
A24	data[25]		8	I/O	Data bus signal
A23	data[26]		8	I/O	Data bus signal
B22	data[27]		8	I/O	Data bus signal
C21	data[28]		8	I/O	Data bus signal
A22	data[29]		8	I/O	Data bus signal
B21	data[30]		8	I/O	Data bus signal
C20	data[31]		8	I/O	Data bus signal
E1	data_mask[0]		8	O	SDRAM data mask signal
F2	data_mask[1]		8	O	SDRAM data mask signal
G3	data_mask[2]		8	O	SDRAM data mask signal
F1	data_mask[3]		8	O	SDRAM data mask signal
C5	clk_in[0]			I	SDRAM feedback clock. Connect to clk_out[0].
D2	clk_in[1]			I	Connect to GND
E3	clk_in[2]			I	Connect to GND

Table 5: System Memory interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
E2	clk_in[3]			I	Connect to GND
B4	byte_lane_sel_n[0]		8	O	Static memory byte_lane_enable[0] or write_enable_n[0] for byte-wide device signals
F4	byte_lane_sel_n[1]		8	O	Static memory byte_lane_enable[1] or write_enable_n[1] for byte-wide device signals
D1	byte_lane_sel_n[2]		8	O	Static memory byte_lane_enable[2] or write_enable_n[2] for byte-wide device signals
F3	byte_lane_sel_n[3]		8	O	Static memory byte_lane_enable[3] or write_enable_n[3] for byte-wide device signals
B5	cas_n		8	O	SDRAM column address strobe
A8	dy_cs_n[0]		8	O	SDRAM chip select signal
B8	dy_cs_n[1]		8	O	SDRAM chip select signal
A6	dy_cs_n[2]		8	O	SDRAM chip select signal
C7	dy_cs_n[3]		8	O	SDRAM chip select signal
C6	st_oe_n		8	O	Static memory output enable
D6	ras_n		8	O	SDRAM row address strobe
H1	dy_pwr_n		8	O	SyncFlash power down
B10	st_cs_n[0]		8	O	Static memory chip select signal
C10	st_cs_n[1]		8	O	Static memory chip select signal
B9	st_cs_n[2]		8	O	Static memory chip select signal
C9	st_cs_n[3]		8	O	Static memory chip select signal
B6	we_n		8	O	SDRAM write enable. Used for static and SDRAM devices.
J3	ta_strb	U		I	Slow peripheral transfer acknowledge

Table 5: System Memory interface pinout

System Memory interface signals

Table 6 describes the System Memory interface signals in more detail. All signals are internal to the chip. Figure 6, "SDRAM clock termination," on page 18, shows NS9750 SDRAM clock termination.

Name	I/O	Description
addr[27:0]	O	Address output. Used for both static and SDRAM devices. SDRAM memories use bits [14:0]; static memories use bits [25:0].
clk_en[3:0]	O	SDRAM clock enable. Used for SDRAM devices. **Note:** The clk_en signals are associated with the dy_cs_n signals.
clk_out[3:1]	O	SDRAM clocks. Used for SDRAM devices.
clk_out[0]	O	SDRAM clk_out[0] is connected to clk_in[0].
data[31:0]	I/O	Read data from memory. Used for the static memory controller and the dynamic memory controller.
data_mask[3:0]	O	Data mask output to SDRAMs. Used for SDRAM devices.
clk_in[3:1]	I	Feedback clocks. Used for SDRAM devices.
clk_in[0]	I	Feedback clock [0]. Always connects to clk_out[0].
byte_lane_sel_n[3:0]	O	Static memory byte lane select, active low, or write_enable_n for byte-wide devices.
cas_n	O	Column address strobe. Used for SDRAM devices.
dy_cs_n[3:0]	O	SDRAM chip selects. Used for SDRAM devices.
st_oe_n	O	Output enable for static memories. Used for static memory devices.
ras_n	O	Row address strobe. Used for SDRAM devices.
st_cs_n[3:0]	O	Static memory chip selects. Default active low. Used for static memory devices.
we_n	O	Write enable. Used for SDRAM and static memories.
ta_strb	I	*Slow peripheral transfer acknowledge* can be used to terminate static memory cycles sooner than the number of wait states programmed in the chip select setup register.

Table 6: System Memory interface signal descriptions

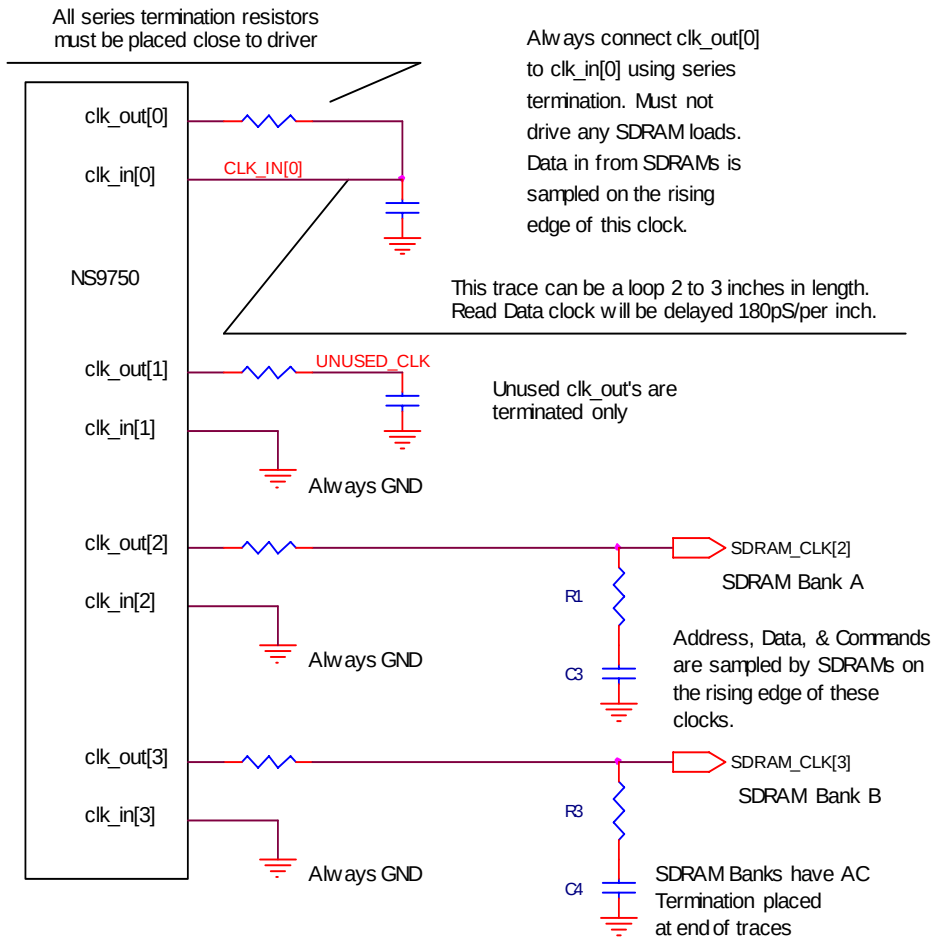


Figure 6: SDRAM clock termination

Ethernet interface

Pin #	Signal name		U/D	OD (mA)	I/O	Description	
	MII	RMII				MII	RMII
AB1	col	N/C			I	Collision	Pull low external to NS9750
AA2	crs	crs_dv			I	Carrier sense	Carrier sense
AC1	enet_phy_int_n	enet_phy_int_n	U		I	Ethernet PHY interrupt	Ethernet PHY interrupt
AA3	mdc	mdc		4	O	MII management interface clock	MII management interface clock
AB2	mdio	mdio	U	2	I/O	MII management data	MII management data
T3	rx_clk	ref_clk			I	Receive clock	Reference clock
V2	rx_dv	N/C			I	Receive data valid	Pull low external to NS9750
W1	rx_er	rx_er			I	Receive error	Optional signal; pull low to NS9750 if not used.
V1	rxd[0]	rxd[0]			I	Receive data bit 0	Receive data bit 0
U3	rxd[1]	rxd[1]			I	Receive data bit 1	Receive data bit 1
U2	rxd[2]	N/C			I	Receive data bit 2	Pull low external to NS9750
U1	rxd[3]	N/C			I	Receive data bit 3	Pull low external to NS9750
V3	tx_clk	N/C			I	Transmit clock	Pull low external to NS9750
AA1	tx_en	tx_en		2	O	Transmit enable	Transmit enable
Y3	tx_er	N/C		2	O	Transmit error	N/A
Y2	txd[0]	txd[0]		2	O	Transmit data bit 0	Transmit data bit 0
W3	txd[1]	txd[1]		2	O	Transmit data bit 1	Transmit data bit 1
Y1	txd[2]	N/C		2	O	Transmit data bit 2	N/A
W2	txd[3]	N/C		2	O	Transmit data bit 3	N/A

Table 7: Ethernet interface pinout

Clock generation/system pins

Pin #	Signal name	U/D	OD (mA)	I/O	Description
C8	x1_sys_osc			I	System clock crystal oscillator circuit input
B7	x2_sys_osc			O	System clock crystal oscillator circuit output
D9	x1_usb_osc			I	USB clock crystal oscillator circuit input. (Connect to GND if USB is not used.)
A7	x2_usb_osc			O	USB clock crystal oscillator circuit output
AC21	reset_done	U	2	I/O	CPU is enabled once the boot program is loaded. Reset_done is set to 1.
H25	reset_n	U		I	System reset input signal
AD20	bist_en_n			I	Enable internal BIST operation
AF21	pll_test_n			I	Enable PLL testing
AE21	scan_en_n			I	Enable internal scan testing
B18	sys_pll_dvdd				System clock PLL 1.5V digital power
A18	sys_pll_dvss				System clock PLL digital ground
B17	sys_pll_avdd				System clock PLL 3.3V analog power
C17	sys_pll_avss				System clock PLL analog ground
J2	lcdclk	U		I	External LCD clock input
T2	boot_strap[0]	U	2	I/O	Chip select 1 static memory byte_lane_enable_n, or write_enable_n for byte-wide devices bootstrap select
N3	boot_strap[1]	U	2	I/O	CardBus mode bootstrap select
P1	boot_strap[2]	U	2	I/O	Memory interface read mode bootstrap select
P2	boot_strap[3]	U	2	I/O	Chip select 1 data width bootstrap select
P3	boot_strap[4]	U	2	I/O	Chip select 1 data width bootstrap select

Table 8: Clock generation/system pins pinout

bist_en_n, pll_test_n, and scan_en_n

Table 9 is a truth/termination table for bist_en_n, pll_test_n, and scan_en_n.

	Normal operation	Arm debug	
pll_test_n	pull up	pull up	10K recommended
bist_en_n	pull down	pull up	10K pullup = debug 2.4K pulldown = normal
scan_en_n	pull down	pull down	2.4K recommended

Table 9: bist_en_n, pll_test_n, & scan_en_n truth/termination table

PCI interface

The PCI interface can be set to PCI host or PCI device (slave) using the pci_central_resource_n pin.

Notes:

- All output drivers for PCI meet the standard PCI driver specification.
- All table notes can be found after Table 11: CardBus IO muxed signals.

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
J24	ad[0][1]		N/A	I/O	PCI time-multiplexed address/data bus
H26	ad[1][1]		N/A	I/O	PCI time-multiplexed address/data bus
J25	ad[2][1]		N/A	I/O	PCI time-multiplexed address/data bus
J26	ad[3][1]		N/A	I/O	PCI time-multiplexed address/data bus
K24	ad[4][1]		N/A	I/O	PCI time-multiplexed address/data bus
K25	ad[5][1]		N/A	I/O	PCI time-multiplexed address/data bus
K26	ad[6][1]		N/A	I/O	PCI time-multiplexed address/data bus
L24	ad[7][1]		N/A	I/O	PCI time-multiplexed address/data bus
L26	ad[8][1]		N/A	I/O	PCI time-multiplexed address/data bus
M24	ad[9][1]		N/A	I/O	PCI time-multiplexed address/data bus
M25	ad[10][1]		N/A	I/O	PCI time-multiplexed address/data bus
M26	ad[11][1]		N/A	I/O	PCI time-multiplexed address/data bus
N24	ad[12][1]		N/A	I/O	PCI time-multiplexed address/data bus
N25	ad[13][1]		N/A	I/O	PCI time-multiplexed address/data bus
N26	ad[14][1]		N/A	I/O	PCI time-multiplexed address/data bus
P26	ad[15][1]		N/A	I/O	PCI time-multiplexed address/data bus

Table 10: PCI interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
U24	ad[16][1]		N/A	I/O	PCI time-multiplexed address/data bus
V26	ad[17][1]		N/A	I/O	PCI time-multiplexed address/data bus
V25	ad[18][1]		N/A	I/O	PCI time-multiplexed address/data bus
W26	ad[19][1]		N/A	I/O	PCI time-multiplexed address/data bus
V24	ad[20][1]		N/A	I/O	PCI time-multiplexed address/data bus
W25	ad[21][1]		N/A	I/O	PCI time-multiplexed address/data bus
Y26	ad[22][1]		N/A	I/O	PCI time-multiplexed address/data bus
W24	ad[23][1]		N/A	I/O	PCI time-multiplexed address/data bus
Y24	ad[24][1]		N/A	I/O	PCI time-multiplexed address/data bus
AA25	ad[25][1]		N/A	I/O	PCI time-multiplexed address/data bus
AB26	ad[26][1]		N/A	I/O	PCI time-multiplexed address/data bus
AA24	ad[27][1]		N/A	I/O	PCI time-multiplexed address/data bus
AB25	ad[28][1]		N/A	I/O	PCI time-multiplexed address/data bus
AC26	ad[29][1]		N/A	I/O	PCI time-multiplexed address/data bus
AD26	ad[30][1]		N/A	I/O	PCI time-multiplexed address/data bus
AC25	ad[31][1]		N/A	I/O	PCI time-multiplexed address/data bus
L25	cbe_n[0][1]		N/A	I/O	Command/byte enable
P25	cbe_n[1][1]		N/A	I/O	Command/byte enable
U25	cbe_n[2][1]		N/A	I/O	Command/byte enable
AA26	cbe_n[3][1]		N/A	I/O	Command/byte enable
T26	devsel_n[2]		N/A	I/O	Device select
U26	frame_n[2]		N/A	I/O	Cycle frame
Y25	idsel[3, 4]		N/A	I	Initialization device select: ■ For PCI host applications, connect to AD11. ■ For PCI device applications, connection is determined by the PCI device number assigned to the NS9750. ■ For CardBus applications, connect to external pullup resistor. ■ Do not allow input to float in any application.
T24	irdy_n[2]		N/A	I/O	Initiator ready
P24	par[1]		N/A	I/O	Parity signal
R25	perr_n[2]		N/A	I/O	Parity error

Table 10: PCI interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
R26	serr_n[2]		N/A	I/O	System error: Input: pci_central_resource_n = 0 Output: pci_central_resource_n = 1
R24	stop_n[2]		N/A	I/O	Stop signal
T25	trdy_n[2]		N/A	I/O	Target ready
AC24	pci_arb_gnt_1_n[6]		N/A	O	PCI channel 1 grant
AD23	pci_arb_gnt_2_n[6]		N/A	O	PCI channel 2 grant
AE24	pci_arb_gnt_3_n[6]		N/A	O	PCI channel 3 grant
AD25	pci_arb_req_1_n[2]		N/A	I	PCI channel 1 request
AB23	pci_arb_req_2_n[2]		N/A	I	PCI channel 2 request
AC22	pci_arb_req_3_n[2]		N/A	I	PCI channel 3 request
AF23	pci_central_resource_n	D	N/A	I	PCI internal central resource enable
AF25	pci_int_a_n[2]		N/A	I/O	PCI interrupt request A, output if external central resource used
AF24	pci_int_b_n[2]		N/A	I/O	PCI interrupt request B, CCLKRUN# for CardBus applications
AE23	pci_int_c_n[2]		N/A	I	PCI interrupt request C
AD22	pci_int_d_n[2]		N/A	I	PCI interrupt request D
AE26	pci_reset_n[3]		N/A	I/O	PCI reset, output if internal central resource enabled
AB24	pci_clk_in	U	N/A	I	PCI clock in. (Connected to pci_clk_out or an externally generated PCI reference clock.)
AA23	pci_clk_out		N/A	O	PCI clock out

Table 10: PCI interface pinout

PCI/CardBus signals

Most of the CardBus signals are the same as the PCI signals. Other CardBus signals are unique and multiplexed with PCI signals for the NS9750. Table 11 shows these unique signals. Figure 7 illustrates how to terminate an unused PCI.

PCI signal	CardBus signal	CardBus type	Description
INTA#	CINT#[4]	Input	CardBus interrupt pin. The INTA2PCI pin in the PCI Miscellaneous Support register must be set to 0.
INTB#	CCLKRUN#[4]	Bidir	CardBus pin used to negotiate with the external CardBus device before stopping the clock. Allows external CardBus device to request that the clock be restarted.
INTC#	CSTSCHG[5]	Input	CardBus status change interrupt signal.
GNT1#	CGNT#[4]	Output	Grant to external CardBus device from NS9750's internal arbiter.
GNT2#	CVS1	Output	Voltage sense pin. Normally driven low by NS9750, but toggled during interrogation of the external CardBus device to find voltage requirements. **Note:** Do not connect directly to the CardBus connector see the diagram "CardBus system connections to NS9750" in the *NS9750 Hardware Reference.*
GNT3#	CVS2	Output	Voltage sense pin. Normally driven low by NS9750, but toggled during interrogation of the external CardBus device to find voltage requirements.
REQ1#	CREQ#[4]	Input	Request from external CardBus device to NS9750's internal arbiter.
REQ2#	CCD1[4]	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.
REQ3#	CCD2[4]	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.

Table 11: CardBus IO muxed signals

Notes:

1 Add external pulldown resistor *only* if the PCI interface is not being used. See the discussion of PCI bridge configuration in *NS9750 Sample Driver Configurations* for information about eliminating the pulldown resistor.

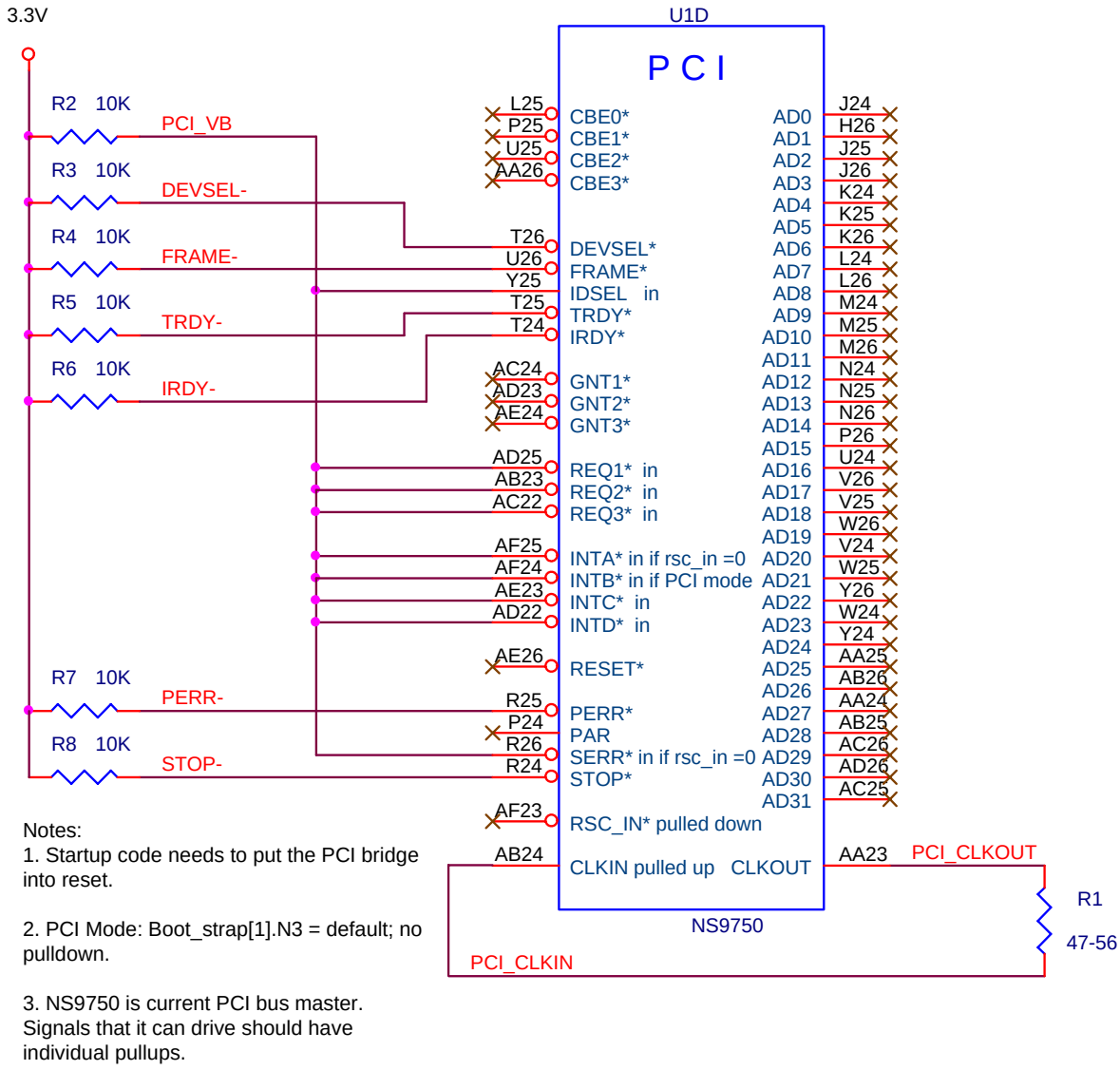
2 Add external pullup resistors *regardless* of whether the PCI interface is being used.

3 Add external pullup resistor *only* if the PCI interface is not being used.

4 Add external pullup resistor in CardBus mode.

5 Add external pulldown resistor in CardBus mode.

6 Add external pullup only if the PCI interface is being used and this signal is also being used.



Notes:
1. Startup code needs to put the PCI bridge into reset.

2. PCI Mode: Boot_strap[1].N3 = default; no pulldown.

3. NS9750 is current PCI bus master. Signals that it can drive should have individual pullups.

Figure 7: NS9750 unused PCI termination

GPIO MUX

Note: The BBus utility contains the control pins for each GPIO MUX bit. Each pin can be selected individually; that is, you can select any option (00, 01, 02, 03) for any pin by setting the appropriate bit in the appropriate register. Some signals are muxed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as such in the Descriptions column in the table.

The 00 option for the serial ports (B, A, C, and D) are configured for UART and SPI mode, respectively; that is, the UART option is shown first, followed by the SPI option if there is one. If only one value appears, it is the UART mode value. SPI options all begin with *SPI*.

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AF19	gpio[0]	U	2	I/O	00 Ser port B TxData / SPI port B dout 01 DMA ch 1 done (duplicate) 02 Timer 1 (duplicate) 03 GPIO 0
AE18	gpio[1]	U	2	I/O	00 Ser port B RxData / SPI port B din 01 DMA ch 1 req (duplicate) 02 Ext IRQ 0 03 GPIO 1
AF18	gpio[2]	U	2	I/O	00 Ser port B RTS 01 Timer 0 02 DMA ch 2 read enable 03 GPIO 2
AD17	gpio[3]	U	2	I/O	00 Ser port B CTS 01 1284 nAck (peripheral-driven) 02 DMA ch 1 req 03 GPIO 3
AE17	gpio[4]	U	2	I/O	00 Ser port B DTR 01 1284 busy (peripheral-driven) 02 DMA ch 1 done 03 GPIO 4
AF17	gpio[5]	U	2	I/O	00 Ser port B DSR 01 1284 PError (peripheral-driven) 02 DMA ch 1 read enable 03 GPIO 5
AD16	gpio[6]	U	2	I/O	00 Ser port B RI / SPI port B clk 01 1284 nFault (peripheral-driven)[1] 02 Timer 7 (duplicate) 03 GPIO 6

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AE16	gpio[7]	U	2	I/O	00 Ser port B DCD / SPI port B enable 01 DMA ch 1 read enable (duplicate) 02 Ext IRQ 1 03 GPIO 7
AD15	gpio[8]	U	2	I/O	00 Ser port A TxData / SPI port A dout 01 Reserved 02 Reserved 03 GPIO 8
AE15	gpio[9]	U	2	I/O	00 Ser port A RxData / SPI port A din 01 Reserved 02 Timer 8 (duplicate) 03 GPIO 9
AF15	gpio[10]	U	2	I/O	00 Ser port A RTS 01 Reserved 02 Reserved 03: GPIO 10
AD14	gpio[11]	U	2	I/O	00 Ser port A CTS 01 Ext IRQ2 (duplicate) 02 Timer 0 (duplicate) 03 GPIO 11
AE14	gpio[12]	U	2	I/O	00 Ser port A DTR 01 Reserved 02 Reserved 03 GPIO 12
AF14	gpio[13]	U	2	I/O	00 Ser port A DSR 01 Ext IRQ 0 (duplicate) 02 Timer 10 (duplicate) 03 GPIO 13
AF13	gpio[14]	U	2	I/O	00 Ser port A RI / SPI port A clk 01 Timer 1 02 Reserved 03 GPIO 14
AE13	gpio[15]	U	2	I/O	00 Ser port A DCD / Ser port A enable 01 Timer 2 02 Reserved 03 GPIO 15
AD13	gpio[16]	U	2	I/O	00 Reserved 01 1284 nFault (peripheral-driven, duplicate)[1] 02 Timer 11 (duplicate) 03 GPIO 16

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AF12	gpio[17]	U	2	I/O	00	USB power relay
					01	Reserved
					02	Reserved
					03	GPIO 17
AE12	gpio[18]	U	4	I/O	00	Ethernet CAM reject
					01	LCD power enable
					02	Ext IRQ 3 (duplicate)
					03	GPIO 18
AD12	gpio[19]	U	4	I/O	00	Ethernet CAM req
					01	LCD line-horz sync
					02	DMA ch 2 read enable (duplicate)
					03	GPIO 19
AC12	gpio[20]	U	8	I/O	00	Ser port C DTR
					01	LCD clock
					02	Reserved
					03	GPIO 20
AF11	gpio[21]	U	4	I/O	00	Ser port C DSR
					01	LCD frame pulse-vert
					02	Reserved
					03	GPIO 21
AE11	gpio[22]	U	4	I/O	00	Ser port C RI / SPI port C clk
					01	LCD AC bias-data enable
					02	Reserved
					03	GPIO 22
AD11	gpio[23]	U	4	I/O	00	Ser port C DCD / SPI port C enable
					01	LCD line end
					02	Timer 14 (duplicate)
					03	GPIO 23
AF10	gpio[24]	U	4	I/O	00	Ser port D DTR
					01	LCD data bit 0
					02	Reserved
					03	GPIO 24
AE10	gpio[25]	U	4	I/O	00	Ser port D DSR
					01	LCD data bit 1
					02	Timer 15 (duplicate)
					03	GPIO 25
AD10	gpio[26]	U	4	I/O	00	Ser port D RI / SPI port D clk
					01	LCD data bit 2
					02	Timer 3
					03	GPIO 26

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AF9	gpio[27]	U	4	I/O	00	Ser port D DCD / SPI port D enable
					01	LCD data bit 3
					02	Timer 4
					03	GPIO 27
AE9	gpio[28]	U	4	I/O	00	Ext IRQ 1 (duplicate)
					01	LCD data bit 4
					02	LCD data bit 8 (duplicate)
					03	GPIO 28
AF8	gpio[29]	U	4	I/O	00	Timer 5
					01	LCD data bit 5
					02	LCD data bit 9 (duplicate)
					03	GPIO 29
AD9	gpio[30]	U	4	I/O	00	Timer 6
					01	LCD data bit 6
					02	LCD data bit 10 (duplicate)
					03	GPIO 30
AE8	gpio[31]	U	4	I/O	00	Timer 7
					01	LCD data bit 7
					02	LCD data bit 11 (duplicate)
					03	GPIO 31
AF7	gpio[32]	U	4	I/O	00	Ext IRQ 2
					01	1284 Data 1 (bidirectional)
					02	LCD data bit 8
					03	GPIO 32
AD8	gpio[33]	U	4	I/O	00	Timer 8
					01	1284 Data 2 (bidirectional)
					02	LCD data bit 9
					03	GPIO 33
AD7	gpio[34]	U	4	I/O	00	Timer 9
					01	1284 Data 3 (bidirectional)
					02	LCD data bit 10
					03	GPIO 34
AE6	gpio[35]	U	4	I/O	00	Timer 10
					01	1284 Data 4 (bidirectional)
					02	LCD data bit 11
					03	GPIO 35
AF5	gpio[36]	U	4	I/O	00	Reserved
					01	1284 Data 5 (bidirectional)
					02	LCD data bit 12
					03	GPIO 36

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AD6	gpio[37]	U	4	I/O	00	Reserved
					01	1284 Data 6 (bidirectional)
					02	LCD data bit 13
					03	GPIO 37
AE5	gpio[38]	U	4	I/O	00	Reserved
					01	1284 Data 7 (bidirectional)
					02	LCD data bit 14
					03	GPIO 38
AF4	gpio[39]	U	4	I/O	00	Reserved
					01	1284 Data 8 (bidirectional)
					02	LCD data bit 15
					03	GPIO 39
AC6	gpio[40]	U	4	I/O	00	Ser port C TxData / SPI port C dout
					01	Ext IRQ 3
					02	LCD data bit 16
					03	GPIO 40
AD5	gpio[41]	U	4	I/O	00	Ser port C RxData / SPI port C din
					01	Timer 11
					02	LCD data bit 17
					03	GPIO 41
AE4	gpio[42]	U	4	I/O	00	Ser port C RTS
					01	Timer 12
					02	LCD data bit 18
					03	GPIO 42
AF3	gpio[43]	U	4	I/O	00	Ser port C CTS
					01	Timer 13
					02	LCD data bit 19
					03	GPIO 43
AD2	gpio[44]	U	4	I/O	00	Ser port D TxData / SPI port D dout
					01	1284 Select (peripheral-driven)
					02	LCD data bit 20
					03	GPIO 44
AE1	gpio[45]	U	4	I/O	00	Ser port D RxData / SPI port D din
					01	1284 nStrobe (host-driven)
					02	LCD data bit 21
					03	GPIO 45
AB3	gpio[46]	U	4	I/O	00	Ser port D RTS
					01	1284 nAutoFd (host-driven)
					02	LCD data bit 22
					03	GPIO 46

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AA4	gpio[47]	U	4	I/O	00 Ser port D CTS 01 1284 nInit (host-driven) 02 LCD data bit 23 03 GPIO 47
AC2	gpio[48]	U	2	I/O	00 Timer 14 01 1284 SelectIn (host-driven) 02 DMA ch 2 req 03 GPIO 48
AD1	gpio[49]	U	2	I/O	00 Timer 15 01 1284 peripheral logic high (peripheral-driven) 02 DMA ch 2 done 03 GPIO 49

Table 12: GPIO MUX pinout

Note:

1 The `nFault` signal GPIO6 or GPIO16 can be used as a code-controlled direction pin for the transceiver. The polarity cannot be altered inside the NS9750; an inverter will be required.

LCD module signals

The LCD module signals are multiplexed with GPIO pins. They include seven control signals and up to 24 data signals. Table 13 describes the control signals. Table 14 and Table 15 provide details for the data signals.

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN) / horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN) / vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLD[23:0]	Output	LCD panel data (see Table 14 and Table 15)
CLLE	Output	Line end signal

Table 13: LCD module signal descriptions

The CLD[23:0] signal has eight modes of operation:

- TFT 24-bit interface
- TFT 18-bit interface
- Color STN single panel
- Color STN dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel

Table 14 shows which CLD[23:0] pins provide the pixel data to the STN panel for each mode of operation.

Legend:

- Ext pin = External pin
- CUSTN = Color upper panel STN, dual and/or single panel
- CLSTN = Color lower panel STN, single
- MUSTN = Mono upper panel STN, dual and/or single panel
- MLSTN = Mono lower panel STN, single
- N/A = not used
- 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See "GPIO MUX" on page 26 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[23]	AA4 = LCD data bit 23 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[22]	AB3 = LCD data bit 22 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[21]	AE1 = LCD data bit 21 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[20]	AD2 = LCD data bit 20 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[19]	AF3 = LCD data bit 19 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[18]	AE4 = LCD data bit 18 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[17]	AD5 = LCD data bit 17 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	AC6 = LCD data bit16 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	AF4 = LCD data bit 15 (O2)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	AE5 = LCD data bit 14 (O2)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	AD6 = LCD data bit 13 (O2)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	AF5 = LCD data bit 12 (O2)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]

Table 14: CLD[23:0] pin descriptions for STN display

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[11]	AE6 = LCD data bit 11 (O2) AE8 = LCD data bit 11 (O2)	N/A	CLSTN[4]	N/A	MLSTN[0][1]	N/A	MLSTN[4]
CLD[10]	AD7 = LCD data bit 10 (O2) AD9 = LCD data bit 10 (O2)	N/A	CLSTN[5]	N/A	MLSTN[1]	N/A	MLSTN[5]
CLD[9]	AD8 = LCD data bit 9 (O2) AF8 = LCD data bit 9 (O2)	N/A	CLSTN[6]	N/A	MLSTN[2]	N/A	MLSTN[6]
CLD[8]	AF7 = LCD data bit 8 (O2) AE9 = LCD data bit 8 (O2)	N/A	CLSTN[7]	N/A	MLSTN[3]	N/A	MLSTN[7]
CLD[7]	AE8 = LCD data bit 7 (O1)	CUSTN[0][1]	CUSTN[0][1]	N/A	N/A	MUSTN[0]	MUSTN[0][1]
CLD[6]	AD9 = LCD data bit 6 (O1)	CUSTN[1]	CUSTN[1]	N/A	N/A	MUSTN[1]	MUSTN[1]
CLD[5]	AF8 = LCD data bit 5 (O1)	CUSTN[2]	CUSTN[2]	N/A	N/A	MUSTN[2]	MUSTN[2]
CLD[4]	AE9 = LCD data bit 4 (O1)	CUSTN[3]	CUSTN[3]	N/A	N/A	MUSTN[3]	MUSTN[3]
CLD[3]	AF9 = LCD data bit 3 (O1)	CUSTN[4]	CUSTN[4]	MUSTN[0]	MUSTN[0][1]	MUSTN[4]	MUSTN[4]
CLD[2]	AD10 = LCD data bit 2 (O1)	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	AE10 = LCD data bit 1 (O1)	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	AF10 = LCD data bit 0 (O1)	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

1 This data bit corresponds to the first "pixel position." For example, for an 8-bit mono STN display, `CUSTN[0]` is the leftmost pixel on the panel and `CUSTN[7]` is the rightmost pixel within the 8-bit data. For a color STN display, bits [7, 6, 5] form the leftmost pixel.

Table 14: CLD[23:0] pin descriptions for STN display

Table 15 shows which `CLD[23:0]` pins provide the pixel data to the TFT panel for each of the multiplexing modes of operation.

External pin	TFT 24 bit	TFT 18 bit
CLD[23]	BLUE[7]	Reserved
CLD[22]	BLUE[6]	Reserved
CLD[21]	BLUE[5]	Reserved
CLD[20]	BLUE[4]	Reserved
CLD[19]	BLUE[3]	Reserved
CLD[18]	BLUE[2]	Reserved
CLD[17]	BLUE[1]	BLUE[4]

Table 15: CLD[23:0] pin descriptions for TFT display

External pin	TFT 24 bit	TFT 18 bit
CLD[16]	BLUE[0]	BLUE[3]
CLD[15]	GREEN[7]	BLUE[2]
CLD[14]	GREEN[6]	BLUE[1]
CLD[13]	GREEN[5]	BLUE[0]
CLD[12]	GREEN[4]	Intensity bit
CLD[11]	GREEN[3]	GREEN[4]
CLD[10]	GREEN[2]	GREEN[3]
CLD[9]	GREEN[1]	GREEN[2]
CLD[8]	GREEN[0]	GREEN[1]
CLD[7]	RED[7]	GREEN[0]
CLD[6]	RED[6]	Intensity bit
CLD[5]	RED[5]	RED[4]
CLD[4]	RED[4]	RED[3]
CLD[3]	RED[3]	RED[2]
CLD[2]	RED[2]	RED[1]
CLD[1]	RED[1]	RED[0]
CLD[0]	RED[0]	Intensity bit

Table 15: CLD[23:0] pin descriptions for TFT display

I²C interface

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AC15	iic_scl		4	I/O	I²C serial clock line. Add a 10K resistor to VDDA(3.3V) if not used.
AF16	iic_sda		4	I/O	I²C serial data line. Add a 10K resistor to VDDA(3.3V) if not used.

Table 16: I²C interface pinout

USB Interface

Notes:

- If not using the USB interface, these pins should be pulled down to ground through a 15K ohm resistor.
- All output drivers for USB meet the standard USB driver specification.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AB4	usb_dm			I/O	USB data -
AC3	usb_dp			I/O	USB data +

Table 17: USB interface pinout

JTAG interface for ARM core/boundary scan

Note: `trst_n` must be pulsed low to initialize the JTAG when a debugger is not attached. See Figure 8, "JTAG interface," on page 36.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
AE20	tck			I	Test clock
AD18	tdi	U		I	Test data in
AE19	tdo		2	O	Test data out
AC18	tms	U		I	Test mode select
AF20	trst_n	U		I	Test mode reset
AD19	rtck	U	2	I/O	Returned test clock, ARM core only

Table 18: JTAG interface/boundary scan pinout

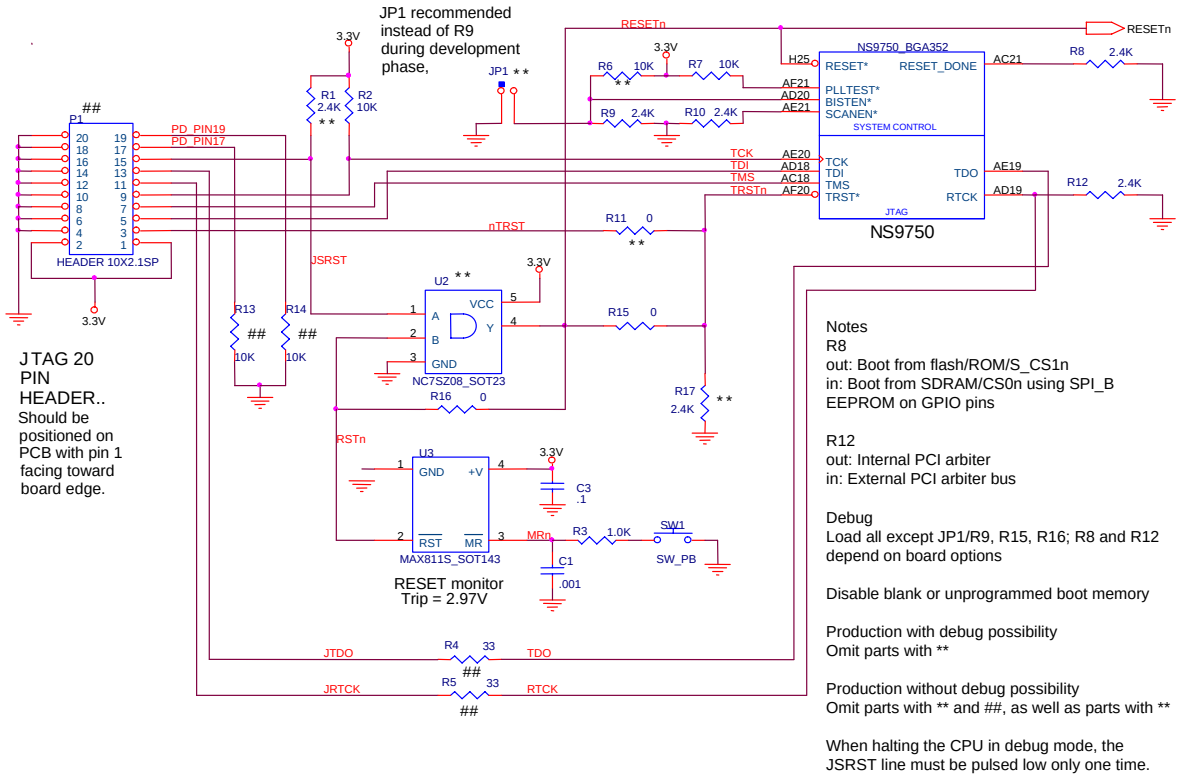


Figure 8: JTAG interface

Reserved pins

Pin#	Description
J1	Tie to ground directly
K3	Tie to ground directly
K2	Tie to ground directly
K1	Tie to ground directly
R1	Tie to ground directly
R2	Tie to ground directly
R3	Tie to ground directly
T1	Tie to ground directly
AF6	Tie to ground directly
AE3	Tie to ground directly
AC5	Tie to ground directly
AD4	Tie to 1.5V core power
AF2	Tie to 3.3V I/O power
AE7	No connect
L3	No connect
L2	No connect
L1	No connect
M3	No connect
M2	Tie to ground directly
M1	Tie to ground directly
N1	Tie to ground directly
N2	Tie to ground directly
AF22	No connect
AD21	No connect
AE22	No connect

Table 19: Reserved pins

Power ground

Pin #	Signal name	Description
J23, L23, K23, U23, T23, V23, D18, D17, AC17, D16, AC16, D11, D10, AC11, AC10, AC9, J4, L4, K4, U4, T4, V4	VDDC	Core power, 1.5V
G23, H23, M23, R23, P23, N23, Y23, W23, D20, AC20, D19, AC19, D14, D13, AC14, AC13, D8, D7, AC8, AC7, G4, H4, M4, R4, P4, N4, Y4, W4	VDDS	I/O power, 3.3V
A26, B25, AE25, AF26, D23, C24, AD24, AC23, D5, D4, C4, E4, AC4, A3, A2, D3, C3, C2, B3, B2, AE2, AD3, A1, C1, B1, AF1	VSS2	Ground

Table 20: Power ground pins

Address and register maps

System address map

The system memory address is divided to allow access to the internal and external resources on the system bus, as shown in Table 21.

Address range	Size	System functions
0x0000 0000 – 0x0FFF FFFF	256 MB	System memory chip select 4 - Dynamic memory (default)
0x1000 0000 – 0x1FFF FFFF	256 MB	System memory chip select 5 - Dynamic memory (default)
0x2000 0000 – 0x2FFF FFFF	256 MB	System memory chip select 6 - Dynamic memory (default)
0x3000 0000 – 0x3FFF FFFF	256 MB	System memory chip select 7 - Dynamic memory (default)
0x4000 0000 – 0x4FFF FFFF	256 MB	System memory chip select 0 - Static memory (default)
0x5000 0000 – 0x5FFF FFFF	256 MB	System memory chip select 1 - Static memory (default)
0x6000 0000 – 0x6FFF FFFF	256MB	System memory chip select 2 - Static memory (default)
0x7000 0000 – 0x7FFF FFFF	256 MB	System memory chip select 3 - Static memory (default)
0x8000 0000 – 0x8FFF FFFF	256 MB	PCI memory
0x9000 0000 – 0x9FFF FFFF	256 MB	BBus memory
0xA000 0000 – 0xA00F FFFF	1 MB	PCI IO
0xA010 0000 – 0xA01F FFFF	1 MB	PCI CONFIG_ADDR
0xA020 0000 – 0xA02F FFFF	1 MB	PCI CONFIG_DATA
0xA030 0000 – 0xA03F FFFF	1 MB	PCI arbiter
0xA040 0000 – 0xA04F FFFF	1 MB	BBus-to-AHB bridge
0xA050 0000 – 0xA05F FFFF	1 MB	Reserved
0xA060 0000 – 0xA06F FFFF	1 MB	Ethernet Communication module
0xA070 0000 – 0xA07F FFFF	1 MB	Memory controller
0xA080 0000 – 0xA08F FFFF	1 MB	LCD controller
0xA090 0000 – 0xA09F FFFF	1 MB	System Control module
0xA0A0 0000 – 0xFFFF FFFF	1526 MB	Reserved

Table 21: System address memory map

BBus peripheral address map

The BBus bridge configuration registers are located at base address 0xA040 0000. The BBus peripherals are located at base address 0x9000 0000 and span a 256 MB address space. Each BBus peripheral, with the exception of the SER controllers, resides in a 1 MB address space. Table 22 specifies the address space given to each peripheral.

Base address	Peripheral
0x9000 0000	BBus DMA controller
0x9010 0000	USB controller
0x9020 0000	SER Port B
0x9020 0040	SER Port A
0x9030 0000	SER Port C
0x9030 0040	SER Port D
0x9040 0000	IEEE 1284 controller
0x9050 0000	I^2C controller
0x9060 0000	BBus utility

Table 22: BBus peripheral address map

Electrical characteristics

The NS9750 operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Permanent device damage can occur if the absolute maximum ratings are exceeded even for an instant.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.9	V
DC input voltage	V_{INA}	-0.3 to V_{DDA} +0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA} +0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	°C

† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface

Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics" on page 43) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC} (core)	1.4 to 1.6	V
	V_{DDC} (PLL)	1.425 to 1.575	V
Maximum junction temperature	T_J	125	°C

† V_{DDA}: Ratings of I/O cells for 3.3V interface
V_{DDC}: Ratings of internal cells

Maximum power dissipation

Table 23 shows the maximum power dissipation, including sleep mode information, for I/O and core:

	Operation			Sleep mode with wake up on			
CPU clock	Full	No PCI	No PCI, LCD	All ports	BBus ports	AHB bus ports	No wake up ports
Total @ 200 MHz	1.7 W	1.55 W	1.5 W	350 mW	285 mW	240 mW	180 mW
Core	1.05 W	1 W	1 W	260mW	210 mW	220 mW	170 mW
I/O	0.65 W	0.55 W	0.5 W	90 mW	75 mW	20 mW	10 mW
Total @ 162 MHz	1.4 W	1.25 W	1.2 W	285 mW	235 mW	200 mW	145 mW
Core	0.9 W	0.8 W	0.8 W	210 mW	170 mW	180 mW	140 mW
I/O	0.5 W	0.45 W	0.4 W	75 mW	65 mW	20 mW	5 mW
Total @ 125 MHz	1.05 W	1 W	950 mW	220 mW	180 mW	150 mW	110 mW
Core	0.65 W	0.65 W	640 mW	210 mW	130 mW	140 mW	105 mW
I/O	0.4 W	0.35 W	310 mW	75 mW	50 mW	10 mW	5 mW

Table 23: NS9750 maximum power dissipation

Typical power dissipation

Figure 24 shows typical power dissipation for I/O and core at 200 MHz:

	Operation		
CPU clock	Full	No PCI	No PCI, LCD
Total @ 200 MHz	952 mW	886 mW	809 mW
Core	419 mW	353 mW	287 mW
I/O	533 mW	533 mW	522 mW

Table 24: NS9750 typical power dissipation

DC electrical characteristics

DC electrical characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level PCI level		Min	 2.0 $0.5V_{DDA}$	 V V
V_{IL}	Low-level input voltage: LVTTL level PCI level		Max	 0.8 $0.3V_{DDA}$	 V V
I_{IH}	High-level input current (no pulldown) Input buffer with pulldown	$V_{INA} = V_{DDA}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{IL}	Low-level input current (no pullup) Input buffer with pullup	$V_{INA} = V_{SS}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{OZ}	High-impedance leakage current	$V_{OUTA} = V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
I_{DDS}	Quiescent supply current	$V_{INA} = V_{DDA}$ or V_{SS}	Max	TBD	

USB DC electrical inputs

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input high level (driven)	2.0	V_{DDA}-0.6	V	
V_{IZ}	Input high level (floating)	2.7	3.6	V	
V_{IL}	Input low level		0.8	V	
V_{DI}	Differential input sensitivity	0.2		V	1
V_{CM}	Differential common mode range	0.8	2.5	V	2

Notes:

1 |(usb_dp) - (usb_dm)|

2 Includes V_{DI} range.

Outputs

All electrical outputs are 3.3V interface.

Sym	Parameter	Value		Unit
V_{OH}	High-level output voltage (LVTTL)	Min	V_{DDA}-0.6	V
V_{OL}	Low-level output voltage (LVTTL)	Max	0.4	V
V_{OH}	PCI high-level output voltage	Min	$0.9V_{DDA}$	V
V_{OL}	PCI low-level output voltage	Max	$0.1V_{DDA}$	V

USB DC electrical outputs

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Output low level	0.0	0.3	V	1
V_{OH}	Output high level	2.8	3.6	V	2
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	3

Notes:

1 Measured with R_L of 1.425k ohm to 3.6V.

2 Measured with R_L of 14.25k ohm to GND.

3 Excluding the first transition from the idle state.

Power sequencing

Use these requirements for power sequencing:

- 3.3 volt and 1.5 volt power must be applied to the NS9750 ASIC simultaneously, but never more than 100 milliseconds difference.
- The ASIC NS9750 3.3 volt/1.5 volt supplies must maintain a relationship to the power supplies for the external board circuits such that ASIC I/O input voltage does not exceed ±0.3V before the ASIC power supplies are applied.
- 3.3 and 1.5 volt power should never be cycled more than 100 times per day.

AC Characteristics

This section provides the AC characteristics, or timing specifications, integral to the operation of the NS9750.

Memory timing

Note: All AC characteristics are measured with 35pF, unless otherwise noted.

Memory timing contains parameters and diagrams for both SDRAM and SRAM timing.

Table 25 describes the values shown in the SDRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M1	data input setup time to rising	1.6		ns	
M2	data input hold time to rising	3.3		ns	
M3	clk_out high to clk_en high		6.1	ns	
M4	clk_out high to address valid		6.1	ns	
M5	clk_out high to data_mask		6.1	ns	1, 2
M6	clk_out high to dy_cs_n low		6.1	ns	3, 4
M7	clk_out high to ras_n low		6.1	ns	
M8	clk_out high to cas_n low		6.1	ns	
M9	clk_out high to we_n low		6.1	ns	
M10	clk_out high to data out		6.1	ns	
M11	address hold time	3.5			
M12	data out hold time	3.8			
M13	clk_en high to sdram access	2	2	clock	
M14	end sdram access to clk_en low	2	2	clock	

Table 25: SDRAM timing parameters

Notes:

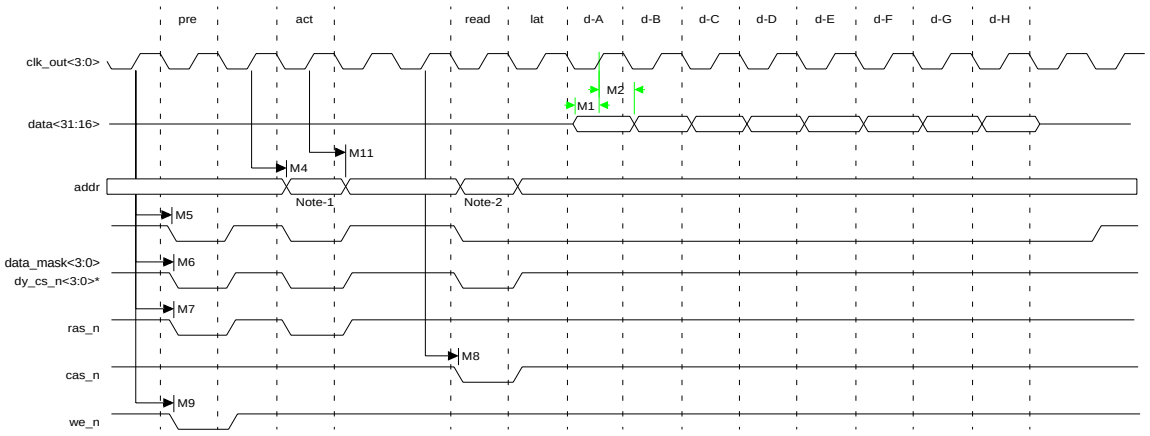
1 All four data_mask signals are used for all transfers.

2 All four data_mask signals will go low during a read cycle, for both 16-bit and 32-bit transfers.

3 Only one of the four `clk_out` signals is used.

4 Only one of the four `dy_cs_n` signals is used.

SDRAM burst read (16-bit)

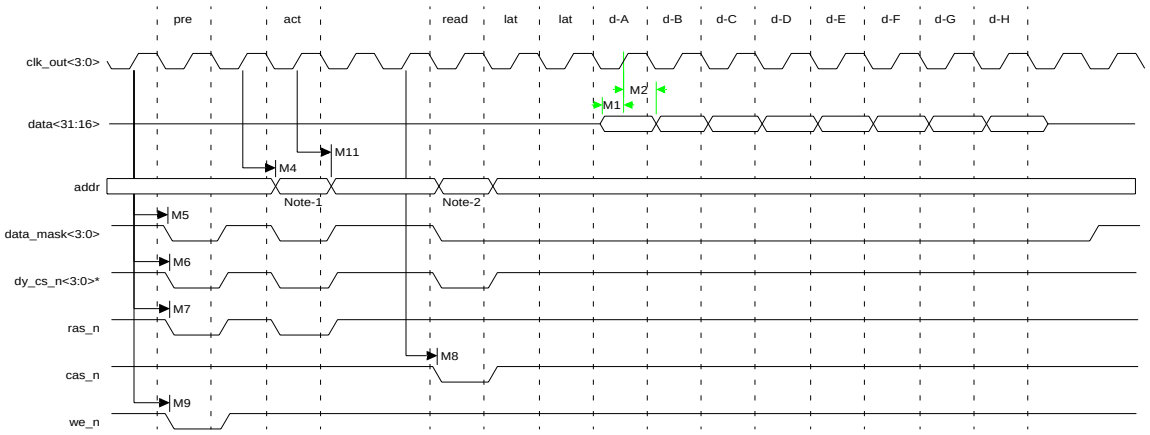


Notes:

1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM burst read (16-bit), CAS latency = 3

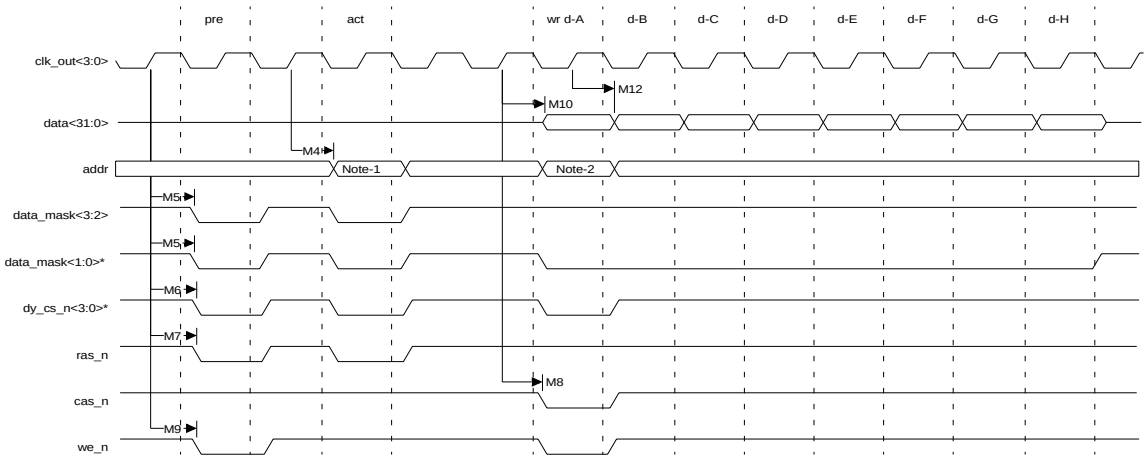


Notes:

1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM burst write (16-bit)

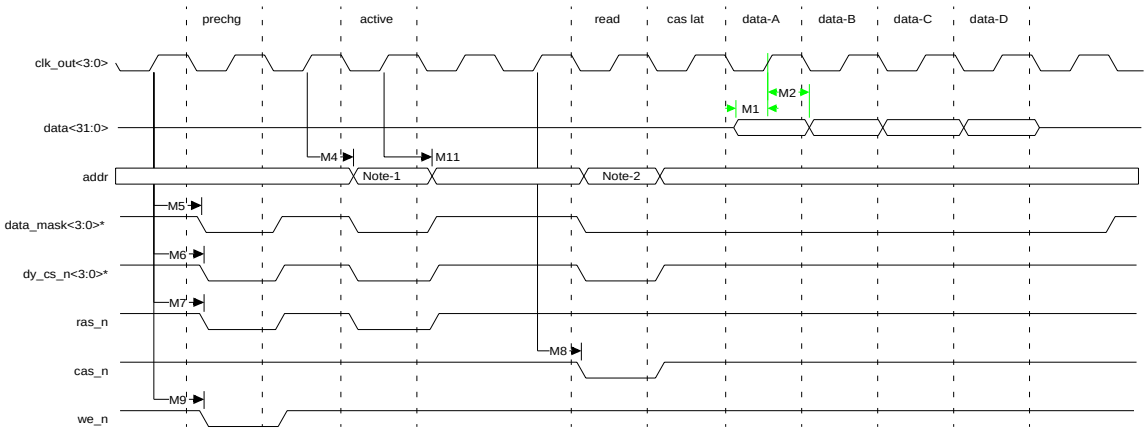


Notes:

1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM burst read (32-bit)

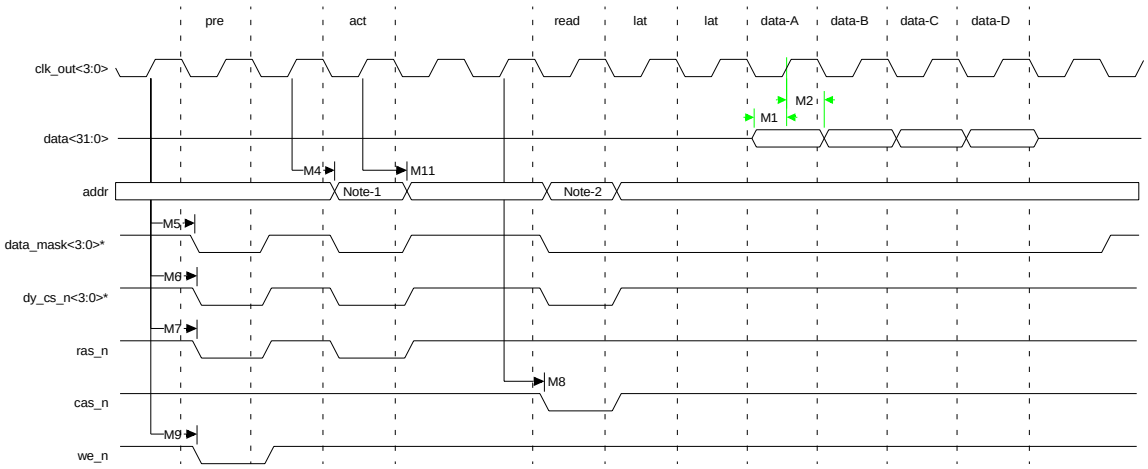


Notes:

1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM burst read (32-bit), CAS latency = 3

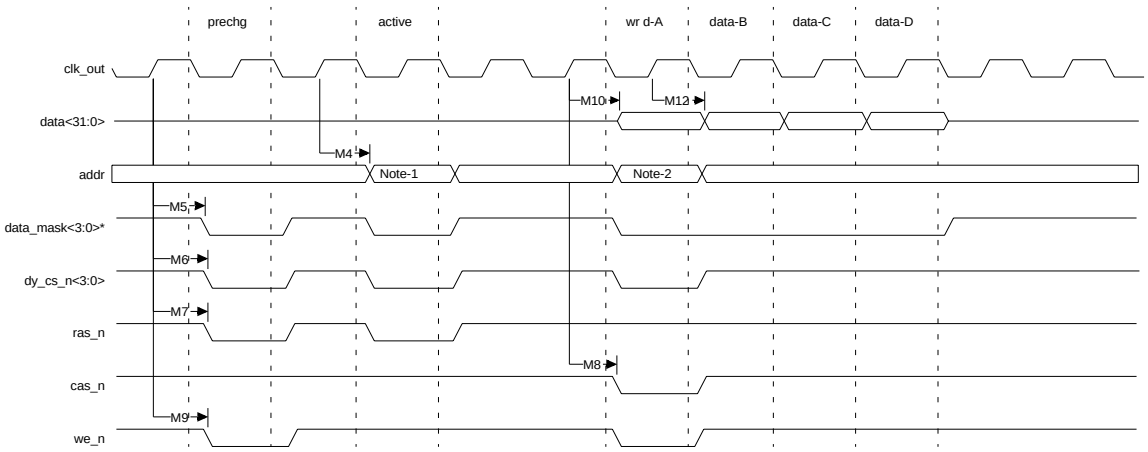


Notes:

1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM burst write (32-bit)

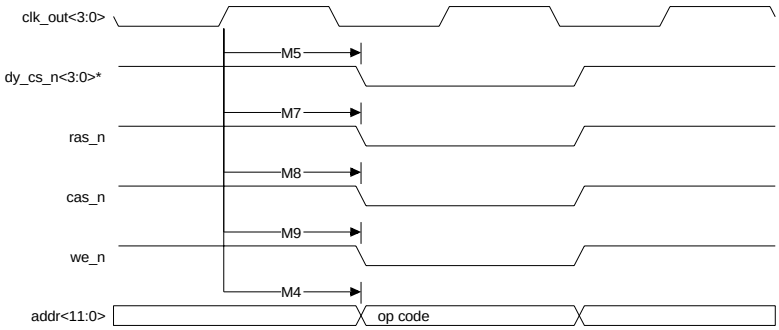


Notes:

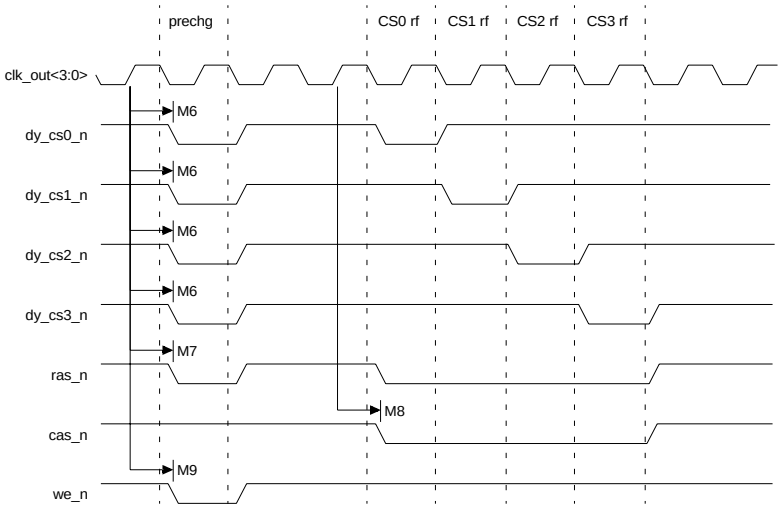
1 This is the Bank and RAS address.

2 This is the CAS address

SDRAM load mode



SDRAM refresh mode



Clock enable timing

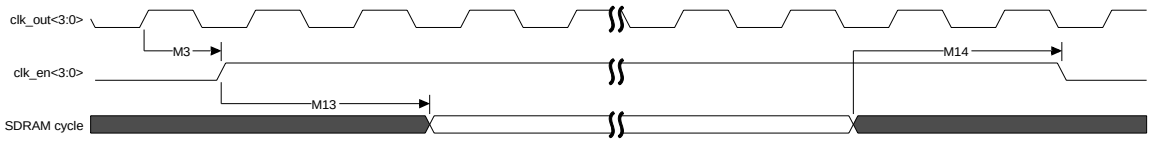


Table 26 describes the values shown in the SRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid	-2	+2	ns	
M16	data out hold time from clock high	-2	+2	ns	
M17	clock high to address valid	-2	+2	ns	
M18	address hold time from clock high	-2	+2	ns	
M19	clock high to st_cs_n low	-2	+2	ns	2
M20	clock high to st_cs_n high	-2	+2	ns	2
M21	clock high to we_n low	-2	+2	ns	
M22	clock high to we_n high	-2	+2	ns	
M23	clock high to byte_lanes low	-2	+2	ns	
M24	clock high to byte_lanes high	-2	+2	ns	
M25	data input setup time to rising clk	10		ns	
M26	data input hold time to rising clk	0		ns	
M27	clock high to oe_n low	-2	+2	ns	
M28	clock high to oe_n high	-2	+2	ns	

Table 26: SRAM timing parameters

Notes:

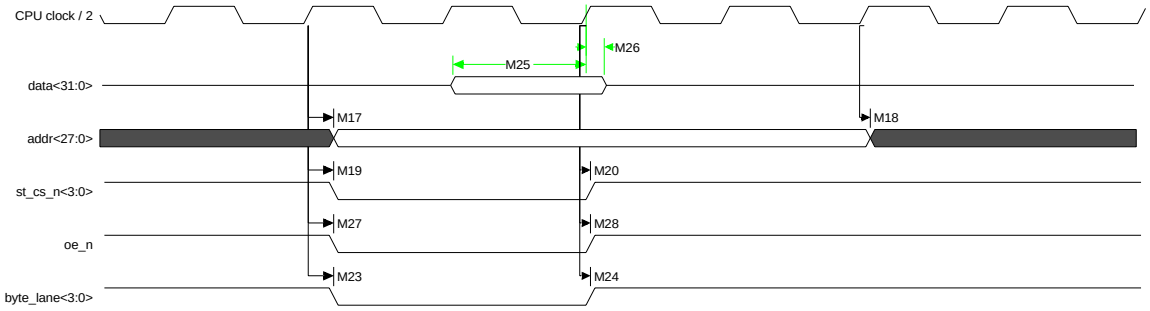
1 The (CPU clock out /2) signal is for reference only.

2 Only one of the four dy_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with the PC field.

3 Use this formula to calculate the length of the st_cs_n signal:

Tacc + board delay + (optional buffer delays, both address out and data in) + 10ns

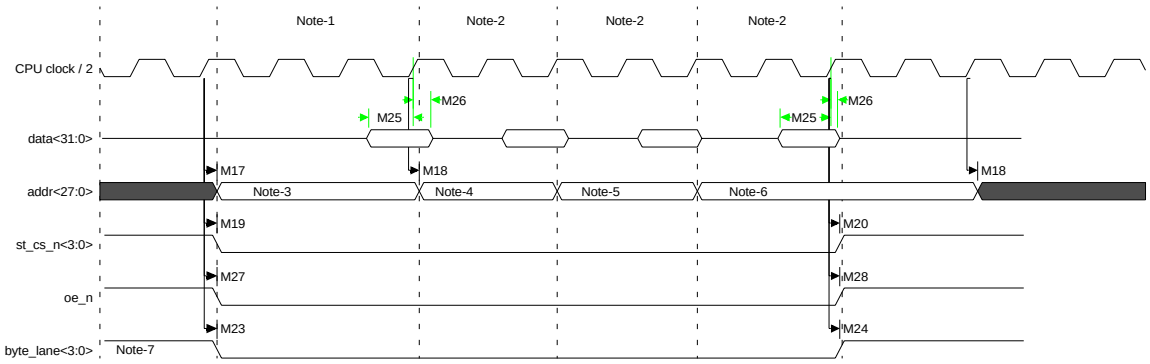
Static RAM read cycles with 0 wait states



- WTRD = 1

  WOEN = 1
- If the PB field is set to 1, all four `byte_lane` signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the `byte_lane` signal will always be high.

Static RAM asynchronous page mode read, WTPG = 1



- WTPG = 1

  WTRD = 2
- If the PB field is set to 1, all four `byte_lane` signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- The asynchronous page mode will read 16 bytes in a page cycle. A 32-bit bus will do four 32-bit reads, as shown (3-2-2-2). A 16-bit bus will do eight 16-bit reads (3-2-2-2-3-2-2-2) per page cycle, and an 8-bit bus will do sixteen reads (3-2-2-2-3-2-2-2-3-2-2-2-3-2-2-2) per page cycle. 3-2-2-2 is the example used here, but the WTRD and WTPG field can set them differently.

Notes:

1 The length of the first cycle in the page is determined by the WTRD field.

2 The length of the 2nd, 3rd, and 4th cycles is determined by the WTPG field.

3 This is the starting address. The least significant two bits will always be ‘00.’

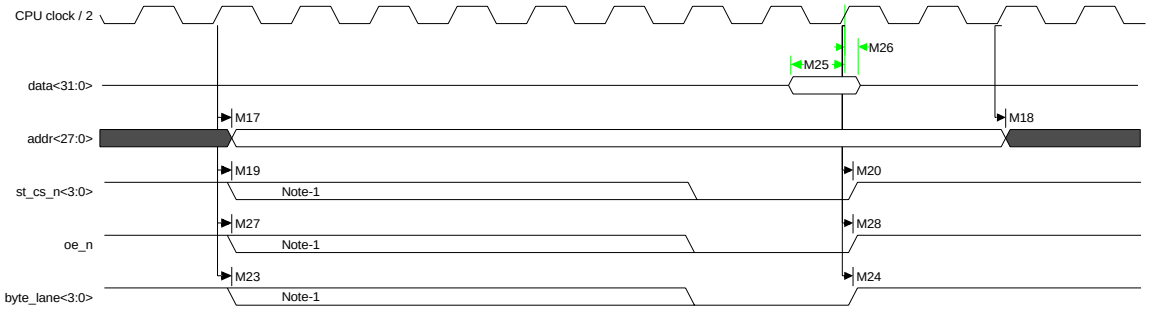
4 The least significant two bits in the second cycle will always be ‘01.’

5 The least significant bits in the third cycle will always be ‘10.’

6 The least significant two bits in the fourth cycle will always be ‘11.’

7 If the PB field is set to 0, the byte_lane signal will always be high during a read cycle.

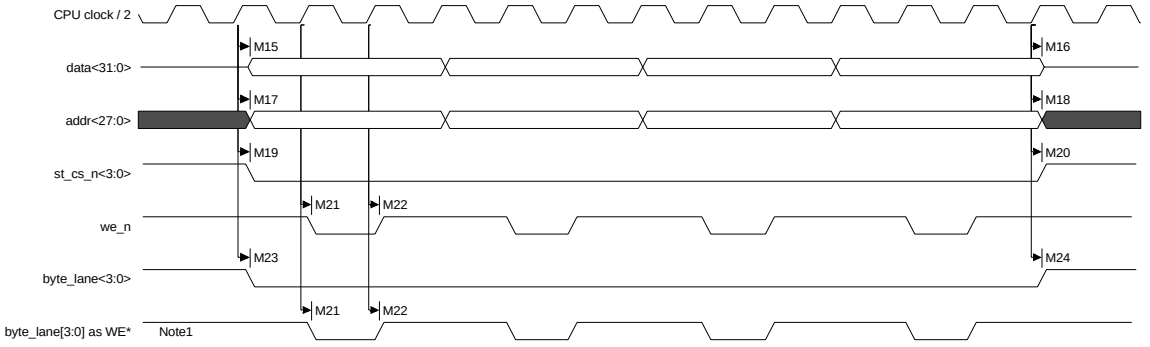
Static RAM read cycle configurable wait states



- WTRD = from 1 to 15
  WOEN = from 0 to 15
- If the PB field is set to 1, all four `byte_lane` signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the `byte_lane` signal will always be high.
- The length of the read cycle is determined by the WTRD field.

Note: The length of the `st_cs_n`, `oe_n`, and the `byte_lane` signals are determined by a combination of the WTRD and the WOEN fields.

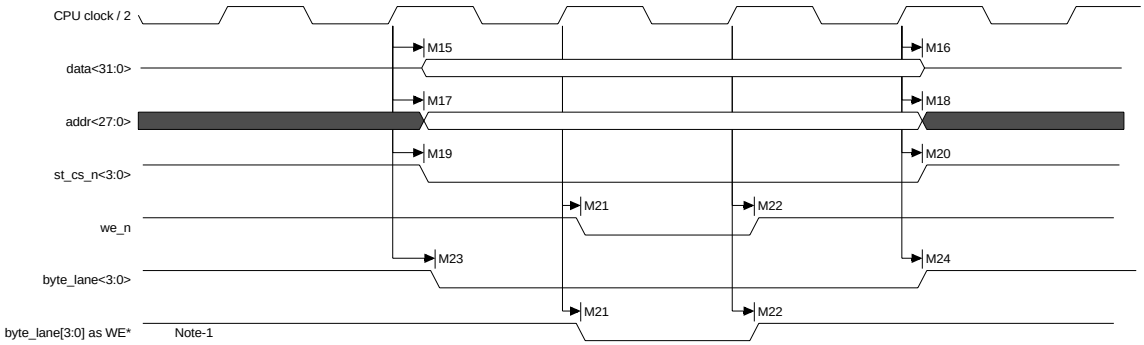
Static RAM sequential write cycles



- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four `byte_lane` signals will go low.
- During a 16-bit transfer, two `byte_lane` signals will go low.
- During an 8-bit transfer, only one `byte_lane` signal will go low.

Note: If the PB field is set to 0, the `byte_lane` signals will function as write enable signals and the `we_n` signal will always be high.

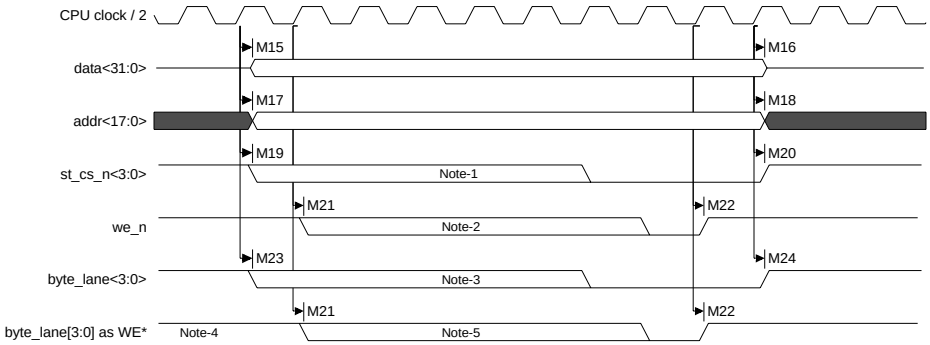
Static RAM write cycle



- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four `byte_lane` signals will go low.
- During a 16-bit transfer, two `byte_lane` signals will go low.
- During an 8-bit transfer, only one `byte_lane` signal will go low.

Note: If the PB field is set to 0, the `byte_lane` signals will function as write enable signals and the `we_n` signal will always be high.

Static write cycle with configurable wait states



- WTWR = from 0 to 15
  WWEN = from 0 to 15
- The WTWR field determines the length on the write cycle.
- During a 32-bit transfer, all four `byte_lane` signals will go low.
- During a 16-bit transfer, two `byte_lane` signals will go low.
- During an 8-bit transfer, only one `byte_lane` signal will go low.

Notes:

1 Timing of the `st_cs_n` signal is determined with a combination of the WTWR and WWEN fields. The `st_cs_n` signal will always go low at least one clock before `we_n` goes low, and will go high one clock after `we_n` goes high.

2 Timing of the `we_n` signal is determined with a combination of the WTWR and WWEN fields.

3 Timing of the `byte_lane` signals is determined with a combination of the WTWR and WWEN fields. The byte_lane signals will always go low one clock before `we_n` goes low, and will go one clock high after `we_n` goes high.

4 If the PB field is set to 0, the `byte_lane` signals will function as the write enable signals and the `we_n` signal will always be high.

5 If the PB field is set to 0, the timing for the `byte_lane` signals is set with the WTWR and WWEN fields.

Ethernet timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 27 describes the values shown in the Ethernet timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
E1	MII tx_clk to txd, tx_en, tx_er	3	11	ns	2
E2	MII rxd, rx_en, rx_er setup to rx_clk rising	3		ns	
E3	MII rxd, rx_en, rx_er hold from rx_clk rising	1		ns	
E4	mdio (input) setup to mdc rising	10		ns	
E5	mdio (input) hold from mdc rising	0		ns	
E6	mdc to mdio (output)	18	38	ns	1, 2
E7	mdc period	80		ns	
E8	RMII ref_clk to txd, tx_en	3	12	ns	2
E9	RMII rxd, crs, rx_er setup to ref_clk rising	3		ns	
E10	RMII rxd, crs, rx_er hold from ref_clk rising	1		ns	
E11	MII rx_clk to cam_req	3	10	ns	
E12	MII cam_reject setup to rx_clk rising	N/A		ns	3
E13	MII cam_reject hold from rx_clk rising	N/A		ns	3

Table 27: Ethernet timing characteristics

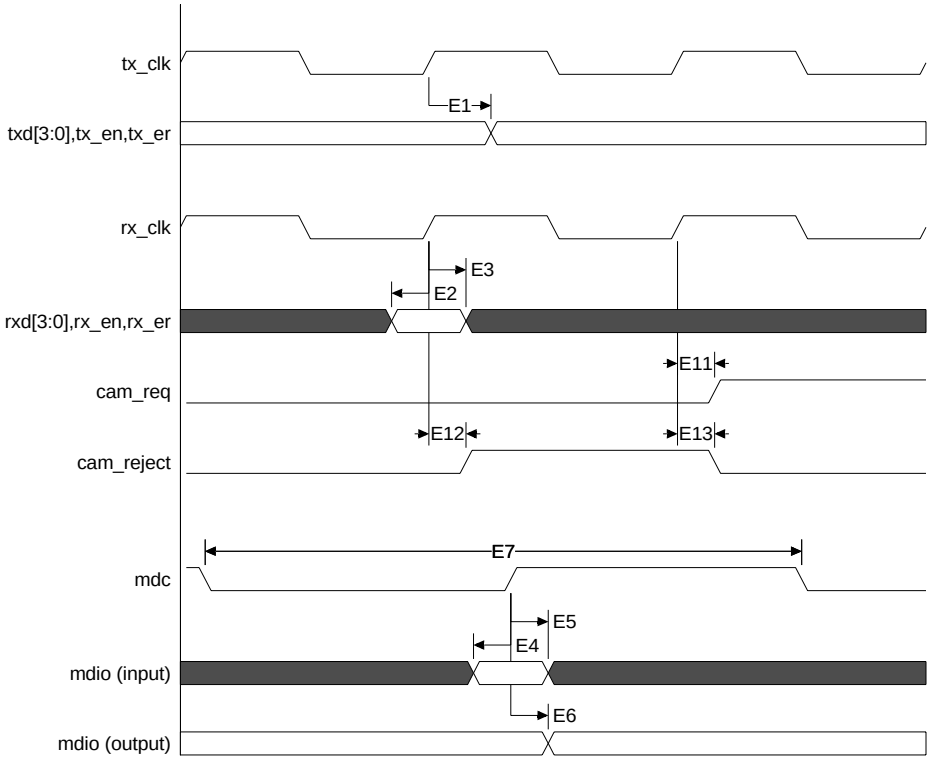
Notes:

1 Minimum specification is for fastest AHB bus clock of 100 MHz. Maximum specification is for slowest AHB bus clock of 50 MHz.

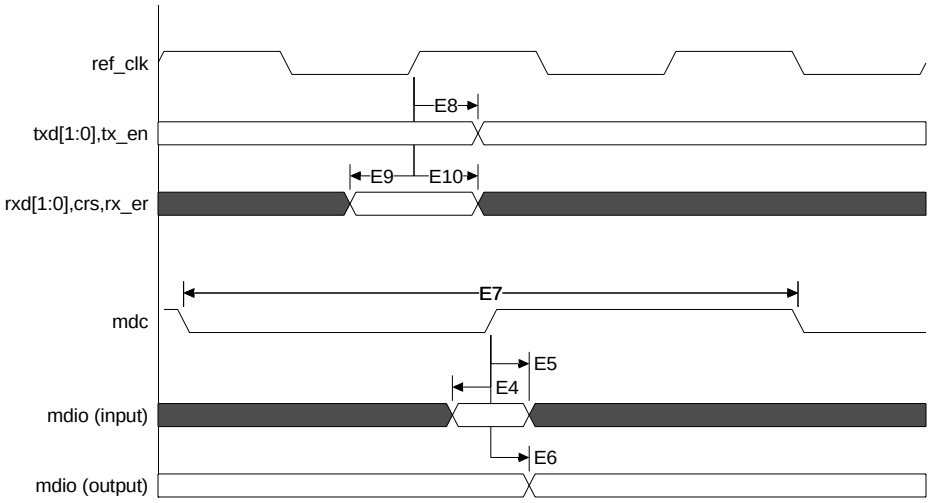
2 C_{load} = 10pF for all outputs and bidirects.

3 No setup and hold requirements for `cam_reject` because it is an asynchronous input. This is also true for RMII PHY applications.

Ethernet MII timing



Ethernet RMII timing



PCI timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 28 and Table 29 describe the values shown in the PCI timing diagrams.

Parameter	Description	Min	Max	Units	Notes
P1	pci_clk_in to signal valid delay	2	9	ns	1, 2
P2	input setup to pci_clk_in	5		ns	1
P3	input hold from pci_clk_in	0		ns	
P4	pci_clk_in to signal active	2		ns	2
P5	pci_clk_in to signal float		28	ns	2
P6	pci_clk_out high time	50%-1	50%+1	ns	3
P7	pci_clk_out low time	50%-1	50%+1	ns	3
P8	pci_clk_in cycle time	30		ns	
P9	pci_clk_in high time	11		ns	
P10	pci_clk_in low time	11		ns	

Table 28: PCI timing characteristics

Notes:

1 Parameters same for bussed and point-to-point signals.

2 C_{LOAD} = 10pf on all outputs

3 `pci_clk_out` high and low times specified as 50% of the clock period +/-1 ns.

Parameter	Description	Min	Max	Units	Notes
P1	pci_clk_in to signal valid delay	2	10	ns	1
P2	input setup to pci_clk_in	5		ns	1
P3	input hold from pci_clk_in	0		ns	
P4	pci_clk_in to signal active	2		ns	1
P5	pci_clk_in to signal float		28	ns	1
P6	pci_clk_out high time	50%-1	50%+1	ns	2
P7	pci_clk_out low time	50%-1	50%+1	ns	2
P8	pci_clk_in cycle time	30		ns	
P9	pci_clk_in high time	11		ns	
P10	pci_clk_in low time	11		ns	

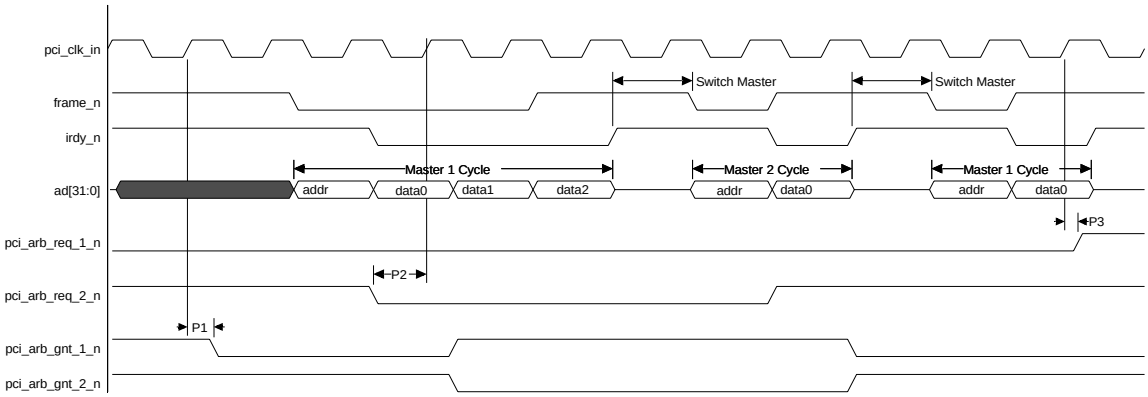
Table 29: CardBus timing characteristics

Notes:

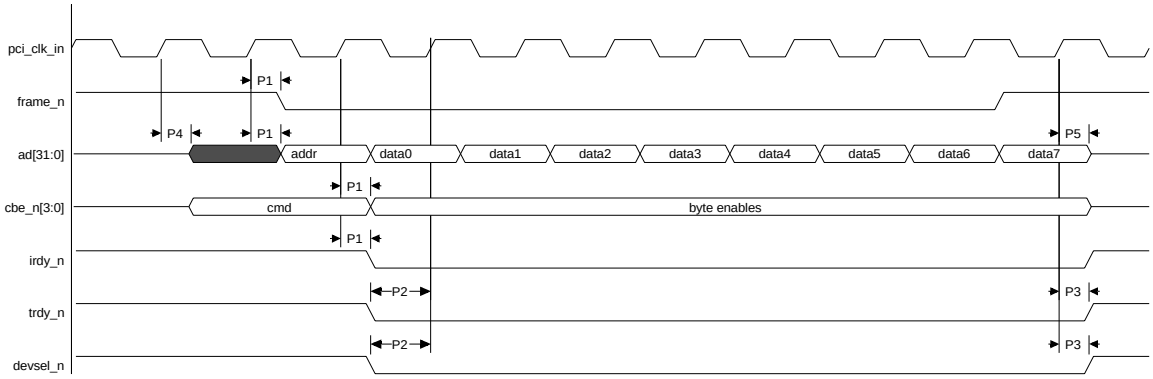
1 Minimum times are specified with 0pf and maximum times are specified with 30pf.

2 `pci_clk_out` high and low times specified as 50% of the clock period +/-1 ns.

Internal PCI arbiter timing

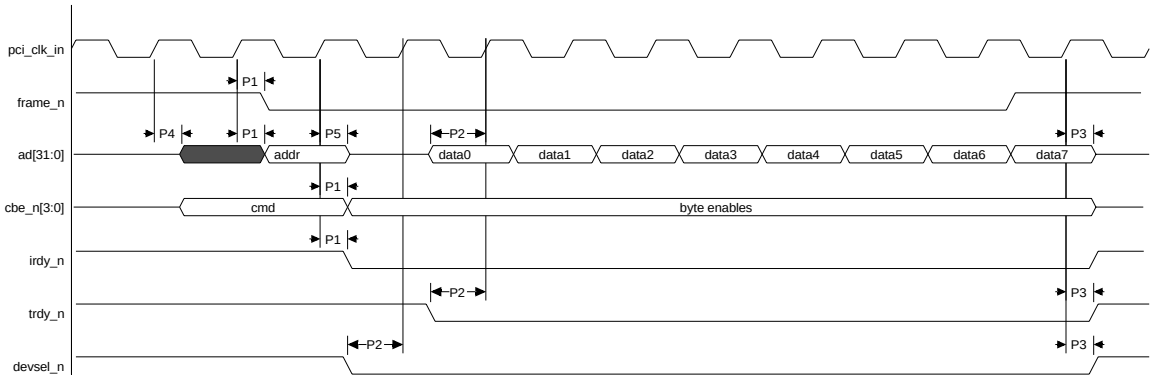


PCI burst write from NS9750 timing



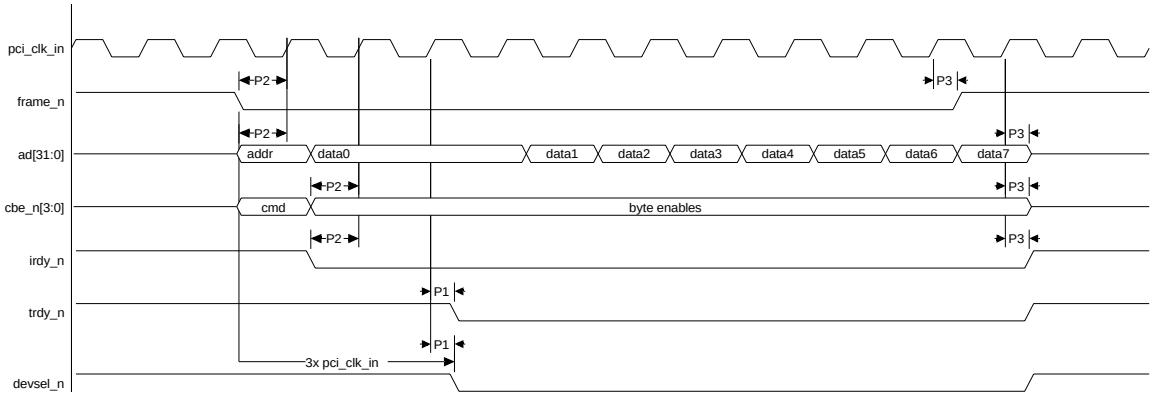
Note:
The functional timing for `trdy_n` and `devsel_n` shows the fastest possible response from the target.

PCI burst read from NS9750 timing

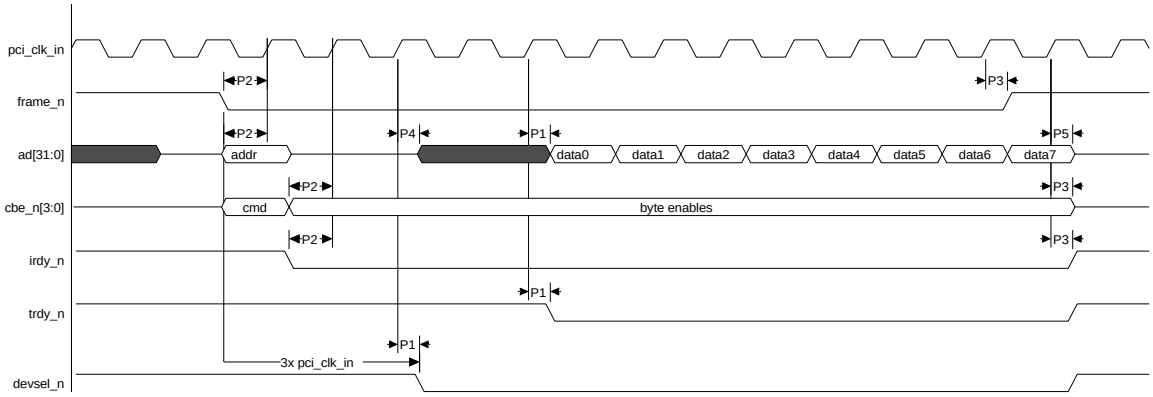


Note:
The functional timing for `trdy_n`, `devsel_n`, and the read data on `ad[31:0]` shows the fastest possible response from the target.

PCI burst write to NS9750 timing

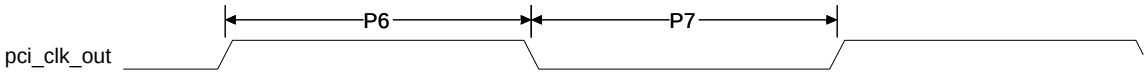


PCI burst read to NS9750 timing

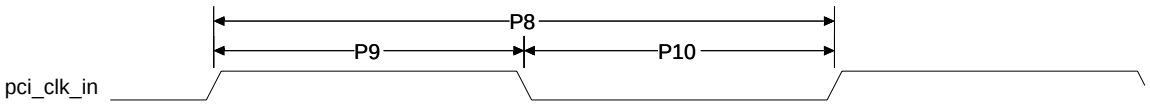


Note:
The functional timing for valid read data on `ad[31:0]` is just an example. The actual response time will depend on when the PCI bridge gets access to the AHB bus internal to NS9750.

pci_clk_out timing



pci_clk_in timing



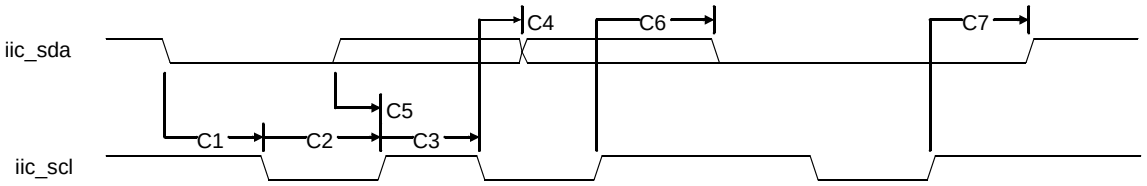
I²C timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 30 describes the values shown in the I²C timing diagram.

		Standard mode		Fast mode		
Parm	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
C1	iic_sda to iic_scl START hold time	4.0		0.6		µs
C2	iic_scl low period	4.7		1.3		µs
C3	iic_scl high period	4.0		0.6		µs
C4	iic_scl to iic_sda DATA hold time	0		0		µs
C5	iic_sda to iic_scl DATA setup time	250		100		ns
C6	iic_scl to iic_sda START setup time	4.7		0.6		µs
C7	iic_scl to iic_sda STOP setup time	4.0		0.6		µs

Table 30: I²C timing parameters



LCD timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 31 describes the values shown in the LCD timing diagrams.

Parm	Description	Register	Value	Units
L1	Horizontal front porch blanking	LCDTiming0	HFP + 1	CLCP periods
L2	Horizontal sync width	LCDTiming0	HSW + 1	CLCP periods
L3	Horizontal period	N/A	L1 + L2 + L15 + L4	CLCP periods
L4	Horizontal backporch	LCDTiming0	HBP + 1	CLCP periods
L5	TFT active line	LCDTiming0	16*(PPL + 1) (see note 3)	CLCP periods
L6	LCD panel clock frequency	LCDTiming1	**For BCD = 0:** CLCDCLK/(PCD + 2) **For BCD = 1:** CLCDCLK (see note 1)	MHz
L7	TFT vertical sync width	LCDTiming1	VSW + 1	H lines
L8	TFT vertical lines/frame	N/A	L7 + L9 + L10 + L11	H lines
L9	TFT vertical back porch	LCDTiming1	VBP	H lines
L10	TFT vertical front porch	LCDTiming1	VFP	H lines
L11	Active lines/frame	LCDTiming1	LPP + 1	H lines
L12	STN HSYNC inactive to VSYNC active	LCDTiming0	HBP + 1	CLCP periods
L13	STN vertical sync width	N/A	1	H lines
L14	STN vertical lines/frame	N/A	L11 + L16	H lines
L15	STN active line	LCDTiming2	CPL–1 (see note 4)	CLCP periods
L16	STN vertical blanking	LCDTiming1	VSW + VFP + VBP + 1	H lines
L17	STN CLCP inactive to HSYNC active	LCDTiming0	HFP + 1.5	CLCP periods
L18	CLCP to data/control (see notes 7 and 8)		-1.0 (min) + 1.5 (max)	ns
L19	CLCP high (see notes 8, 9)		50% ± 0.5ns	ns
L20	CLCP low (see notes 8, 9)		50% ± 0.5ns	ns
L21	TFT VSYNC active to HSYNC active (see note 8)		-0.1ns (min) + 0.1ns (max)	ns
L22	TFT VSYNC active to HSYNC inactive	LCDTiming0	HSW	CLCP periods
L23	STN VSYNC active to HSYNC inactive	LCDTiming0	**STN color:** 14 + HSW + HFP **STN Mono8:** 6 + HSW + HFP **STN Mono4:** 10 + HSW + HFP	CLCP periods

Table 31: LCD timing parameters

Parm	Description	Register	Value	Units
L24	STN HSYNC inactive to VSYNC inactive	LCDTiming0	HBP + 1	CLCP periods
L25	STN VSYNC inactive to HSYNC active	LCDTiming0	**STN color:** HFP + 13 **STN Mono8:** HFP + 15 **STN Mono4:** HFP + 9	CLCP periods
L26	CLCP period		12.5 ns (min)	ns

Table 31: LCD timing parameters

Notes:

1 CLCDCLK is selected from 5 possible sources:
   — lcdclk/2 (lcdclk is an external oscillator)
   — AHB clock
   — AHB clock/2
   — AHB clock/4
   — AHB clock/8
   See the LCD chapter in the *NS9750 Hardware Reference* for acceptable clock frequencies for the different display configurations.

2 The polarity of CLLP, CLFP, CLCP, and CLAC can be inverted using control fields in the LCDTiming1 register.

3 The CPL field in the LCDTiming1 register must also be programmed to T5-1 (see the LCD chapter in the *NS9750 Hardware Reference*).

4 The PPL field in the LCDTiming0 register must also be programmed correctly (see the LCD chapter in the *NS9750 Hardware Reference*).

5 These data widths are supported:
   — 4-bit mono STN single panel
   — 8-bit mono STN single panel
   — 8-bit color STN single panel
   — 4-bit mono STN dual panel (8 bits to LCD panel)
   — 8-bit mono STN dual panel (16 bits to LCD panel)
   — 8-bit color STN dual panel (16 bits to LCD panel)
   — 24-bit TFT
   — 18-bit TFT

6 See the LCD chapter in the *NS9750 Hardware Reference* for definitions of the bit fields referred to in this table.

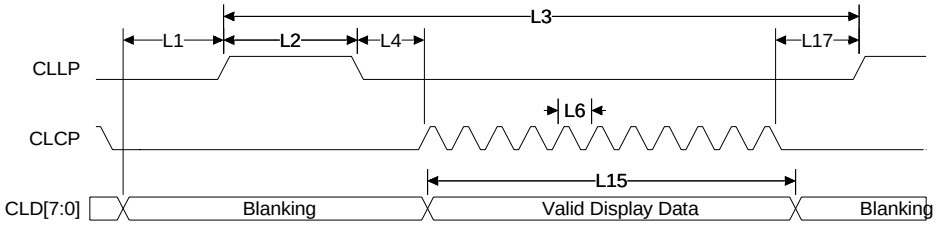
7 Note that data is sampled by the LCD panel on the falling edge of the CLCP in "LCD output timing" on page 66). If the polarity of CLCP is inverted, this parameter is relative to CLCP falling.

8 C_{load} = 10pf on all outputs.

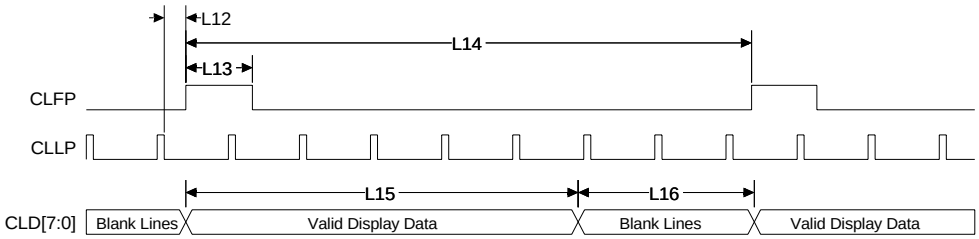
9 CLCP high and low times specified as 50% of the clock period +/- 0.5ns.

10 Maximum allowable LCD panel clock frequency is 80 MHz.

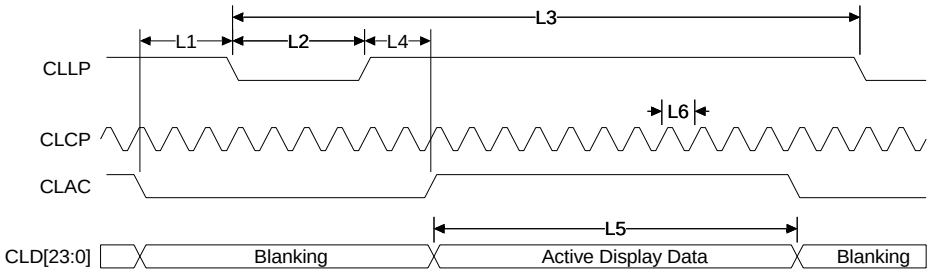
Horizontal timing for STN displays



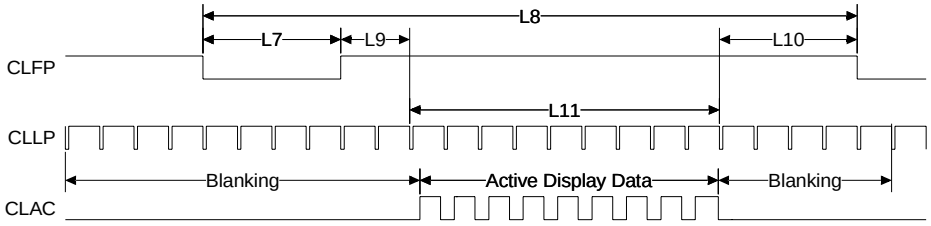
Vertical timing for STN displays



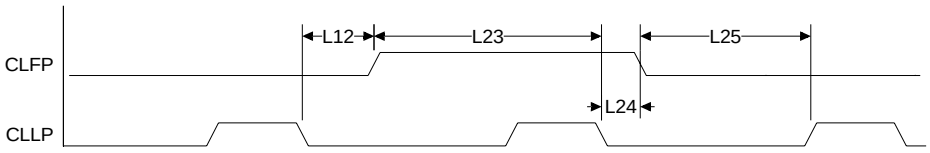
Horizontal timing for TFT displays



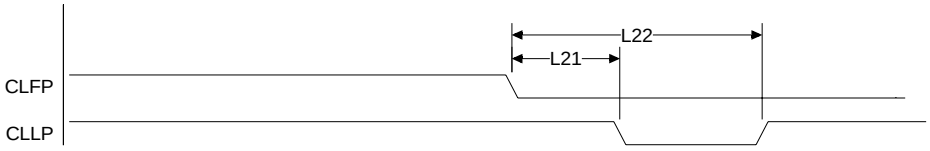
Vertical timing for TFT displays



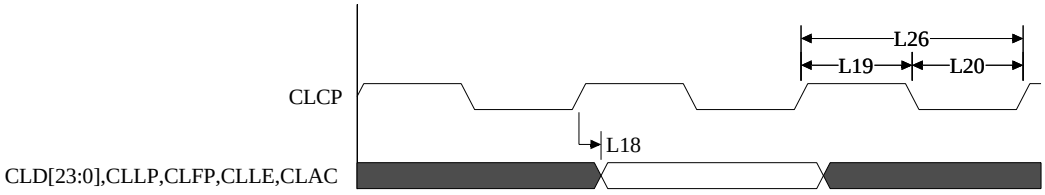
HSYNC vs VSYNC timing for STN displays



HSYNC vs VSYNC timing for TFT displays



LCD output timing



SPI timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 32 describes the values shown in the SPI timing diagrams.

Parm	Description	Min	Max	Unit	Modes	Notes
SPI master parameters						
SP0	SPI enable low setup to first SPI CLK out rising	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP1	SPI enable low setup to first SPI CLK out falling	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP3	SPI data in setup to SPI CLK out rising	30		ns	0, 3	
SP4	SPI data in hold from SPI CLK out rising	0		ns	0, 3	
SP5	SPI data in setup to SPI CLK out falling	30		ns	1, 2	
SP6	SPI data in hold from SPI CLK out falling	0		ns	1, 2	
SP7	SPI CLK out falling to SPI data out valid		10	ns	0, 3	6
SP8	SPI CLK out rising to SPI data out valid		10	ns	1, 2	6
SP9	SPI enable low hold from last SPI CLK out falling	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP10	SPI enable low hold from last SPI CLK out rising	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP11	SPI CLK out high time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP12	SPI CLK out low time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP13	SPI CLK out period	$T_{BCLK}*6$		ns	0, 1, 2, 3	3
SPI slave parameters						
SP14	SPI enable low setup to first SPI CLK in rising	30		ns	0, 3	1
SP15	SPI enable low setup to first SPI CLK in falling	30		ns	1, 2	1
SP16	SPI data in setup to SPI CLK in rising	0		ns	0, 3	
SP17	SPI data in hold from SPI CLK in rising	60		ns	0, 3	
SP18	SPI data in setup to SPI CLK in falling	0		ns	1, 2	
SP19	SPI data in hold from SPI CLK in falling	60		ns	1, 2	
SP20	SPI CLK in falling to SPI data out valid	20	70	ns	0, 3	6
SP21	SPI CLK in rising to SPI data out valid	20	70	ns	1, 2	6
SP22	SPI enable low hold from last SPI CLK in falling	15		ns	0, 3	1
SP23	SPI enable low hold from last SPI CLK in rising	15		ns	1, 2	1

Table 32: SPI timing parameters

Parm	Description	Min	Max	Unit	Modes	Notes
SP24	SPI CLK in high time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5
SP25	SPI CLK in low time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5
SP26	SPI CLK in period	T_{BCLK}*10		ns	0, 1, 2, 3	

Table 32: SPI timing parameters

Notes:

1 Active level of SPI enable is inverted (that is, 1) if the CSPOL bit in Serial Channel B/A/C/D Control Register B (see the *NS9750 Hardware Reference*) is set to 1. Note that in SPI slave mode, only a value of 0 (low enable) is valid; the SPI slave is fixed to an active low chip select.

2 SPI data order is reversed (that is, LSB last and MSB first) if the BITORDR bit in Serial Channel B/A/C/D Control Register B (see the *NS9750 Hardware Reference*) is set to 0.

3 T_{BCLK} is period of BBus clock.

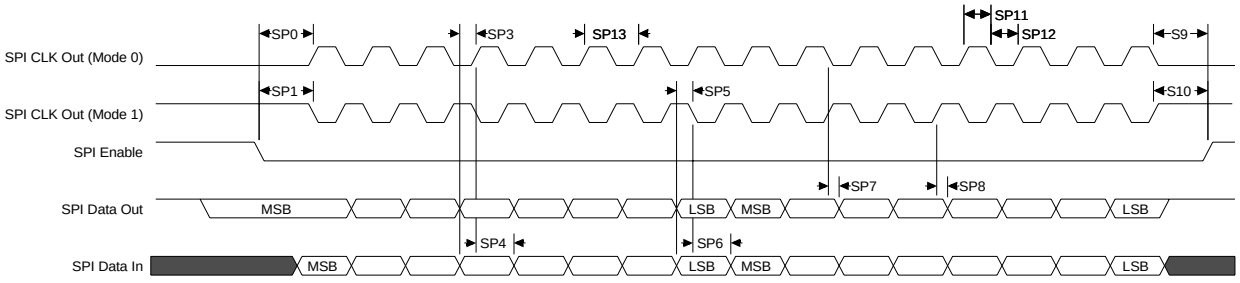
4 +/- 5% duty cycle skew.

5 +/- 10% duty cycle skew.

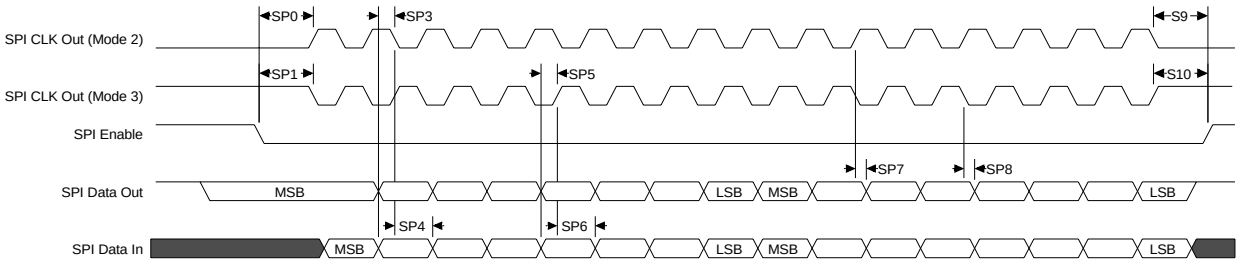
6 C_{load} = 10pf for all outputs.

7 SPI data order can be reversed such that LSB is first. Use the BITORDR bit in Serial Channel B/A/C/D Control Register A.

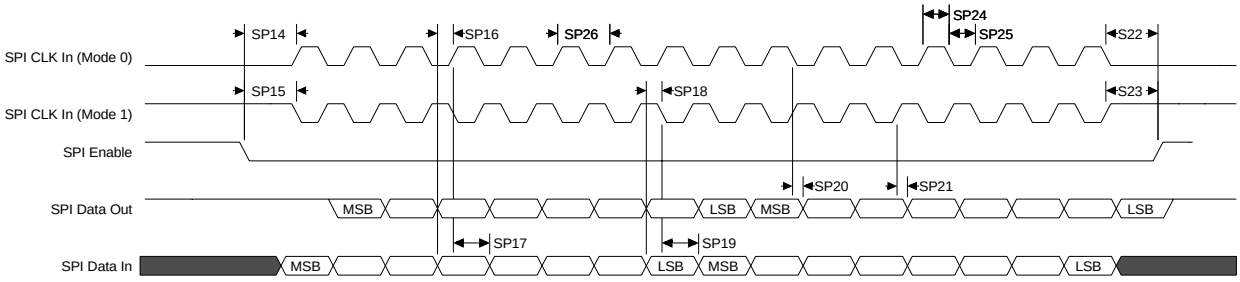
SPI master mode 0 and 1: 2-byte transfer (see note 7)



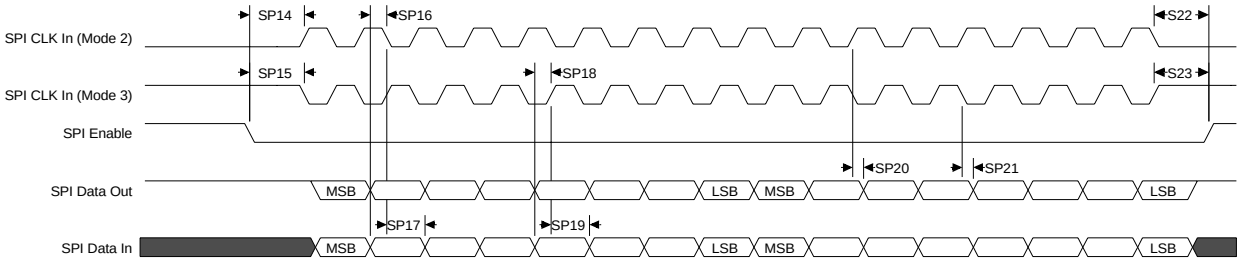
SPI master mode 2 and 3: 2-byte transfer (see note 7)



SPI slave mode 0 and 1: 2-byte transfer (see note 7)



SPI slave mode 2 and 3: 2-byte transfer (see note 7)



IEEE 1284 timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 33 describes the values shown in the IEEE 1284 timing diagram.

Parameter	Description	Min	Max	Unit	Note
IE1	Busy-while-Strobe	0	500	ns	1
IE2	Busy high to nAck low	0		ns	
IE3	Busy high		1000	ns	2
IE4	nAck low		500	ns	3
IE5	nAck high to Busy low		500	ns	3

Table 33: IEEE 1284 timing parameters

Notes:

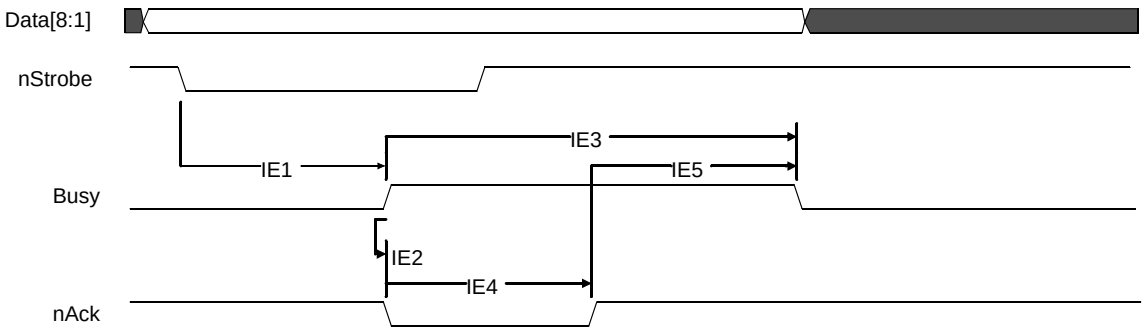
1 The range is 0ns up to one time unit.

2 Two time units.

3 Three time units.

IEEE 1284 timing example

The IEEE 1284 timing is determined by the BBus clock and the Granularity Count register (GCR) setting. In this example, the BBus clock is 50 MHz and the Granularity Count register is set to 25. The basic time unit is `1/50 MHz x 25`, which is 500ns.



USB timing

Table 34 and Table 35 describe the values shown in the USB timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	4	20	ns	1
U2	Fall time (10%–90%)	4	20	ns	1
U3	Differential rise and fall time matching	90	111.11	%	2, 5
U4	Driver output resistance	28	44	ohms	3

Table 34: USB full speed timing parameters

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	75	300	ns	4
U2	Fall time (10%–90%)	75	300	ns	4
U3	Differential rise and fall time matching	80	125	%	2, 5

Table 35: USB low speed timing parameters

Notes:

1 Load shown in "USB full speed load."

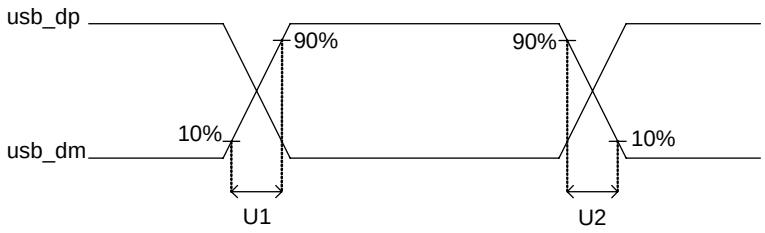
2 U1/U2.

3 Includes resistance of 27 ohm +/- 2 ohm external series resistor.

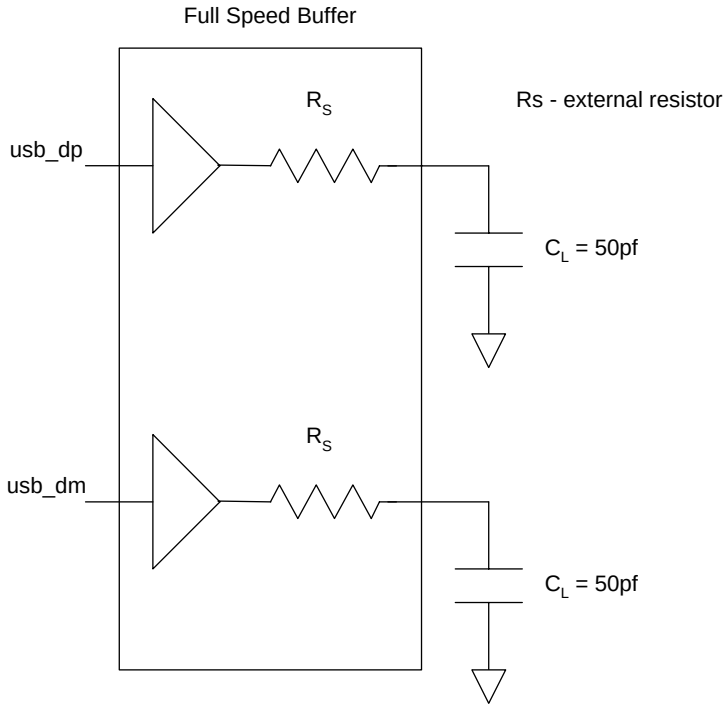
4 Load shown in "USB low speed load."

5 Excluding the first transition from the idle state.

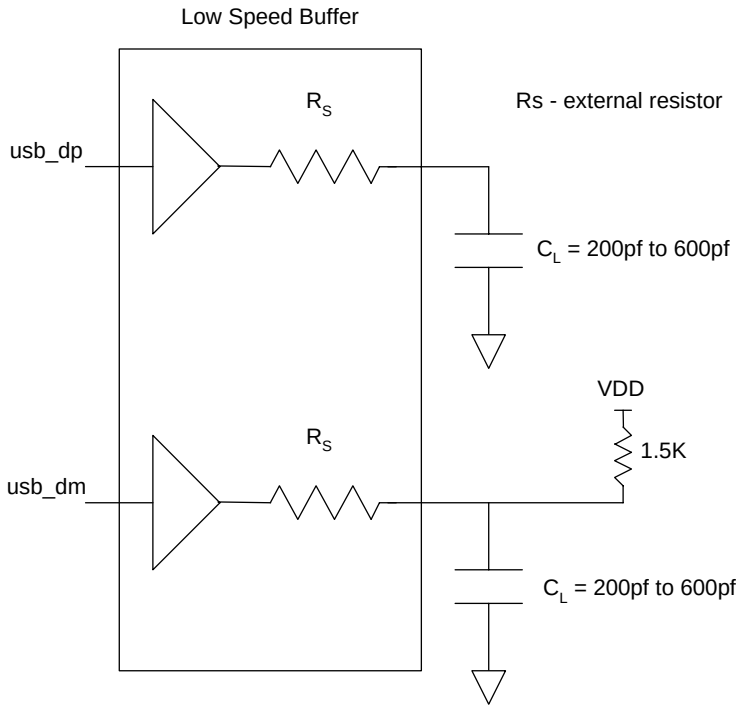
USB differential data timing



USB full speed load



USB low speed load



Reset and hardware strapping timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

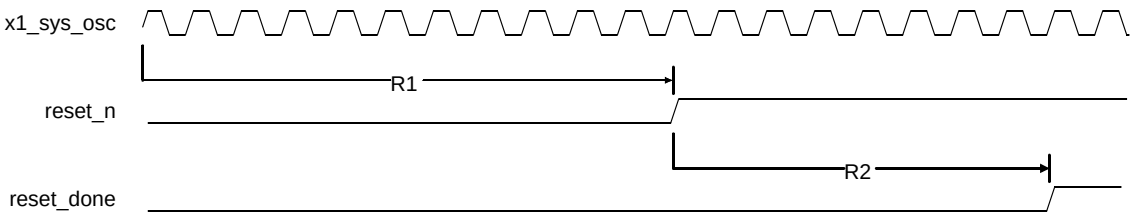
Table 36 describes the values shown in the reset and hardware strapping timing diagram.

Parameter	Description	Min	Max	Unit	Notes
R1	reset_n minimum time	10		x1_sys_osc clock cycles	1
R2	reset_n to reset_done		4	ms	

Table 36: Reset and hardware strapping timing parameters

Note:

1 The hardware strapping pins are latch 5 clock cycles after `reset_n` is deasserted (goes high).



- R1: `reset_n` must be held low for a minimum of 10 `x1_sys_osc` clock cycles after power up.
- R2: `reset_done` is asserted 4ms after `reset_n` is driven high.
- The hardware strapping pins are latched when `reset_done` is asserted.

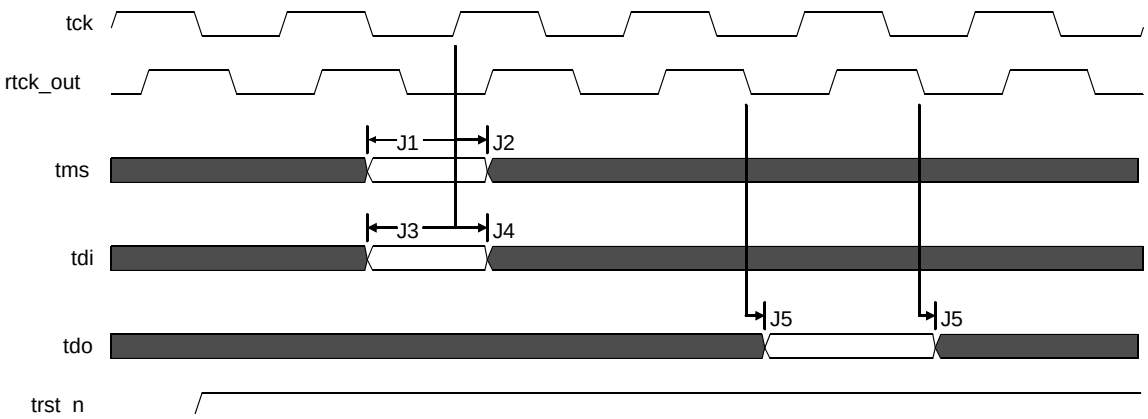
JTAG timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

Table 37 describes the values shown in the JTAG timing diagram.

Parameter	Description	Min	Max	Unit
J1	tms (input) setup to tck rising	5		ns
J2	tms (input) hold to tck rising	2		ns
J3	tdi (input) setup to tck rising	5		ns
J4	tdi (input) hold to tck rising	2		ns
J5	tdo (output) to tck falling	2.5	10	ns

Table 37: JTAG timing parameters



Notes:

1 maximum tck rate is 10 MHz.

2 `rtck_out` is an asynchronous output, driven off of the CPU clock.

3 `trst_n` is an asynchronous input.

Clock timing

Note: All AC characteristics are measured with 10pF, unless otherwise noted.

The next three timing diagrams pertain to clock timing.

USB crystal/external oscillator timing

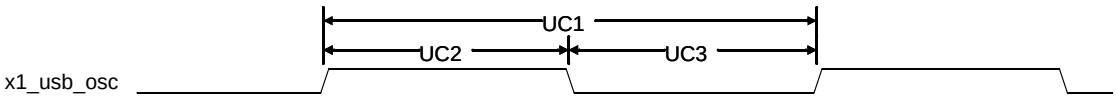
Table 38 describes the values shown in the USB crystal/external oscillator timing diagram.

Parameter	Description	Min	Max	Unit	Notes
UC1	x1_usb_osc cycle time	20.831	20.835	ns	1
UC2	x1_usb_osc high time	(UC1/2) x 0.4	(UC1/2) x 0.6	ns	
UC3	x1_usb_osc low time	(UC1/2) x 0.4	(UC1/2) X 0.6	ns	

Table 38: USB crystal/external oscillator timing parameters

Note:

1 If using a crystal, the tolerance must be +/- 100 ppm or better.



LCD input clock

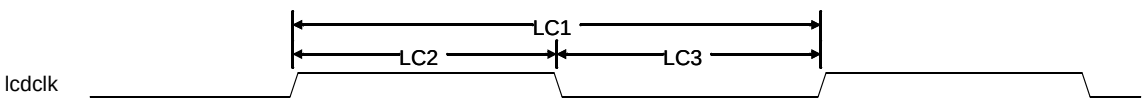
Table 39 describes the values shown for the LCD input clock timing diagram.

Parameter	Description	Min	Max	Unit	Notes
LC1	lcdclk cycle time	6.25		ns	1
LC2	lcdclk high time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	
LC3	lcdclk low time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	

Table 39: LCD input clock timing parameters

Note:

1 The clock rate supplied on `lcdclk` is twice the actual LCD clock rate.



System PLL reference clock timing

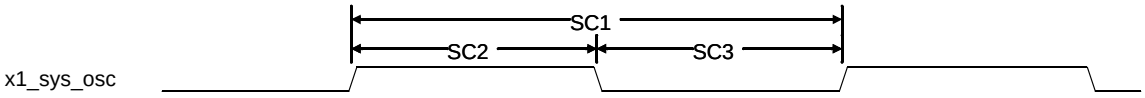
Table 40 describes the values shown in the system PLL reference clock timing diagram.

Parameter	Description	Min	Max	Unit	Notes
SC1	x1_sys_osc cycle time	2.5	5	ns	1
SC2	x1_sys_osc high time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns	
SC3	x1_sys_osc low time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns	

Table 40: System PLL reference clock timing parameters

Note:

1 The system PLL can be bypassed. In this mode, the CPU clock is 1/2 of `x1_sys_osc`.



Packaging

The NS9750 dimensions and pinout are shown in the next two diagrams.

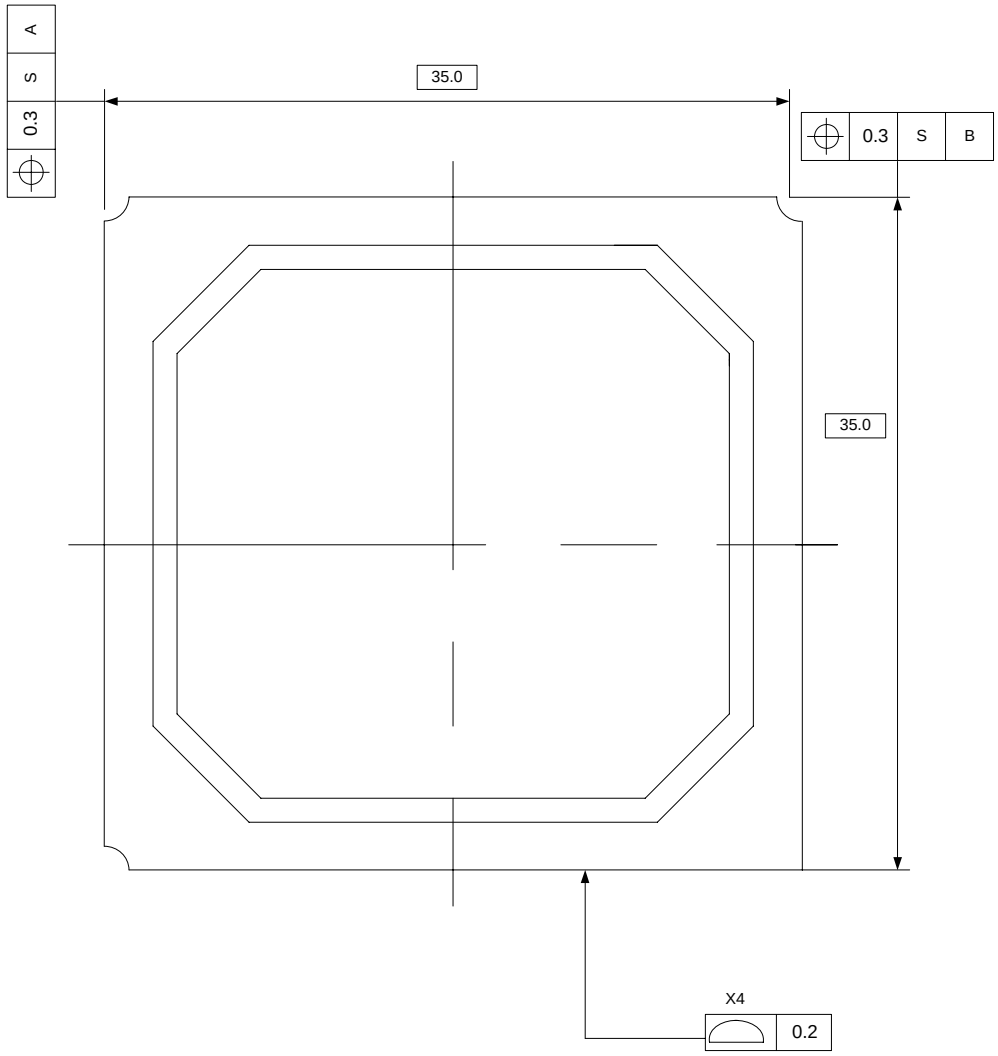


Figure 9: NS9750 top view

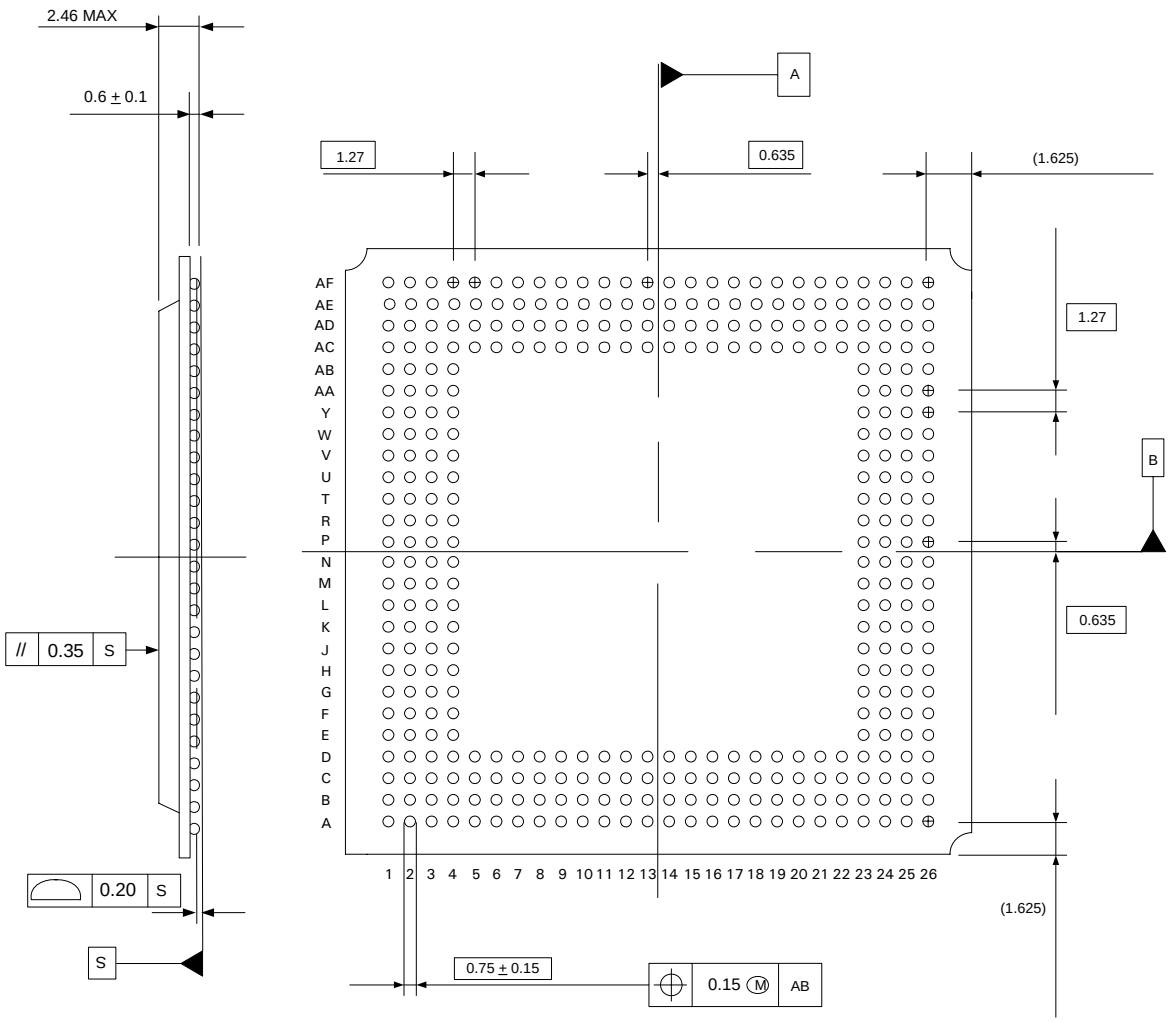


Figure 10: NS9750 bottom and side view

Figure 11 shows the layout of the NS9750, for use in setting up the board.

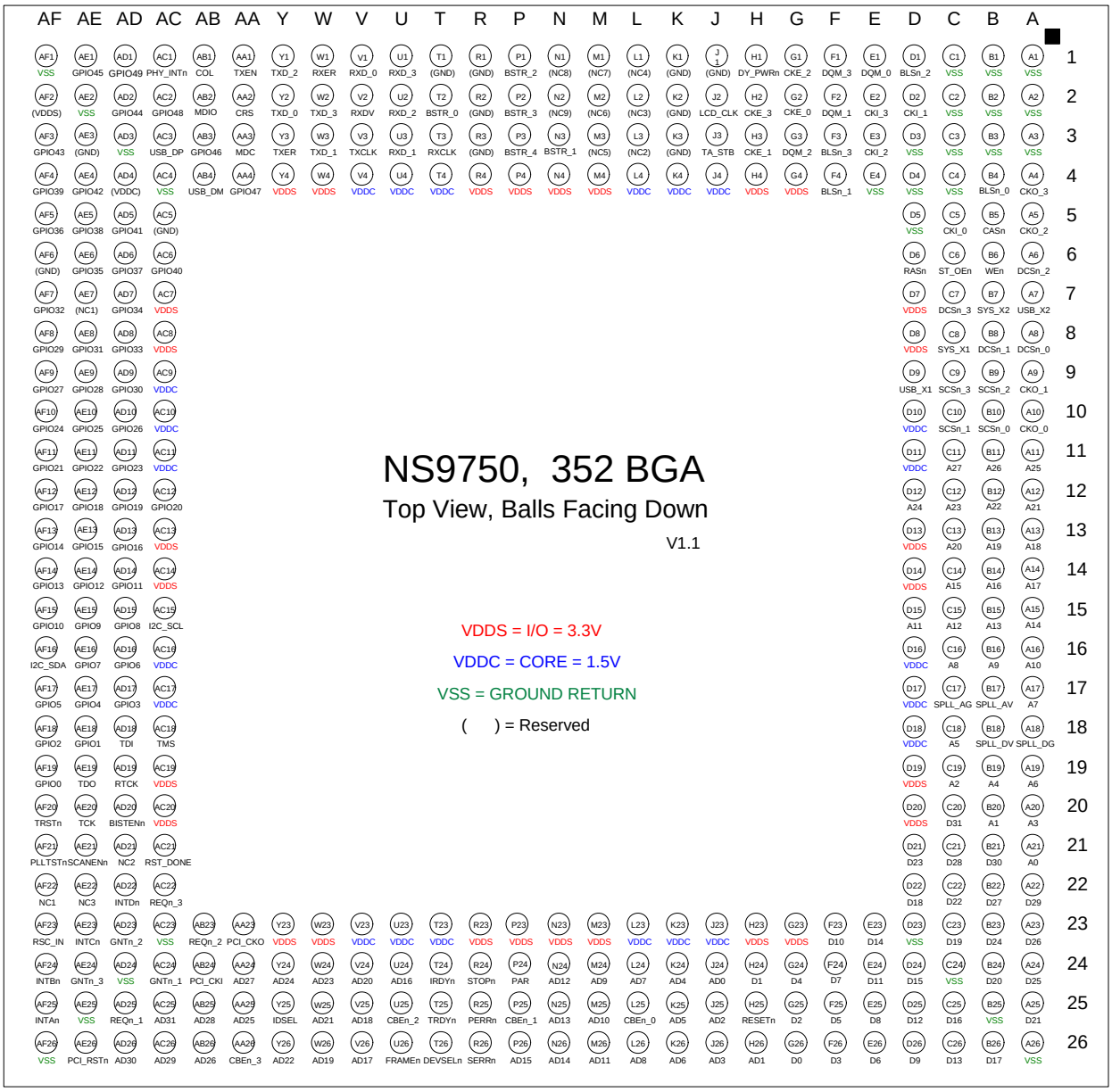


Figure 11: NS9750 BGA layout

P/N: 91001206_D

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