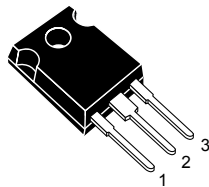
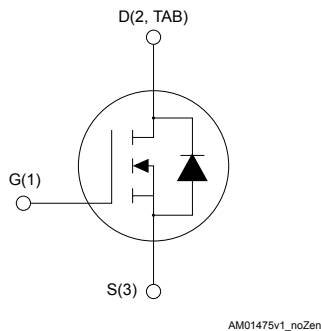


N-channel 600 V, 90 mΩ typ., 45 A MDmesh Power MOSFET in a TO-247 package


TO-247

Product status link
[STW45NM60](#)
Product summary

Order code	STW45NM60
Marking	W45NM60
Package	TO-247
Packing	Tube

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STW45NM60	600 V	110 mΩ	45 A

- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. This device offers extremely low on-resistance, high dv/dt, and excellent avalanche characteristics. Using STMicroelectronics's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance that is superior to similar products on the market.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	45	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	28	
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	417	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$
T_J	Maximum operation junction temperature	150	$^{\circ}\text{C}$

1. Pulse width is limited by safe operating area.

2. $I_{SD} \leq 45\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.3	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 35\text{ V}$)	850	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$	-	-	10	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	100	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 22.5\text{ A}$	-	90	110	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3800	-	pF
C_{oss}	Output capacitance		-	1250	-	pF
C_{rss}	Reverse transfer capacitance		-	80	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	340	-	pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 45\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 13. Test circuit for gate charge behavior)	-	96	134 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	31	-	nC
Q_{gd}	Gate-drain charge		-	43	-	nC
R_g	Gate input resistance	$f = 1\text{ MHz}$, open drain	-	1.4	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 22.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	30	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_f	Fall time		-	23	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 45\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	508	-	ns
Q_{rr}	Reverse recovery charge		-	10	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	40	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	650	-	ns
Q_{rr}	Reverse recovery charge		-	14	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	43	-	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

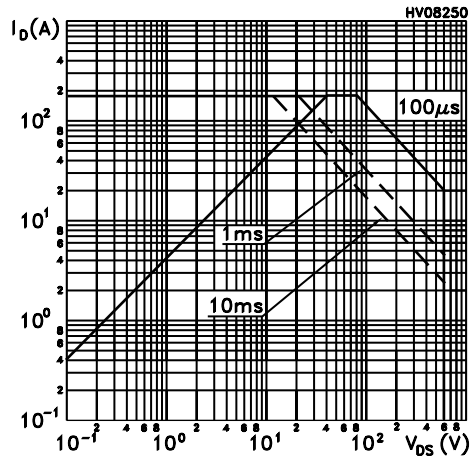
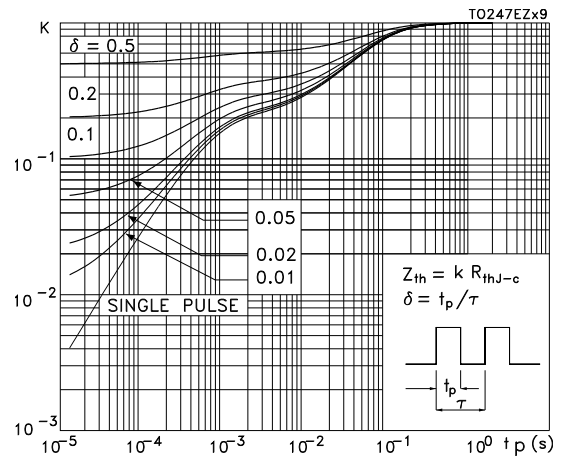
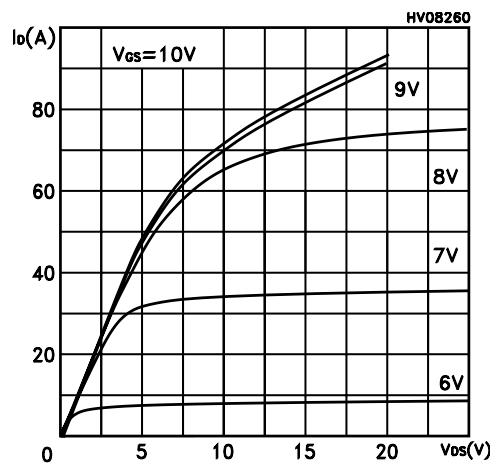
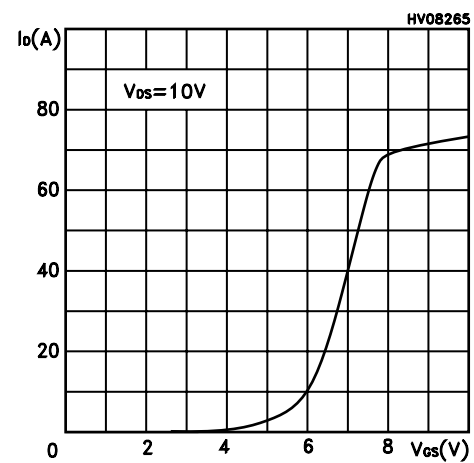
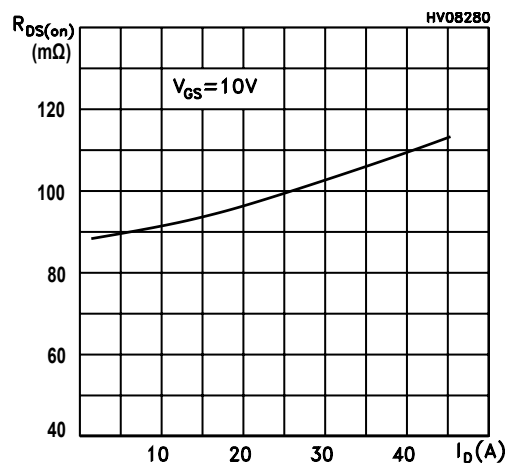
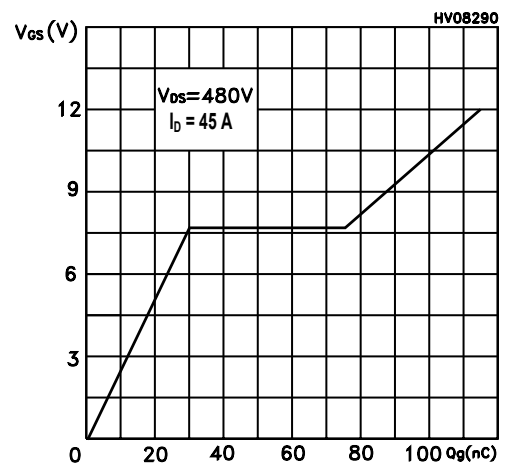
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Static drain-source on-resistance

Figure 6. Gate charge vs gate-source voltage


Figure 7. Capacitance variations

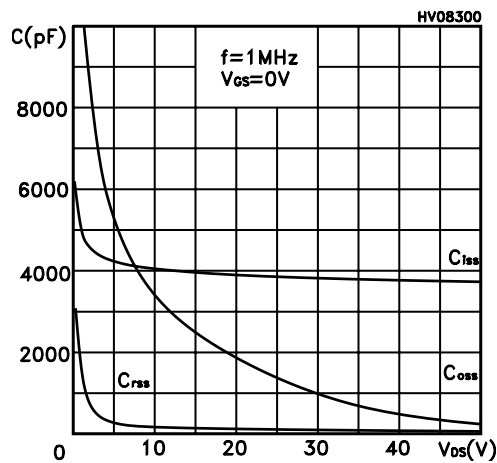


Figure 8. Normalized gate threshold vs temperature

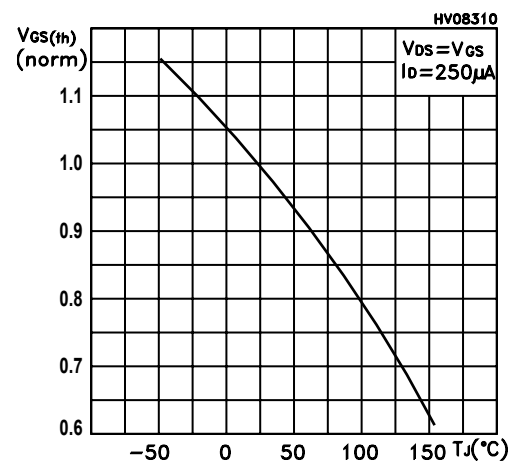


Figure 9. Normalized on-resistance vs temperature

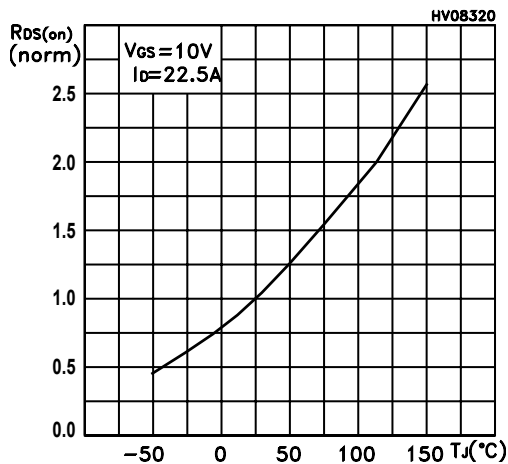


Figure 10. Source-drain diode forward characteristics

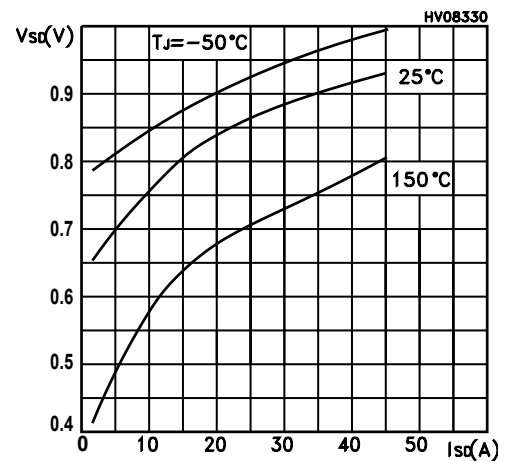
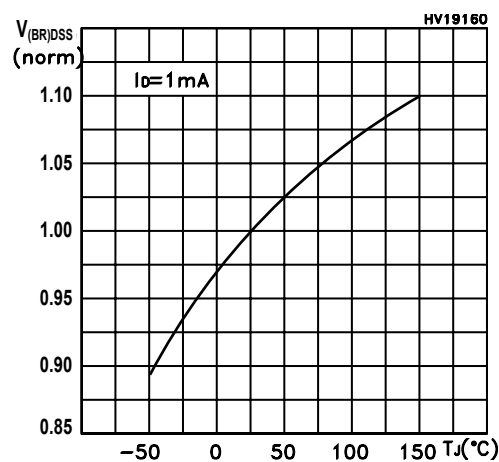
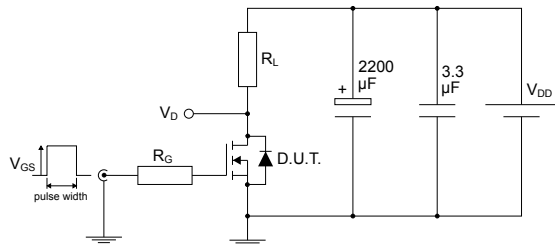


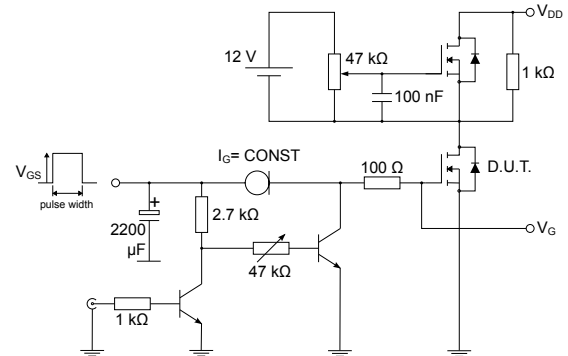
Figure 11. Normalized breakdown voltage vs temperature



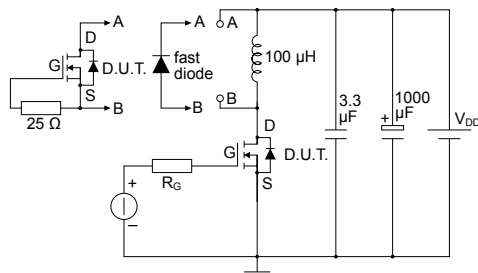
3 Test circuits

Figure 12. Test circuit for resistive load switching times


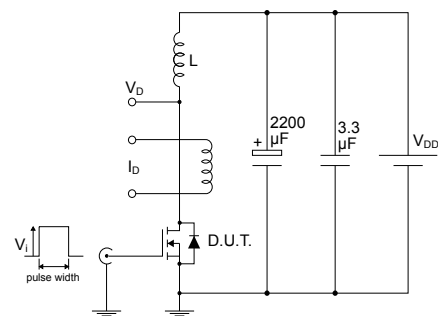
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Figure 13. Test circuit for gate charge behavior


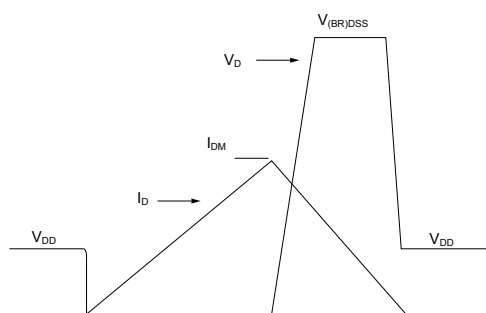
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Figure 14. Test circuit for inductive load switching and diode recovery times


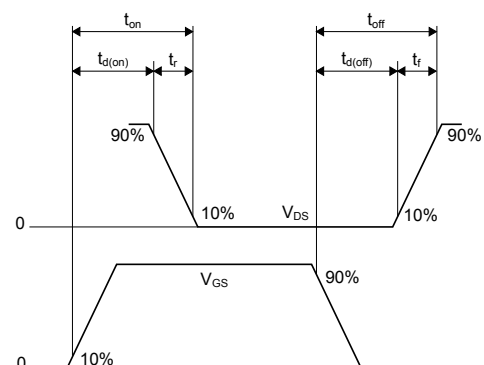
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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


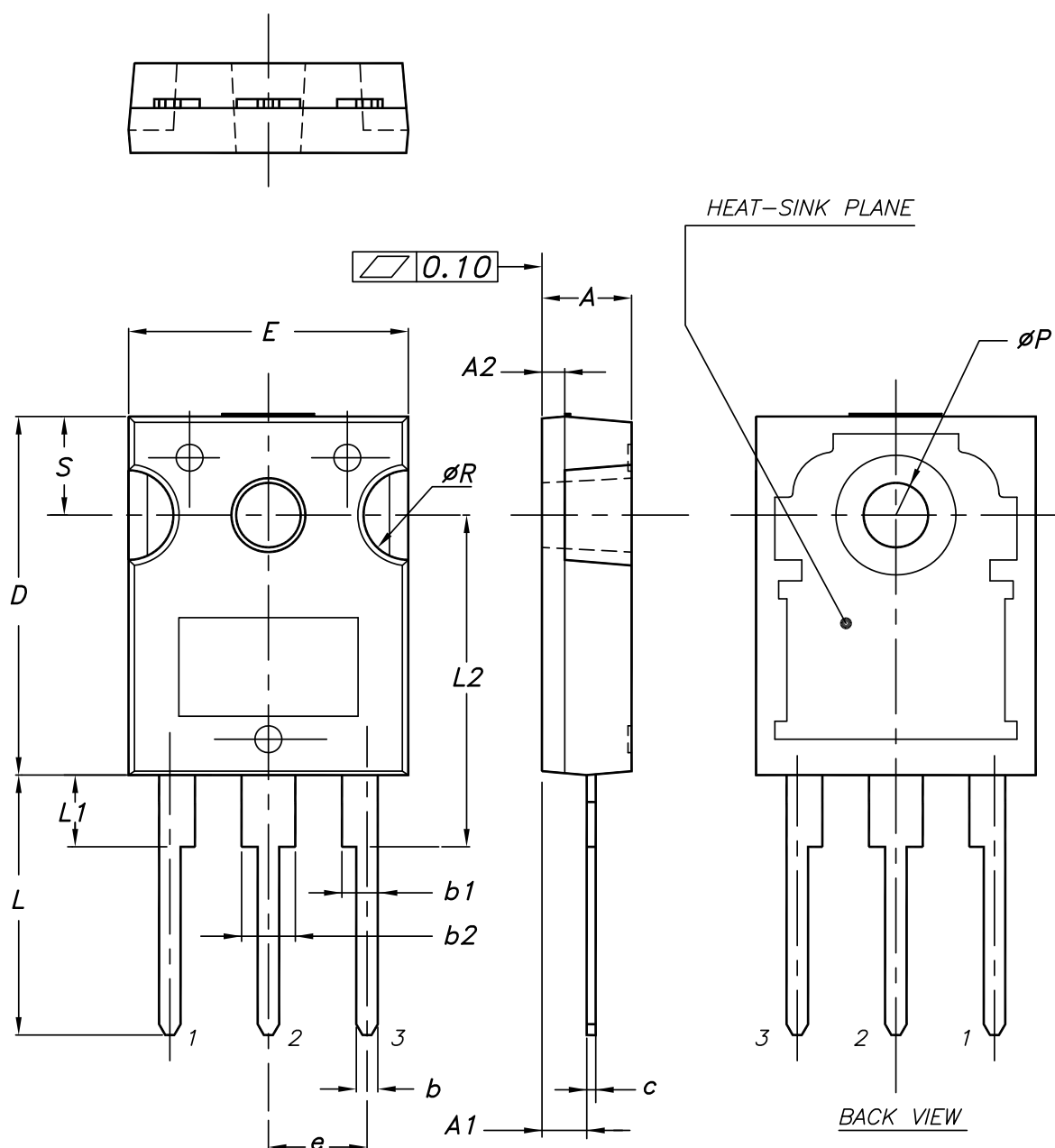
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 18. TO-247 package outline



0075325_11

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. Document revision history

Date	Revision	Changes
05-Mar-2005	5	Complete document with curves.
16-May-2006	6	The document has been reformatted.
18-Dec-2006	7	Updates curves: <i>Figure 1</i> , <i>Figure 4</i> and <i>Figure 6</i> .
02-Apr-2007	8	<i>Figure 1</i> has been updated.
15-Jan-2026	9	Updated Section 4: Package information . Minor text changes.

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