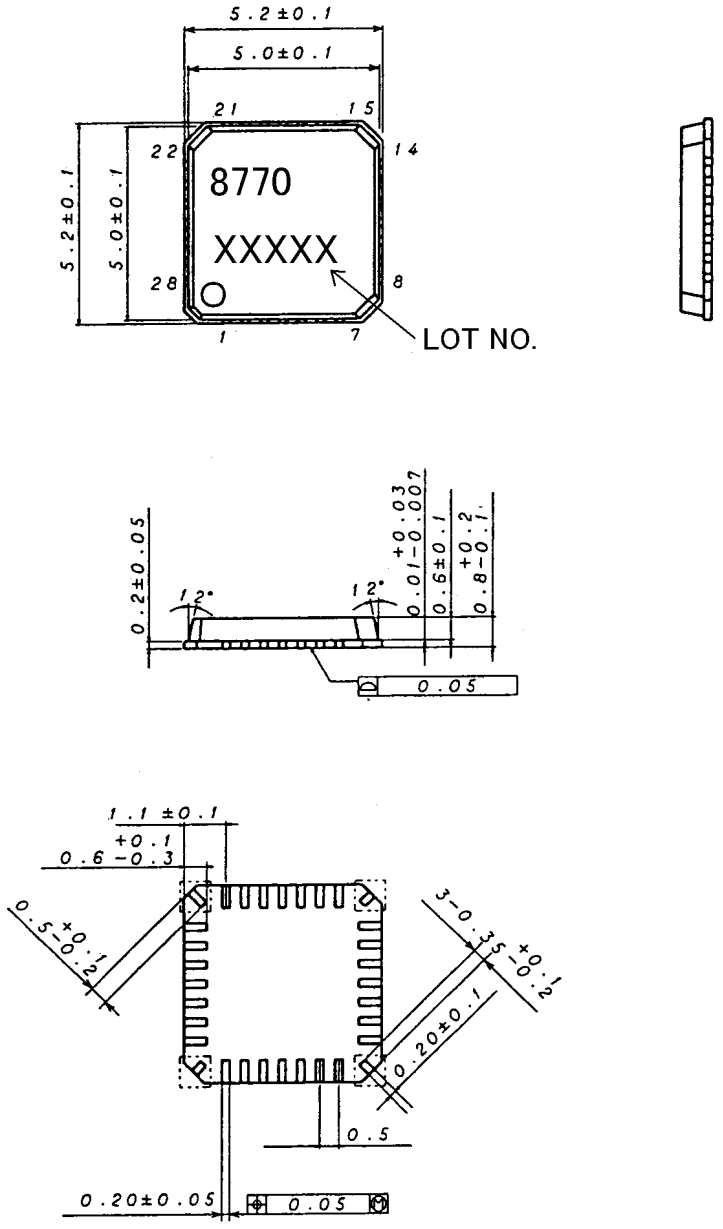
Structure	Silicon Monolithic Integrated Circuit
Product	LED Driver for mobile telephone
Type	BU8770KN
Package Outline	Fig.1 (Plastic Mold)
Block Diagram	Fig.2

Function

- ○ Each color can be controlled by PWM in 128 steps.
- ○ DC/DC converter for LED drive.
- ○ Serial interface.
- ○ QFN28V Package.
- ○ Standby Function.

INDEX

1 Package Outline



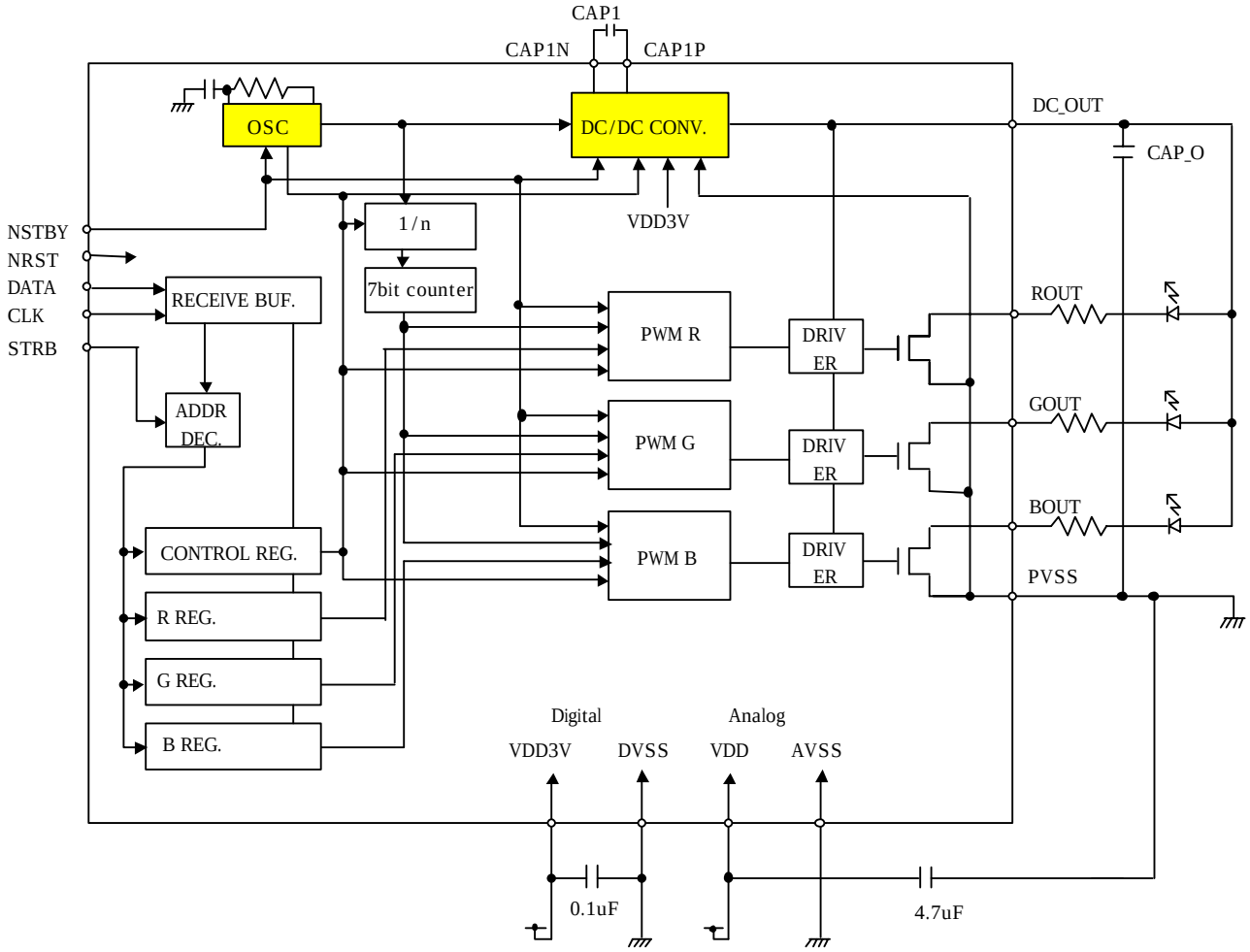
注）点線部は実装を推奨しておりません
NOTICE) Not recommend soldering the part of the dotted line.

(Plastic Mold)

Fig. 1 Package Outline

2 Block Diagram

2-1)Block Diagram



Analog

Digital

A power supply is separate in the digital(VDD3V) and the analog (VDD).
Refer to a "Pin Condition Table" for the pin arrangement.
The capacitor value of the power supply line of VDD, VDD3V is recommendation value.
DC_OUT is being used for open-drain drive in the "DRIVER" block.
A part of the "DC/DC CONV block" inside uses PVSS for the ground.

電源はデジタル系(VDD3V)とアナログ系(VDD)に分かれています。
ピン配置は「端子条件表」を参照してください。
なお、VDD,VDD3V の電源ラインのコンデンサ値は推奨値です。
DRIVERブロックではオープンドレインゲート駆動にDC_OUTを使用しています。
DC/DC CONV.ブロック内の一部はグランドに PVSS を使用しています。

Fig. 2 Block Diagram

2-2)Circuit Configuration

<CPU Interface Block>

Data are received from the CPU, and the value is sent to the PWM control block.

Block	Function
RECEIVE BUFFER	The temporary buffer from CPU. The data inputted from the "DATA" are received in positive edge of the "CLK".
ADDRESS DECODER	An address is decoded with positive edge of "STRB" from the "receive buffer". When it is an valid address, the part of the data on the "Receive Buffer" is transferred to the "RGB register" as the RGB data.
CONTROL REGISTER	The output ON/OFF of the DC/DC converter. And PWM control output ON/OFF of LED. It is initialized by input of resetting.
RGB REGISTER	The RGB(PWM) value established from the CPU is stored. It is initialized by input of resetting.

* It becomes standby condition during resetting.

<PWM Control Block>

PWM control of LED from PWM value.

Block	Function
1/n(Divider)	Programmable divider.(See Register Map)
7bit COUNTER	This block is counted with the output of Divider. It stops at standby mode.
PWM R PWM G PWM B	PWM control is done from the PWM value from "RGB decoder" and the value of "7bit counter". "PWM R" is outputted to Rout. "PWM G" is outputted to Gout. "PWM B" is outputted to Bout. It stops at standby mode.(All LEDs are lights-out condition.)

＜OSC Block＞

The frequency of 700kHz is generated by the built-in capacitor and resistor.

It stops at standby mode.

＜DC/DC Converter Block＞

This IC is the DC/DC converter of charge pump type.

The capacitor of ripple absorption is necessary for the DC_OUT output.

DC/DC converter stops because oscillator stops at standby mode.

Never: You must not take out current from the DC_OUT pin at the time of standby mode.
The voltage of the DC_OUT pin is almost "VDD-Vf [V]".
(Vf: For the voltage drop of the inside analog switch transistor. About 0.2V(TYP))

注意） スタンバイ時は DC_OUT 端子から電流を引き出さないで下さい。
DC_OUT 端子の電位はおよそ VDD-Vf[V]になっています。
(Vf:内部アナログスイッチトランジスタの電圧降下分。約 0.2V(TYP))

3 Pin Condition

3-1)Pin Arrangement

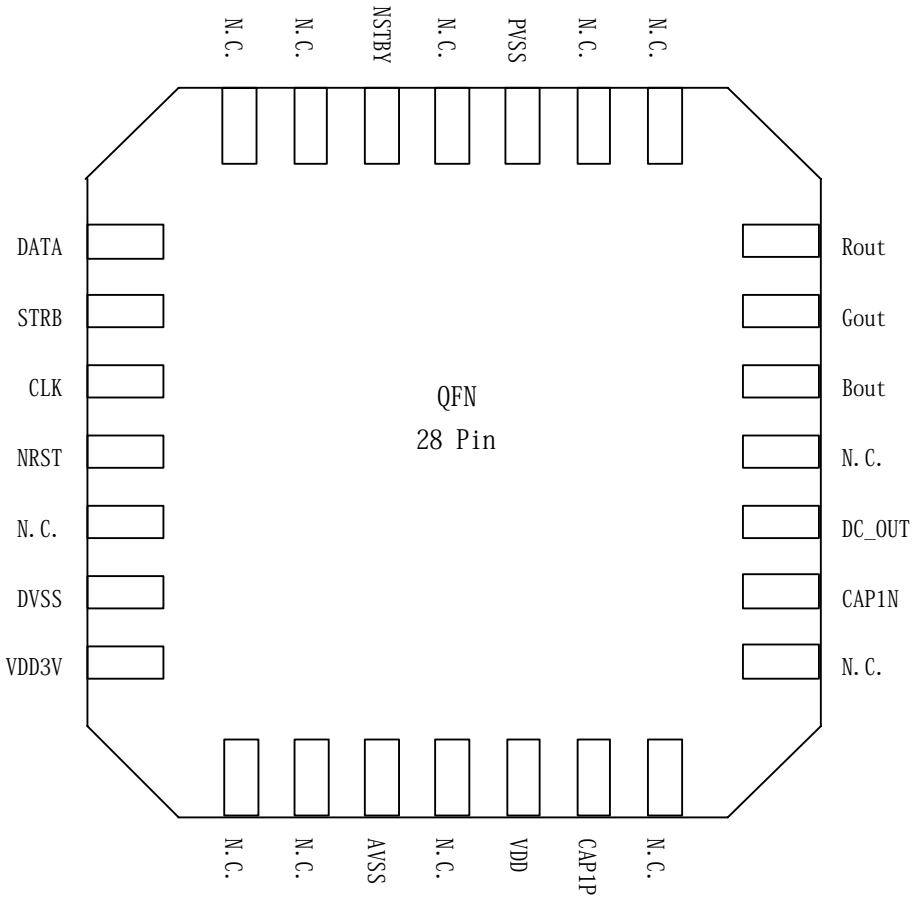


Fig. 3 Pin Arrangement Figure

3- 2)Pin Condition

Table 1 Pin Condition Table

No.	PIN NAME	I/O	TYPE	CIRCUIT	NOTICE
1	DATA	I	DI	A	Serial data input
2	STRB	I	DI	A	Serial data strobe
3	CLK	I	DS	B	Serial data clock (schmitt input)
4	NRST	I	DI	A	Reset input, Low active
5	N.C.	-	-	-	
6	DVSS		G		Ground(for digital)
7	VDD3V	I	G	E	reference voltage 3V & digital power supply
8	N.C	-	-	-	
9	N.C.	-	-	-	
10	AVSS		G		Ground(for analog)
11	N.C.	-	-	-	
12	VDD		G		analog power supply
13	CAP1P	I/O	AH	DH	external capacitor(for charge pomp)
14	N.C.	-	-	-	
15	N.C.	-	-	-	
16	CAP1N	I/O	AL	DL	external capacitor(for charge pomp)
17	DC_OUT	O	AH	C	DC/DC converter output
18	N.C.	-	-	-	
19	Bout	O	DO	C	OPEN-DRAIN output(blue)
20	Gout	O	DO	C	OPEN-DRAIN output(green)
21	Rout	O	DO	C	OPEN-DRAIN output(red)
22	N.C.	-	-	-	
23	N.C.	-	-	-	
24	PVSS		G		Ground(for OPEN DRAIN,DC/DC CONV.)
25	N.C.	-	-	-	
26	NSTBY	I	DI	A	Standby input, Low active
27	N.C.	-	-	-	
28	N.C.	-	-	-	

Type:

DI Digital input pin

DS Digital input pin(schmitt)

DO Digital output pin(OPEN-DRAIN)

AL Analog pin(Low voltage)

AH Analog pin(High voltage)

G Power supply or ground pin

3-3) I/O Circuit

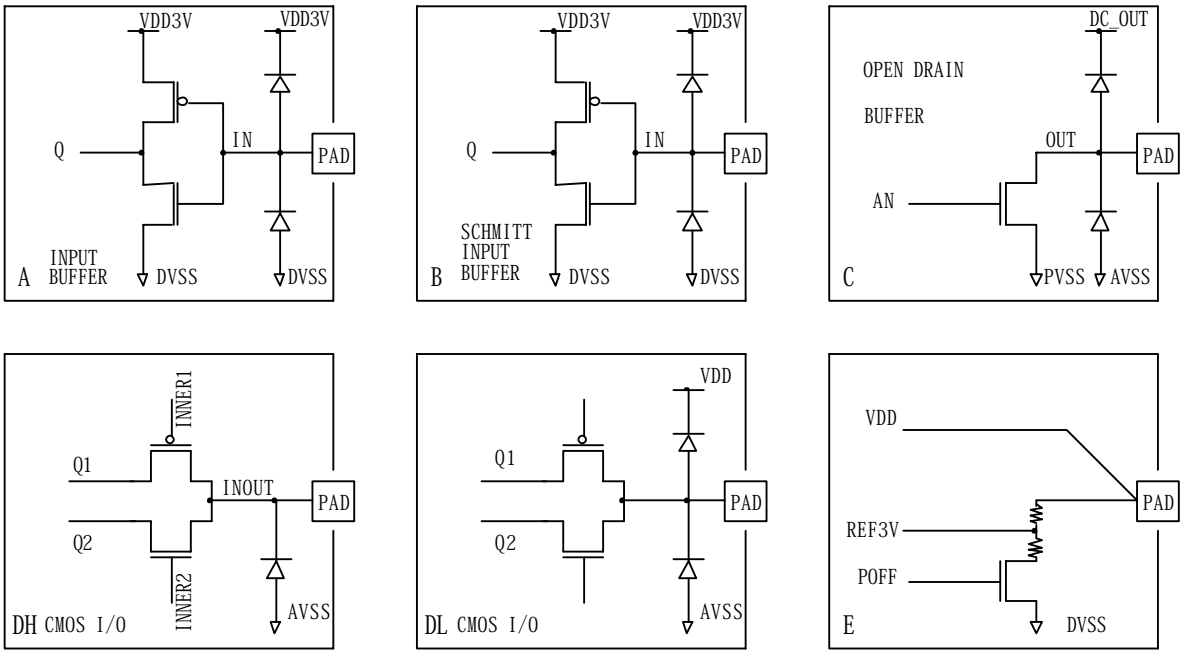


Fig. 4 I/O Circuit Figure

4 Pin Function

＜CPU Interface Block＞

Pin name	Active	Function	Note
NSTBY	L	Standby request input pin. "L": Standby mode "H": Normal function mode Built-in oscillator stops at standby mode. PWM output is OFF, and LED turns off the light. (Rout,Gout,Bout pin is Hi-Z) But, data from the CPU can be received.	You may store "0" in the Control register "DDSW" to make it standby condition. The initial value of the DDSW register is "0".
DATA	-	Serial data input pin from CPU.	see timing chart.
STRB	↑	Serial strobe input pin. Serial data is stored at positive edge of this pin.	
CLK	↑	Serial clock input pin. The conditions of the "DATA" are stored to the receiving buffer at every positive edge of this pin.	
NRST	L	Reset pin. It becomes reset condition if this terminal is made "L". And, it is returned in the normal condition if it is returned to "H".	It becomes standby condition after the thing during resetting and resetting.

＜PWM Control Block＞

Pin name	Initial	Function	Note
Rout Gout Bout	HiZ	PWM control data are outputted. Cathode side of LED is connected here.	See PWM control output wave shape
PVSS	-	Ground for Rout,Gout,Bout. It is connected to the ground level.	

＜DC/DC Converter Block＞

Pin name	Initial	Function	Note
CAP1P /CAP1N	-	The external capacitor for the DC/DC converter is connected. Don't connect anything except for the capacitor to this terminal.	See Electrical characteristics of analog
DC_OUT	-	The output terminal of the DC/DC converter. Prohibition of use under standby condition.	

5 Electrical Characteristics

5- 1)Absolute Maximum Ratings

DVSS=AVSS=PVSS=0V,Ta=25℃

Parameter	Symbol	Min	Max	Unit	Note
Maximum supply voltage	VDD	---	6.0	V	
Input voltage range	VIN	AVSS - 0.3	VDD + 0.3	V	
Power dissipation	Pd	---	※ 450	mW	
Operating temperature range	Ta	-30	+80	℃	
Storage temperature range	Tstg	-40	+125	℃	

※ Temperature dilating: 4.5mW/℃ when Ta>25℃

(with 70×70×1.6mm Glass epoxy substrate)

5- 2)Recommended Operating Conditions

Unless otherwise specified, VDD=3.60V,VDD3V=3.05V,Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power supply voltage	VDD	3.15	3.60	4.80	V	
Circuit current of VDD	IDDS	---	0.1	1	uA	Standby mode ※1
	IDDN	---	420	650	uA	Normal mode(No load)※2
	IDD1	---	82	120	mA	Normal mode(VDD=3.3V)※3
	IDD2	---	82	110	mA	Normal mode(VDD=4.2V)※3
Reference voltage	VDD3V	2.80	3.05	3.20	V	reference voltage 3V
Circuit current of VDD3V	IDD3V0	---	0.1	1	uA	Standby mode ※1
	IDD3V1	---	30	60.0	uA	Normal mode ※4

注1） Condition: NSTBY='L',DATA='L',STRB='L',CLK='L',NRST='H',IOUT=0mA

注2） Condition: NSTBY='H',DATA='L',STRB='L',CLK='L',NRST='H',IOUT=0mA and

Only a capacitor is connected to the DC_OUT terminal.(CAP_O)

注3） Condition: NSTBY='H',DATA='L',STRB='L',CLK='L',NRST='H',IOUT=40mA

注4） Condition: NSTBY='H',DATA='L',STRB='L',CLK='L',NRST='H',IOUT=0～40mA

5- 3)Electrical Characteristics of Digital DC

Unless otherwise specified, VDD=3.60V,VDD3V=3.05V,Ta=25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Relation Pin
Input high level 1	VIH1	VDD3V=3.05V	2.35	3.05	---	V	NSTBY,DATA,STRB,
Input low level 1	VIL1	DVSS=0V	---	0	0.70	V	NRST
Input high level 2	VIH2		2.75	3.05	---	V	CLK
Input low level 2	VIL2		---	0	0.30	V	
Hysteresis value	Vhys		---	0.50	---	V	※3
Input current (High level)	IIH	VIH=3V	---	---	1	uA	NSTBY,DATA,STRB, CLK,NRST
Input current (Low level)	IIL	VIL=0V	1	---	---	uA	
Input capacitance	Icap		---	4	---	pF	
Output low level	VOL	IOL=40mA	0.0	0.1	0.2	V	Rout,Gout,Bout ※1
VOL channel balance	dVOL	IOL=40mA	---	---	50	mV	
Leak current in Hi-Z	IOFF	VIH=5V	---	---	1	uA	
Maximum input current	IIMAX (IOL)		---	---	40	mA	
VOL Temperature fluctuation rate	DVOL	IOL=40mA	---	0.36	---	%/℃	
Total permissible current of OPEN-DRAIN Channels	IOMAX		---	---	70	mA	PVSS ※2

※1 Digital output is only OPEN-DRAIN type.

※2 The total curent of Rout,Gout,Bout never exceed 70mA.

※3 Hysteresis width is "0.5×VDD3V±Vhys",it is design value.(There is no test)

5- 4)Electrical Characteristics of Digital AC

Unless otherwise specified, VDD=3.60V,VDD3V=3.05V,Ta=25℃.

Parameter	Symbol	Pin	min	typ	max	Unit	Note
Rising transition time	tCKON	NSTBY,NRST,	---	---	50	nsec	Fig.5
Falling transition time	tCKOFF	CLK,STRB,DATA	---	---	50	nsec	
Clock frequency	fCK	CLK	---	1.8	2.0	MHz	Fig.6
Clock input high level time	tCKH		200	---	---	nsec	
Clock input low level time	tCKL		200	---	---	nsec	
DATA input setup time	tDIS	DATA	100	---	---	nsec	
DATA input hold time	tDIH		100	---	---	nsec	
CLK ? STRB input time	tSTBS	CLK-STRB	200	---	---	nsec	
STRB input high level time	tSTBH	STRB	100	---	---	nsec	
DATA input disable time	tDIDIS	DATA	250	---	---	nsec	
DATA input enable time	tDIEN	DATA	500	---	---	nsec	
Clock input setup time	tCKS	STRB-CLK	500	---	---	nsec	

5- 5)Timing Chart

<Input Wave Form Condition>

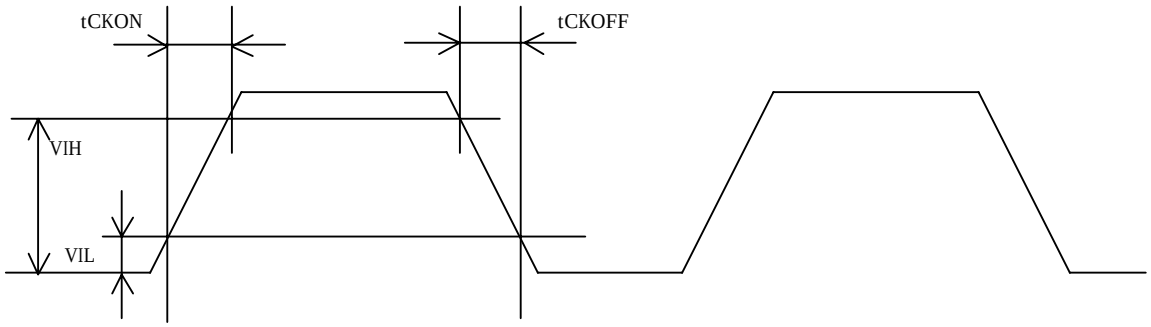


Fig. 5 Input Wave Form Condition

<CPU Interface Data Format>

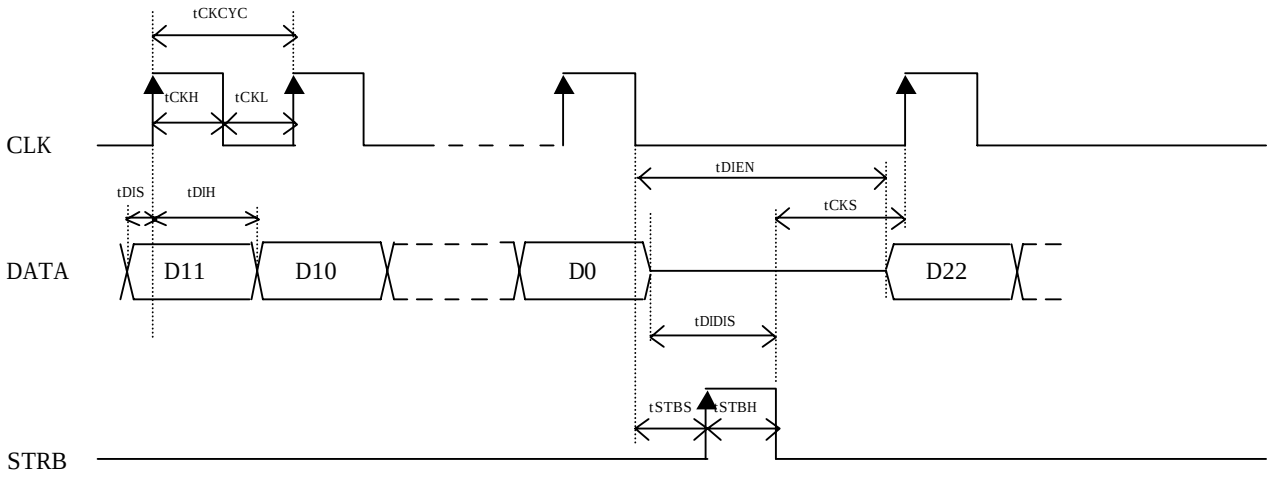
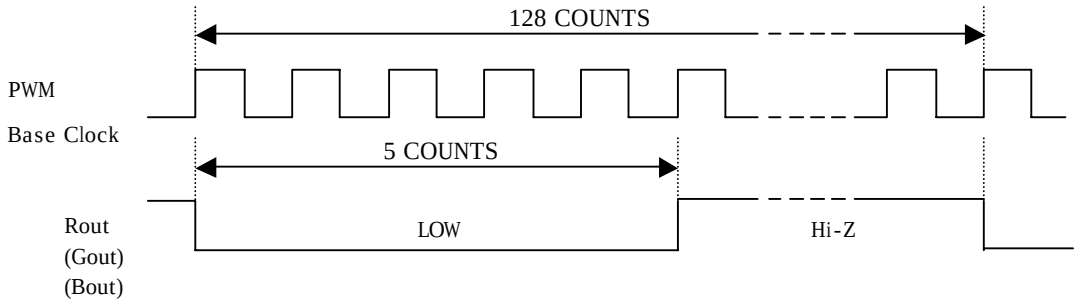


Fig. 6 CPU Interface Data Format

<LED PWM Control Output Format>



※ As for the example, PWM value is the case of Ron="0000000"(00H),Roff="0000101"(05H).

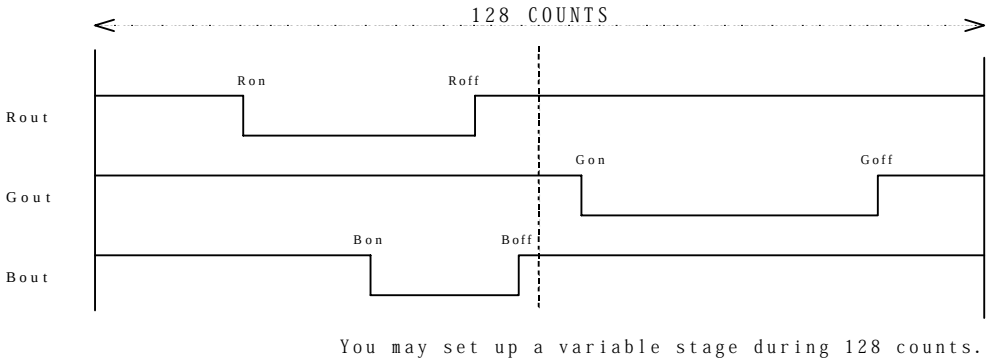


Fig. 7 PWM Control Output Wave Form

5- 6)Electrical Characteristics of Analog

Unless otherwise specified, VDD=3.60V,VDD3V=3.05V,Ta=25℃.

＜OSC Block＞

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Note
Output frequency	fout	---	525	700	875	kHz	

＜DC/DC Converter Block＞

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Note
Reference voltage input	VDD3V	VDD3V	2.80	3.05	3.20	V	Output voltage depends on this voltage.
Output voltage	VOUT	DC_OUT	1.574×VDD3V +10%,-5%			V	※1
Output current	IOUT		---	---	40	mA	VOUT=4.8V
Output turn-on delay time ※3	toh0		---	---	500	usec	IOUT=0mA
	toh		---	---	1000	usec	IOUT=40mA
Capacitor	CAP1	CAP1P, CAP1N	0.22±20%			uF	
	CAP_O	DC_OUT	4.7±20%			uF	
Switching frequency	Fosc	CAP1P, CAP1N	---	---	fout	kHz	※2

注1) Some examples of VOUT.

VDD3V=2.80V : VOUT=1.574×2.80=4.4072V

VDD3V=3.05V : VOUT=1.574×3.05=4.8007V

VDD3V=3.20V : VOUT=1.574×3.20=5.0368V

注2) Switching frequency depends on a load.

It is 1/n (n is an integer.) of the oscillator frequency.

Maximum frequency is fout[kHz].

注3) The time until DC_OUT output meets regulation value after standby condition is canceled.

5- 7)Attention for Use

Typical conditions are VDD=3.6V, VDD3V=3.05V, Ta=25℃.

＜The Ripple and Spike Voltage of DC_OUT＞

This IC is the DC/DC converter of charge pump type.

This is different from the regulator IC, and there is no series regulator circuit in the output.

This IC stabilizes an output voltage the "Up-Converting Time" by controlling it.

Therefore, ripples from charge pump circuit comes out to DC_OUT pin.

A ripple voltage is influenced by ESR of the capacitor (CAP_O) connected to the DC_OUT pin.

You should use the capacitor of the low ESR value to make a ripple voltage small.

And, if VDD becomes high, a ripple voltage becomes big, too.

A spike voltage is influenced by ESL of the capacitor (CAP_O).

You should use the capacitor of the low ESL value to make a spike voltage small.

Then, CAP_O is put near the IC, and it is important to reduce parasitic resistance and inductance.

You can make ripples and spikes voltage small with such work.

You can make ripples and spikes voltage smaller by composing LPF like an example in the DC_OUT output.

本 IC はチャージポンプ型の DC/DC コンバータです。
一般の電源用 IC とは異なり出力段にシリーズレギュレータ回路は無く、昇圧時間を制御することにより出力電圧を安定化しています。
よって DC_OUT 端子には IC 内部のチャージポンプ回路からのリップルが現れます。
リップル電圧は出力段のコンデンサ(以下 CAP_O)の等価直列抵抗成分(以下 ESR)が影響します。
リップル電圧幅を小さく抑えるためには低 ESR 値のコンデンサを使用する事をお奨めします。
なお、電源電圧(VDD)が高くなればリップル電圧幅も大きくなります。
スパイク電圧は CAP_O の等価直列インダクタンス成分(以下 ESL)が影響します。
スパイク電圧幅を小さく抑えるためには低 ESL 値のコンデンサを使用する事をお奨めします。
リップルとスパイク電圧幅を小さくするためには外付けコンデンサを IC の直近に配置して寄生の抵抗･インダクタンス成分を小さくする工夫をしてください。
また、DC_OUT 出力に LPF を構成するとさらにリップル･スパイク電圧幅を小さくすることができます。

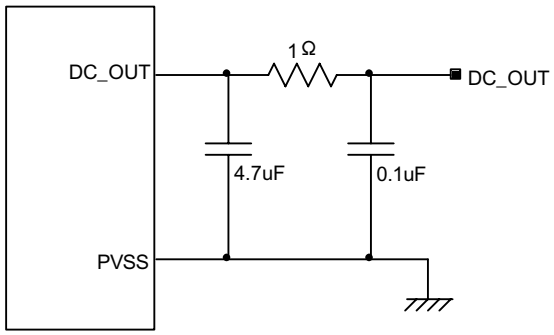


Fig. 8 LPF Composition Example

＜The Rush Current of VDD＞

Inflow electric current of VDD changes intermittently by the charge-pump state.

Charge-current flows into the capacitor(CAP1) in the charging cycle from VDD.

Therefore transitional rush current flows in the charging cycle.

Connect a high-performance bypass capacitor in the high frequency, because rush current is absorbed.

The capacitor of the high response and low ESR and ESL is effective as a bypass capacitor.

Recommendation value is given in the following. It is a ceramics capacitor together.

(See Fig2 Block diagram)

VDD-PVSS : 4.7uF

VDD3V-DVSS: 0.1uF

昇圧･充電時のスイッチング動作により VDD 端子への流入電流は断続的に変化します。
充電時には昇圧用コンデンサ(以下 CAP1)に VDD からの充電電流が発生します。
そのため動作開始時には過渡的に大きな電流(以下突入電流)が流れます。
電源ライン(VDD)には高周波特性の優れたバイパスコンデンサを接続してください。
コンデンサは ESR, ESL 値が低く応答性に優れたものを使用する事をお奨めします。
推奨値として VDD には 4.7uF 以上, VDD3V には 0.1uF 以上で、共にセラミックコンデンサです。
（図 2 ブロック図参照）

<Power On Sequence>

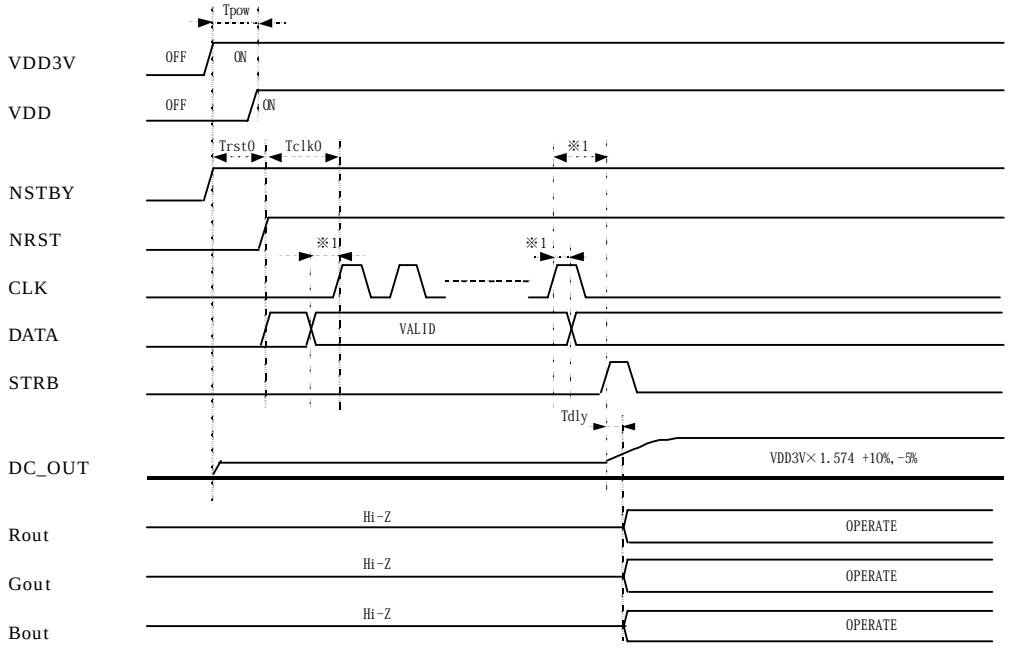
Typical timing diagram from POWER ON.(※1 See 5- 4)Electrical Characteristics of Digital AC)

Attention: Led may be illuminated momentarily when the riser of VDD3V is after VDD.

Because the power source of the control circuit is VDD3V.

下図は電源の立上げからの一例です。(図中 ※1 は 5- 4)Electrical Characteristics of Digital AC参照)

VDD3V の立ち上がりが VDD より遅れるとリセット(NRST='L')が認識されず LED が点灯する場合があります。



ITEM	SIMBOL	MIN	TYP	MAX	UNIT	NOTICE
VDD Delay	tpow	1	---	---	usec	
NRST Delay	Trst0	1	---	---	usec	
DATA Delay	Tclk0	200	---	---	nsec	
NSTBY Delay	Tstby0	0	---	---	sec	
DC/DC Wakeup Delay	Tdly	0	---	1/fout	msec	

6 Register Map

Serial data are 23 bits.

Address are lower 8 bits

Data are upper 15 bits.

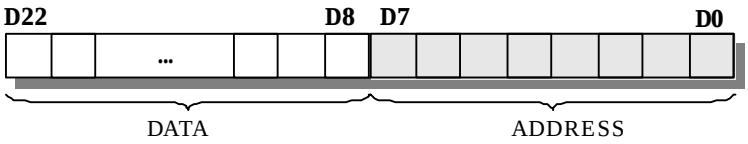
The upper line of the table is a register name.

And, the upper line of the table is a initial value.

ADDR	Parameter	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
ODH	Control Register	IC TEST MODE(Store necessarily '0')							CLK[3:0]				RSW	GSW	BSW	DDSW
		0000000							0000				0	0	0	0
2DH	PWM Red PWM setting of Rout	Ron[6:0]							*	Roff[6:0]						
		0000000							-	0000000						
4DH	PWM Green PWM setting of Gout	Gon[6:0]							*	Goff[6:0]						
		0000000							-	0000000						
6DH	PWM Blue PWM setting of Bout	Bon[6:0]							*	Boff[6:0]						
		0000000							-	0000000						

* :DON'T CARE

BIT STREAM



6-1)Control Register(ODH)

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7-0
0	0	0	0	0	0	0	CLK[3:0]				RSW	GSW	BSW	DDSW	00001101

* :DON'T CARE

D8:DDSW DC/DC Converter ON/OFF Control 0:OFF 1:ON

The condition of the built-in DC/DC converter is controlled by this bit.

When a '0' is stored in this bit, built-in oscillator stops, and becomes the standby mode.

D9:BSW Switch of blue LED 0:OFF 1:ON

PWM control is active by store of '1'.

Bout pin is always HI-Z by store of '0'.(PWM control is inactive)

D10:GSW Switch of Green LED 0:OFF 1:ON

PWM control is active by store of '1'.

Gout pin is always HI-Z by store of '0'.(PWM control is inactive)

D11:RSW Switch of Red LED 0:OFF 1:ON

PWM control is active by store of '1'.

Rout pin is always HI-Z by store of '0'.(PWM control is inactive)

D15-12:CLK[3:0]

Setting of count rate. 0000～1111:Ratio

'0000':Bypass mode(PWM Base Clock = OSC Clock)

'0001':1/2,'0010':1/4, ... '1111':1/32768

PWM Base Clock = OSC Clock/(2^CLK[3:0]) (See <LED PWM Control output format>)

D22-16:IC TEST MODE

Store necessarily '0' (Initial value is '0')

Initial Condition

D15	D14	D13	D12	D11	D10	D9	D8
0000				0	0	0	0

6-2)PWM Red(2DH)

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7-0
Ron[6:0]							*	Roff[6:0]							00101101

* :DON'T CARE

D22-16:Ron[6:0]

Red LED lighting position.

The position of lighting of the red LED is specified by the value of 0 - 127.

Ron=Roff: Always light on(Duty100%). Rsw=0: Lights-out

Ron>Roff: Illegal condition.(Never set up.)

D14-8:Roff[6:0]

Red LED lights-out position. (See Timing chart)

The position of lights-out of the red LED is specified by the value of 0 - 127.

Initial Condition

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
0000000							*	0000000						

* :DON'T CARE

6-3)PWM Green(4DH)

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7-0
Gon[6:0]							*	Goff[6:0]							01001101

* :DON'T CARE

D22-16:Gon[6:0]

Green LED lighting position.

The position of lighting of the green LED is specified by the value of 0 - 127.

Gon=Goff: Always light on(Duty100%). Gsw=0: Lights-out

Gon>Goff: Illegal condition.(Never set up.)

D14-8:Goff[6:0]

Green LED lights-out position. (See Timing chart)

The position of lights-out of the green LED is specified by the value of 0 - 127.

Initial Condition

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
0000000							*	0000000						

* :DON'T CARE

6-4)PWM Blue(6DH)

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7-0
Boff[6:0]							*	Bon[6:0]							01101101

* :DON'T CARE

D22-16:Bon[6:0]

Blue LED lighting position.

The position of lighting of the blue LED is specified by the value of 0 - 127.

Bon=Boff: Always light on(Duty100%). Bsw=0: Lights-out

Bon>Boff: Illegal condition.(Never set up.)

D14-8:Boff[6:0]

Blue LED lights-out position. (See Timing chart)

The position of lights-out of the blue LED is specified by the value of 0 - 127.

Initial Condition

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
0000000							*	0000000						

* :DON'T CARE