

SSM3K2615TU

1. Applications

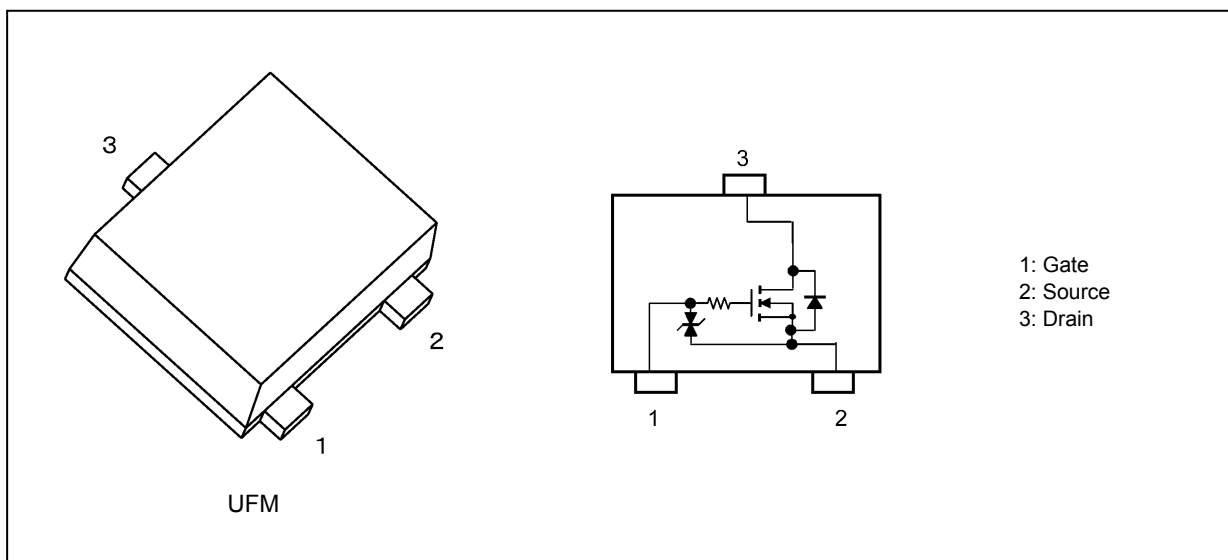
- Load Switches
- Motor Drivers

2. Features

- (1) AEC-Q101 Qualified (Note1).
- (2) 3.3-V gate drive voltage.
- (3) Low drain-source on-resistance
 - : $R_{DS(ON)} = 380 \text{ m}\Omega$ (typ.) (@ $V_{GS} = 3.3 \text{ V}$, $I_D = 0.5 \text{ A}$)
 - $R_{DS(ON)} = 330 \text{ m}\Omega$ (typ.) (@ $V_{GS} = 4.0 \text{ V}$, $I_D = 1.0 \text{ A}$)
 - $R_{DS(ON)} = 230 \text{ m}\Omega$ (typ.) (@ $V_{GS} = 10 \text{ V}$, $I_D = 1.0 \text{ A}$)

Note1: For detail information, please contact to our sales.

3. Packaging and Pin Assignment



Start of commercial production
2016-06

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Drain current (DC) (Note 1)	I_D	2	A
Drain current (pulsed) (Note 1), (Note 2)	I_{DP}	6	
Power dissipation (Note 3)	P_D	0.8	W
Power dissipation (t = 10 s) (Note 3)	P_D	1.6	
Channel temperature	T_{ch}	150	$^{\circ}\text{C}$
Single-pulse avalanche energy (Note 4)	E_{AS}	52.9	mJ
Avalanche current	I_{AR}	2	A
Storage temperature	T_{stg}	-55 to 150	$^{\circ}\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed $150\text{ }^{\circ}\text{C}$.

Note 2: Pulse width (PW) $\leq 10\text{ ms}$, duty $\leq 1\%$

Note 3: Device mounted on an FR4 board. (25.4 mm $\times$ 25.4 mm $\times$ 1.6 mm, Cu pad: 645 mm²)

Note 4: $V_{DD} = 25\text{ V}$, $T_{ch} = 25^{\circ}\text{C}$ (Initial state), $L = 20\text{ mH}$, $R_G = 25\Omega$, $I_{AR} = 2\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 16\text{ V}$	—	—	± 10	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	60	—	—	V
Gate threshold voltage (Note 1)	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	0.8	—	2.0	V
Drain-source on-resistance (Note 2)	$R_{DS(ON)}$	$I_D = 0.5\text{ A}$, $V_{GS} = 3.3\text{ V}$	—	0.38	0.58	Ω
		$I_D = 1.0\text{ A}$, $V_{GS} = 4.0\text{ V}$	—	0.33	0.44	
		$I_D = 1.0\text{ A}$, $V_{GS} = 10\text{ V}$	—	0.23	0.30	
Forward transfer admittance (Note 2)	$ Y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 1.0\text{ A}$	1.0	2.0	—	S

Note 1: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be below (1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.

Take this into consideration when using the device.

Note 2: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	150	—	pF
Reverse transfer capacitance	C_{rss}		—	25	—	
Output capacitance	C_{oss}		—	70	—	
Switching time (rise time)	t_r	$V_{DD} \approx 30\text{ V}$, $I_D = 1\text{ A}$ $V_{GS} = 0\text{ to }10\text{ V}$, $R_G = 50\text{ }\Omega$	—	25	—	ns
Switching time (turn-on time)	t_{on}		—	30	—	
Switching time (fall time)	t_f		—	50	—	
Switching time (turn-off time)	t_{off}		—	150	—	

5.3. Switching Time Test Circuit

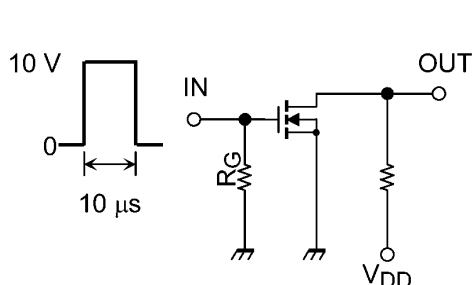


Fig. 5.3.1 Switching Time Test Circuit

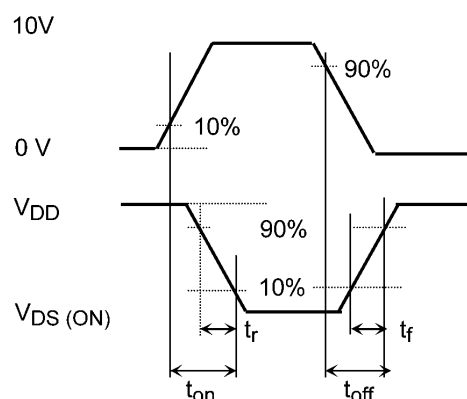


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 48\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 2.0\text{ A}$	—	6.0	—	nC
Gate-source charge 1	Q_{gs1}		—	0.5	—	
Gate-drain charge	Q_{gd}		—	1.4	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 1)	I_{DR}	—	—	—	2	A
Reverse drain current (pulsed) (Note 1)	I_{DRP}	—	—	—	6	A
Diode forward voltage (Note 2)	V_{DSF}	$I_D = -2.0\text{ A}$, $V_{GS} = 0\text{ V}$	—	-0.9	-1.5	V
Reverse recovery time	t_{rr}	$I_{DR} = 2\text{ A}$, $V_{GS} = 0\text{ V}$, $dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	100	—	ns
Reverse recovery charge	Q_{rr}		—	40	—	nC

Note 1: Ensure that the channel temperature does not exceed $150\text{ }^{\circ}\text{C}$.

Note 2: Pulse measurement.

6. Marking

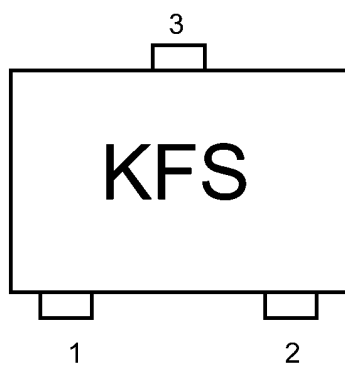


Fig. 6.1 Marking

7. Characteristics Curves (Note)

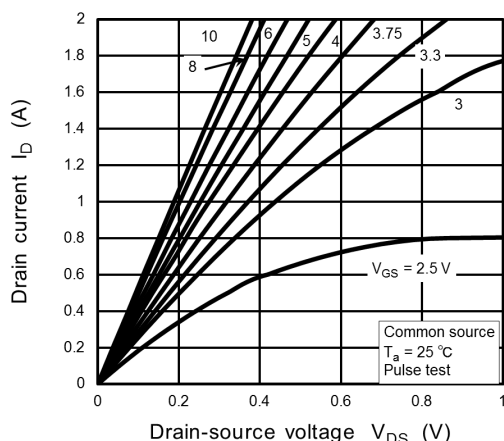


Fig. 7.1 $I_D - V_{DS}$

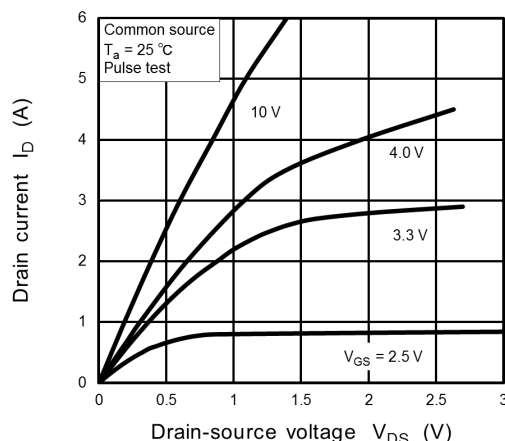


Fig. 7.2 $I_D - V_{DS}$

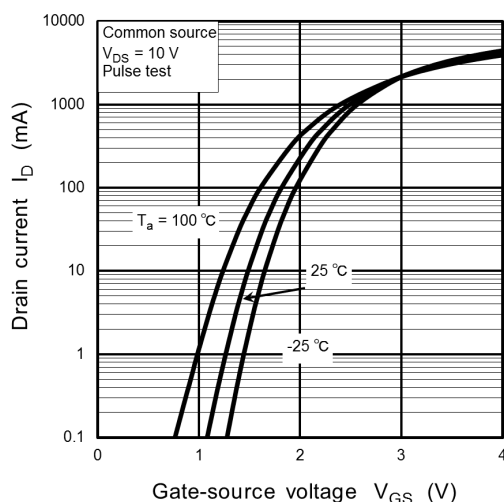


Fig. 7.3 $I_D - V_{GS}$

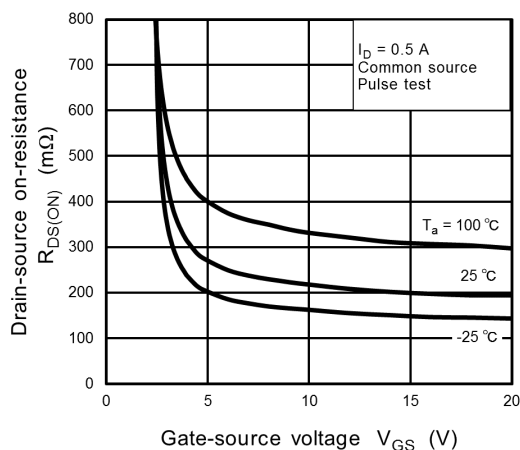


Fig. 7.4 $R_{DS(ON)} - V_{GS}$

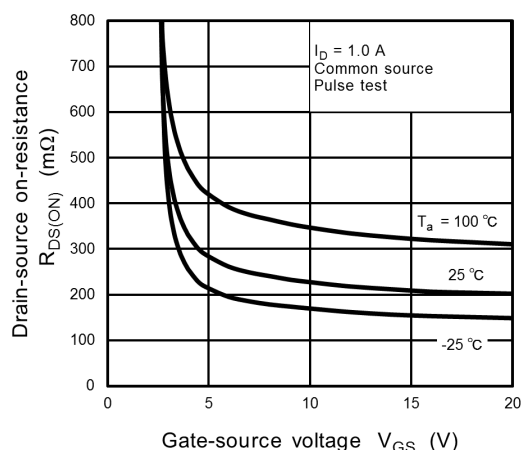


Fig. 7.5 $R_{DS(ON)} - V_{GS}$

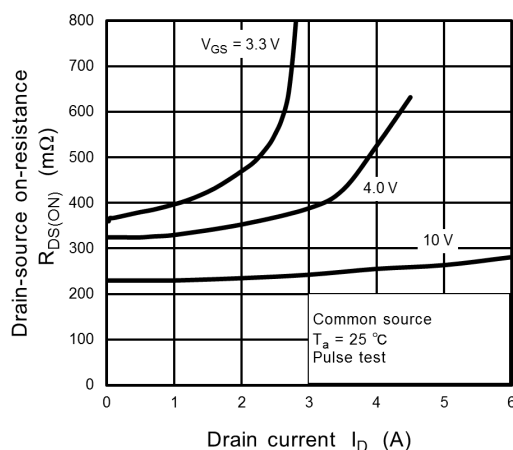


Fig. 7.6 $R_{DS(ON)} - I_D$

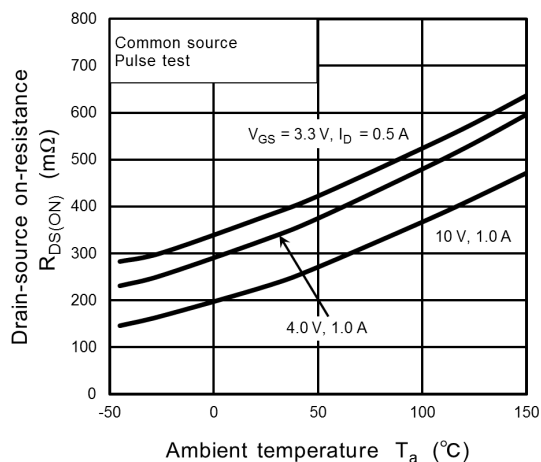


Fig. 7.7 $R_{DS(ON)} - T_a$

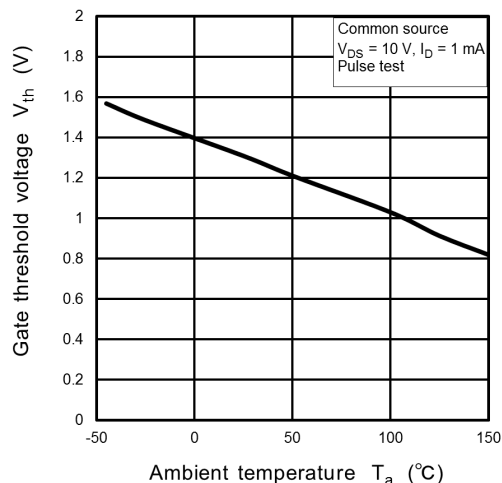


Fig. 7.8 $V_{th} - T_a$

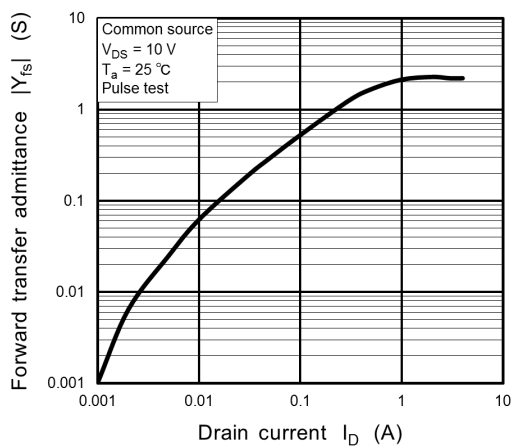


Fig. 7.9 $|Y_{fs}| - I_D$

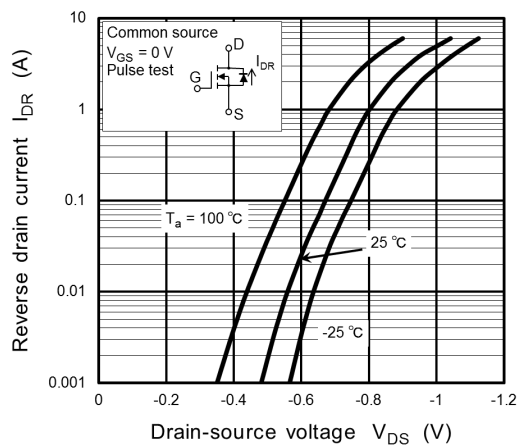


Fig. 7.10 $I_{DR} - V_{DS}$

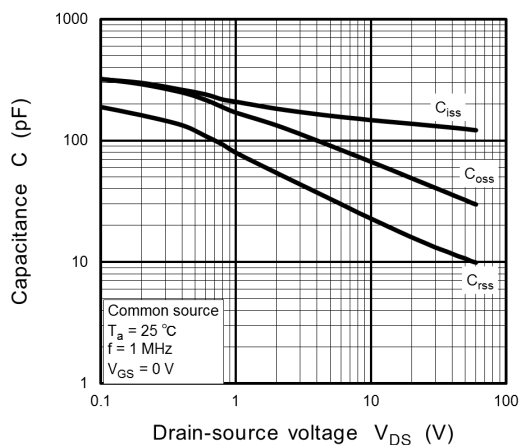


Fig. 7.11 $C - V_{DS}$

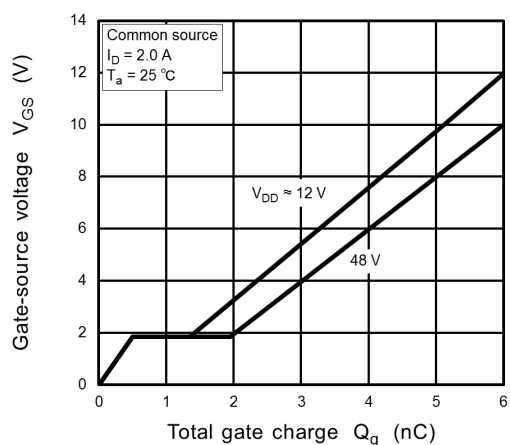


Fig. 7.12 Dynamic Input Characteristics

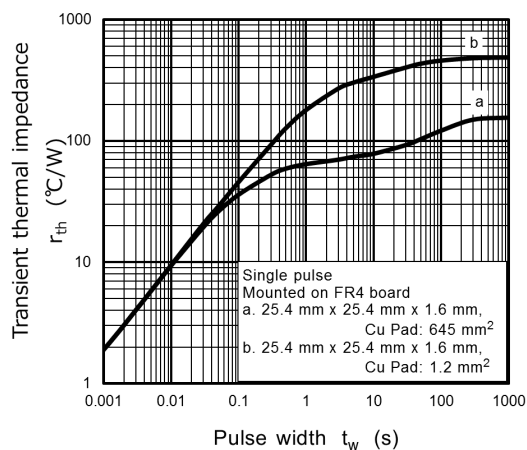


Fig. 7.13 $r_{th} - t_w$

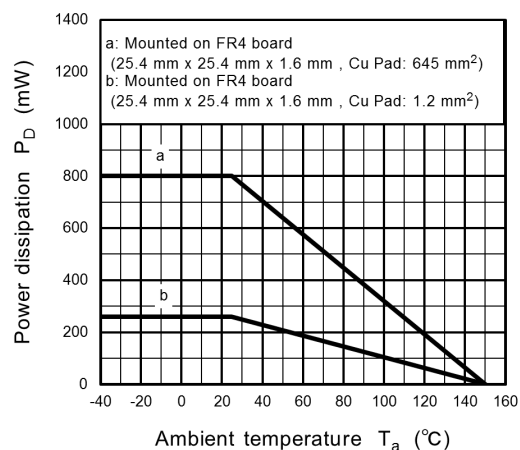


Fig. 7.14 $P_D - T_a$

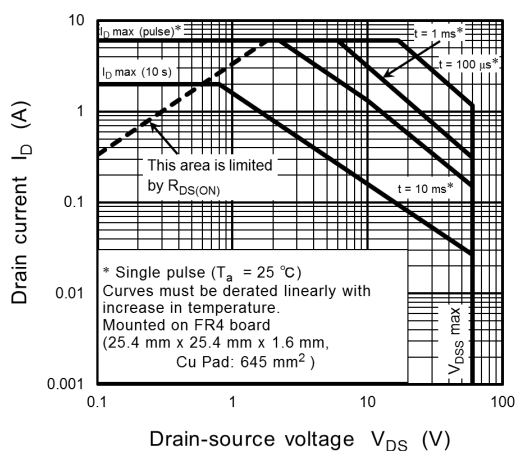


Fig. 7.15 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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