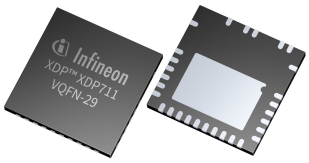
Wide input voltage range (7 V to 80 V) system monitoring and protection IC



RoHS

Halogen-free

Lead-free

Features

- Compatible with Infineon's OptiMOS™
- Compatible with Infineon's Linear FET and Linear FET2
- Tested with ISC035N10NM5LF2
- Wide input voltage range: 7 V to 80 V
- Transient withstand: up to 100 V for 500 ms
- Dedicated current and voltage ADCs: 12-bit
- Analog current and power monitor (AMON)
- Programmable and pre-set FET active SOA protection
- Variable pulse SOA control (Boost Mode)
- Integrated gate driver and charge pump for external n-channel MOSFET
- Configurable fast FET's shut down: two step turn-off or 1.5 A pull-down current
- Improved FET health monitoring
- Surge immunity protection
- PMBus interface: 1 MHz
- Precision input and output voltage monitoring and reporting: ≤ 0.4%
- Precision FET's current monitoring and reporting: ≤ 0.65% at full ADC range for 25 mV, 50 mV and 100 mV sense ranges
- Precision input power monitoring and reporting: ≤ 1.05% for 25 mV, 50 mV and 100 mV sense ranges
- Energy monitoring and reporting
- Programmable input and output OV and UV protections
- Support for external temperature sensor and OT protection
- Sequential turn-on capability
- 29-lead (6 mm x 6 mm) VQFN package
- -40°C to 125°C junction temperature

Potential applications

- Server and data center
- 24 V to 48 V Industrial systems
- Power distribution systems
- Intelligent e-fuse
- Network router and switches

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.

Description

XDP711 is a wide input voltage hot-swap and system monitoring controller IC that drives a single or multiple parallel n-channel MOSFETs. In addition to a controlled turn ON, XDP711 provides continuous system health monitoring and communication to the main MCU via PMBus interface. The high speed communication through PMBus allows system designers to disable the downstream sub-systems fully or partially.

It incorporates an extensive variety of system protections for safety operation and generates various protection responses depending on the severity of the incident. Latch off, reset, system shutdown and retry are some examples of response types. Its SOA protection effectively ensures that the system FET always operates under safe condition.

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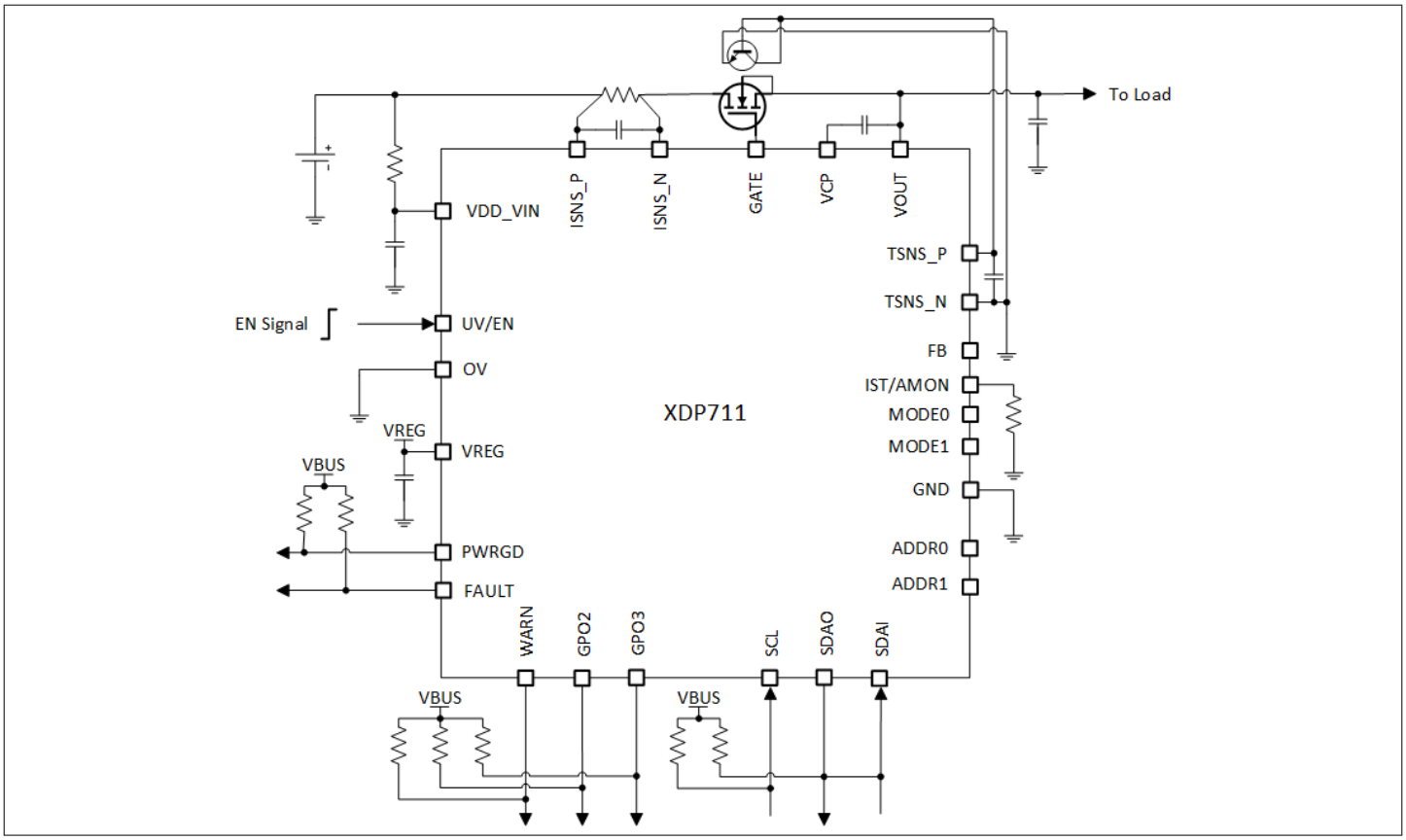

Type	Package	Marking
XDP711-001	PG-VQFN-29	XDP711-001

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1 Device comparison

Table 1 XDP7xx features comparison

Feature	XDP710-002	XDP711-001
Input voltage range	5.5 V - 80 V	7 V - 80 V
VDS fault	Not present	Present
Surge protection	Not present	Present
Hybrid mode	Not present	Present
AMON current and power monitor	Not present	Present
Pre-programmed FETs	–	Updated list with new FETs
OV fault hysteresis	Fixed	Configurable
Power telemetry averaging	Up to 128 samples	Up to 32768 samples
SOA current regulation offset	Not present	Present
Restart	Trigger via RESTART com mand only	Can be triggered via RESTART command or RESTARTN pin
Energy readings	8 bits rollover count	8 or 24 bits rollover count
CONFIG_ID	Not present	Present
Gate fast recovery	Present	Not present

Table 2 XDP7xx pins comparison

Pin number	XDP710-002	XDP711-001
10	GPO2/CGDN	GPO2/CGDN/RESTARTN: RESTARTN feature has been added to this pin
19	IST	IST/AMON: Pin can be configured either as IST or AMON
24	VOUT	VCP: Internal charge pump Voltage Reservoir Capacitor
25	SOURCE	SOURCE/VOUT: both functionalities are combined in a single pin

***Note**: Pins not listed in this table are the same in both devices.*

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2 Block Diagram

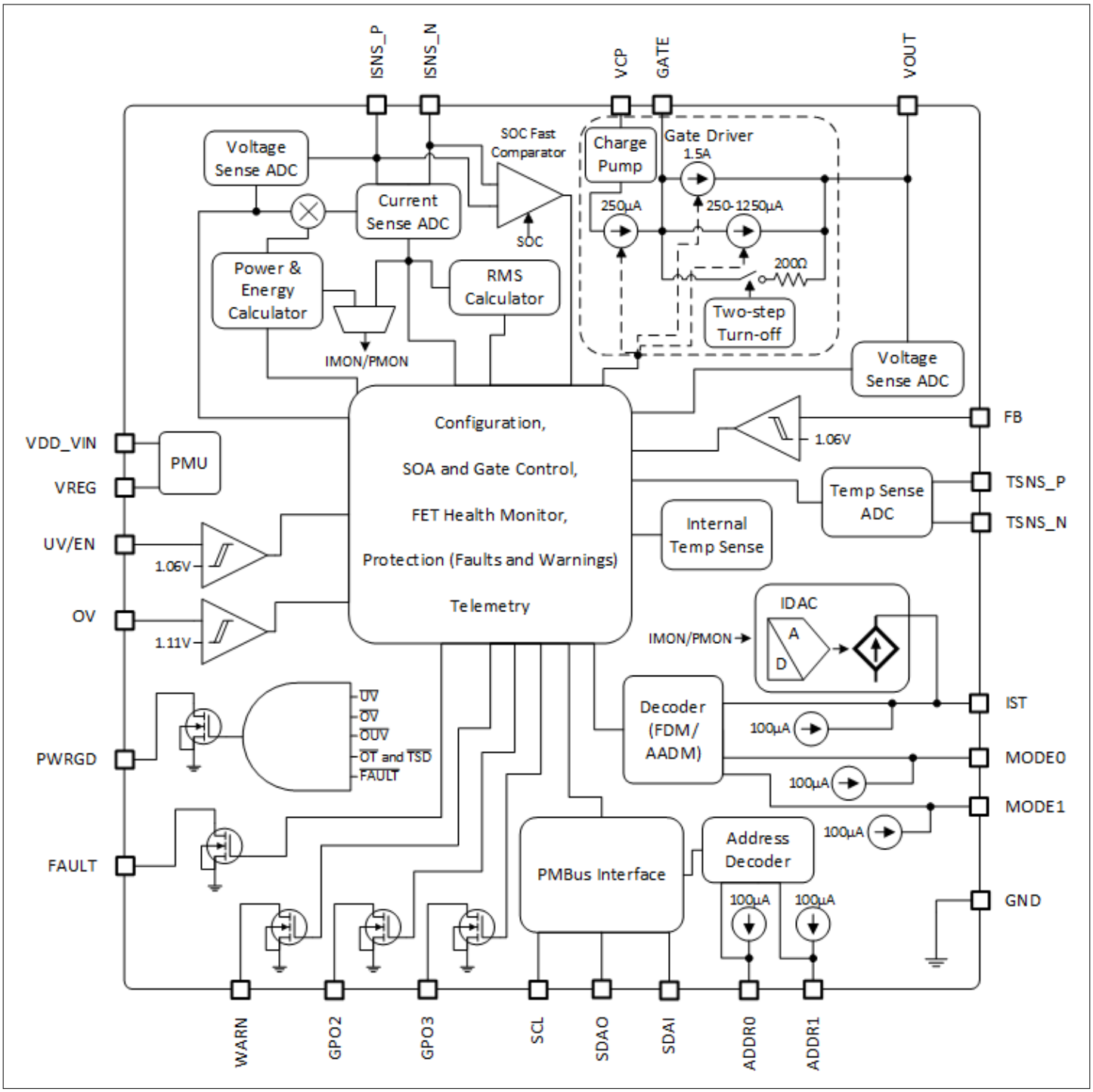

Figure 1 **XDP711 Block diagram**

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3 Pin configuration

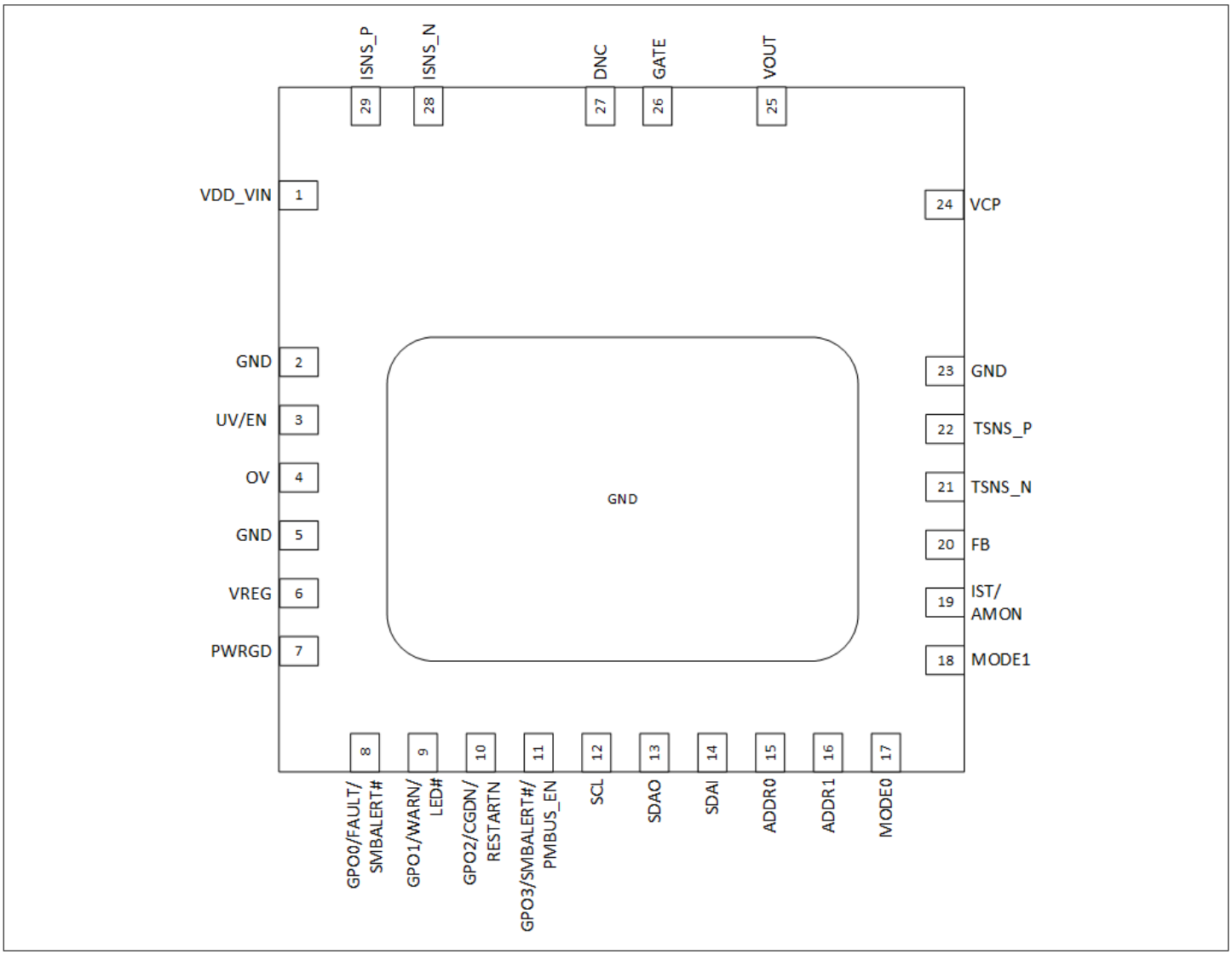

Figure 2 **VQFN-29 6x6 Pinout**

Table 3 **Pin definitions**

Pin #	Name	I/O	Type	Description	Connection if unused
1	VDD_VIN	–	P	**Power Supply** pin. A 100 nF capacitor from this pin to GND is strongly recommended.	VDD_VIN
2	GND	–	G	**Ground** reference. Internally connected to the exposed pad. To be connected externally to system ground	GND
3	UV/EN	I	A	**Undervoltage Detection/Enable** input. A voltage lower than lower threshold on this pin turns off the FET	VREG

(table continues...)

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Table 3 (continued) Pin definitions

Pin #	Name	I/O	Type	Description	Connection if unused
4	OV	I	A	**Overvoltage Detection** input. A voltage higher than upper threshold on this pin turns off the FET	GND
5	GND	–	G	**Ground** reference, to be connected to system ground	GND
6	VREG	–	P	**VREG** (internal 5V regulator) output. Connect a 1µF capacitor from this pin to GND	Connect a 1 µF capacitor from this pin to GND
7	PWRGD	O	D	**Power Good open drain** output. Pin is asserted when VOUT has reached its final level and steady state, FET is fully enhanced and no faults are detected. Its polarity is configurable	Open
8	GPO0/FAULT/ SMBALERT#	O	D	**General-Purpose Digital Output 0**. Pin configuration is programmable. **Fault open drain output** if configured. The pin asserts High/Low (programmable) when a fault occurs. The faults that can trigger the pin can be configured. **SMBALERT# open drain output** if configured, the pin asserts low when a fault or warning occurs (depending on configuration). The faults and warnings that can trigger the pin can be configured. **Default configuration:** FAULT.	Open
9	GPO1/ WARN/LED#	O	D	**General-Purpose Digital Output 1**. Pin configuration is programmable. **Warning open drain output** if configured. The pin asserts High/Low (programmable) when a warning occurs. The warnings that can trigger the pin can be configured. **LED# open drain output** if configured, the pin asserts low when a fault occurs. The faults that can trigger the pin can be configured. **Default configuration:** WARN.	Open

(table continues...)

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Table 3 (continued) Pin definitions

Pin #	Name	I/O	Type	Description	Connection if unused
10	GPO2/CGDN/ RESTARTN	I/O	D	**General-Purpose Digital Output 2**. Pin configuration is programmable. **Connector Good (CGDN)** if configured, if this pin is pulled externally low, the controller is allowed to turn on the FET. **RESTARTN:** Falling Edge Triggered Automatic Restart input (with internal pull-up resistor of 100kΩ) if configured. The FET remains off for 10 sec typ., and then powers back on **Default configuration:** Disabled.	Open
11	GPO3/ SMBALERT#/ PMBUS_EN	I/O	D	**General-Purpose Digital Output 3**. Pin configuration is programmable. **SMBALERT# open drain output** if configured, the pin asserts low when a fault or warning occurs (depending on configuration). The faults and warnings that can trigger the pin can be configured. **PMBUS_EN:** if configured, if this pin is pulled low externally then PMBus communication is disabled. **Default configuration:** Disabled.	Open
12	SCL	I	D	**PMBus Clock** input. The interface is rated to 1MHz	Pull-up to VREG or external source
13	SDAO	O	D	**PMBus Data Output**. Open drain pin. The serial data is split into an input and an output for easy use with isolators	Pull-up to VREG or external source
14	SDAI	I	D	**PMBus Data Input**. The serial data is split into an input and an output for easy use with isolators	Pull-up to VREG or external source
15	ADDR0	I	A	**Device Address Configuration 0 and 1** inputs. These pins can be tied to GND, left open or tied to GND through a resistor for a total of 16 unique PMBus device addresses	Open
16	ADDR1	I	A		
17	MODE0	I	A	**Mode of Operation 0 and 1** inputs. These pins can be tied to GND, left open or tied to GND through a resistor to select	Open

(table continues...)

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Table 3 (continued) Pin definitions

Pin #	Name	I/O	Type	Description	Connection if unused
18	MODE1	I	A	between Fully Digital Mode and Analog Assisted Digital Mode. Leave both pins open to select Fully Digital Mode	
19	IST/AMON	IO	A	**Start-up Current** setting input. A resistor to GND on this pin limits the maximum current allowed at start-up phase **Analog Monitor** output. Pin sources an analog current proportional to monitored FET current (IMON) or input power (PMON) level	Open
20	FB	I	A	**Output Voltage Feedback** input. A tap on the voltage divider placed from VOUT to GND is connected to this pin and sets the Output Under Voltage level. A voltage level lower than lower threshold will trigger the Output Under Voltage fault	VREG (ACM), Open (DCM)
21	TSNS_N	IO	A	**Temperature Sense Negative** terminal. Tie this pin to the emitter of an external NPN BJT to sense the FET's temperature. Connect a 1nF capacitor from this pin to TSNS_P. This pin must be connected locally to GND.	GND
22	TSNS_P	IO	A	**Temperature Sense Positive** terminal. Tie this pin to the base and collector of an external NPN BJT to sense the FET's temperature. Connect a 1nF capacitor from this pin to TSNS_N. If unused, this pin must be connected to GND.	GND
23	GND		G	**Ground** reference. Internally connected to the exposed pad. To be connected externally to system ground	GND
24	VCP	IO	A	Internal charge pump **Voltage Reservoir Capacitor** pin. Connect an external capacitor from this pin to VOUT pin to store energy required to support fast gate recovery. Ensure that the size of C_{VCP} is at least 10 times that of the parasitic gate capacitance	Open

(table continues...)

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Table 3 (continued) Pin definitions

Pin #	Name	I/O	Type	Description	Connection if unused
25	VOUT	IO	A	**Output Voltage Sense input and Source** terminal, single or multiple parallel external N channel FETs return path. Pin is directly connected to the source of the FET/FETs. The GATE pin is referenced from this pin and pull-down currents flow through this pin	SOURCE
26	GATE	O	A	**Gate Driver** output of single or multiple parallel external N channel FETs, referenced to VOUT. It uses a charge pump to provide a pull-up current to charge the FET gate/gates. The FET/FETs is/are regulated to a maximum allowed current by regulating the GATE pin voltage. GATE is pulled down when the supply is not within UV and OV or fault occurs	GATE
27	DNC	–	–	**Do not connect** pin to provide isolation between high and low voltage signals (GATE and ISNS_N). Corresponding copper pad on the PCB must be electrically isolated and appropriately spaced from other signals	Open
28	ISNS_N	I	A	**Current Sense Negative** input. A 100nF capacitor is recommended between the ISNS_x pins.	ISNS_N
29	ISNS_P	I	A	**Current Sense Positive** input	ISNS_P
EP	GND	–	G	**Ground** reference. The exposed pad to be connected to system ground	GND

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4 General Product Characteristics

4.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	VDD_VIN_{DC}	-0.3	–	80	V	–
Supply voltage transients at VDD_VIN pin	VDD_VIN_{AC}	–	–	100	V	For 500 ms max
Voltage slew rate at VDD_VIN pin	VDD_VIN_{SR}	–	–	80	V/µs	The RC filter (i.e. 10Ω/100nF, or 100Ω/10nF, etc.) on the pin is recommended, especially for high voltage (i.e. 48 V) applications
Voltage slew rate at ISNS_P and ISNS_N pins	$V_{ISNS_P_SR}$, $V_{ISNS_N_SR}$	–	–	80	V/µs	The resistor (i.e.10Ω) in series to each pin is recommended if an excessive dV/dt may occur in the application
Voltage slew rate at VOUT pin	V_{SOURCE_SR}, V_{OUT_SR}	–	–	80	V/µs	An output cap (10µF min) limits a slew rate on the pin
Output voltage at VCP pin	V_{VCP_DC}	-0.3	–	92	V	–
Voltage transients at VCP pin	V_{VCP_AC}	–	–	100	V	For 500ms max
VCP to VOUT voltage	$V_{VCP\text{-}VOUT_DC}$	-0.3	–	12	V	–
VCP to VOUT voltage transients	$V_{VCP\text{-}VOUT_AC}$	–	–	15	V	For 500 ms max
Output voltage at GATE pin	V_{GATE_DC}	-0.3	–	92	V	–
Voltage transients at GATE pin	V_{GATE_AC}	–	–	100	V	For 500 ms max
GATE to VOUT voltage	$V_{GATE\text{-}VOUT_DC}$	-0.3	–	12	V	–
GATE to VOUT voltage transients	$V_{GATE\text{-}VOUT_AC}$	–	–	15	V	For 500 ms max
Output voltage at VREG pin	V_{VREG}	-0.3	–	6	V	–
Digital pins output voltage (PWRGD, FAULT, WARN, GPOx, SDAO)	V_{PWRGD}, V_{FAULT}, V_{WARN}, V_{GPOx}, V_{SDAO}	-0.3	–	6	V	–

(table continues...)

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Table 4 (continued) Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage at VOUT pin	V_{OUT_DC}	-0.3	–	80	V	–
Input voltage transients at VOUT pin	V_{OUT_AC}	–	–	100	V	For 500 ms max
Input voltage at ISNS_P, ISNS_N pins	$V_{ISNS_P_DC}$, $V_{ISNS_N_DC}$	-0.3	–	80	V	–
Input voltage transients at ISNS_P, ISNS_N pins	$V_{ISNS_P_AC}$, $V_{ISNS_N_AC}$	–	–	100	V	For 500 ms max
Current sense input voltage (ISNS_P - ISNS_N)	$V_{\Delta ISNS}$	-0.8	–	0.8	V	–
Analog pins input voltage (UV/EN, OV, ADDRx, MODEx, IST, FB, TSNS_N)	V_{UV_EN}, V_{OV}, V_{ADDRx}, V_{MODEx}, V_{IST}, V_{FB}, V_{TSNS_N}	-0.3	–	6	V	–
Input voltage at TSNS_P pin	V_{TSNS_P}	-0.3	–	2.5	V	–
Digital pins input voltage (SCL, SDAI)	V_{SCL}, V_{SDAI}	-0.3	–	6	V	–
AMON pull-up voltage	V_{AMON}	–	–	3.3	V	–
Junction temperature range	T_J	-40	–	150	°C	–
Storage temperature range	T_S	-55	–	150	°C	–

4.2 Functional range

Table 5 Functional and performance ranges description

Absolute voltage range at VDD_VIN [V]	Communication Interface	FET Gate	VREG
$0 \le V_{in} < 7$	Off	Off (passive pull-down)	Off
$7 \le V_{in} < 9$	On	Limited operation: - Off (active pull-down); - limited SOA regulation depending on gate driver supply; - On/enhancement is not guaranteed (but ≥ 4.5 V)	4.5 V (min)
$9 \le V_{in} \le 80$		Full operation: - Off (active pull-down); - full SOA regulation; - On/enhancement (typ 10.5 V)	5.0 V (typ)

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Table 6 Functional range

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	VDD_VIN	7	–	80	V	–
Supply voltage at VDD_VIN pin to enable all features	VDD_VIN_{EN}	9	–	–	V	See Table 5
ISNS_P sense pin input voltage	V_{ISNS_P}	7	–	80	V	–
VOUT sense pin input voltage	V_{OUTS}	0	–	80	V	–
Current sense input voltage (ISNS_P - ISNS_N)	$V_{\Delta ISNS}$	-0.4	–	0.4	V	–
Minimum overcurrent setting	I_{OC_MIN}	5	–	–	A	Minimum I_{OC} ($I_{OC} = V_{SNS_CS}/R_{SNS}$, see Setting I_{OC}) for optimum stability
Analog pins input voltage (UV/EN, OV, ADDRx, MODEx, IST, FB)	V_{UV_EN}, V_{OV}, V_{ADDRx}, V_{MODEx}, V_{IST}, V_{FB}	0	–	5.5	V	–
Digital pins input voltage (SCL, SDAI)	V_{SCL}, V_{SDAI}	0	–	5.5	V	–
Output voltage at VREG pin	V_{VREG}	4.5	5	5.5	V	At 10 mA max external load
Digital pins output voltage (PWRGD, FAULT, WARN, GPOx, SDAO)	V_{PWRGD}, V_{FAULT}, V_{WARN}, V_{GPOx}, V_{SDAO}	0	–	5.5	V	–
Junction temperature range	T_J	-40	–	125	°C	–

4.3 Thermal characteristics

Table 7 PCB characteristics for thermal simulation

Parameter	Standard	λ_{therm} [W/m-K]
Metalization	JEDEC 2s2p (JESD 51-7, JESD 51-5)	388
Cooling area [mm^2]	none	388

Notes:

1. *Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.*
2. *This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to* www.jedec.org

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Table 8 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction-to-case (bottom)	$R_{\Theta JC_Bot}$	–	5	–	K/W	PCB simulation setup as described in Table 7
Thermal resistance junction-to-case (top)	$R_{\Theta JC_Top}$	–	30	–	K/W	PCB simulation setup as described in Table 7
Thermal resistance junction-to-ambient	$R_{\Theta JA}$	–	33	–	K/W	PCB simulation setup as described in Table 7
Package power dissipation	P_{PAK}	–	–	0.8	W	–

4.4 Current consumption

Table 9 Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption	I_{VDD}	–	7	10	mA	VDD_VIN supply current: FET is fully on, telemetry in on, AMON feature is disabled
Current consumption	I_{VDD}	–	9.5	12	mA	VDD_VIN supply current: FET is fully on, telemetry is on, AMON feature is enabled, voltage drop at the I_SNSx pins is close to CS_RNG

4.5 ESD robustness

Table 10 ESD robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness HBM	V_{ESD_HBM}	-1.5	–	1.5	kV	[1] Human body model sensitivity as per ANSI/ESDA/JEDEC JS-001
ESD robustness CDM	V_{ESD_CDM}	-500	–	500	V	Charged device model sensitivity as per ANSI/ESDA/JEDEC JS-002

1) 1.5 kV rating for all pins except VCP, which is rated for 1 kV

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4.6 Electrical characteristics

Table 11 Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UV/EN, OV and FB in AADM						
Input upper threshold	V_{UVEN_UTH}, V_{OV_UTH}, V_{FB_UTH}	1.09	1.11	1.13	V	–
Input lower threshold	V_{UVEN_LTH}, V_{OV_LTH}, V_{FB_LTH}	1.04	1.06	1.08	V	–
TSNS_P, TSNS_N						
TSNS_P operating voltage range	V_{TSNS_P}	0.25	–	1	V	–
TSNS_N operating voltage	V_{TSNS_N}	–	0	–	V	–
ISNS_P, ISNS_N						
Minimum detectable differential voltage level	V_{SNS_MIN}	0.01 * V_{SNS_CS}	–	–	mV	Between ISNS_P and ISNS_N pins
Current sense differential voltage range	V_{SNS_CS}	–	12.5	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 00
Current sense differential voltage range	V_{SNS_CS}	–	25	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 01
Current sense differential voltage range	V_{SNS_CS}	–	50	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 10
Current sense differential voltage range	V_{SNS_CS}	–	100	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 11
SOC differential voltage level	V_{SNS_SOC}	9.5	12.5	15.5	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 000 and CS_RNG[1:0] = 00 or 01
SOC differential voltage level	V_{SNS_SOC}	15.75	18.75	21.75	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 001 and CS_RNG[1:0] = 00 or 01
SOC differential voltage level	V_{SNS_SOC}	22	25	28	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 010 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 000 and CS_RNG[1:0] = 10 or 11

(table continues...)

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOC differential voltage level	V_{SNS_SOC}	34.5	37.5	40.5	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 011 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 001 and CS_RNG[1:0] = 10 or 11
SOC differential voltage level	V_{SNS_SOC}	47	50	53	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 100 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 010 and CS_RNG[1:0] = 10 or 11
SOC differential voltage level	V_{SNS_SOC}	71	75	79	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 101 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 011 and CS_RNG[1:0] = 10 or 11
SOC differential voltage level	V_{SNS_SOC}	96	100	104	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 110 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 100 and CS_RNG[1:0] = 10 or 11
SOC differential voltage level	V_{SNS_SOC}	145	150	155	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 111 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 101 and CS_RNG[1:0] = 10 or 11
SOC differential voltage level	V_{SNS_SOC}	193	200	207	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 110 and CS_RNG[1:0] = 10 or 11

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOC differential voltage level	V_{SNS_SOC}	290	300	310	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 111 and CS_RNG[1:0] = 10 or 11
Current sense ADC resolution		–	12	–	bits	–
Max allowed negative current	I_{NEG_MAX}	–	240	–	mA	To trigger I_{NEG} warning. V_{SNS_CS} = 12.5 mV, R_{SNS} = 1 mΩ
Max allowed negative current	I_{NEG_MAX}	–	520	–	mA	To trigger INEG warning. V_{SNS_CS} = 25 mV, R_{SNS} = 1 mΩ
Max allowed negative current	I_{NEG_MAX}	–	1100	–	mA	To trigger I_{NEG} warning. V_{SNS_CS} = 50 mV, R_{SNS} = 1 mΩ
Max allowed negative current	I_{NEG_MAX}	–	2200	–	mA	To trigger I_{NEG} warning. V_{SNS_CS} = 100 mV, R_{SNS} = 1 mΩ
GATE						
Gate voltage	V_{GATE}	8.5	10.5	12.0	V	9 V ≤ VDD_VIN ≤ 80 V, I_{GATE} ≤ 5 µA, FET is fully on
Gate voltage	V_{GATE}	4.0	–	–	V	7 V ≤ VDD_VIN < 9 V, I_{GATE} ≤ 5 µA
Pull-up current	I_{GATE_PU}	200	250	300	µA	At V_{GATE} = 5 V
Fast pull-down current	I_{GATE_FPD}	0.825	1.5	2.175	A	Set by GATE_FAST_PD[0]: GATE_FAST_PD[0] = 0
GATE pin two step turn-off fast pull-down	$R_{GATE_2ST_FAST_PD}$	156	200	244	Ω	Set by GATE_FAST_PD[0]: GATE_FAST_PD[0] = 1

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Slow pull-down current	I_{GATE_SPD}	200	250	300	µA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 00 Used for both regular/ slow pull-down and second phase of the two-step turn-off
Slow pull-down current	I_{GATE_SPD}	400	500	600	µA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 01 Used for both regular/ slow pull-down and second phase of the two-step turn-off
Slow pull-down current	I_{GATE_SPD}	600	750	900	µA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 10 Used for both regular/ slow pull-down and second phase of the two-step turn-off
Slow pull-down current	I_{GATE_SPD}	1000	1250	1500	µA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 11 Used for both regular/ slow pull-down and second phase of the two-step turn-off
VDD_VIN						
On-chip input overvoltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	70	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 00
On-chip input overvoltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	75	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 01
On-chip input overvoltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	80	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 10

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-chip input overvoltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	85	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 11
On-chip input overvoltage lower threshold for on-chip input overvoltage fault release	OV_{IN_LTH}	–	OV_{IN_UTH} – 5 V	–	V	For on-chip input overvoltage fault release
VOUT						
Input current	I_{VOUT}	–	15	–	µA	At 48 V
Telemetry						
Monitored voltage range (input and output voltages)	V_{TLM}	22	–	88	V	Set by VTLM_RNG[1:0] bits: • 2'b00: 88 V • 2'b01: 44 V • 2'b10: 22 V • 2'b11: n.a.
Input voltage measurements accuracy	–	-	±0.2	±0.3	%	At ISNS_P vs GND: ISNS_P = 20 V to 40 V or 10 V to 20 V depending on corresponding programmed range V_{TLM}
Output voltage measurements accuracy	–	-	±0.2	±0.3	%	At VOUT vs GND: VOUT = 20 V to 40 V or 10 V to 20 V depending on corresponding programmed range V_{TLM}
Input voltage measurements accuracy	–	–	±0.2	±0.4	%	At ISNS_P vs GND: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V
Output voltage measurements accuracy	–	–	±0.2	±0.4	%	At VOUT vs GND: V_{OUT} = 40 V to 80 V, V_{TLM} = 88 V
Current measurement accuracy	–	–	±0.15	±0.42	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 100 mV or 50 mV
Current measurement accuracy	–	–	±0.25	±0.66	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/2, where V_{SNS_CS} = 100 mV or 50 mV

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current measurement accuracy	–	–	±0.45	±1.2	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/4, where V_{SNS_CS} = 100 mV or 50 mV
Current measurement accuracy	–	–	±0.2	±0.65	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 25 mV
Current measurement accuracy	–	–	±0.4	±1.1	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/2, where V_{SNS_CS} = 25 mV
Current measurement accuracy	–	–	±0.8	±2.0	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/4, where V_{SNS_CS} = 25 mV
Current measurement accuracy	–	–	±0.45	±1.25	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
Current measurement accuracy	–	–	±0.9	±1.9	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/2, where V_{SNS_CS} = 12.5 mV
Current measurement accuracy	–	–	±1.8	±3.4	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS}$ = V_{SNS_CS}/4, where V_{SNS_CS} = 12.5 mV
Calculated input power accuracy	–	–	±0.35	±0.82	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 100 mV or 50 mV
Calculated input power accuracy	–	–	±0.4	±1.1	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 25 mV

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Calculated input power accuracy	–	–	±0.65	±1.7	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
Calculated energy accuracy	–	–	1.4	2.4	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 100 mV or 50 mV
Calculated energy accuracy	–	–	1.4	2.6	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 25 mV
Calculated energy accuracy		–	1.7	3.2	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P & ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
On-chip temperature monitored range	–	-40	–	150	°C	–
On-chip temperature measurement accuracy	–	-5	–	5	°C	–
Temperature measurements accuracy	–	–	±4.0	±12.5	°C	Sourcing currents in TSNS_P pin. Sense the voltage between TSNS_P and TSNS_N pins. External transistor is: MMBT3904

(table continues...)

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VREG						
Output voltage	V_{REG}	4.7	5.0	5.3	V	9 V ≤ VDD_VIN ≤ 80 V. C_{VREG} = 1 µF. Internal load + external load. Package maximum power dissipation limit (P_{PAK}) must not be violated
Output voltage	V_{REG}	4.5	–	–	V	7 V ≤ VDD_VIN ≤ 9 V. C_{VREG} = 1 µF. Internal load + external load. Package maximum power dissipation limit (P_{PAK}) must not be violated
Current capability to supply external load	I_{REG}	–	–	10	mA	–
PWRGD, GPOx, FAULT, WARN, SMBALERT#, CGDN, LED#, RESTARTN						
Output low voltage	V_{OL}	–	–	0.4	V	At 10 mA
Input low voltage	V_{IL}	–	–	0.8	V	–
Input high voltage	V_{IH}	2.0	–	–	V	–
Leakage current	I_{GPO_LEAK}	–	–	5	µA	At 5.5 V, output is HiZ
Current sink capability	I_{GPO_max}	–	–	10	mA	–
SDAI, SDAO, SCL						
Input high voltage	$V_{IN_COMM_H}$	2.0	–	–	V	–
Input low voltage	$V_{IN_COMM_L}$	–	–	0.8	V	–
Output low voltage	$V_{OUT_COMM_L}$	–	–	0.4	V	At 20 mA
Leakage current	I_{COMM_LEAK}	–	–	5.0	µA	At 5.5 V
Nominal bus voltage	V_{BUS}	3.0	3.3 or 5.0	5.5	V	–
Capacitive load per bus segment	C_{LOAD}	–	–	400	pF	–
Pin capacitance	C_{PIN}	–	5	10	pF	–
ADDRx						
Pin sense current	I_{ADDR}	–	100	–	µA	–
Programmability voltage step	V_{ADDR_STEP}	–	0.8	–	V	See Table 15 for more info

(table continues...)

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MODEx						
MODEx pins sense current	I_{MODE}	–	100	–	µA	–
Programmability voltage step	V_{MODE_STEP}	–	0.8	–	V	See Table 21
IST						
Pin sense current	I_{IST}	–	100	–	µA	–
Programmability voltage step	V_{IST_STEP}	–		–	V	See Table 21
On-chip thermal shut-down						
Protection trigger upper threshold	T_{TS_UTH}	130	–	145	°C	Set by ONCHIP_TSD_FAULT_LIMIT[1:0] bits: • 2'b00: 130°C • 2'b01: 135°C • 2'b10: 140°C • 2'b11: 145°C
Protection trigger lower threshold	T_{TS_LTH}	–	T_{TS_UTH} - 10	–	°C	–
On-chip thermal shut-down warning upper limit	$TSDW_{UTH}$	–	125	–	°C	–
On-chip thermal shut-down warning lower threshold	$TSDW_{LTH}$	–	115	–	°C	–
AMON						
IMON output level	I_{IMON}	–	2	–	mA	$V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV, 25 mV, 50 mV or 100 mV
IMON signal accuracy	$IMON_{ACC}$	–	–	5	%	$V_{\Delta ISNS}$ = 0.175 * V_{SNS_CS}, where V_{SNS_CS} = 25 mV, 50 mV or 100 mV
IMON signal accuracy	$IMON_{ACC}$	–	–	6	%	$V_{\Delta ISNS}$ = 0.175 * V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
IMON signal accuracy	$IMON_{ACC}$	–	–	3	%	$V_{\Delta ISNS}$ = 0.375 * V_{SNS_CS}, where V_{SNS_CS} = 25 mV, 50 mV or 100 mV
IMON signal accuracy	$IMON_{ACC}$	–	–	4	%	$V_{\Delta ISNS}$ = 0.375 * V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV

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Table 11 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IMON signal accuracy	$IMON_{ACC}$	–	–	2	%	$V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 25 mV, 50 mV or 100 mV
IMON signal accuracy	$IMON_{ACC}$	–	–	3	%	$V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
PMON signal accuracy	$PMON_{ACC}$	–	±1.9	±2.1	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P and ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 100 mV or 50 mV.
PMON signal accuracy	$PMON_{ACC}$	–	±1.9	±2.4	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P and ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 25 mV
PMON signal accuracy	$PMON_{ACC}$	–	±2.2	±3	%	At ISNS_P vs GND voltage: ISNS_P = 40 V to 80 V, V_{TLM} = 88 V. And voltage between ISNS_P and ISNS_N pins: $V_{\Delta ISNS}$ = V_{SNS_CS}, where V_{SNS_CS} = 12.5 mV
IMON/PMON compliance voltage	V_{CMPL}	3.0	3.3	3.6	V	–
Current DAC (IDAC) accuracy during analog PMON reporting	ε_{IDAC_PMON}	-1.5	–	1.5	%	IDAC accuracy on top of digital PMON accuracy

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4.7 Timing characteristics

Table 12 Timing characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UV/EN						
UV/EN input fixed deglitch time	t_{UVEN_DG}	6.5	10	13.5	µs	Input filter before processing the signal
UV/EN deglitch time on rising edge before start the FET	t_{UVEN_ON}	0	-	512	ms	Set by bits EN_DG[3:0]
OV						
OV input fixed deglitch time	t_{OV_DG}	6.5	10	13.5	µs	Input filter before processing the signal
FB						
FB input fixed deglitch time	t_{FB_DG}	6.5	10	13.5	µs	Input filter before processing the signal
PWRGD						
Power good assertion deglitch time	t_{PG_DGR}	0	–	15	ms	Configurable by means of PWRGD_DG_TMR[3:0] bits
Power good assertion deglitch time programming step	$t_{PG_DGR_STP}$	0.9	1.0	1.1	ms	–
Power good deassertion deglitch time	t_{PG_DGF}	0	–	15	ms	Configurable by means of PWRGDN_DG_TMR[3:0] bits
Power good deassertion deglitch time programming step	$t_{PG_DGF_STP}$	0.9	1.0	1.1	ms	–
ADC						
Conversion rate of current and voltage measurements	t_{ADC_IV}	–	102.4	–	µs	–
Conversion rate of temperature measurements	t_{ADC_t}	–	200	–	ms	–

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Table 12 (continued) Timing characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Faults, warnings and timers						
Time for any gate discharge in fault state	$t_{FLT_PD_GATE}$	9	10	11	ms	In FAULT state, when any gate pull down/discharge method is activated, a timer starts simultaneously. If FET's V_{GS} does not go below 1.04 V before this timer expires, SGD fault will be triggered
Fault strong pull down activation time for fast gate discharge	$t_{FLT_PD_FAST}$	13.5	15	16.5	µs	When strong/fast gate pull down is configured, the 1.5 A switch is activated for this time
Fault reaction time	$t_{FLT_GATE_OFF}$	–	0.3	1.0	µs	Response time from fault triggered to activation of gate pin turn-off. In the case of timer dependent faults, fault triggered means "after timer has expired"
FAULT pin hold time	t_{FAULT_MIN}	20	–	–	µs	Hold time of the FAULT signal when it is set Open-drain output: At C_L= 50 pF; External pull-up resistor of 10 kΩ
Hot swap retry cool down period	t_{COOL}	0	–	64	s	Set by bits COOLD_TMR[2:0]
Retry OK deglitch timer	t_{RETRY_DG}	0	–	8	s	Set by bits RETD_TMR[2:0]
First step power-down timer	t_{STEP1}	0	–	25575	ns	Set by GATE_PD_TMR[9:0]
UV timer	t_{UV}	0	–	1000	ms	Set by bits UV_TMR[2:0]
OV timer	t_{OV}	0	–	1000	ms	Set by OV_TMR[2:0] bits
OVin deglitch timer	t_{OV_DG}	0	–	1000	µs	Set by OVIN_TMR[2:0] bits
OVin detection time	t_{OVin_DET}	–	–	2.0	µs	–
OUV timer	t_{OUV}	0	–	1000	ms	Set by OUV_TMR[2:0] bits
Watchdog timer	$t_{WATCHDOG}$	5	–	15000	ms	Set by WATCHDOG[3:0] bits
OC/SOA deglitch timer	t_{SOAD}	0	–	10	ms	Set by SOAD_TMR[2:0] bits

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Table 12 (continued) Timing characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OC/SOA regulation timer	t_{SOAR}	0	–	1000	ms	Set by SOAR_TMR[2:0] bits
RMS current calculator integration time	t_{RMS_INT}	1.64	–	838.86	ms	Set by RMS_SAMPLE_TMR[1:0] bits
SOC fault digital deglitch timer	$t_{SOC_DIG_DG}$	0	–	1000	ms	Set by SOC_TMR[2:0] bits
SOC fault analog deglitch timer	$t_{SOC_ANA_DG}$	0	–	1000	ns	Set by SOC_DG_TMR[1:0] bits
Boost mode						
Boost pulse timer	t_{BOOST_PULSE}	0.1	–	1	ms	Set by BOOSTMODE_TMR[0]
Boost mode duty cycle	t_{BOOST_DC}	2	–	50	%	Set by BOOSTMODE_DC[2:0] bits.
PMBus						
Clock frequency	f_{SCL}	10	–	1000	kHz	–
Detect clock low timeout	$t_{TIMEOUT}$	25	–	35	ms	–
Bus free time between STOP and START condition	t_{BUF}	0.5	–	–	µs	See Figure 11
Hold time after (REPEATED) START condition	t_{HD_STA}	0.26	–	–	µs	After this period, the first clock is generated. See Figure 11
REPEATED START condition setup time	t_{SU_STA}	0.26	–	–	µs	See Figure 11
STOP condition setup time	t_{SU_STO}	0.26	–	–	µs	See Figure 11
Data hold time	t_{HD_DAT}	0	–	–	ns	See Figure 11
Data setup time	t_{SU_DAT}	50	–	–	ns	See Figure 11
Clock low period	t_{LOW}	0.5	–	–	µs	See Figure 11
Clock high period	t_{HIGH}	0.26	–	50	µs	See Figure 11
Clock/data fall time	t_F	–	–	120	ns	The fall time measurement limits are defined as follows: Fall time limits: ($V_{IH,MIN}$ + 0.15 V) to ($V_{IL,MAX}$ - 0.15 V) See Figure 11

(table continues...)

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Table 12 (continued) Timing characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, $V_{\Delta ISNS}$ = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J= −40°C to +125°C, unless otherwise noted

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock/data rise time	t_R	–	–	120	ns	The rise time measurement limits are defined as follows: Rise time limits: ($V_{IL,MAX}$ - 0.15 V) to ($V_{IH,MIN}$ + 0.15 V) See Figure 11
PMBus deglitch time	t_{DGL_PMBUS}	50	–	–	ns	–
AMON						
IMON signal time constant	t_{IMON}	2.9	–	4.0	µs	–
IMON signal delay	t_{DEL_IMON}	–	–	5	µs	Tested with a load step from 0% to 100% and a di/dt of 10 A/µs

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5 Product Features

5.1 Functional Description

5.1.1 Modes of Operation

Fully Digital Mode (FDM)

This mode is recognized by keeping MODE0 and 1 pins open. In this mode, FET to be used can be selected by means of the FET_SELECT bits in the MODE PMBus command or a FET SOA can be programmed accurately in the SOA PMBus command so that controller effectively protects FET from going out of SOA. For pre-programmed FETs, there are two different SOA options to select from: DC line and half DC line. The programmed SOA line will be used for both INIT_SOA_REG and I_REG regulation described in Chapter 5.1.2. Other lines can be selected or programmed manually if desired by means of the SOA programmable section of the OTP memory.

If desired, analog comparators at the OV, FB and UV/EN pins, which have a faster response than digital comparators, can be used for OV and UV protection. This is specified by clearing the MODE bit in the MODE PMBus command, which selects the analog comparators mode (ACM).

Digital comparators can be used by leaving the MODE bit to its default (digital comparators mode, DCM). All other XDP711 features like voltage and current faults and warnings limits and timers can be programmed digitally too, including the IST limit, which is set in the START_ILIM bits in the I_SNS_CFG PMBus command. This reduces the amount of external components, as shown in Figure 30. If the MODE bit is left to its default value of 1, UV/EN pin does not have a UV fault functionality, but it's only used to enable or disable the device.

The PMBus address can be set at ADDR1 and ADDR0 (see Table 15) pins by keeping them open or tying to GND directly or via external resistors, or in PMBUS_CFG command. If PMBUS_CFG command is used for programming the address, different addresses can be programmed in multiple devices connected to a single bus by means of the PMBus enable feature mapped onto GPO3.

Analog Assisted Digital Mode (AADM)

Use simple analog programming at MODE0 and 1 pins for selecting the pre-programmed configurations for controlled FETs. FET can be selected by tying these pins through a resistor to GND.

MODE bit in MODE command is ignored in AADM. In this case, OV, OUV and UV faults limits are set via voltage dividers at the OV, FB and UV/EN pins respectively. Voltages are sensed via analog comparators at the corresponding pins. Warnings are disabled by default, unless they are enabled and programmed digitally.

The Current Sense Range (V_{SNS_CS}) and IST limit can be set by means of a resistor at the IST pin as shown in Table 21, therefore the CS_RNG and START_ILIM bits in I_SNS_CFG PMBus command are ignored.

The PMBus address shall be set at ADDR1 and ADDR0 (see Table 15) pins by keeping them open or tying to GND directly or via external resistors.

Hybrid Mode

Hybrid mode is a sub-mode of FDM to support surge immunity feature. In this mode, detection of OUV fault is done by the analog comparator in the FB pin (as in AADM), while UV and OV faults are detected digitally as in FDM. This mode is selected by setting both MODE and FB_COMP_SEL bits in MODE PMBus command.

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Table 13 Modes of operation

Mode of operation	MODEx pins	MODE bit	FB_COMP_SEL	Device address	FET selection	OV/UV detection	OUV detection	IST
FDM	Open	1	0	Set by means of ADDRx pins or PMBUS_CFG command	Selected by means of FET_SELECT bits	Digital Comparators Mode (DCM)		Set by means of START_ILIM bits
		0	X			Analog Comparators Mode (ACM)		
AADM	Resistor to GND	X	X	Set by means of ADDRx pins or PMBUS_CFG command	Selected by means of MODEx pins	Analog Comparators Mode (ACM)Analog Comparators Mode (ACM)		Set by means of IST pin
Hybrid mode	Open	1	1	Set by means of ADDRx pins or PMBUS_CFG command	Selected by means of FET_SELECT bits	Digital Comparators Mode (DCM)	Analog Comparators Mode (ACM)	Set by means of START_ILIM bits

Configuration of MODE1/0 Pins

Setting the voltage level (between 0.8 V and 2.4 V) at MODE1 and MODE0 pins shall be done using external resistors (see Setting the voltage at MODE1/0 pins in AADM).

Table 14 Configuration of MODE1/0 pins

MODE1 pin voltage [V]	MODE1 pin resistance [kΩ]	MODE0 pin voltage [V]	MODE0 pin resistance [kΩ]	FET selection
MODE1 < 0.8	GND	MODE0 < 0.8	GND	BSC027N10NS5ATMA1
MODE1 < 0.8	GND	0.8 ≤ MODE0 < 1.6	12	ISC022N10NM6
MODE1 < 0.8	GND	1.6 ≤ MODE0 < 2.4	20	ISC027N10NM6
MODE1 < 0.8	GND	MODE0 ≥ 2.4	Open	IPTG011N08NM5
0.8 ≤ MODE1 < 1.6	12	MODE0 < 0.8	GND	IPTC012N08NM5
0.8 ≤ MODE1 < 1.6	12	0.8 ≤ MODE0 < 1.6	12	IPB017N10N5LFATMA1
0.8 ≤ MODE1 < 1.6	12	1.6 ≤ MODE0 < 2.4	20	ISC025N08NM5LF2
0.8 ≤ MODE1 < 1.6	12	MODE0 ≥ 2.4	Open	ISC035N10NM5LF2
1.6 ≤ MODE1 < 2.4	20	MODE0 < 0.8	GND	IPTG014N10NM5
1.6 ≤ MODE1 < 2.4	20	0.8 ≤ MODE0 < 1.6	12	IPTC015N10NM5

(table continues...)

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Table 14 (continued) Configuration of MODE1/0 pins

MODE1 pin voltage [V]	MODE1 pin resistance [kΩ]	MODE0 pin voltage [V]	MODE0 pin resistance [kΩ]	FET selection
1.6 ≤ MODE1 < 2.4	20	1.6 ≤ MODE0 < 2.4	20	IPT015N10N5ATMA1
1.6 ≤ MODE1 < 2.4	20	MODE0 ≥ 2.4	Open	IPB017N10N5ATMA1
MODE1 ≥ 2.4	Open	MODE0 < 0.8	GND	IPB018N10NM6
MODE1 ≥ 2.4	Open	0.8 ≤ MODE0 < 1.6	12	ISC030N10NM6
MODE1 ≥ 2.4	Open	1.6 ≤ MODE0 < 2.4	20	IPB020N10N5ATMA1
MODE1 ≥ 2.4	Open	MODE0 ≥ 2.4	Open	FET_SELECT (ROM or OTP)

Configuration of ADDR1/0 Pins

These pins can be tied to GND, left floating or tied low through a resistor for a total of 16 unique PMBus device addresses according to Table 15.

Setting the voltage level (between 0.8 V and 2.4 V) at ADDR1 and ADDR0 pins shall be done using external resistors (see Setting the voltage at ADDR1/0 pins). If more addresses are required, the base address can be modified using the PMBUS_CFG command.

Table 15 Configuration of ADDR1/0 pins

ADDR1 pin voltage [V]	ADDR1 pin resistance [kΩ]	ADDR0 pin voltage [V]	ADDR0 pin resistance [kΩ]	Base address field [6:4]	Device address field [3:0]
ADDR1 < 0.8	GND	ADDR0 < 0.8	GND	As configured in PMBUS_CFG command. Default = 001	0000
ADDR1 < 0.8	GND	0.8 ≤ ADDR0 < 1.6	12		0001
ADDR1 < 0.8	GND	1.6 ≤ ADDR0 < 2.4	20		0010
ADDR1 < 0.8	GND	ADDR0 ≥ 2.4	Open		0011
0.8 ≤ ADDR1 < 1.6	12	ADDR0 < 0.8	GND		0100
0.8 ≤ ADDR1 < 1.6	12	0.8 ≤ ADDR0 < 1.6	12		0101
0.8 ≤ ADDR1 < 1.6	12	1.6 ≤ ADDR0 < 2.4	20		0110
0.8 ≤ ADDR1 < 1.6	12	ADDR0 ≥ 2.4	Open		0111
1.6 ≤ ADDR1 < 2.4	20	ADDR0 < 0.8	GND		1000
1.6 ≤ ADDR1 < 2.4	20	0.8 ≤ ADDR0 < 1.6	12		1001
1.6 ≤ ADDR1 < 2.4	20	1.6 ≤ ADDR0 < 2.4	20		1010
1.6 ≤ ADDR1 < 2.4	20	ADDR0 ≥ 2.4	Open		1011
ADDR1 ≥ 2.4	Open	ADDR0 < 0.8	GND		1100
ADDR1 ≥ 2.4	Open	0.8 ≤ ADDR0 < 1.6	12		1101
ADDR1 ≥ 2.4	Open	1.6 ≤ ADDR0 < 2.4	20		1110
ADDR1 ≥ 2.4	Open	ADDR0 ≥ 2.4	Open		Program in OTP (PMBUS_CFG)

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5.1.2 Operational states

Table 16 Operational states

	State	Name	Description	Next state No fault	Next state fault
Initialization	0	POR_INIT	Internal circuitry is initialized as soon as VDD_VIN > 7 V.	READ_CFG	NA
	1	READ_CFG	POR and initialization complete. OTP and external pins configuration are read at this point.	CHK_FET	NA
Power-up procedure	2	CHK_FET	Controller checks FET for drain to source or gate to drain shorts.	STANDBY	FAULT
	3	STANDBY	Controller checks that VDD_VIN is within a valid range (within UV and OV), device temperature is in appropriate range and EN signal is deasserted or ON bit in OPERATION command is cleared. Before going out of STANDBY and into INIT_SOA_REG state, XDP711 checks the input voltage level according to OV, UV and OVin limits (with corresponding hystereses). If it's out of range, it will go to FAULT state.	INIT_SOA_REG	FAULT
Power-up procedure	4	INIT_SOA_REG	EN signal is asserted and ON bit in OPERATION command is set. Turn-on Watchdog timer starts running. SOA regulation phase: Controller regulates the current according to the programmed SOA (see section Current Limit During Operation for more info), depending on VDS value in order to charge the output capacitor. INIT_SOA_REG phase stops when FET V_{DS} < 1.0 V, V_{GS} > 7.8 V and no faults are detected during this procedure. Due to the current regulation nature of the Power-up algorithm, start-up time depends on the output capacitance.	ON	FAULT
Normal operation	5	ON	Normal operation phase starts. FET is fully enhanced. Current regulation can start again if OC is detected or FET SOA is violated if SOAR_TMR is enabled. Watchdog reset procedure starts at this point.	ON, I_REG or WAIT_10S	FAULT

(table continues...)

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Table 16 (continued) Operational states

	State	Name	Description	Next state No fault	Next state fault
Normal operation	6	I_REG	If I_{OC} level is exceeded or programmed FET SOA limits are violated, SOAD_TMR timer will start. If condition persists after SOAD_TMR timer expires, the SOA regulation timer SOAR_TMR starts and FET's current will be regulated at I_{OC} or FET SOA level by lowering FET VGS.	ON or WAIT_10S	FAULT
Idle	7	FAULT	Fault that turns off the FET has occurred. System will stay idle in FAULT state until: a) Fault conditions are cleared in the case of non-retry dependent faults. b) Cool down timer expires in the case of retry dependent faults. If retry counter has expired, system will go to LATCH_OFF state directly after FAULT.	CHK_FET/STANDBY or LATCH_OFF	NA
Idle	8	LATCH_OFF	If the maximum number of retries has been reached, system will latch off until faults are cleared and restart has been issued (power cycling or PMBus command).	POR_INIT (power cycling) or CHK_FET (PMBus command) or LATCH_OFF	NA
Idle	9	MEM_FAULT	If an OTP read or write error is detected, XDP711 will go to FAULT and consecutively MEM_FAULT state, which initiates controller's latch-off. A power cycle is required in order to go out of MEM_FAULT.	POR_INIT (power cycling)	NA
	10	WAIT_10S	A RESTART command has been issued. XDP711 turns off the FET and stays in this state for 10 seconds. After this time, system goes to STANDBY and, if the necessary conditions are met, FET is automatically turned back on, going to ON state.	STANDBY	NA
	11	SURGE	Wait in this state for 15µs	GREC1	FAULT

(table continues...)

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Table 16 (continued) Operational states

	State	Name	Description	Next state No fault	Next state fault
Idle	12	GREC1	Gate boosting phase: gate is pulled up fast. The phase is over when the voltage drop at the current sense resistor reaches 12.5mV level (if V_{SNS_CS} is 12.5mV or 25mV) or 25mV level (if V_{SNS_CS} is 50mV or 100mV)	GREC2	FAULT
	13	GREC2	Allow gate to recover and wait for when V_{DS} is less than 1.0 V comparator and V_{GS} is greater than 7.8 V gate comparator.	ON	FAULT

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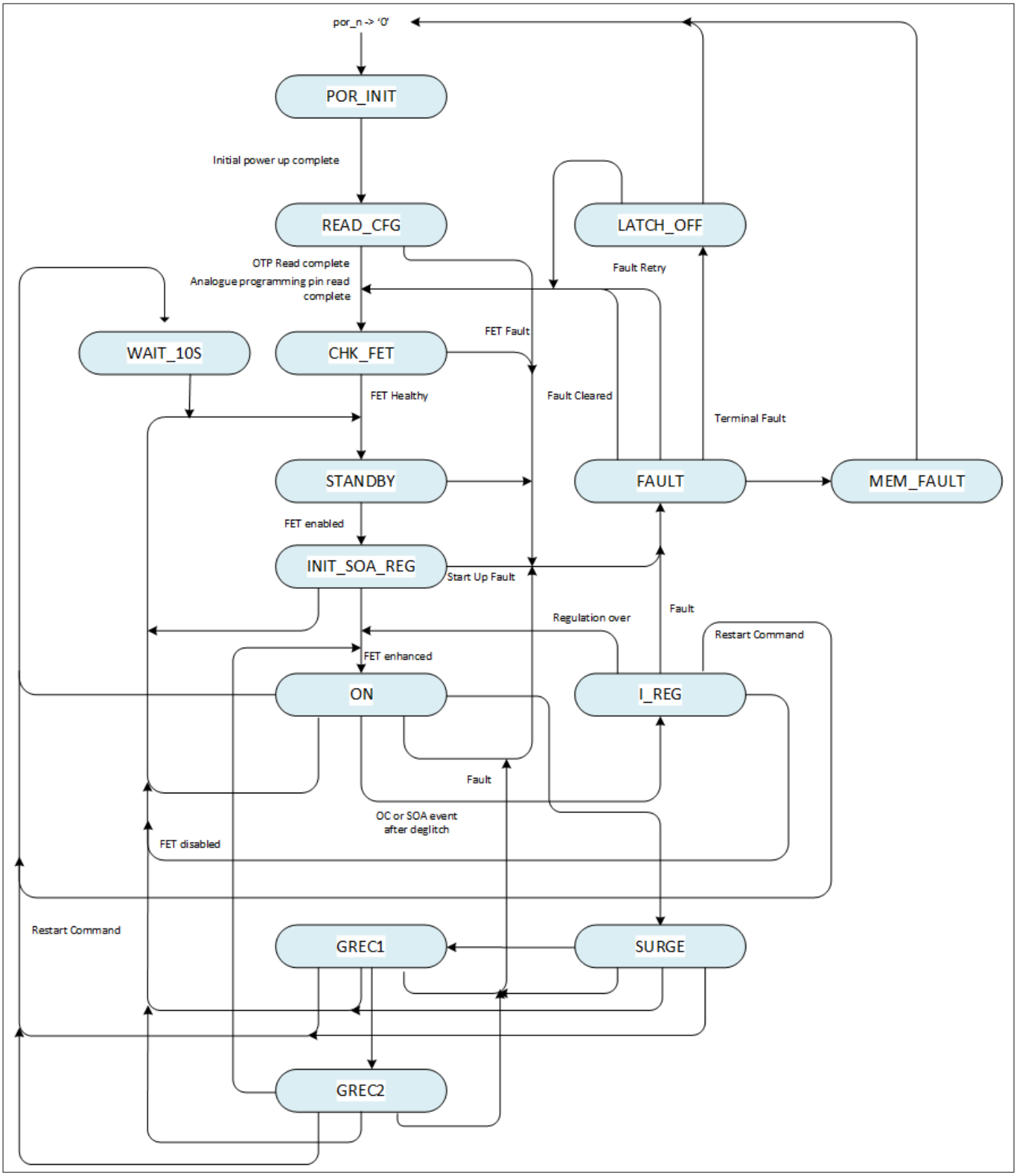

Figure 3 **XDP711 state machine**

5.1.3 Enable and disable

The PMBus interface communication and controller's programmability is functional at minimum operative VDD_VIN.

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XDP711's gate pin can be enabled or disabled by means of the UV/EN pin or PMBus command. By default, it starts up as soon as the necessary conditions are detected: proper voltage level between UV and OV pins. To disable this “enabled by default” feature, the corresponding bit has to be programmed accordingly in OPERATION PMBus command.

In DCM, the UV/EN pin has a deglitch timer EN_DG[3:0], which deglitches every UV/EN transition. This timer starts running as soon as the voltage at this pin rises above V_{UVEN_UTH}. The system turns on as soon as it expires if voltage is still above this level.

When UV/EN pin is tied low, the FET turns off, but the communication circuitry is still available. When the device is disabled but in STANDBY state, VREG and the communication via PMBus will still be enabled so that the device can be programmed and FAULT status bits will keep their latest status.

Also in DCM, it is possible to implement a manual input voltage deglitch by delaying the toggling of the UV/EN signal. Faults detection starts when UV/EN signal is toggled. In this case, EN_DG can be set to 0.

In ACM, the EN_DG[3:0] debounces the input voltage in a hot-plug event instead of the UV/EN pin and only runs after POR. If the supply voltage is enough to power up the controller, the EN_DG timer will run regardless of the voltage level at UV/EN pin. Subsequent transitions at UV/EN pin in ACM don't make the EN_DG timer run either.

The UV input (under-voltage monitoring input to support the UV fault) and EN input are combined in one pin.

The UV/EN pin configuration is dependent on mode of operation:

Table 17 UV/EN Input Configuration

Mode of operation	UV/EN pin configuration
FDM - DCM (digital comparators for OV and UV faults)	EN input
FDM - ACM (analog comparators for OV and UV faults)	UV input
AADM	UV input
Hybrid mode	EN input

If the pin is configured as UV input its voltage is sensed by an analog comparator to support UV fault detection and release. Turn-on and off of the device can still be controlled by toggling the pin high or low respectively. When pin is toggled low, XDP711 follows the configured UV fault procedure before turning off.

If pin is configured as EN, turn-on and off of the device can be controlled without following UV fault procedure.

The EN input controls the state of the controlled FET together with PMBus OPERATION command:

- EN = Low (voltage level is ≤ V_{UVEN_LTH}) --> FET is OFF;
- EN = High (voltage level is ≥ V_{UVEN_UTH}) --> the FET's state depends on the PMBus OPERATION command.

The EN High-to-Low transition clears any fault (including ones that cause Latch-off) as it is described in Latch-off. Only the memory OTP (MEM) fault is not affected.

The Connector Good Negated input (CGDN) provides a way to detect if a connector is correctly plugged to the system. If pulled externally Low (voltage level is ≤ V_{IL} Max), the controller is allowed to turn FET on. When the pin is floating or pulled externally High (voltage level is ≥ V_{IH} Min), the FET is turned off. This reduces arcing by turning off the FET before the connector is removed.

The table below shows the relations between OPERATION command and state of UV/EN and CGDN (if configured) pins:

Inputs			State of the FET
OPERATION command	UV/EN	CGDN	
ON	H	L	Active (can be ON / Regulated / OFF due to fault)
OFF	H	L	OFF
ON	L	L	OFF

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OFF	L	L	OFF
ON	H	H	OFF
OFF	H	H	OFF
ON	L	H	OFF
OFF	L	H	OFF

5.1.4 Control of FET's current

XDP711 controls the FET's current according to four different limits:

- **Programmed FET SOA limit:** To protect the FET, current flow through the FET is regulated according to its V_{DS}, following the FET's SOA line, which is stored in ROM or OTP. Pre-programmed SOA lines correspond to 65°C or 125°C temperature, this is in order to account for systems that will be working at temperatures higher than the usual ambient of 25°C. They are selectable between DC and half DC in FDM. DC only in AADM. Care must be taken to program the corresponding SOA fault timers according to the voltage and current levels so that maximum FET capabilities are not exceeded. If FET temperature monitoring feature (TSNS_x pins) is used, the SOA line to be used is adjusted automatically according to the sensed temperature. Below 105°C, the 65°C line is used, and above 105°C, the 125°C line is used. SOA can also be manually programmed to give the user the flexibility to work with different SOA curves or limit the power allowed;
- **Overcurrent (OC) limit:** To protect the load and source, this limit is normally set according to the maximum allowed current flow through the circuit by means of I_{OC}. This limit is active during INIT_SOA_REG, ON and I_REG states. See Setting I_{OC} for info about how to set it.
- **FET Start-up current (IST) limit:** To reduce voltage overshoots due to the output capacitance by increasing start-up time, this limit can be set in case SOA and OC limits are too high. This limit is taken into account during INIT_SOA_REG state only and disregarded as soon as ON state is reached.
- **SOC limit:** The severe overcurrent limit provides a fast response in case current reaches critical levels.

5.1.4.1 MOSFET's Power-up - Continuous Safe Operating Area (SOA) Control

During a system initialization, XDP711 provides bias current to turn on the MOSFET in a controlled manner to avoid any SOA violations, while ensuring that the system is turned on without any inrush event.

During power-up, the lowest of the three limits:

- FET SOA
- OC: Programmed overcurrent limit
- IST: Programmed system startup current limit

defines the system maximum allowed current.

In the following example, the green dotted line indicates the maximum current allowed through the MOSFET (IPB020N10N5LF) during a startup. The programmed safe operating area (SOA) of the MOSFET is indicated by the solid blue line. In this example, the maximum current allowed by the controller is limited by IST since it is the lowest current limit allowed by this specific application.

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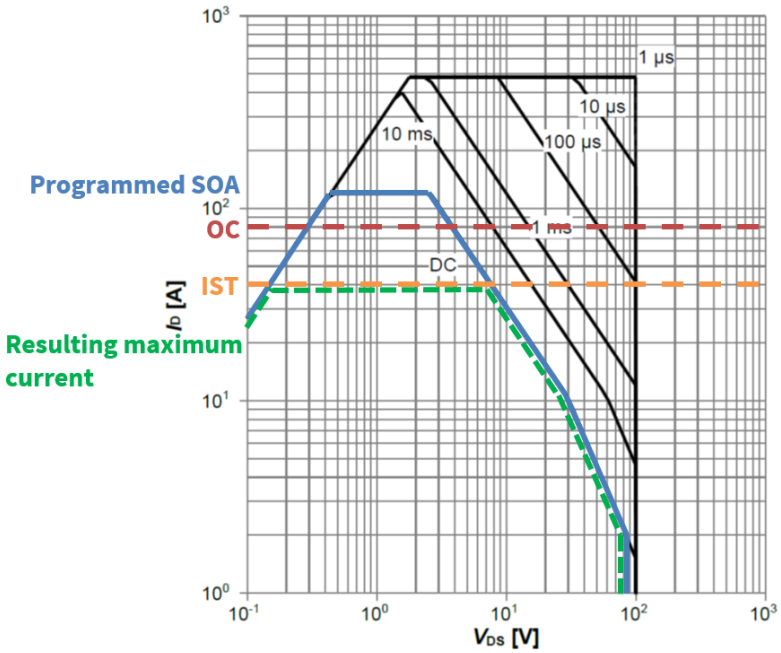

Figure 4 Safe operating area

SOA is digitally programmed in the SOA command as a look-up table with 80 values, corresponding to V_{DS} = 1 V to 80 V. Each value represents the current I_D allowed for each voltage point. The following table contains the DC curve data shown in the previous figure for FET IPB020N10N5LF at 65°C. XDP711 target SOA has a resolution of 0.5 A and an absolute minimum regulation level of 0.25 A. This level is limited by the combination of VSNS_CS, chosen sense resistor and internal ADC resolution. Due to these factors, it can result in a higher level.

Where 180.31 is the resolution of the ADC and 3 is the margin in LSBs for noise protection.

The **Target SOA I_{SOA} (A)** column shows the rounded values:

Table 18 SOA Table for IPB020N10N5LF

V_{DS} [V]	I_D [A]	Target SOA I_{SOA} [A]
1	120	120
2	120	120
3	104.2	104
4	78.1	78
5	62.5	62.5
6	52.1	52
7	44.6	44.5
8	39.1	39
...	...	...
73	2.5	2.5
74	2.5	2.5
75	2.4	2

(table continues...)

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Table 18 (continued) SOA Table for IPB020N10N5LF

V_{DS} [V]	I_D [A]	Target SOA I_{SOA} [A]
76	2.4	2
77	2.3	2
78	2.2	2
79	2.2	2
80	2.1	2

As an example, a typical 48 V input application with the DC line of figure above is taken.

- Before the FET is turned on, there are 48 V at the input (with respect to GND) and 0 V at the output, since the output capacitor is discharged. So V_{DS} = 48 V.
- XDP711 starts charging the output capacitor by regulating the current through the FET according to the maximum allowed in the SOA. From Figure 4, the DC line allows an $I_{SOA} \cong 4.5$ A at 48 V.
- While the capacitor charges, V_{DS} of the FET will be reduced, allowing current increase according to SOA. For example, V_{DS} = 40 V allows a current of $I_{SOA} \cong 6.5$ A, so, when V_{DS} reaches 40 V, XDP711 increases the current through the FET to 6.5 A.
- Current keeps increasing while voltage keeps decreasing until output voltage is charged to the desired level and FET gets fully enhanced. This current limitation delays the charging of the output capacitor, significantly reducing the inrush current at start-up while keeping the FET safe at all times.

5.1.4.1.1 Control loop current offset

To allow continuous SOA control in high power applications, the regulated current target level can be reduced by introducing a negative offset in I_SOA_REG_OFFSET[4:0] bits, which a resolution of V_{SNS_CS} / 180.31 per LSB. To calculate the I_SOA_REG_OFFSET[4:0] for a specific offset:

$$I_SOA_REG_OFFSET = \frac{offset * R_{SNS}}{V_{SNS_CS}/180.31} \quad (1)$$

Where:

I_SOA_REG_OFFSET is the decimal value to be converted to hexadecimal and programmed in I_SOA_REG_OFFSET[4:0] bits,

offset is the desired current offset in A,

R_{SNS} is the value of the sense resistor in Ω,

and V_{SNS_CS} must be specified in V

5.1.4.1.2 Control loop

XDP711's control loop consists on a closed loop system that senses the FET current by means of the voltage drop on the sense resistor and input and output voltages. It calculates the FET's V_{DS} by substracting V_{OUT} - V_{IN} and regulates the current according to the maximum allowed in the SOA table, depending on the sensed V_{DS}. This regulation is done by adjusting the FET's V_{GS}.

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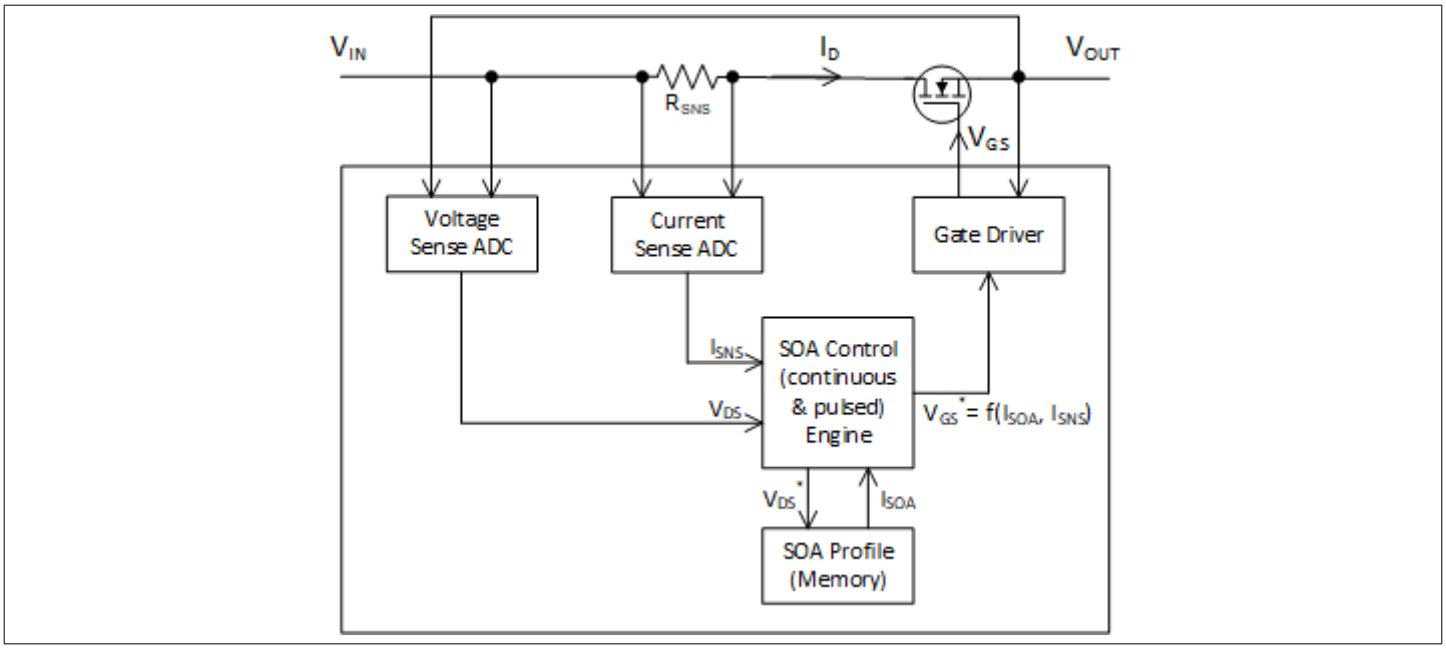

Figure 5 **XDP711's Control loop block diagram**

5.1.4.1.3 Setting OC and IST levels

In XDP711 FDM the current sense (CS) range and overcurrent (OC) level are set digitally by means of CS_RNG bits in I_SNS_CFG PMBus command.

Table 19 **CS_RNG values**

CS_RNG [1:0]	OC level [mV]
00	12.5
01	25
10	50
11	100

If required, the Non-RMS and RMS OC levels can be trimmed by CS_RNG_TRIM.

The start-up current limit (IST) through the FET is set digitally using dedicated START_ILIM bits in I_SNS_CFG command:

Table 20 **START_ILIM current limit**

START_ILIM[2:0]	Start-up current limit (IST)
000	100% of Ioc level (disabled, default)
001	75% of Ioc level
010	50% of Ioc level
011	25% of Ioc level
100	15% of Ioc level
101	12.5% of Ioc level

(table continues...)

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Table 20 (continued) START_ILIM current limit

START_ILIM[2:0]	Start-up current limit (IST)
110	9% of Ioc level
111	5% of Ioc level

In AADM, the default OC range and the start-up current limit (IST) through the FET can be set by means of a voltage on IST pin. If settings different than the ones in Table 21 are desired, they can be configured manually in the corresponding PMBus commands.

Table 21 IST pin configuration

IST pin voltage [V]	V_{SNS_CS} [mV]	Start-up current limit (IST)
IST > 2.8 (Open)	25	Set by START_ILIM bits in I_SNS_CFG command
2.2 < IST ≤ 2.8		50% of V_{SNS_CS} (25mV)
1.7 < IST ≤ 2.2		25% of V_{SNS_CS} (25mV)
1.3 < IST ≤ 1.7		12.5% of V_{SNS_CS} (25mV)
0.9 < IST ≤ 1.3	12.5	12.5% of V_{SNS_CS} (12.5mV)
0.6 < IST ≤ 0.9		25% of V_{SNS_CS} (12.5mV)
0.3 < IST ≤ 0.6		50% of V_{SNS_CS} (12.5mV)
IST ≤ 0.3 (GND)		Set by START_ILIM bits in I_SNS_CFG command

Setting the voltage level (between 0.3 V and 2.8 V) at IST pin shall be done using external resistor connected to GND.

To set the desired voltage level at the pin, choose the resistor by simply dividing desired voltage over sourced pin current (100 µA ± 7%).

The 1% (or lower) tolerance resistors are recommended in this case. For example:

Table 22 IST pin resistor

Voltage [V]	IST pin resistor [kΩ]
2.49	24.9
1.96	19.6
1.5	15
1.1	11
0.75	7.5
0.453	4.53

5.1.4.2 Control of current during FET's normal operation

In normal operation (during ON and I_REG states) the FET's current is limited by OC and FET's SOA limits. If RMS OC fault is enabled, the FET's current limitation set by OC limit is disregarded, the OC_{RMS} event comes from the digital RMS overcurrent detector.

5.1.5 Boost mode power-up

For high V_{DS} values, the I_{SOA} target is often in low current range, that is, below 1 A. For some FETs it could be even lower than the minimum SOA current regulation level (0.25 A). Running FET's power-up with continuous SOA control

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under those conditions may result in FET overstress and failing, especially in the systems with large output capacitors.

The XDP711 features a programmable variable pulse SOA control (also called boost mode), which enables the device to "boost" the output current by pulsing the I_D at a higher level, leveraging the FET's increased current capability during shorter pulses. This advanced control mechanism also incorporates a cool-down period between pulses to ensure the FET's safe operation. By mimicking a switching-type operation, the MOSFET gate is enhanced in bursts, allowing the output capacitor to be efficiently charged while preventing overheating through intermittent cooling periods.

There are two types of boost mode:

1. Automatic boost: Pulses are applied to the gate of the FET until $I_{SOA} \geq 0.5$ A. Then system continues power-up with continuous SOA regulation mode.
2. Full boost: Pulses are applied to the gate of the FET until V_{DS} of the FET is lower than 1 V. Then system continues power-up with continuous SOA regulation mode.

If this function is enabled by means of the BOOSTMODE_EN bit in the REG_CFG command, XDP711 executes the following procedure at power-up:

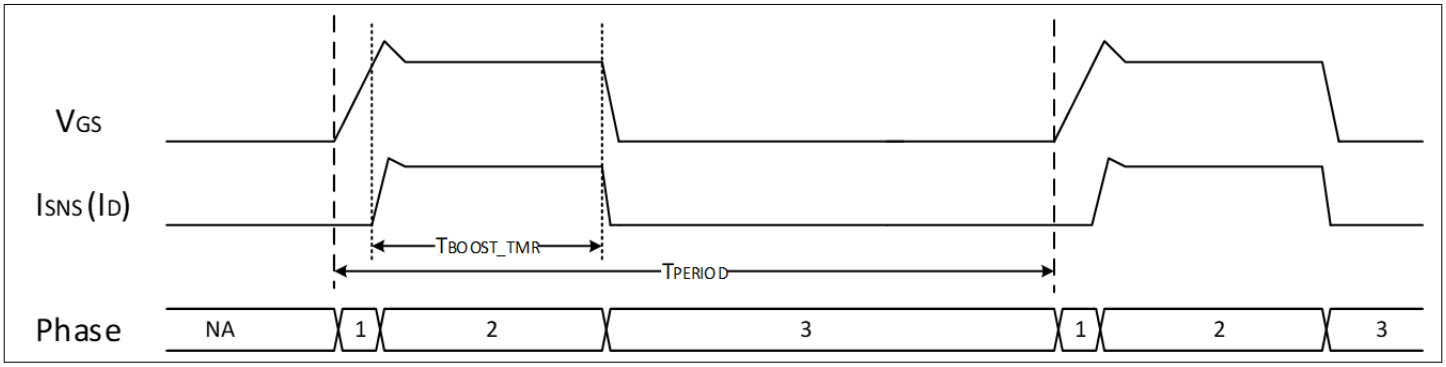

Figure 6 Boost mode power-up

1. **1st phase:** The V_{GS} starts ramping when INIT_SOA_REG state is entered. The T_{PERIOD} timer, defined by BOOSTMODE_TMR and BOOSTMODE_DC, activates at start of V_{GS} ramp.
2. **2nd phase:** The pulse timer T_{BOOST_TMR} (value set in BOOSTMODE_TMR) starts after the V_{GS} ramp has ended. The FET's current target is set to boost target I_{BOOST}:

   - If I_{SOA} (programmed SOA current at actual V_{DS}) programmed value > 0: I_{BOOST} = multiplication factor x I_{SOA} typ. The multiplication factor is taken from a look up table stored in ROM and ranges from 1 to 8 for 1ms BOOSTMODE_DC and from 4 to 128 for 100 µs, depending on the selected FET and SOA line.

   - If I_{SOA} programmed value = 0: I_{BOOST} = 0.25 A typ.
3. **3rd phase:** After T_{BOOST_TMR} has expired, the FET current is set to 0 by turning off the FET.
4. After T_{PERIOD} has expired, next V_{GS} ramp starts and system continues from 1st phase until target $I_{SOA} \geq 0.5$ A for automatic boost or V_{DS} of the FET is lower than 1 V for full boost.
5. After target I_{SOA} or V_{DS} reach these points depending on the selected mode, FET's power-up is finalized via continuous SOA.

To calculate T_{PERIOD}:

$$T_{PERIOD} = \frac{BOOSTMODE_TMR}{BOOSTMODE_DC} \tag{2}$$

For example, if BOOSTMODE_TMR = 1ms and BOOSTMODE_DC = 10%:

$$T_{PERIOD} = \frac{1ms}{10\,\%} = 10ms \tag{3}$$

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Boost mode dynamic resolution

Boost mode has a dynamic resolution that changes at the Resolution Breakpoint programmed in the SOA PMBus command. This value must be programmed according to the FET's SOA and it's the voltage point where the allowed current level is equal to 0.5 A. Below this point, the resolution of the control loop is 1.95 mA. Above this point, the resolution changes to 0.5 A.

Boost mode considerations

- BOOSTMODE_TMR and BOOSTMODE_DC must be configured according to FET max SOA capabilities

5.1.6 Power good

The power good signal is asserted to indicate when the following conditions are met. In ON or I_REG states:

- The input voltage is within the UV and OV/OVin limits, the output voltage is above OUV limit
- FET's and controller's over-temperature protection limits are not violated
- FET is fully enhanced (V_{GS} > 7.8 V and V_{DS} < 1.0 V) after its power-up.
- No fault is present

In SURGE or GRECx states:

- PWRGD is kept asserted for surge immunity protection, regardless of V_{GS} voltage level.

The PWRGD assertion is performed after a programmable power good assertion deglitch time (see Table 12).

The PWRGD de-assertion also has a programmable power good de-assertion deglitch time, which helps to avoid unnecessary signal's re-toggling due to short voltage or current jumps.

PWRGD signal polarity is configurable (active low or active high) by means of the PWRGD_POLARITY bit in order to support sequential turn-on capability.

5.1.7 Support of sequential turn-on

PWRGD, FAULT, WARN and UV/EN pins are used for communication between different devices if sequential turn-on implementation is desired based on "primary/secondary" approach.

Voltage levels of UV/EN, PWRGD, FAULT and WARN pins are compatible so that PWRGD, FAULT or WARN pins of a “primary” device can drive the UV/EN pin of a “secondary” device and control its turn-on or off.

5.1.8 Support of OR-ing capability

When PWRGD output pin is configured as active Low, two controllers can be connected to the same output voltage, so that, when output of the "primary" device goes down, the "secondary" can supply the necessary voltage. It is a backup supply scenario. A deglitch period can be configured between "primary" undervoltage and "secondary" (backup) enable by means of an UV/EN pin response delay or deglitch period. The system has to be designed so that a capacitor can supply the necessary power during this supply outage. The power-up latency of the "secondary" controller has to be taken into account too.

5.1.9 FET power down

Turn-off of the FET can be triggered manually or automatically due to a fault. In general, FET is turned-off by pulling I_{GATE_SPD} from its gate, except for the cases of OVin and SOC faults. In these cases, a configurable two step turn-off has been implemented in order to avoid FET drain-source voltage overshoots.

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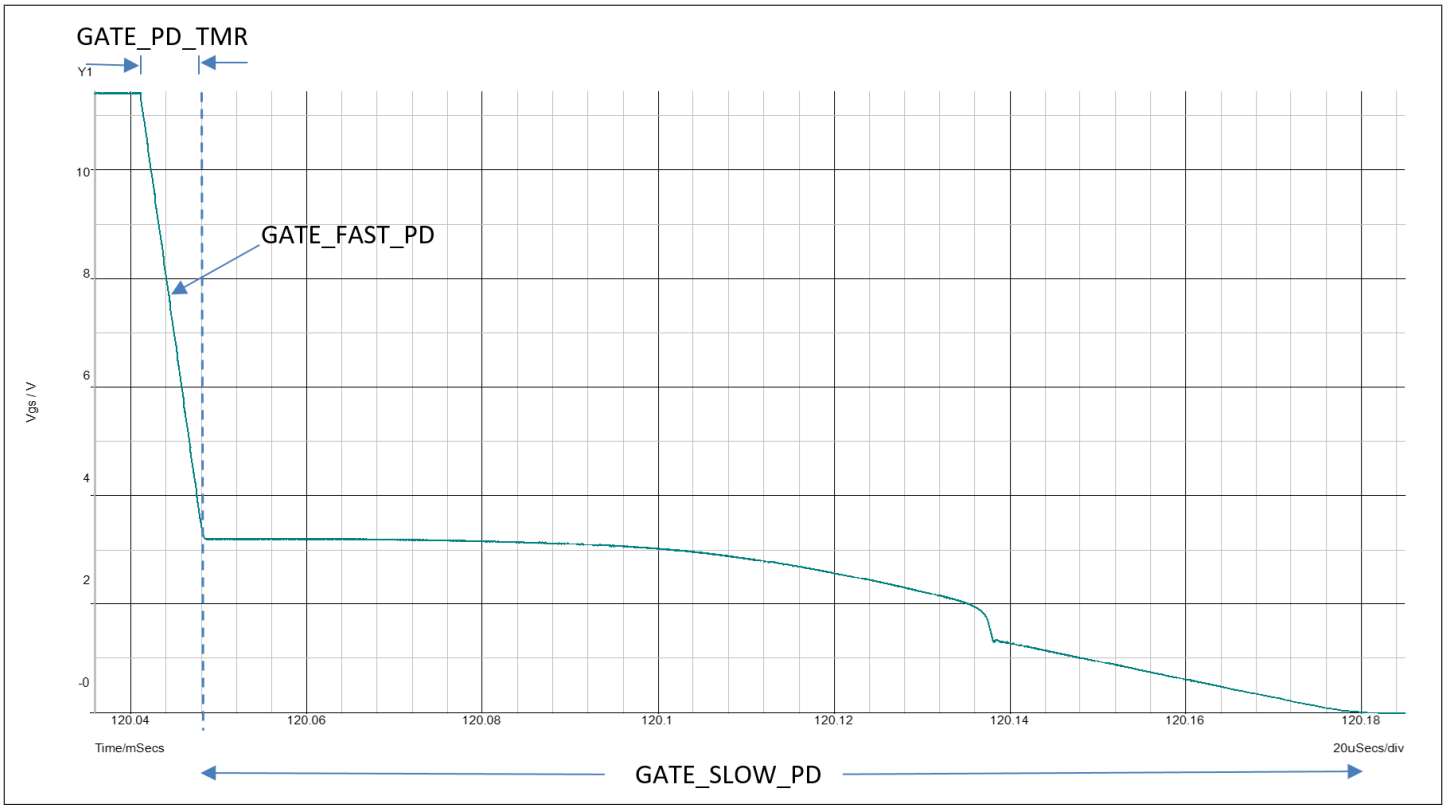

Figure 7 FET power down

The first step is configurable to 1.5 A current source or 200 Ω resistor through the bit GATE_FAST_PD[0]. If 1.5 A is selected, this current will be pulled out of the gate of the FET until it is completely turned off, ignoring the second step. If the 200 Ω resistor is selected, it discharges the gate of the FET for a time defined by the GATE_PD_TMR timer. This timer will start running when the turn-off process starts as soon as fault is detected. The timer must be calculated depending on the FET gate charge so that the plateau voltage is passed in this first stage. This “fast” stage avoids the increase of the current by reaching the FET’s linear region as fast as possible.

Then, the second stage limits the voltage overshoot by slowing down the di/dt of the system. This stage starts when GATE_PD_TMR expires. When it does, level of current being pulled out of the gate changes according to what is programmed in GATE_SLOW_PD[1:0] bits. A lower level of current will keep the FET in linear region for a longer time, which will, as a result, slow down the di/dt until the threshold voltage of the FET is passed and the FET is completely off.

If GATE_PD_TMR is 0 and GATE_FAST_PD[0] = 1, gate discharges slowly with GATE_SLOW_PD only, without a fast pull-down phase. The minimum allowed time to be programmed in GATE_PD_TMR (if it's not 0) is 250ns.

Note: Due to the benefits of the two-step turn-off, it is recommended to always use it after OVin and SOC faults.

5.1.10 Restart

A system reset can be triggered by issuing a RESTART PMBus command or by toggling the RESTARTN pin. If this feature is triggered, FET turns-off for 10 seconds (WAIT_10S state in state machine), removing power from the output. After these 10 seconds, system transitions to STANDBY state and, if all the necessary conditions are met, FET automatically turns back on.

Note: OTP must not be manipulated during WAIT_10S state.

5.2 Surge immunity protection

Surge immunity protects the load of the system from short current surges by turning-off the FET if this kind of event is detected, then turning it back on if the surge is gone. This feature reuses the severe overcurrent (SOC) fault comparator with its SOC_DG_TMR[1:0] to detect current glitches induced by input voltage surges. SOC_TMR[2:0] is

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ignored in this case. If the voltage drop over the ISNS_x pins exceeds the programmed SOC_FAULT_LIMIT[2:0], the controller follows the surge immunity protection procedure by going into SURGE, GREC1 and GREC2 states consecutively

SURGE state: The FET is turned-off with a strong pull-down, then the system waits for 15 µs. Then it goes to GREC1 state.

GREC1 state: The controller pulls-up the gate of the FET with 15 mA. System transitions to GREC2 state as soon as:

- The voltage drop over the sense resistor to reaches 12.5 mV level (if V_{SNS_CS} is 12.5 mV or 25 mV) or 25 mV level (if V_{SNS_CS} is 50 mV or 100 mV). The SOC comparator level is changed temporarily in this state for this purpose.
- Or the FET is fully enhanced (V_{DS} < 1.0 V and V_{GS} > 7.8 V)

GREC2 state: The output capacitor continues to be charged with the programmed OC current level until FET gets fully enhanced. In this state, SOC fault level is changed back to the one programmed in SOC_FAULT_LIMIT bits. If SOC conditions are still present in this state, SOC fault is triggered.

For FET protection during recovery, the SURGE_REC_WATCHDOG[2:0] can be configured from 1 ms to 100 ms or same as WATCHDOG[3:0]. This timer starts running in GREC1 state. If the recovery is not successful before timer expires, XDP711 issues a watchdog (WD) fault.

Both SOC fault and SRG_PROT_EN bit have to be enabled for the IC to follow surge protection feature. If SRG_PROT_EN is disabled and SOC fault is enabled, SOC fault procedure is followed normally.

Notes:

1. VCP capacitor and additional C_{GS} are required for a proper functionality of this feature. To calculate these, see Calculating VCP and Cgs capacitors.
2. When the surge immunity feature is enabled, for a proper functionality, SOC_DG_TMR is restricted to 0 ns or 200 ns settings only.

5.3 Faults

XDP711 incorporates many protections that ensure safe operation for the FET, source and load in different scenarios.

Faults are events that could stop system operation or even potentially damage some part of the circuit, so protective actions are taken in response to this kind of events.

For this purpose, different FET gate pull-down mechanisms are incorporated as described in FET power down:

- Regular/slow pull-down: In case of a fault event that is not dangerous for the system, FET is turned off by pulling a typical current of 250 µA / 500 µA / 750 µA / 1.25 mA (programmable by means of GATE_SLOW_PD bits in TURN_OFF_CTRL PMBus command) from its gate.
- Strong/fast pull-down: In case of an emergency fault,
  - 1) a typical current of 1.5 A are pulled from the FET's gate for extremely fast turn-off or
  - 2) a two step FET's turn-off is applied to keep FET's V_{DS} below avalanche breakdown. Method 1) or 2) has to be selected by means of GATE_FAST_PD bits in TURN_OFF_CTRL command depending on the system setup and requirements.

There are four ways in which XDP711 reports when a fault has occurred:

- Read Fault Status commands via PMBus interface: Each one of the faults has a corresponding bit in the STATUS_FAULTS command which is set after a fault has occurred.
- The fault indication pins: FAULT, LED#, SMBALERT#:
  - GPO0/FAULT NMOS open drain pin (output polarity is programmable): The status bits can be reflected on the FAULT pin to alert the processor/MCU that any of these events has happened.

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- GPO1/LED# pin is also an NMOS open drain pin, which polarity is fixed. If a fault occurs, this pin is driven low. An LED can be connected from a voltage source (anode) to the LED# pin (cathode) for a visual indication of the fault. If VREG is used as the voltage source of the LED#, care must be taken not to exceed the maximum power capabilities of the XDP711 (see Handling external current at VREG pin). LED# pin has a maximum current sink capability of I_{GPO_max}.
- The SMBALERT# is an open drain pin with a fixed active low polarity that can be configured to provide a summary of all triggered faults, warnings or both. Its output is a logic OR of all the faults or warnings, depending on its configuration in GPO_CFG command. SMBALERT# can be output in pins GPO0 or GPO3. Care must be taken to configure only one of them as SMBALERT#.
  - Mask commands are provided for the user to select which faults are to be reflected on the FAULT, LED# and SMBALERT# pins.

As a result of the fault, PWRGD pin is also deasserted.

Faults can be disabled by clearing their enable bits, which means they are not detected nor reported.

The fault status bits and pins will remain set until they are cleared:

- by means of the CLEAR_FAULTS PMBus command
- or by a controller restart (toggling EN pin) or a power cycle

The FAULT pin alerts the processor/MCU when any fault happens. This pin's state is an OR of all unmasked faults, leading to the possibility that if a masked higher priority fault is processed with the pin correctly in inactive state, a lower priority unmasked fault might cause the pin to be driven active.

For a proper detection, when a fault happens, the FAULT pin remains asserted for a minimum time of t_{FAULT_MIN}, regardless of the duration of the fault conditions.

To service the faults properly, CLEAR_FAULTS command and EN pin toggling are ignored in fault state and until fault process has finished and XDP711 has gone to LATCH_OFF state, or, in case of automatic restart, STANDBY or ON. Once the controller has left FAULT state, faults can be cleared (if fault conditions are not present anymore) and device can be restarted. LATCH_OFF state can be monitored by reading the STATUS_LATCH_OFF bit in STATUS_MFR_SPECIFIC command.

Note: For a correct functionality of the faults and in order to avoid enabling/disabling them while any fault conditions are actually present, all faults must only be enabled or disabled while controller is in STANDBY state.

Faults are divided in priority groups. In case a second fault with higher priority comes while servicing another fault, the first one is put on hold until the higher priority is served. When finished serving the high priority fault, system resumes servicing the fault that was put on hold. If the fault being serviced has same or higher priority than the second fault, system acts in a first-come, first-served fashion.

Priority groups and priorities are:

1: MEM

2: SDS, SGD, SGS, UR.

3: SOC.

4: VDS, OT, TSD.

5: OVin.

6: OV.

7: UV.

8: OUV.

9: WD.

10: OC, SOAR.

The following table shows when particular faults detection and processing is active:

Table 23 Faults during operation states

Activation (X) of FAULT's detection during operation states

(table continues...)

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Table 23 (continued) Faults during operation states

FAULT NAME	State of controller												
	POR_INIT	READ_CFG	CHK_FET	STANDBY	INIT_SOA_REG	ON	I_REG	SURGE	GREC1	GREC2	FAULT	WAIT_10S	MEM_FAULT/ LATCH_OFF
MEM	--	X	X	X	X	X	X	X	X	X	X	X	X
SDS	--	--	X	X	--	--	--	--	--	--	X	--	--
SGD	--	--	X	X	--	--	--	--	--	--	X	--	--
SGS	--	--	--	--	X*1	--	--	--	--	--	--	--	--
UR	--	--	--	--	--	--	--	--	--	--	X*2	--	--
SOC	--	--	--	--	X	X*3	X*3	--	--	X	--	--	--
VDS	--	--	--	X*4	--	--	--	--	--	--	--	--	--
OT	--	--	--	X	X	X	X	--	X	X	X	--	--
TSD	--	--	--	X	X	X	X	--	X	X	X	--	--
UV	--	--	--	X	X	X	X	--	X	X	X	--	--
OV	--	--	--	X	X	X	X	--	X	X	X	--	--
OVin	--	--	--	X	X	X	X	--	X	X	X	--	--
OUV	--	--	--	--	--	X	X	--	X	X	--	--	--
WD	--	--	--	--	X	--	--	--	X	X	--	--	--
OC	--	--	--	--	--	X	X	--	--	--	--	--	--
SOAR	--	--	--	--	--	X	X	--	--	--	--	--	--

Notes:

*1): Right at the point when watchdog timer expires.

*2): The UR fault can occur only in FAULT state when retry counter expires after any of the retry fault events (SOC, OUV, WD, OC, SOAR).

*3): If SRG_PROT_EN bit in RETRY PMBus command is '0' (surge protection is disabled).

*4): Detection is active after POR or after RESTART event.

5.3.1 Memory fault

Memory OTP (MEM) Fault

If an OTP read or write error is detected during READ_CFG state, XDP711 switches to FAULT and consecutively to the MEM_FAULT state, which initiates controller's latch-off. FET is switched off and PWRGD signal is deasserted. This fault can be cleared by means of a power cycle only, in which case the system restarts from the POR_INIT state.

5.3.2 Damaged FET faults

There is a FET health check phase after READ_CFG state and until STANDBY phase has finished.

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The drain-source and gate-drain low voltage checks start as soon as the READ_CFG phase is over at first plug-in or just before starting any retry attempt.

As a consequence of any of these faults, XDP711 switches to FAULT state and then passes directly to the LATCH_OFF state.

Shorted FET Drain-Source (SDS) Fault

If current above SDS limit (see table below) through the sense resistor is detected in CHK_FET, STANDBY or FAULT states, and V_{GS} of the FET is lower than 1 V while gate pin is weakly driven low, an SDS fault is issued.

The following table shows the corresponding typical current limit in Amp at R_{SNS} = 1 mΩ.

Table 24 SDS limit

V_{SNS_CS} (mV)	12.5	25	50	100
SDS limit (A)	0.24	0.52	1.1	2.2

Shorted FET Gate-Drain (SGD) Fault

SGD fault is triggered in the CHK_FET, FAULT or STANDBY states:

- In CHK_FET state: If the FET's V_{GS} goes above 1 V and current flow at the ISNS_x pins exceeds the limits in Table 24.
- When controller enters the FAULT or STANDBY state and activates any gate pull down. If the FET's VGS does not go below 1 V within 10 ms.
- In FAULT and STANDBY state: If, after FET's V_{GS} goes below 1 V within 10 ms when FET's gate is weakly driven low (regular/slow gate pull down), the FET's V_{GS} goes back above 1 V and current flow at the ISNS_x pins exceeds the limits in Table 24.

Shorted FET Gate-Source (SGS) Fault

If no power good is achieved in power-up procedure when the watchdog timer expires and V_{GS} < 1 V at this point, SGS fault will be issued.

Note: WATCHDOG timer is used for this fault even if watchdog fault is disabled. If a specific timer value is desired to cover SGS in this case, the timer must be configured accordingly.

Since boost mode pulses the FET's gate voltage on and off, it is possible that it is low at the time the watchdog timer expires, generating a false SGS fault. Therefore SGS fault must always be disabled when using boost mode.

Pre-charged Output Voltage (VDS) Fault

This fault is enabled according to Table 23 and, in STANDBY state, after EN_DG[3:0] timer has expired for the first time after power-up. V_{DS} of the FET is measured digitally at pins VOUT and ISNS_P pin and, if it goes below the limit programmed in VDS_FAULT_LIMIT[1:0], the fault is triggered and the controller goes to FAULT state, which keeps the FET off and asserts the FAULT or SMBALERT pins. VDS fault is released as soon as the V_{DS} voltage of the FET exceeds the same programmed limit or the voltage at VOUT pin is lower than 2 V. In which case the controller goes back to STANDBY state and, if conditions allow, the FET can be turned-on.

If this feature is enabled, it is recommended that the EN_DG timer is enabled (different than 0) too so that the supply voltage is stable when VDS is checked.

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5.3.3 Input voltage faults

System Input Undervoltage (UV) Fault

In FDM mode, if MODE bit = 1 (DCM), the UV fault limit is set digitally by VIN_UV_FAULT_LIMIT.

In AADM mode or FDM mode, if MODE bit = 0 (ACM), the limit V_{UVEN_LTH} is set by means of external components (see Setting OV, UV and OUV in ACM).

If the input voltage reaches or falls below the corresponding limit, UV_TMR[2:0] starts running. If voltage raises above VIN_UV_FAULT_LIMIT or V_{UVEN_UTH} before the timer expires, system stays in ON state. Otherwise, if voltage is still low when timer expires, fault will be triggered and FET is turned off with a regular pull-down.

UV fault has a configurable hysteresis in FDM-DCM mode, by means of the VIN_UV_HYST[3:0] bits and it depends on the configured VTLM_RNG. In the case of 88 V VTLM_RNG, the hysteresis can be configured from 2 V to 13 V. If VTLM_RNG is configured to 44 V or 22 V, it is scaled accordingly. This hysteresis is not only valid after a UV fault has happened, but also at power-up. System doesn't transition from STANDBY to INIT_SOA_REG if input voltage is lower than VIN_UV_FAULT_LMIT + VIN_UV_HYST.

To avoid false triggering of the UV fault when the voltage is ramping up at first power-up, the detection of this fault starts only when the EN_DG[3:0] timer has expired and the fault's programmed limit (analog or digital) plus its corresponding hysteresis is crossed for the first time.

System Input Overvoltage (OV) Fault

In FDM mode, if MODE bit = 1 (DCM), OV fault limit is set digitally by VIN_OV_FAULT_LIMIT.

In AADM mode or FDM mode, if MODE bit = 0 (ACM), the limit V_{OV_UTH} is set by means of external components (see Setting OV, UV and OUV in ACM).

If the input voltage reaches or raises above the corresponding limit, OV_TMR[2:0] starts running. If the voltage falls below VIN_OV_FAULT_LIMIT or V_{OV_LTH} before the timer expires, the system stays in ON state. Otherwise, if the voltage is still high when timer expires, a fault is triggered and FET is turned off with a regular pull-down.

XDP711 waits until FET is completely turned-off, then keep monitoring the input voltage and stay idle in the FAULT state until it falls below VIN_OV_FAULT_LIMIT minus a programmable hysteresis (DCM mode) or V_{OV_LTH} (ACM mode). In this case, the power-up sequence is initiated.

OV fault has a configurable hysteresis in FDM-DCM mode, by means of the VIN_OV_HYST[2:0] bits and it depends on the configured VTLM_RNG. In the case of 88 V VTLM_RNG, the hysteresis can be configured from 1 V to 8 V. If VTLM_RNG is configured to 44 V or 22 V, it is scaled accordingly.

In STANDBY state, the detection of this fault starts only when the EN_DG[3:0] timer has expired for the first time.

On-chip Input Overvoltage (OVin) Fault

If, during STANDBY, INIT_SOA_REG, normal operation or FAULT state, the input voltage goes above the limit set by OVIN_FAULT_LIMIT bits in V_SNS_CFG PMBus command, OVIN_TMR starts running. When it expires, a fault is triggered and FET is immediately turned-off with a fast or two-step pull-down (depending on configuration). XDP711 waits until FET is completely turned-off, then stays idle in FAULT state until input voltage goes below the lower OVin threshold of OVIN_FAULT_LIMIT minus a hysteresis of 5 V. Then power-up sequence is initiated.

In STANDBY state, the detection of this fault starts only when the EN_DG[3:0] timer has expired for the first time.

5.3.4 Output voltage faults

Output Undervoltage (OUV) Fault

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If, during normal operation, the output voltage falls below the OUV threshold set by a voltage divider at the FB pin (ACM mode) or the limit set by VOUT_UV_FAULT_LIMIT (DCM mode), OUV_TMR[2:0] timer starts running. If voltage goes back up before timer expires, the system continues normal operation. If OUV condition persists when timer expires, a fault is issued and FET is turned-off with a regular pull-down.

The system will retry to power-up after a cool-down period according to the RETRY command settings. In ACM mode, the analog comparator has a hysteresis with an upper limit of V_{FB_UTH}. The hysteresis of the digital comparator in DCM mode is shown in Table 25.

It is recommended to set OUV to a level lower than UV. This is because OUV sends the device to LATCH_OFF state, while UV sends it to FAULT. If both of them are set to the same level or if OUV is set to a level above UV, the device will be sent to LATCH_OFF state, instead of FAULT due to UV.

Table 25 Voltage hysteresis

V_{TLM_RNG} (V)	88	44	22
Voltage (V)	2.06	1.03	0.52

5.3.5 Current and temperature faults

Overcurrent (OC) Fault

An OC condition is detected if, during normal operation, FET current reaches its programmed level of I_{OC}. If this condition occurs, the SOAD_TMR[2:0] timer starts. If the FET current goes below I_{OC} - 10% of hysteresis (with a minimum of 0x04) before timer expires, the system continues normal operation. If the OC condition persists when the timer expires, XDP711 starts the OC/SOA regulation timer (SOAR_TMR[2:0]) and current regulation at I_{OC} level (I_REG state) by lowering FET's V_{GS} voltage. If I_REG state ends (FET is fully enhanced again) before this second timer expires, the system goes back to normal. Otherwise an OC fault is triggered and FET is turned off with a regular pull-down.

The system will retry power-up after cool down period according to RETRY command settings.

The SOA regulation timer configurable steps are compliant with common SOA lines so that the protection can be implemented according to the maximum allowed timer for a specific V_{DS} vs I_{DS} scenario.

Note: For safety reasons during I_REG state, if current through the FET goes below 1 A, the regulation will stop, FET is turned off and a SOAR fault is declared.

Severe Overcurrent (SOC) Fault

An SOC event is detected when FET's I_{DS} current reaches the level which creates a voltage drop over the sense resistor exceeding programmable level of V_{SNS_SOC}. The detection is done by means of an analog comparator for a faster reaction. This comparator has programmable SOC_DG_TMR analog deglitch and SOC_TMR digital deglitch timers for detection. This fault's detection is enabled according to the following table:

SRG_PROT_EN bit setting	Surge immunity protection	SOC fault
0	Disabled	SOC fault is processed in INIT_SOA_REG, ON and I_REG states
1	Enabled	SOC fault is processed in INIT_SOA_REG and GREC2 states

If V_{SNS_SOC} level of current is detected, SOC_DG_TMR and SOC_TMR will start running sequentially. If the SOC conditions are cleared before the timers expire and no other fault conditions are present, the system goes back to normal. Otherwise a fault is triggered and FET is opened with a fast or two-step pull-down (depending on configuration) as soon as this timer expires.

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The system will retry a power-up after a cool down period according to RETRY command setting. The fault indication pins are automatically de-asserted when fault conditions are cleared and PWRGD asserted after a successful retry.

In INIT_SOA_REG, ON and I_REG states, SOC fault configuration is done by means of the SOC_FAULT_LIMIT bits, and it depends on CS_RNG configuration, according to the following table:

Table 26 Configuration of SOC levels [mV]

		I_SNS_CFG.CS_RNG[1:0]			
		00	01	10	11
I_SNS_CFG.SOC_FAULT_LIMIT[2:0]	000	12.5		25	
	001	18.75		37.5	
	010	25		50	
	011	37.5		75	
	100	50		100	
	101	75		150	
	110	100		200	
	111	150		300	

In GREC2 state, SOC fault is triggered if the FET's drain to source voltage exceeds 5.5 V. This is an absolute limit for any VTLM_RNG setting.

RMS Current (RMS)

OC protection can be configured to react at RMS current calculation limit instead of instantaneous measurements.

RMS_EN bit in REG_CFG command enables or disables the RMS calculation function of the OC protection. If enabled, the protection level is based on RMS calculation. Since RMS is a sub-function of OC, OC must be enabled (by means of the OC bit in ENABLE_FAULTS command) if the RMS function is desired.

RMS does not have mask and status bits, but OC corresponding mask and status bits are used instead.

RMS_SAMPLE_TMR specifies the integration time for the RMS current protection calculation.

If the RMS_EN bit is set (RMS function is enabled), the CS_RNG_TRIM bits specifies the RMS current level (as a proportion of V_{SNS_CS}) at which the OC fault is triggered. If this RMS current level is exceeded, FET is turned off immediately with a regular pull-down, skipping the deglitch and regulation phases configured in the SOAD_TMR[2:0] and SOAR_TMR[2:0] bits.

SOA Regulation (SOAR) Fault

After ON state is reached and FET is fully enhanced, there could be different possible scenarios in which FET SOA limits are violated. For example:

- Input voltage suddenly increases generating a certain V_{DS} meanwhile the output cap is charged up to the new voltage level
- R_{DSON} is too high
- During I_REG state after an OC event, V_{DS} has to increase too much in order to keep the current at an appropriate level

In this scenario, the SOAD_TMR[2:0] deglitch timer starts. If FET V_{DS} and I_{DS} go back within the SOA limits before the timer expires, the system continues normal operation in ON state. Otherwise the SOAR_TMR[2:0] regulation timer

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starts while the system continues to regulate the current to stay within the SOA limits. If SOAR condition is cleared before this second timer expires, system goes back to ON state. If it persists, a SOA regulation fault is triggered and FET is opened with a regular pull-down.

If the regulated current through the FET goes below a level of 1 A, regulation stops, FET is turned off and a SOAR fault is declared.

The system will retry power-up after a cool down period according to RETRY command settings.

Note: The SOAR fault disabling means that a fault is never triggered and FET is never turned off in case of a SOA limits violation. It is recommended to keep the SOAR fault enabled for safety reasons.

Overtemperature (OT) Fault

If, during STANDBY, INIT_SOA_REG, normal operation or FAULT, the temperature measured between the TSNS_P and TSNS_N pins raises above the OT_FAULT_LIMIT value, a fault is triggered and FET is opened with a regular pull-down.

XDP711 waits until FET is completely turned off, then keeps monitoring the FET temperature and stays in the FAULT state until it drops below OT_FAULT_LIMIT - 25°C. In this case, the power-up sequence initiates and PWRGD pin asserts as soon as the necessary conditions are met.

On-chip Thermal Shut-down (TSD) Fault

XDP711 has an on-chip temperature sensor with a programmable fault limit of T_{TS_UTH}. If die temperature exceeds this value, a fault is triggered and FET is opened with a regular pull-down. XDP711 waits until FET is completely turned-off, then remains idle in the FAULT state until the temperature drops below T_{TS_LTH} (which is equivalent to T_{TS_UTH} - 10°C), at which point the power-up procedure is started.

5.3.6 Power-up faults

Unsuccessful Power-up (Watchdog, WD) Fault

The watchdog timer can be configured by means of the WATCHDOG[3:0] bits. Its configurable steps are compliant with common SOA lines so that protection can be implemented according to the maximum allowed timer for a specific V_{DS} vs I_{DS} scenario. It starts running as soon as power-up procedure starts in the INIT_SOA_REG state. If FET is not fully enhanced (V_{DS} < 1.0 V and V_{GS} > 7.8 V) before the timer expires, a WD fault is triggered and FET is turned-off with a regular pull-down.

A power-up is retried according to the RETRY command settings, in which case, the fault indication pins are cleared when leaving FAULT state before any retry attempt. The corresponding status bit remains set until it is manually cleared or device is restarted or power cycled.

Unsuccessful Retry (UR) Fault

The UR fault can only occur in FAULT state when the retry counter expires after one of the retry fault events (SOC, OUV, WD, OC, SOAR). The retry counter decrements on each retry event. If it reaches a value of zero (maximum number of programmed retries has been reached), a UR fault is triggered and the system goes to and remains in LATCH_OFF state.

5.3.7 Internal protection fault

VREG Fault

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If, at any point of operation, voltage at VREG pin goes below 4.1 V, system will trigger a power-on reset. This fault is not signaled at the fault indication pins, nor does it have a bit in the STATUS_FAULTS PMBus command.

5.4 Retry

XDP711 can be configured to automatically retry FET's power-up after FET shut down due to the following faults: OUV, Watchdog, OC, SOAR, SOC.

The number of retries can be configured from 0 (system latches off after first fault event) to 32 by setting the corresponding number in the RETRY_COUNTER[2:0] bits in the RETRY PMBus command.

The retry counter can also be disabled, which means the system will keep retrying an infinite number of times until it is turned off or reset.

The controller waits for a cool down period configurable from 0 to 64 seconds (COOLD_TMR[2:0] bits in RETRY PMBus command) before every retry attempt. During this period, the controller remains in FAULT state and CLEAR_FAULTS command and EN pin toggling will be ignored.

Retry mask bits are provided so that the cool down period can be turned on or off for any of the faults individually. If both RETRY_COUNTER and fault retry masks are set to 0, system will keep retrying indefinitely skipping the cool down period.

If a successful FET's power-up is achieved during a retry attempt, the retry OK deglitch timer (RETD_TMR[2:0] bits in RETRY PMBus command) starts running as soon as ON state is reached.

If no fault has occurred when this timer expires, the retry counter is set to its initial state.

If the maximum number of retries is reached without success, an unsuccessful retry fault, which initiates Latch-off, is issued.

If the retry feature is used to avoid long start-up times due to the fault that caused the retry, it is recommended to enable the watchdog (WD) fault and its corresponding watchdog retry mask in MASK_FAULTS PMBus command.

5.5 Latch-off

LATCH_OFF and MEM_FAULT are latch-off states. In case of a latch-off fault, the controller's FAULT state is followed by the LATCH_OFF or MEM_FAULT state and controller:

- Keeps FET off and remains in LATCH_OFF or MEM_FAULT state
- Latches the state of all status commands including fault and warning ones, except for STATUS_CML. This is in order to support reporting of COM warning in LATCH_OFF state
- Latches the state of status pins (PWRGD, FAULT, LED#, SMBALERT#, WARN)
- Keeps service blocks (including VREG), telemetry, communication PMBus interface and necessary digital running to support data communication

Latch-off is immediately triggered by the following faults:

- Memory OTP fault
- FET's Drain-source short fault
- FET's Gate-drain short fault
- FET's Gate-source short fault

Latch-off is triggered if during the following faults the max number of retries has been reached without successful recovery from fault (Unsuccessful retry (UR) fault occurs):

- Output undervoltage (OUV) fault
- Unsuccessful power-up (watchdog) fault
- Overcurrent (OC) fault
- SOA regulation fault
- Severe overcurrent (SOC) fault

If the retry counter set to zero the Latch-off is triggered right after any fault listed above occurs.

XDP711 can go out of LATCH_OFF or MEM_FAULT states by means of a power cycle. In which case, it starts operation from POR_INIT state.

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Alternative ways to go out of LATCH_OFF (not applicable to MEM_FAULT) are the PMBus CLEAR_FAULTS command or the external EN signal High-to-Low transition (if the pin is configured as EN, see Enable and Disable). If either of these methods is used, the following actions take place:

- De-assert/release status pins (PWRGD, FAULT, WARN)
- Clear the FAULT and WARNING status commands
- Continue operation from CHK_FET state

5.6 Warnings

Warnings are defined as alerts that do not turn off the FET. They are alerted through the WARN or SMBALERT# pins to the processor/MCU so that it can decide if any action is needed in response.

Each one of the warnings has a corresponding bit in the STATUS_WARNS command that is set when a warning has occurred.

These bits can be reflected in the GPO1/WARN pin to alert the processor/MCU that any of these events has happened. GPO1/WARN is an NMOS open drain pin (output polarity is programmable).

The SMBALERT# pin can be configured to provide a summary of all triggered faults, warnings or both. Its output is a logic OR of all the faults or warnings, depending on its configuration in GPO_CFG command. A mask command is provided for the user to select which warnings are to be reflected on the WARN and SMBALERT# pins.

Warnings can be disabled by clearing their enable bits, which means they are not detected and are not reported.

Each one of the warnings descriptions below specifies when the "warning is cleared". This indicates when the conditions that generate one or more warnings are cleared.

The warning status bits and pins remain set until they are cleared:

- by means of the CLEAR_FAULTS PMBus command
- or by a controller restart (toggling EN pin) or a power cycle

Note: Due to the nature of the COM warning, there are some exceptions on the way it is reported through the WARN pin and the way it is cleared. See details in Communication warning.

The table below shows when particular warning's processing is active.

Table 27 Warnings during operation states

Activation (X) of WARNING's processing during operation states												
WARNING NAME	State of controller											
	POR_INIT	READ_CFG	CHK_FET	STANDBY	INIT_SOA_REG	ON	I_REG	SURGE	GREC1 and 2	FAULT	WAIT_10S	MEM_FAULT/ LATCH_OFF
VGSL	--	--	--	--	--	X	--	--	--	--	--	--
OT	--	--	--	X	X	X	X	X	X	X	--	--
TSD	--	--	--	X	X	X	X	X	X	X	--	--
UV	--	--	--	X	X	X	X	X	X	X	--	--
OV	--	--	--	X	X	X	X	X	X	X	--	--
OOV	--	--	--	X	X	X	X	X	X	X	--	--
OUV	--	--	--	--	--	X	X	X	X	--	--	--
SOAR	--	--	--	--	--	X	X	--	--	--	--	--
OUC	--	--	--	--	--	X	X	--	--	--	--	--

(table continues...)

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Table 27 (continued) Warnings during operation states

OOC	--	--	--	X	X	X	X	X	X	--	--	--
INeg	--	--	--	--	--	X	X	--	--	--	--	--
OP	--	--	--	X	X	X	X	X	X	--	--	--
COM	--	--	X	X	X	X	X	X	X	X	X	X

The following figure shows flow of all warnings.

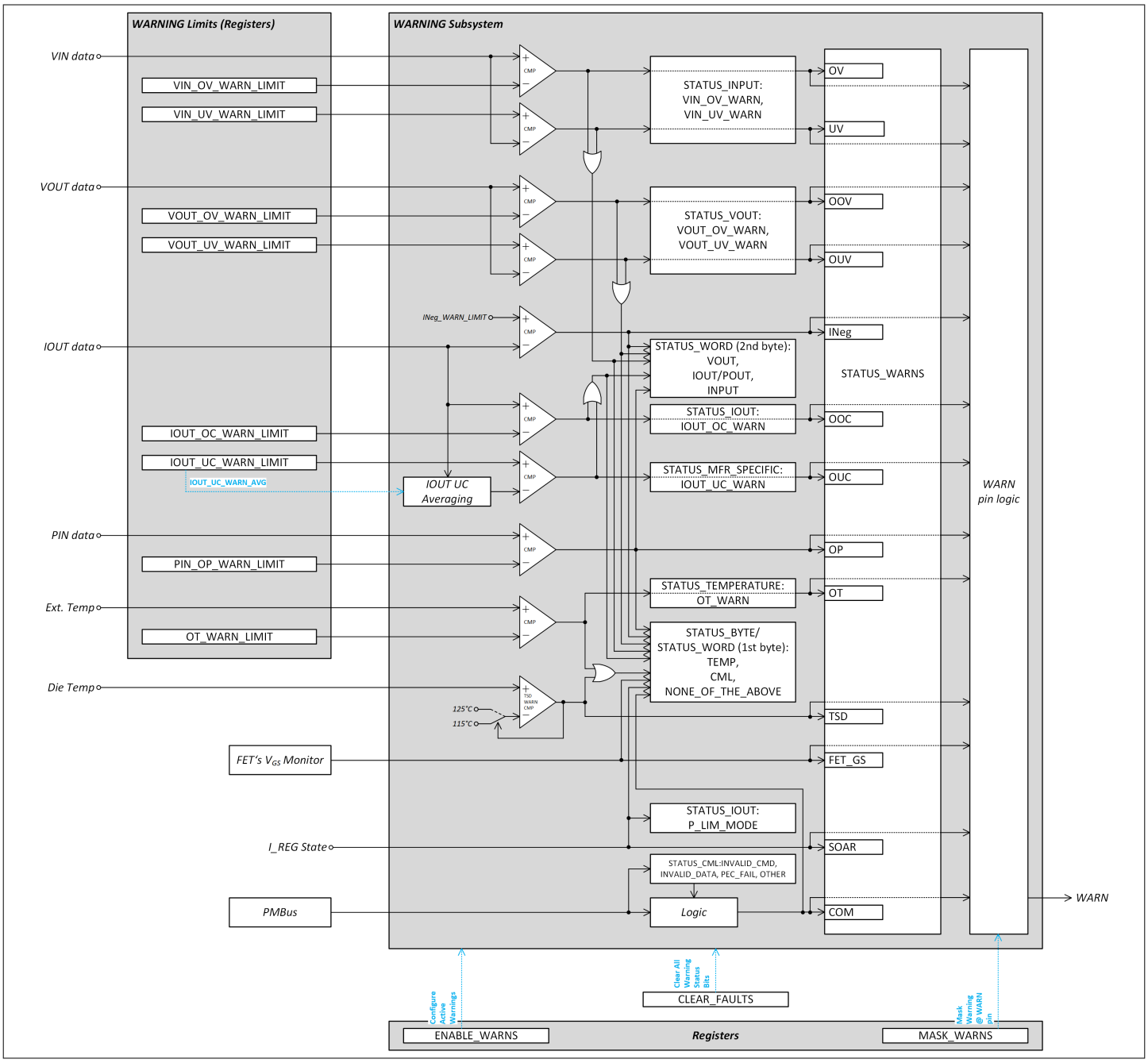

Figure 8 Warnings flow

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5.6.1 Damaged FET warning

Gate-Source Low Voltage (VGSL) Warning

If, during ON state, V_{GS} of the FET goes below 7.8 V, a VGSL warning is triggered indicating that there might be gate-source or gate-drain issues over life time. The warning is cleared as soon as V_{GS} of the FET raises above the same limit.

5.6.2 Input voltage and power warnings

Input Undervoltage (UV) Warning

If the input voltage reaches or falls below VIN_UV_WARN_LIMIT, a warning is triggered. If the voltage raises above this limit plus a hysteresis of 0x60 (see Table 28), the warning is cleared.

Input Overvoltage (OV) Warning

If the input voltage reaches or raises above VIN_OV_WARN_LIMIT, a warning is triggered. If the voltage falls below this limit minus a hysteresis of 0x60 (see Table 28), the warning is cleared.

Table 28 Voltage hysteresis

V_{TLM_RNG} (V)	88	44	22
Voltage (V)	2.06	1.03	0.52

Input Overpower (OP) Warning

If the input power (as a product of VIN * IOUT) goes above the programmed PIN_OP_WARN_LIMIT, the system generates an OP warning. If the input power goes below the limit minus a digital hysteresis of 0x100 (which corresponds to typically 0.4% of the maximum power), the warning is cleared. Averaging of power for this warning is done by the same setting as telemetry: P_TELEMETRY_AVG bits in TELEMETRY_CFG PMBus command.

5.6.3 Output voltage warnings

Output Undervoltage (OUV) Warning

If the output voltage reaches or falls below VOUT_UV_WARN_LIMIT, a warning is triggered. If the voltage raises above this limit plus a hysteresis of 0x60 (see Table 28), the warning is cleared.

Output overvoltage (OOV) Warning

This warning bit will be set if, during Power-up Procedure, Normal Operation or FAULT state, the output voltage exceeds the limit set by VOUT_OV_WARN_LIMIT PMBus command. If the voltage falls below this limit minus a hysteresis of 0x60 (see Table 28), the warning is cleared.

5.6.4 Current and temperature warnings

Output Overcurrent (OOC) Warning

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An OOC warning is detected if the load current sensed by the voltage drop in the sense resistor exceeds the limit set by the IOUT_OC_WARN_LIMIT PMBus command. The warning is cleared if the current goes below the IOUT_OC_WARN_LIMIT minus a digital hysteresis of 0x80 (see Table 29).

Output Undercurrent (OUC) Warning

If, during normal operation, the FET I_{DS} current is less than a programmable value of the IOUT_UC_WARN_LIMIT PMBus command, an undercurrent event is triggered. The warning is cleared as soon as the current goes back above the IOUT_UC_WARN_LIMIT value plus a digital hysteresis of 0x80, which corresponds to the following current levels, depending on the V_{SNS_CS} setting and assuming a 1 mΩ sense resistor:

Table 29 Current hysteresis

V_{SNS_CS} (mV)	12.5	25	50	100
Current (A)	0.55	1.11	2.2	4.4

In order to avoid false triggering of OUC warning due to low current levels during INIT_REG_SOA or at the beginning of ON states, its detection starts only after current goes above the programmed OUC level for the first time in ON state.

SOA Regulation (SOAR) Warning

A warning is issued when the controller enters the I_REG state due to OC or SOA conditions violation if SOAR_TMR[2:0] is not programmed to 0. The warning remains set until the controller leaves the I_REG state.

Negative Current (INeg) Warning

If negative current through the FET over I_{NEG_MAX} level is detected, an INeg warning is triggered. The warning is cleared when the FET/load current sample returns to positive level (≥ 0 A).

Overtemperature (OT) Warning

If temperature raises above OT_WARN_LIMIT, an OT warning is issued. The warning is cleared when the temperature falls below OT_WARN_LIMIT minus a hysteresis of 25°C.

On-chip Thermal Shut-Down (TSD) Warning

XDP711 has an on-chip temperature sensor. If, during power-up procedure, normal operation or FAULT state, temperature exceeds an upper threshold of 125°C, a warning is triggered. The warning is cleared when the temperature falls below 115°C.

5.6.5 Communication warning

PMBus Interface Communication (COM) Warning

This warning is triggered if the PMBus communication (read or write) is detected with fails. COM is the only warning that is enabled during LATCH_OFF state. Since the WARN pin status is latched during this state, the warning is not reported through the pin. The only way to detect this warning during LATCH_OFF is to read the STATUS_CML command.

Note: WARN pin is not cleared by clearing STATUS_CML after a COM warning. WARN pin is a reflection of COMM bit in STATUS_WARNS command, so this is the bit that has to be cleared in order for the WARN pin to be cleared.

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5.7 Telemetry

XDP711 provides real time accurate measurement and calculation data for:

- Input voltage
- Output voltage
- Load/FET current (by means of voltage drop over external shunt resistor), including its squared RMS value (if enabled)
- Input power
- Energy
- External FET temperature
- On-chip temperature

All information is provided through the PMBus interface by issuing the corresponding commands.

The following figure shows the telemetry flow:

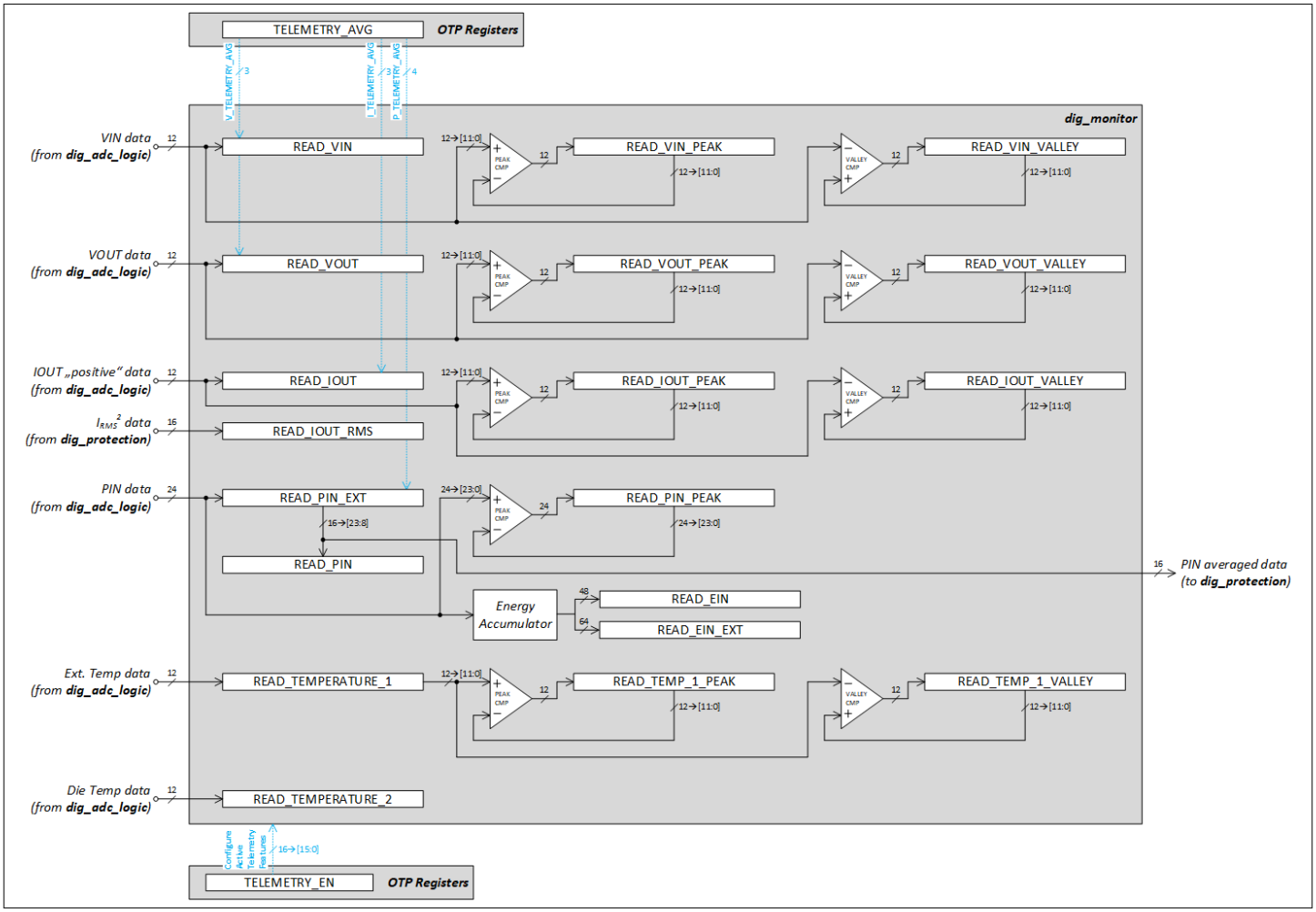

Figure 9 XDP711 Telemetry flow

5.7.1 Telemetry summary table

The following table shows the sensing points of the different telemetry features and the commands to be used for configuration and to get the data read.

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Table 30 Telemetry summary

Parameter	Sensing	Averaging configuration	Instantaneous/ averaged	Peak	Valley
Input voltage	ISNS_P pin	V_TELEMETRY_AVG	READ_VIN	READ_VIN_PEAK	READ_VIN_VALLEY
Load/FET current	ISNS_P/ISNS_N pins	I_TELEMETRY_AVG	READ_IOUT	READ_IOUT_PEAK	READ_IOUT_VALLEY
RMS Load/FET current	ISNS_P/ISNS_N pins	–	READ_IOUT_RMS	–	–
Output voltage	VOUT pin	V_TELEMETRY_AVG	READ_VOUT	READ_VOUT_PEAK	READ_VOUT_VALLEY
Input power (16 bits)	Input voltage x Load/FET current	P_TELEMETRY_AVG	READ_PIN	–	–
Input power (24 bits)			READ_PIN_EXT	READ_PIN_PEAK	–
Energy (48 bits)	Input power accumulated over time	–	READ_EIN	–	–
Energy extended (64 bits)		–	READ_EIN_EXT	–	–
External FET temperature	TSNS_P/TSNS_N pins	–	READ_TEMPERATURE_1	READ_TEMP_1_PEAK	READ_TEMP_1_VALLEY
On-Chip temperature	On-chip temperature sensor	–	READ_TEMPERATURE_2	–	–

5.7.2 Averaged and instantaneous telemetry

5.7.2.1 Averaging telemetry data

Input voltage and power and output voltage and current measurements can be averaged by means of their corresponding bit fields: V_TELEMETRY_AVG[2:0], I_TELEMETRY_AVG[2:0] and P_TELEMETRY_AVG[3:0]. Voltage and current averaging bit fields consist of three bits:

Table 31 Voltage and current telemetry averaging

Bits settings	Averaged number of samples
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

And power averaging bit field consists of four bits:

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Table 32 Power telemetry averaging

Bits settings	Averaged number of samples
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

5.7.2.2 Instantaneous telemetry data

Instantaneous measurements can be obtained by setting the corresponding x_TELEMETRY_AVG[2:0] bits to 000 or P_TELEMETRY_AVG[3:0] to 0000, so that only one sample is taken.

5.7.3 Peaks and valleys

x_PEAK and x_VALLEY commands report the maximum and minimum values (respectively) measured since the last time the command was cleared.

Peaks apply for the following parameters:

- Input voltage
- Output voltage
- Load/FET current
- Input power
- External FET temperature

Valleys apply for the following parameters:

- Input voltage
- Output voltage
- Load/FET current
- External FET temperature

The x_PEAK and x_VALLEY commands are cleared after reading their contents or by means of a power on reset. After reset, the first value read is compared to 0x000 (peaks) or 0xFFF (valleys) and it becomes a new peak or valley respectively.

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As shown in Figure 9, peaks and valleys are calculated from instantaneous data, before it is averaged and regardless of the averaging setting.

5.7.4 Telemetry via PMBus

The following formula converts from PMBus direct format to "real world" values:

$$X = \frac{1}{m} * \left(Y * 10^{-R} - b\right) \tag{4}$$

Where:
X = Calculated "real world" value in the appropriate units (A, V, °C, etc)
m = Slope coefficient, is a two byte, two's complement integer
Y = Two byte two's complement integer received from the PMBus device
b = Offset, is a two byte, two's complement integer
R = Exponent, is a one byte, two's complement integer

To convert from "real world" values to PMBus direct format, use the following formula:

$$Y = \left(mX + b\right) * 10^{R} \tag{5}$$

Where:
Y = two byte two's complement integer to be sent to the unit
m = Slope coefficient, is the two byte, two's complement integer
X = "real world" value, in units such as Amperes or Volts, to be converted for transmission
b = Offset, is the two byte, two's complement integer
R = Exponent, is the decimal value equivalent to the one byte, two's complement integer.

Coefficients for these formulas are specified in the following table:

Table 33 PMBus coefficients

Command	VTLM_RNG	VSNS_CS	m	b	r
VOUT_OV_WARN_LIMIT,	88	-	4653	0	-2
VOUT_UV_WARN_LIMIT,	44		9307	0	-2
VOUT_UV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_FAULT_LIMIT, READ_VIN, READ_VIN_PEAK, READ_VIN_VALLEY, READ_VOUT, READ_VOUT_PEAK, READ_VOUT_VALLEY	22		18614	0	-2
IOUT_OC_WARN_LIMIT,	-	12.5	23165	0	-2

(table continues...)

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Table 33 (continued) PMBus coefficients

Command	VTLM_RNG	VSNS_CS	m	b	r
IOUT_UC_WARN_LIMIT, READ_IOUT, READ_IOUT_PEAK, READ_IOUT_VALLEY		25	11582	0	-2
		50	5791	0	-2
		100	28956	0	-3
READ_IOUT_RMS	-	12.5	20808	0	-2
		25	5202	0	-2
		50	13005	0	-3
		100	32513	0	-4
READ_PIN_EXT, READ_PIN_PEAK	88	12.5	10780	0	0
		25	5390	0	0
		50	26949	0	-1
		100	13474	0	-1
	44	12.5	21559	0	0
		25	10780	0	0
		50	5390	0	0
		100	26949	0	-1
	22	12.5	4312	0	1
		25	21559	0	0
		50	10780	0	0
		100	5390	0	0
PIN_OP_WARN_LIMIT, READ_PIN, READ_EIN	88	12.5	4211	0	-2
		25	21054	0	-3
		50	10527	0	-3
		100	5263	0	-3
	44	12.5	8422	0	-2
		25	4211	0	-2
		50	21054	0	-3
		100	10527	0	-3
	22	12.5	16843	0	-2
		25	8422	0	-2
		50	4211	0	-2
		100	21054	0	-3

(table continues...)

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Table 33 (continued) PMBus coefficients

Command	VTLM_RNG	VSNS_CS	m	b	r
OT_FAULT_LIMIT, OT_WARN_LIMIT, READ_TEMPERATURE_1, READ_TEMP_1_PEAK, READ_TEMP_1_VALLEY	-	-	52	14321	-1
READ_TEMPERATURE_2	-	-	23	6225	-1

Note: Current and power coefficients are normalized to a 1 mΩ sense resistor. See Calculating PMBus direct format limits from "real world" values and vice-versa for examples on how to calculate current and power.

5.7.5 RMS current calculation

RMS current is calculated by integrating the current measurements over a specific period of time set by RMS_SAMPLE_TMR[1:0] bits in the SOA_TMR command.

5.7.6 Input power calculation

Input power is a multiplication of the load/FET current and the input voltage values.

Each time a current measurement is performed, a power calculation is performed, multiplying the recent values of load/FET current and the input voltage together before their corresponding averaging. Input power can be reported in 16 bits format (READ_PIN) or an extended 24 bits format (READ_PIN_EXT).

5.7.7 Energy calculation

Energy is the input power accumulated over time.

The calculated input power value is added to a power accumulator command that may increment a rollover counter if the value exceeds the maximum accumulator value. The power accumulator command also increments a power sample counter. The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time.

The MCU reading the data assigns a time stamp when the data is read. By calculating the time difference between consecutive uses of READ_EIN and determining the delta in power consumed, it is possible for the MCU to determine the total energy consumed over that period.

ROLLOVER_COUNT bit field in READ_EIN_EXT command has 16 extra bits for an extended energy reading.

5.8 Analog IMON/PMON

An analog monitoring and reporting (AMON) of FET current (IMON) or input power (PMON) signal can be output at the IST pin by configuring the corresponding bits in TELEMETRY_CFG PMBus command.

As shown in Figure 10, information is taken from IOUT data path and PIN data output, which goes into a digital multiplexer (1), configurable by means of TELEMETRY_CFG PMBus command. Output of the multiplexer then goes to an IDAC (2), which outputs a current level proportional to the corresponding current or power digital input at the IST pin.

To reduce the noise, it is recommended to add an output RC low pass filter with a bandwidth of 50 kHz to 80 kHz at the IST pin. To calculate this filter and corresponding current and power levels based on the AMON output, see Calculating AMON resulting current and power.

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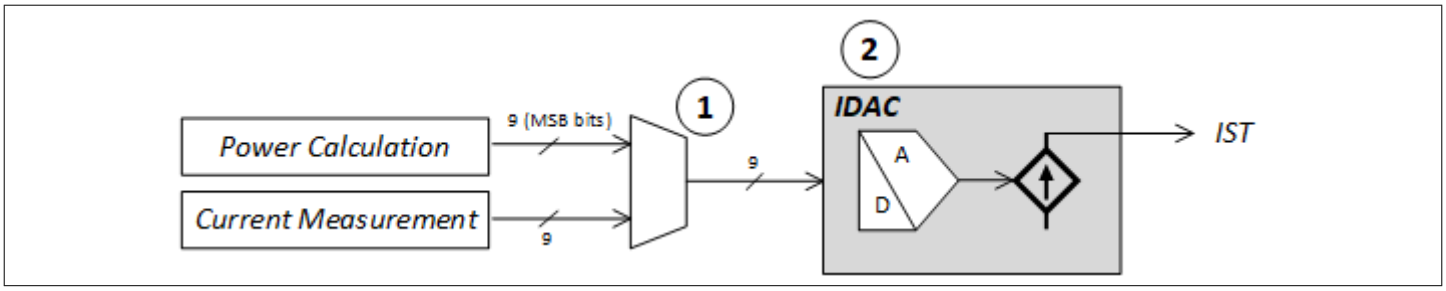

Figure 10 AMON generation

5.9 Communication interfaces

5.9.1 PMBus

The power management bus (PMBus) is an open-standard digital power management protocol: simple, standard, flexible, extensible, and easy to program. The PMBus command language enables communication between components of a power system: CPUs, power supplies, power converters, and more.

XDP711 supported features and commands are based on the PMBus Specification Rev 1.3.1 parts I, II and III.

Communication via PMBus is possible right after internal circuitry initialization, which takes around 2 ms after input voltage is applied.

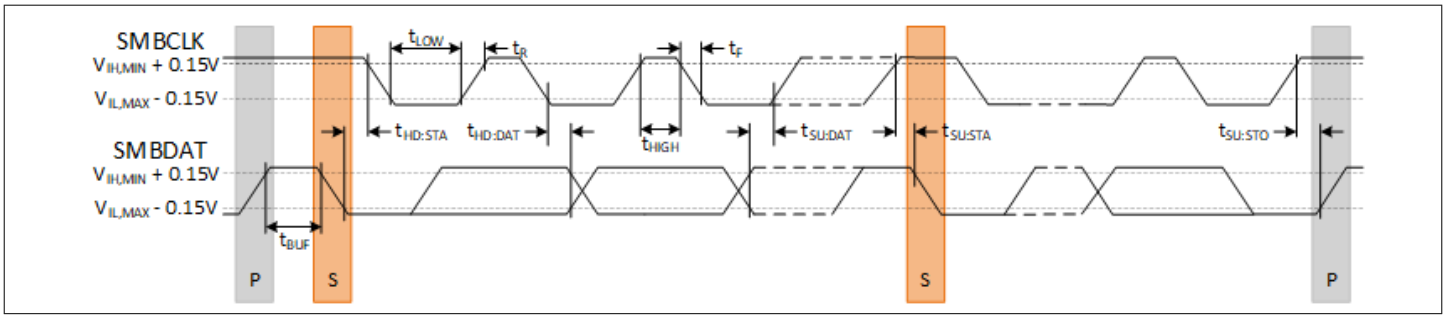

Figure 11 PMBus timing diagram

PMBus communication is enabled by default. It is possible to disable it by means of the PMBus enable signal, which can be configured in GPO3 pin in the GPO_CFG command. If it is configured as PMBus enable, a low level on this pin will disable PMBus communication. This feature is useful in case it is desired to configure different addresses digitally in many devices connected to a single bus.

5.9.1.1 Supported functions

The PMBus is specified to cover a lot of different applications in the realm of power management. For a hot-swap application, only a subset of commands is used.

5.9.1.1.1 Addressing

The device has a slave address controlled by PMBUS_CFG command or by address pins. There are 16 different addresses available for external resistor setting. See Table 15.

5.9.1.1.2 Protocol violations

XDP711 supports the following protocol violations:

- Command not valid
- Command too short
- Data not valid
- Error at repeated start

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- Extra Byte in command
- Page not valid
- Read bit set in address
- Read too few bits
- Read too few bytes
- Read too many bytes
- Send too few bits
- Send too many bytes

5.9.1.1.3 Timeout

If a device is holding onto the bus then the bus may freeze. If the microcontroller sees such an issue it may stop the clock for $t_{TIMEOUT}$. This may also happen if another slave holds the bus incorrectly. This causes all slaves to reset their PMBus interfaces and be ready for a new start command.

5.9.1.2 Protocol

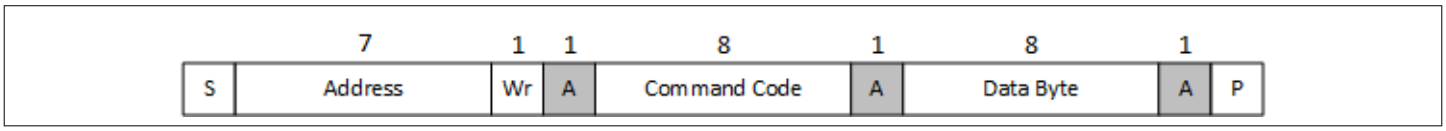

Figure 12 Write Byte protocol

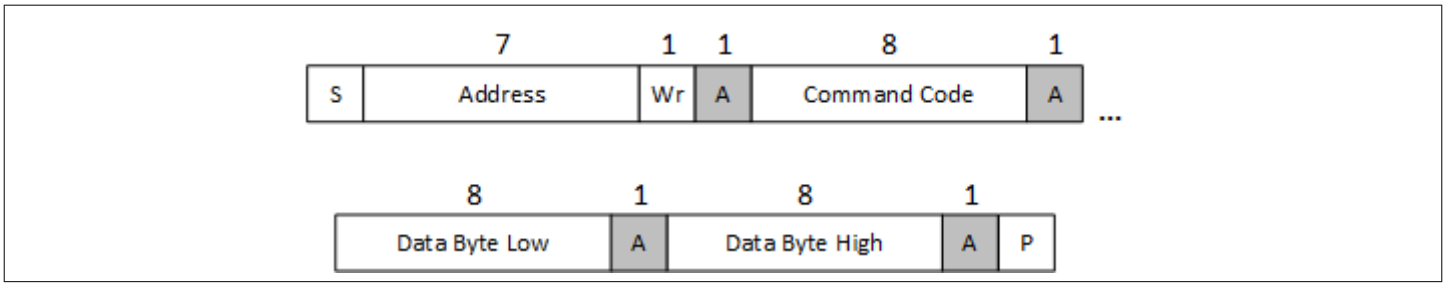

Figure 13 Write Word protocol

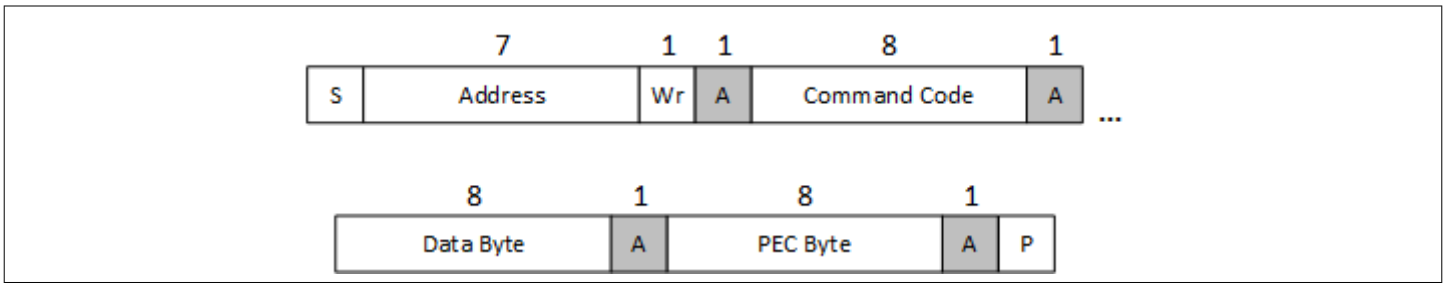

Figure 14 Write Byte protocol with PEC

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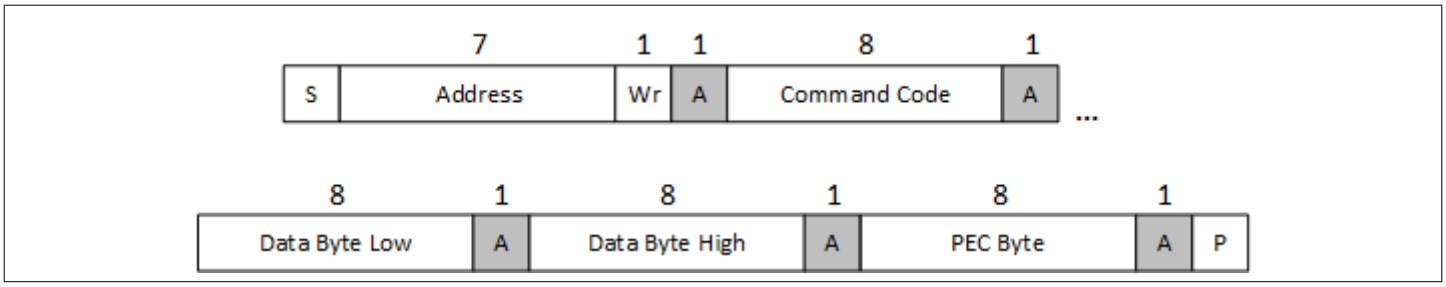

Figure 15 **Write Word protocol with PEC**

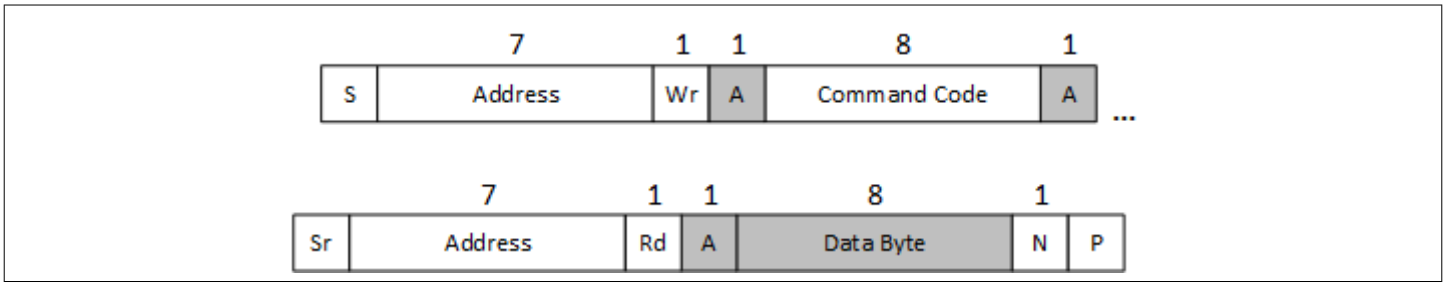

Figure 16 **Read Byte protocol**

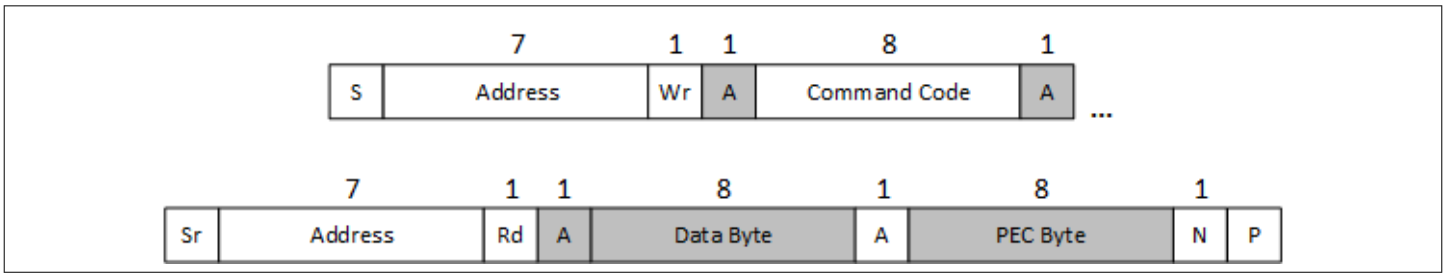

Figure 17 **Read Byte protocol with PEC**

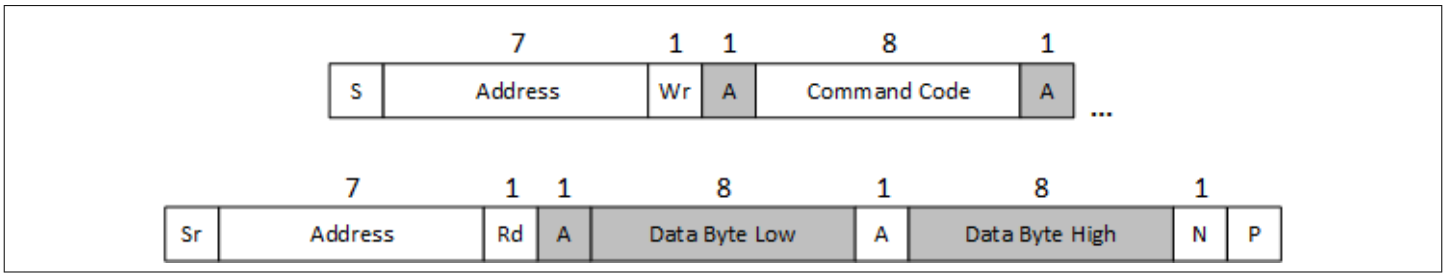

Figure 18 **Read Word protocol**

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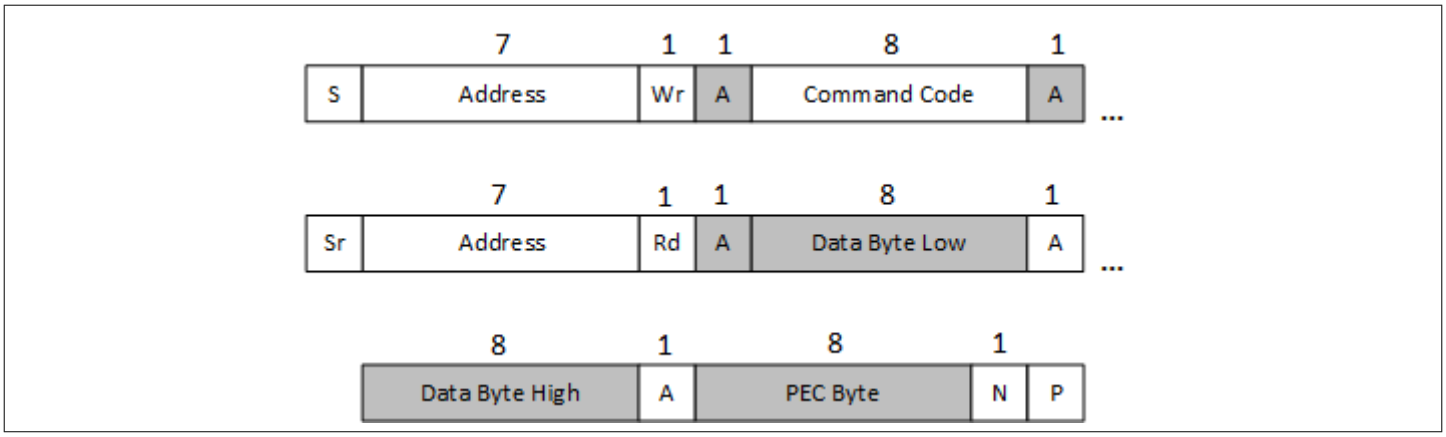

Figure 19 **Read Word protocol with PEC**

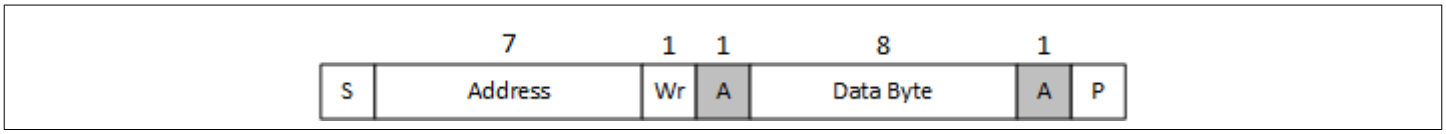

Figure 20 **Send Byte protocol**

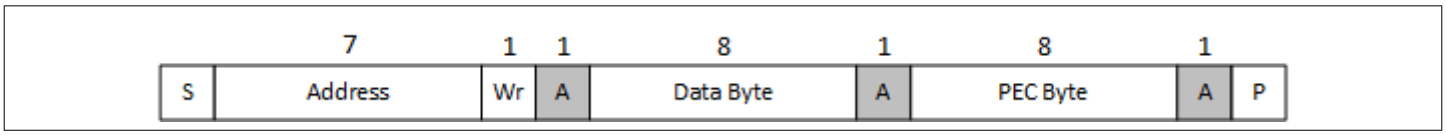

Figure 21 **Send Byte protocol with PEC**

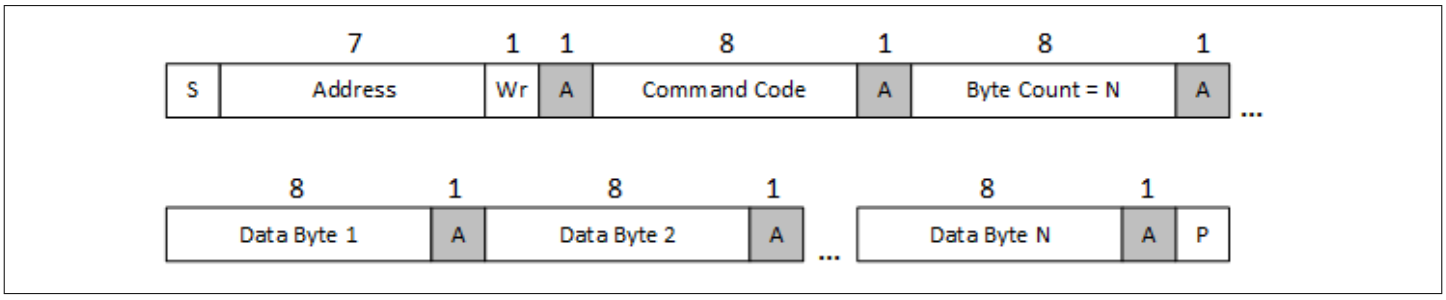

Figure 22 **Block Write**

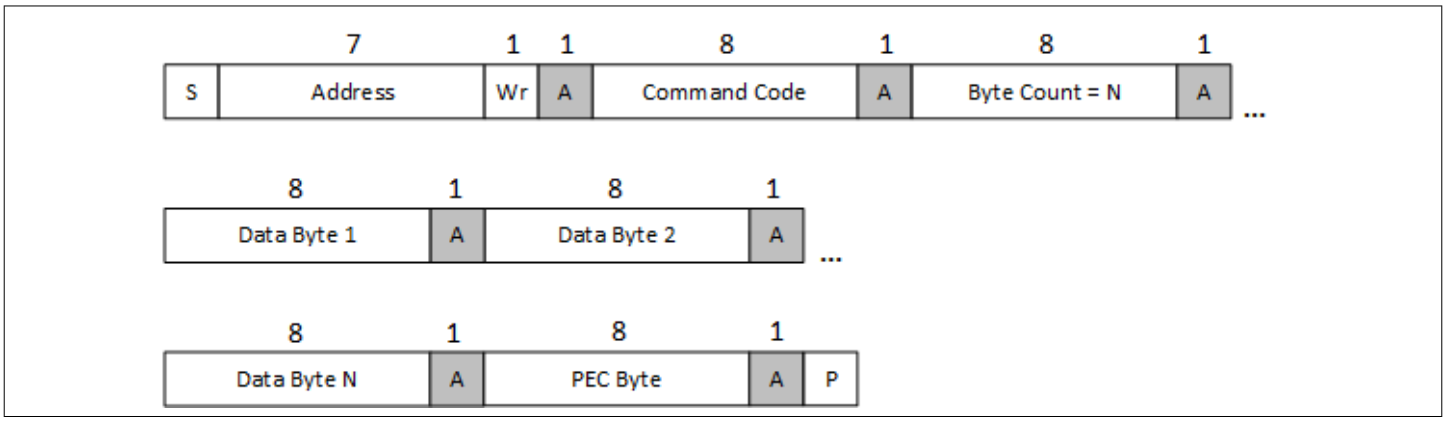

Figure 23 **Block Write with PEC**

Downloaded from Arrow.com.

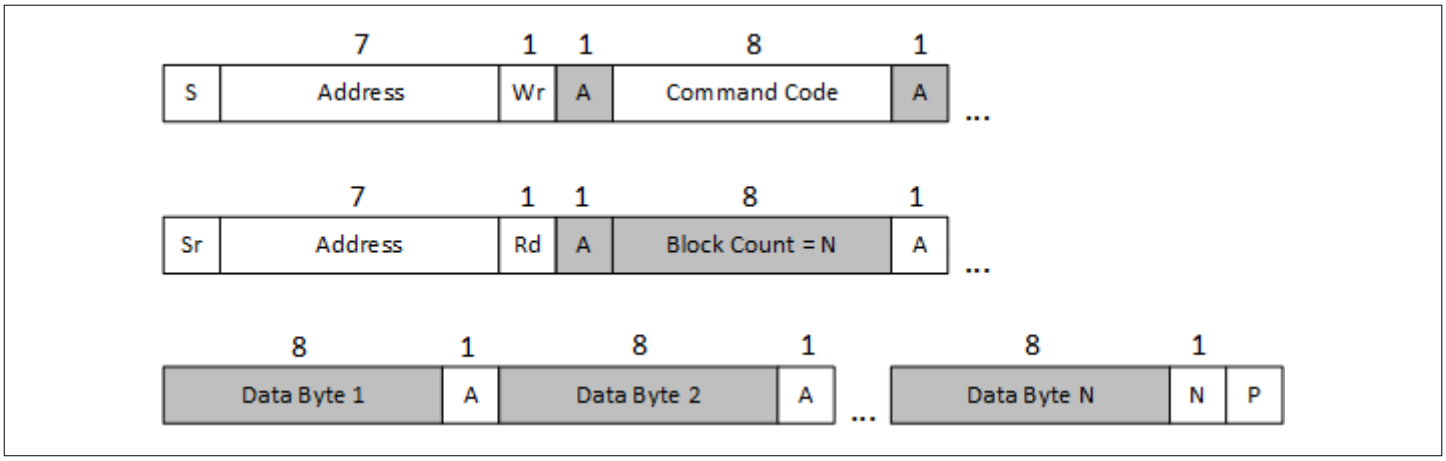

Figure 24 **Block Read**

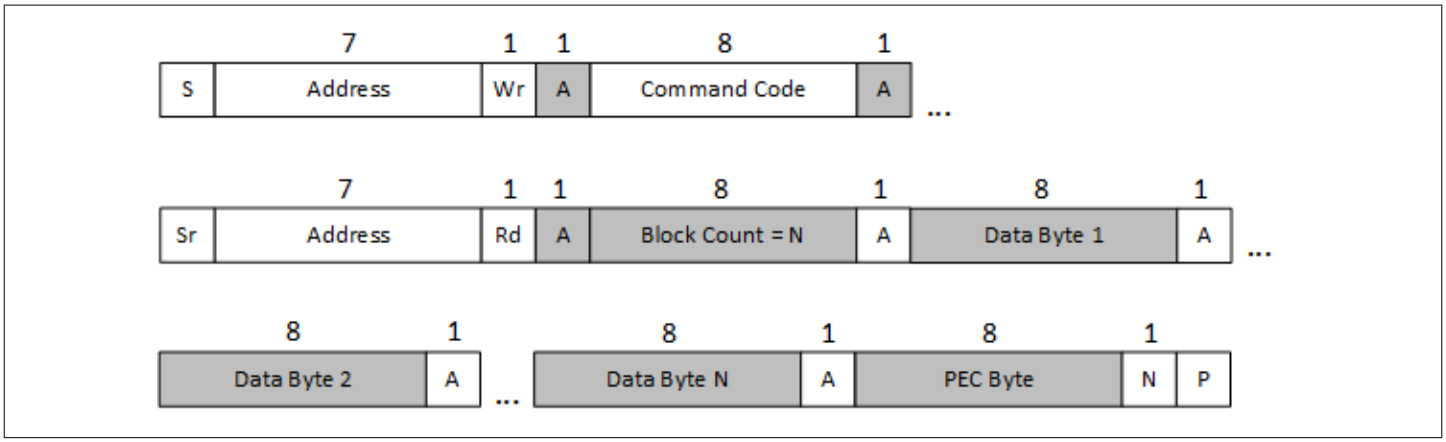

Figure 25 **Block Read with PEC**

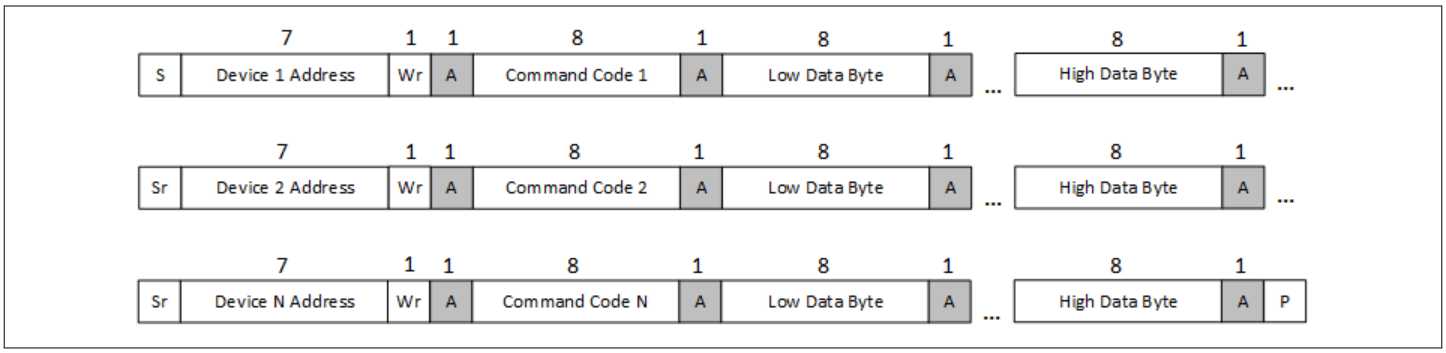

Figure 26 **Group Command protocol**

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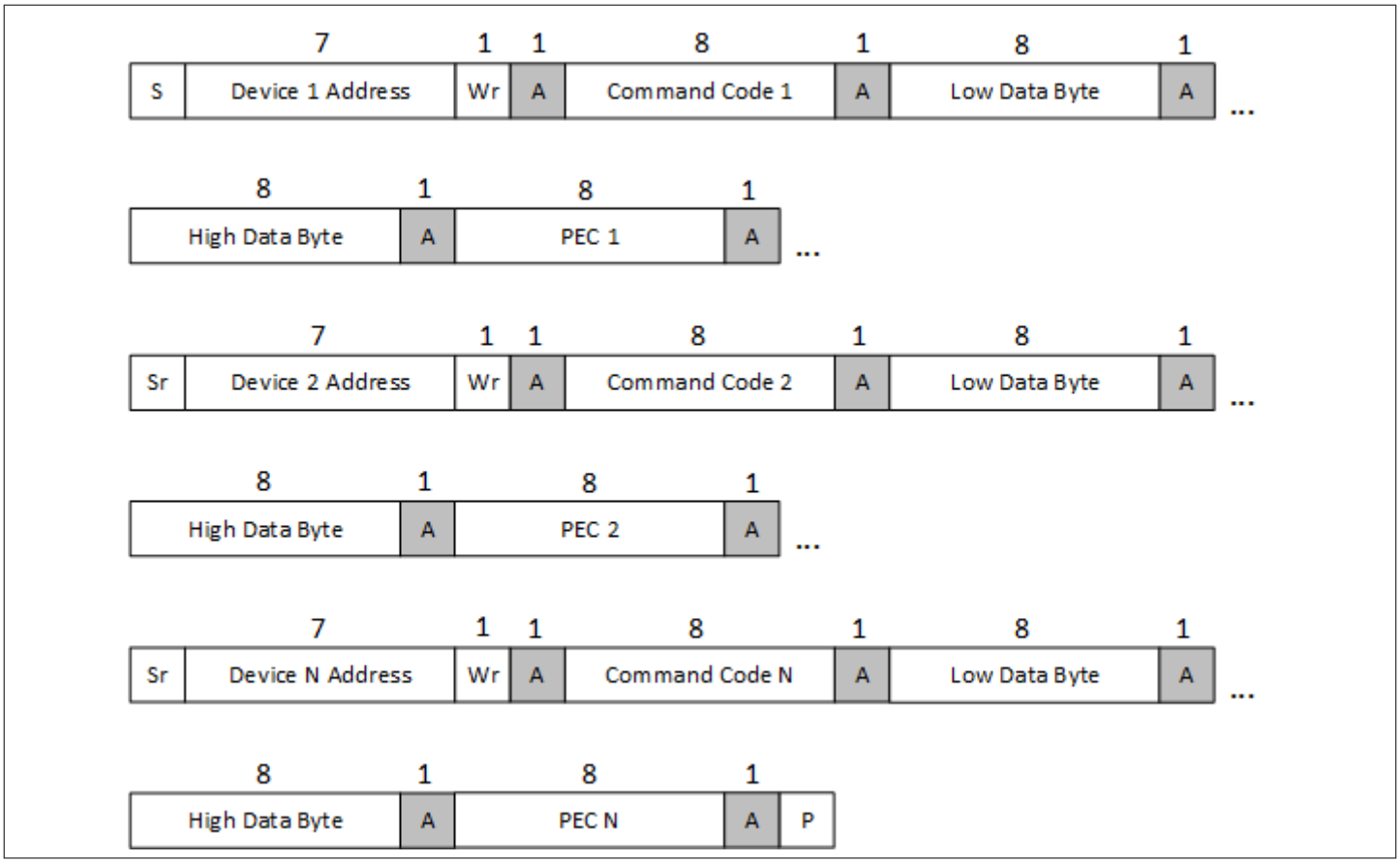

Figure 27 **Group Command protocol with PEC**

Alert Response Address

XDP711 supports SMBus alert response address. This is a method to allow the microcontroller to locate the device that has issued an alert if there are multiple devices connected to the same bus.

1. Device issues an SMBALERT on GPO1 or GPO3 (depending on GPO_CFG command configuration). This is just a normal fault being signaled.
2. Microcontroller sends a special address 0x0C with READ bit "1" (i.e. 0x19).
3. Device responds with its own address:
   - If more than one device responds, the lowest address wins and disables its alert.
4. The microcontroller continues to process all alerts by the same process until there are no alerts signaled.

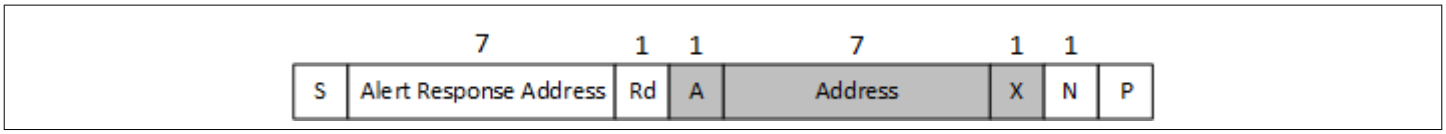

Figure 28 **A 7-bit-Addressable Device responds to an ARA**

Figure 29 **A 7-bit-Addressable Device responds to an ARA with PEC**

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5.10 Memory

XDP711 has three types of memory for programmability:

- Volatile memory
- One time programmable (OTP)
- Multiple time programmable (MTP)

The one time programmable (OTP) memory can be used to fix and save specific command settings. At power-up, during READ_CFG state, all the settings saved in the OTP memory are copied into volatile memory. OTP memory is partitioned into two sub-sections: One for storing PMBus Register values and another for storing user defined SOA data (SOA PMBus command).

XDP711 contains 10 pages of MTP for a multiple time programmability. When the number of reprogramming reaches 10 (indicated by MTP_FULL bit in STATUS_MEM command), the circuit keeps the latest programmed values. The command contained in this memory section is I_SNS_CFG, which contains the following configuration bits: CS_RNG, CS_RNG_TRIM, SOC_FAULT_LIMIT and START_ILIM.

To program the desired settings in internal commands or OTP at power-up, the following steps must be followed:

- Apply a voltage at the VDD_VIN pin:
  - ≥ 7 V to program commands
  - ≥ 20 V to program OTP or MTP memory
- Keep ISNS_P pin connected to the input voltage source that supplies VDD_VIN pin. Input voltage level is sensed through ISNS_P to make sure the level is appropriate for OTP programming.
- Keep the UV/EN pin at chip GND potential
- Communication via PMBus is possible as soon as STANDBY state is entered. At this point, commands, OTP or MTP memory can be programmed.
- For a successful programming, internal temperature of the device must stay below 125°C at all times.

To program OTP or MTP sections:

1. Program the commands in volatile memory as desired.
2. Select the section to be programmed by means of the SEL_SEC bits in WRITE_OTP command.
3. Set the WRITE_OTP bit.
4. The command configuration is automatically copied to the selected section.

If the MTP section is selected, XDP711 automatically locates the latest available page and program it.

PROG_BLOCK and OTP_FAIL indicate the status of the OTP and MTP memory programming according to the following table:

Table 34 OTP programming status

PROG_BLOCK	OTP_FAIL	Meaning
0	0	OTP, MTP or OTP SOA programming has succeeded if OTP_USER, MTP_USER or SOA_PRG bits are set. Otherwise, programming has not started.
0	1	OTP programming started but failed during programming because of OTP issue. Part must be discarded.
1	0	OTP programming must not be started since temperature or input supply are out of range.
1	1	OTP programming started but failed during programming because temperature or voltage going out of range during programming. Part must be discarded.

Once programmed, OTP_USER bit indicates that the OTP memory has been programmed successfully and MTP_USER bits indicates that MTP memory is in use.

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Before programming, PROG_BLOCK must be checked in order to determine if temperature and VIN are in range and programming is allowed. PROG_BLOCK indicates the temperature and voltage status in real time. If, after checking PROG_BLOCK, but before programming starts, any of these conditions goes out of range, programming will be blocked, PROG_BLOCK will be set and OTP_FAIL will remain 0. It is possible that, after a blocked attempt of programming, temperature and voltage go back in range, so PROG_BLOCK will read 0 again. Due to this, it is important to note that, as long as OTP_USER and OTP_FAIL are 0, it is still possible to program OTP.

If temperature and voltage conditions go out of range during programming, OTP_FAIL will indicate an unsuccessful programming after the operation. If temperature and voltage go back in range, PROG_BLOCK will read 0 again and it is only OTP_FAIL that indicates the programming failed.

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6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Typical application schematics

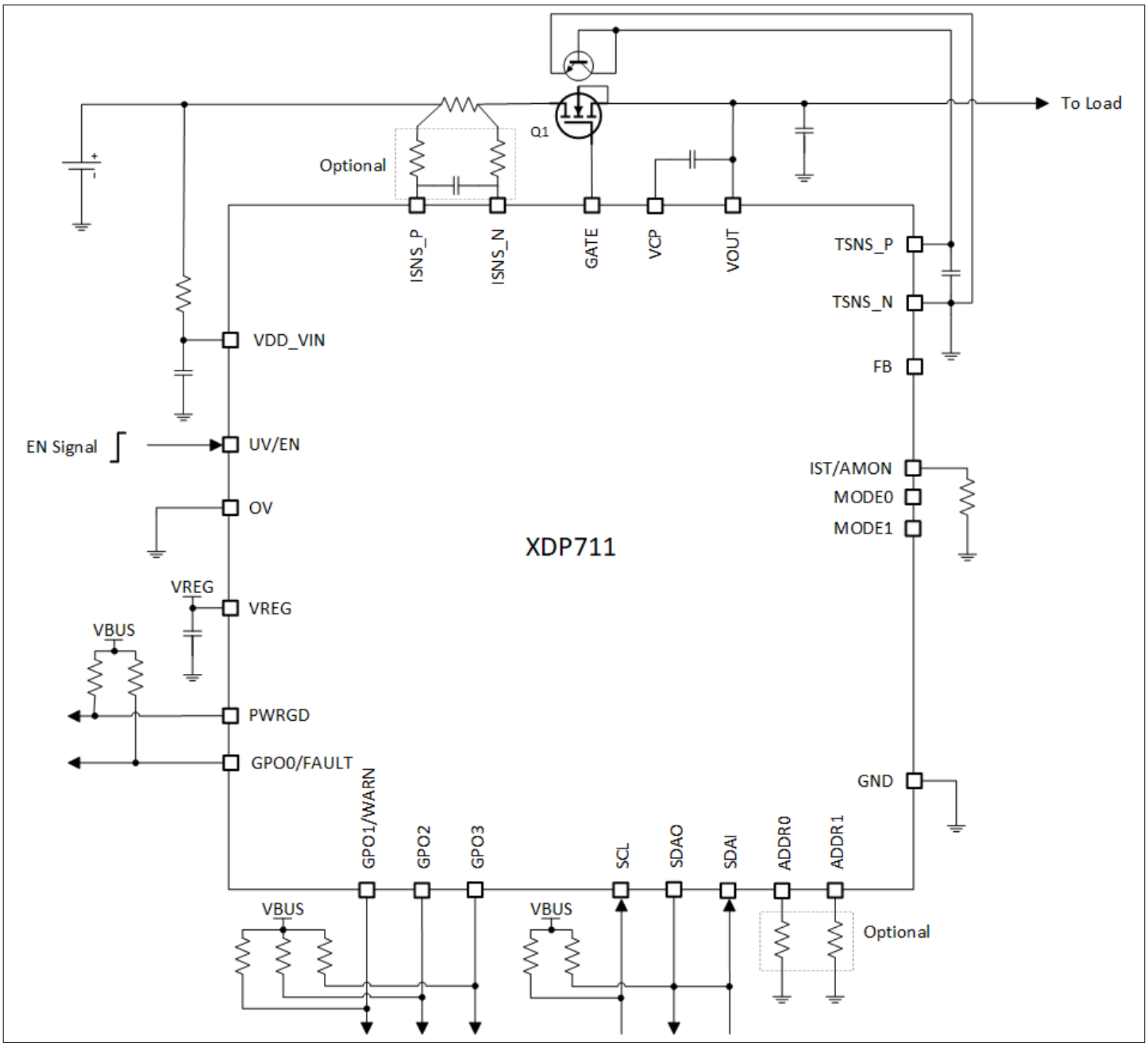

Figure 30 **Fully digital mode DCM (MODE:MODE=0x1) application schematic**

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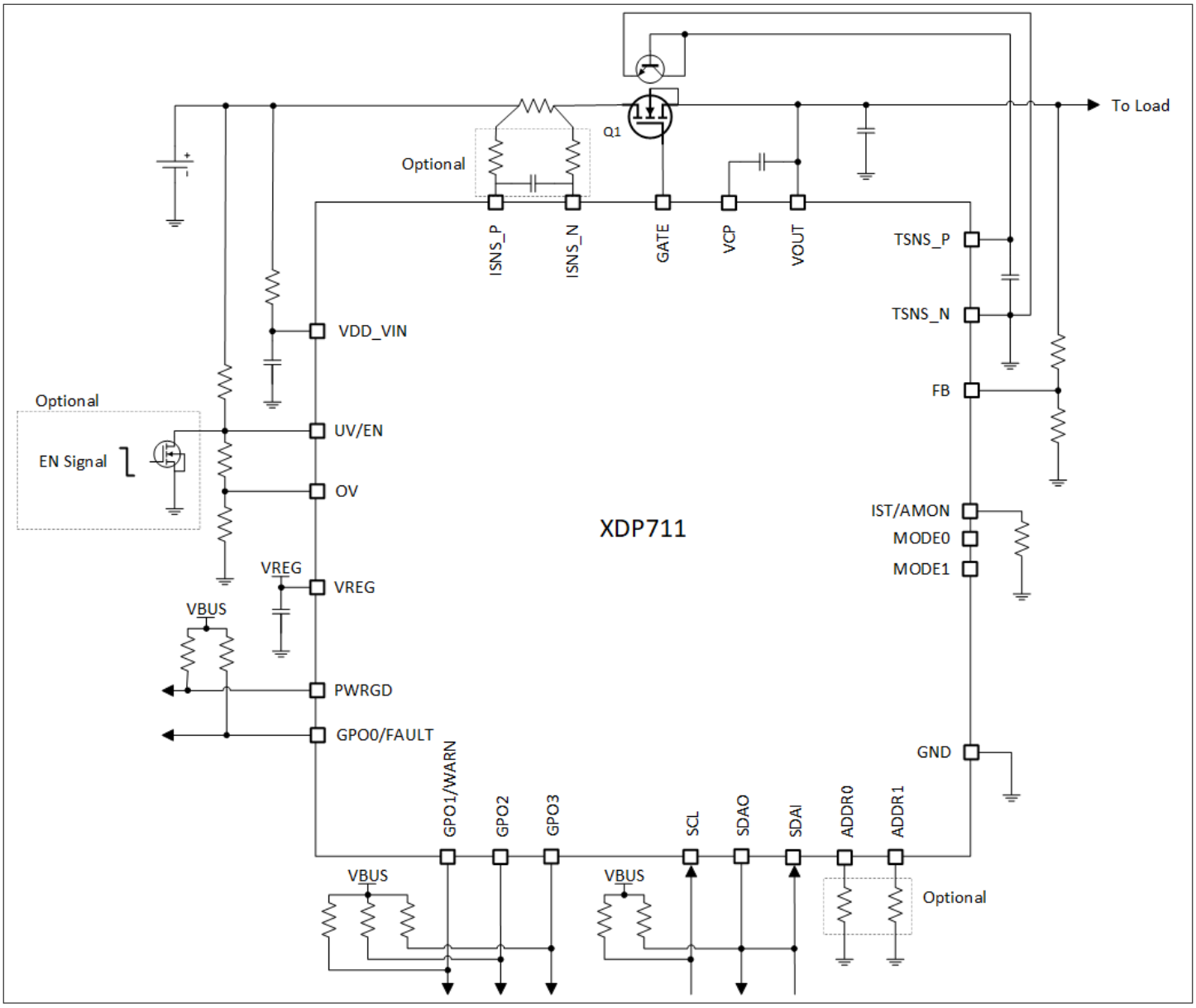

Figure 31 **Fully digital mode ACM (MODE:MODE=0x0) application schematic**

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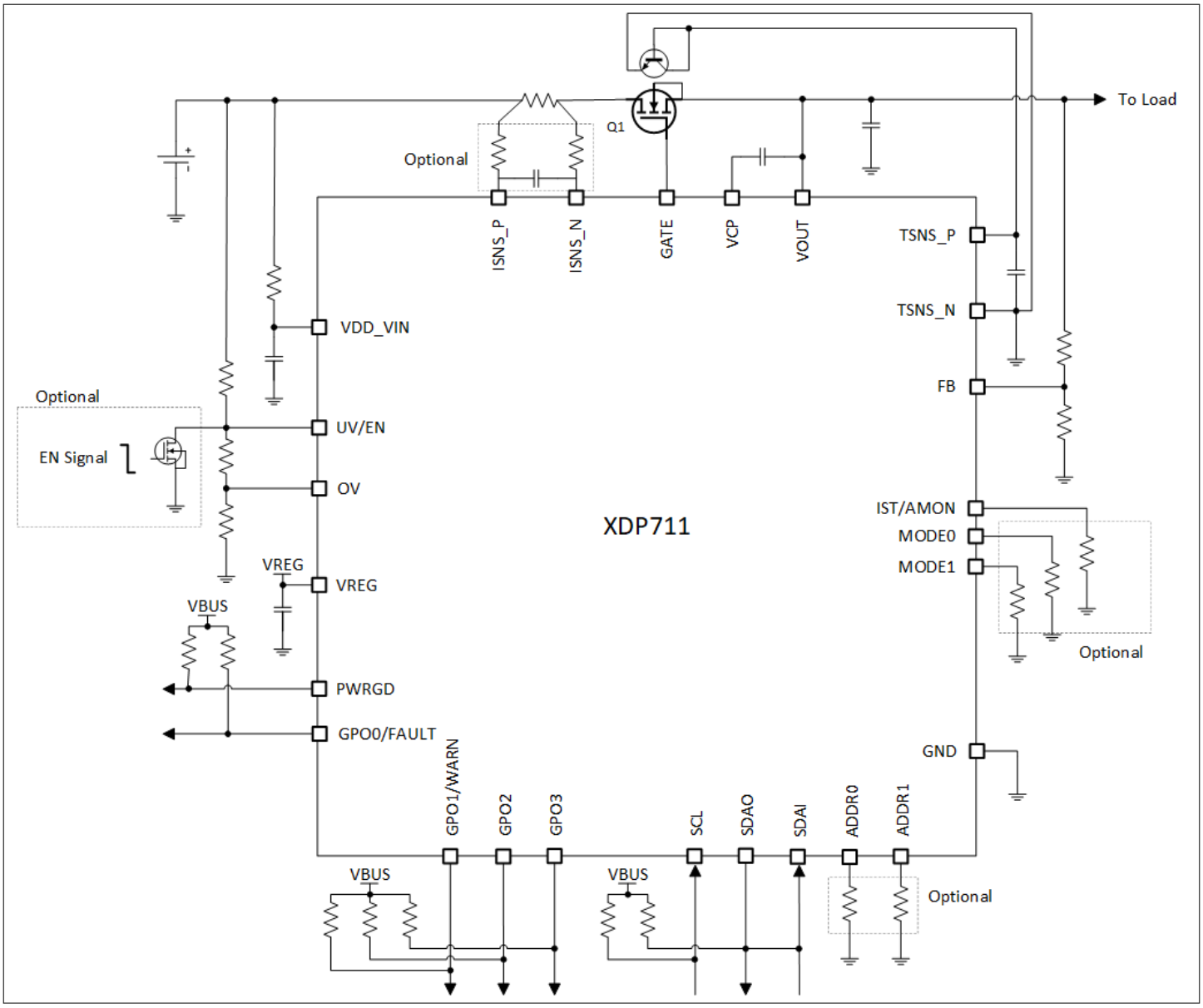

Figure 32 **Analog assisted digital mode application schematic**

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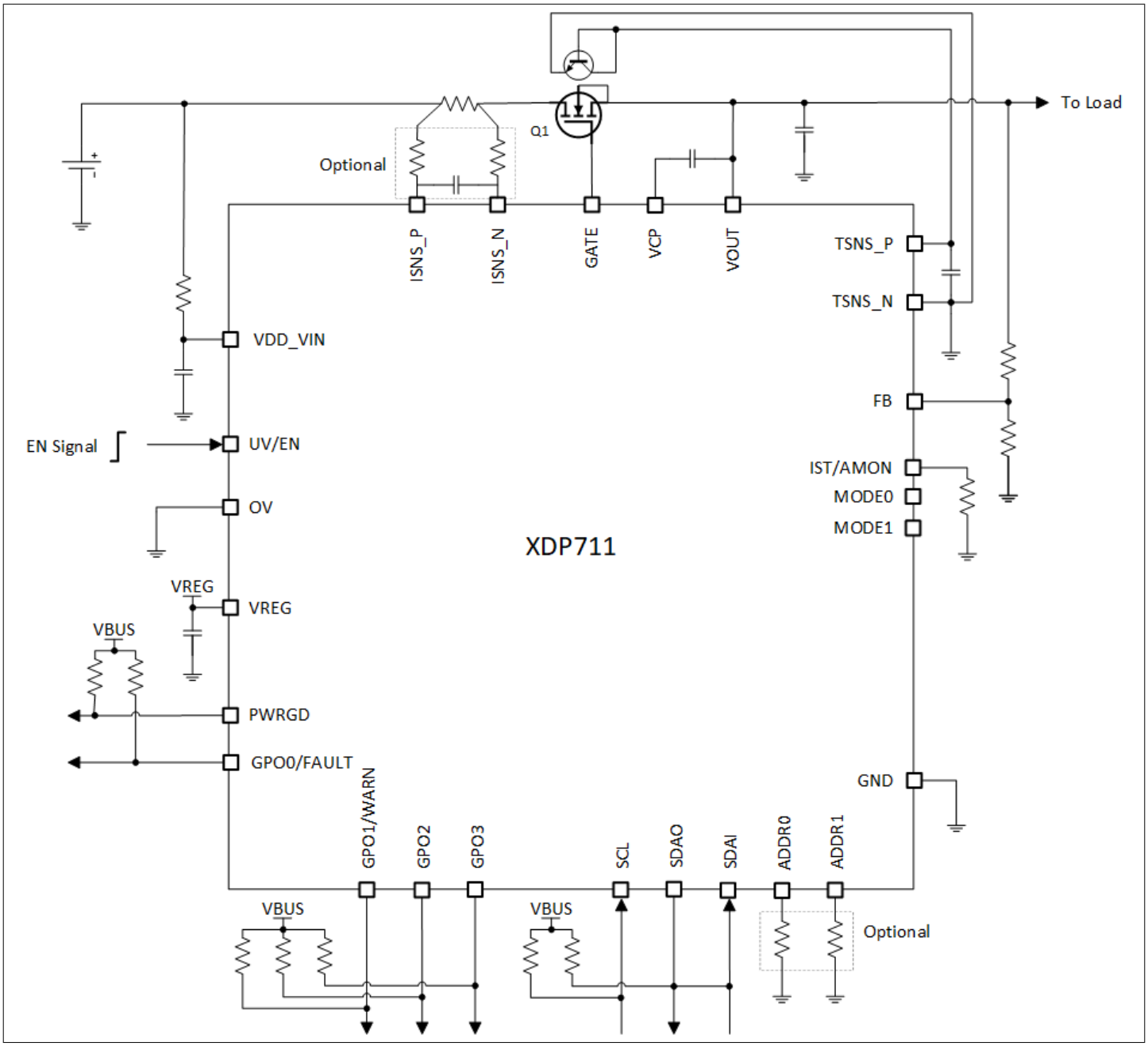

Figure 33 **Hybrid mode (MODE:MODE=0x1, FB_COMP_SEL=0x1) application schematic**

6.2 Setting Ioc

The overcurrent (I_{OC}) limit is set by means of programming the maximum allowed voltage drop between the ISNS_P and ISNS_N pins V_{SNS_CS}. This voltage can be programmed to 12.5 mV, 25 mV, 50 mV or 100 mV.

Lower voltages are more convenient for high current applications and vice-versa. Lower voltages also give the advantage of reducing the power dissipation over the resistor. Higher voltages help improve the accuracy of the measurement due to the ADC resolution.

To select the current sense shunt resistor R_{SNS} calculate:

$$R_{SNS}\left[m\Omega\right] = \frac{V_{SNS_CS}[mV]}{I_{OC}[A]} \tag{6}$$

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where I_{OC} is the maximum desired/allowed constant OC current in Amperes.

Once the resistor is calculated, its value must be chosen from the list provided in the description of the RSNS[5:0] bits of the REG_CFG command. Its value must be set accordingly in these bits. To reduce the power dissipation and for an optimum regulation performance, a sense resistor value between 0.2 mΩ and 10 mΩ is mandatory.

The current sense ADC is designed to sense a maximum current of 83.3 A. Care must be taken when selecting the sense resistor value so that this limit is not exceeded. In addition to the V_{SNS_CS} level, the current limit can be trimmed by means of the CS_RNG_TRIM[7:0] bits, according to the following formula:

$$LIMIT = \frac{I_{OC_TRIMMED} * R_{SNS} * 180.31}{V_{SNS_CS}} \quad (7)$$

Where LIMIT is the decimal value to be programmed in the command, $I_{OC_TRIMMED}$ is the desired current limit value in Amperes, R_{SNS} is the value of the chosen current sense resistor in mΩ and V_{SNS_CS} is the programmed OC value in mV.

Note: For an optimum stability operation, I_{OC} must be ≥ I_{OC_MIN}. If a current limit lower than this is needed, it can be trimmed by means of the CS_RNG_TRIM[7:0] bits. The following table shows minimum and maximum recommended sense resistor values for each one of the V_{SNS_CS} settings:

Table 35 Minimum and maximum recommended sense resistor values

V_{SNS_CS}	Min. R_{SNS} [mΩ]	Equivalent I_{OC} with min. R_{SNS} [A]	Max. R_{SNS} [mΩ]	Equivalent I_{OC} with max. R_{SNS} [A]
12.5	0.2	62.5	2.5	5
25	0.3	83.3	5	5
50	0.6	83.3	10	5
100	1.2	83.3	10	10

6.3 Setting OV, UV and OUV in ACM or Hybrid mode

OV and UV values are set with a three resistor voltage divider, as shown in the following figure:

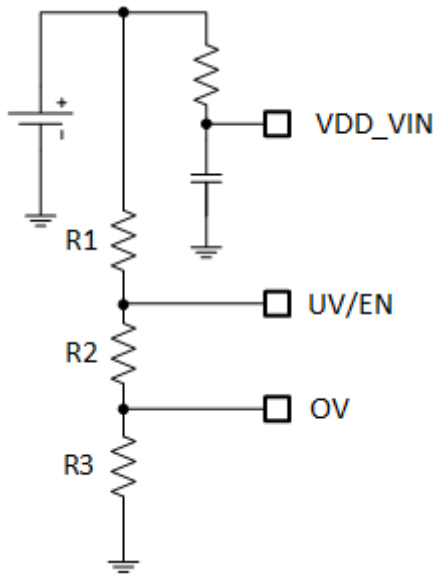

Figure 34 Setting OV and UV in ACM

Calculate the resistors values according to the application specific parameters using the following formulas:

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$$R3 = \frac{R_{TOTAL} * OV_{REF}}{V_OV} \tag{8}$$

$$R2 = \frac{R_{TOTAL} * UV_{REF}}{V_UV} - R3 \tag{9}$$

$$R1 = R_{TOTAL} - R2 - R3 \tag{10}$$

Where V_OV and V_UV are desired OV and UV levels respectively, $OV_{REF} = V_{OV_UTH}$, $UV_{REF} = V_{UVEN_LTH}$ and R_{TOTAL} is calculated after the desired current flow (typically hundreds of µA).

Care must be taken to avoid exceeding the maximum voltage level at the OV or UV pins.

Output Under Voltage (OUV) feature monitors the output voltage and detects when it goes down due to FET gate-to-drain leakage, degraded R_{DSON} or high FET V_{DS} due to current regulation.

The FB pin has an internal comparator with a reference V_{REF} of 1.11V and a hysteresis of 50mV.

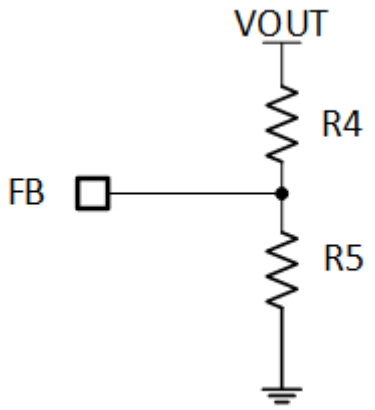

Figure 35 Setting OUV in ACM

To set the minimum allowed output voltage, choose R4 around 100KΩ, then calculate R5:

$$R5 = \frac{V_{REF} * R4}{OUV - V_{REF}} \tag{11}$$

where OUV is the minimum allowed output voltage.

6.4 Calculating VCP and Cgs capacitors

XDP711 needs two external capacitors for a proper functionality of the surge immunity protection feature:

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- VCP: Voltage Reservoir Capacitor for the internal charge pump.
- Cgs: Extra gate to source capacitance. This slows down the recovery of the gate voltage to avoid current spikes.

Total gate charge time from 0V to the FET's gate threshold voltage ($V_{GS(th)}$) must be around 20 µs. To calculate the value of these capacitors, the total capacitance must be calculated applying the capacitor charge formula

$$C = \Delta t \frac{i}{\Delta V} \tag{12}$$

:

$$C_{Total} = 20\mu s \frac{i}{V_{GS(th)}} \tag{13}$$

Where i is the gate charging current. It is dependent on the gate to source voltage and it is equal to:

$$i = i_{max} - \frac{\left(1.33 * V_{GS(th)}\right)}{2} \tag{14}$$

Where i_{max} = 15 mA.

Once C_{Total} is known, C_{GS} can be calculated by subtracting the total FETs capacitance:

$$C_{GS} = C_{Total} - C_{FET} \tag{15}$$

Where C_{FET} is the total FETs gate capacitance. In case FETs are placed in parallel, all the capacitances must be summed.

Finally, VCP must be 10 times the total capacitance:

$$VCP = 10 * C_{Total} \tag{16}$$

Example:

FET: ISC035N10NM5LF2
Number of FETs: 4
$V_{GS(th)}$ = 3.1 V
FETs gate capacitance (C_{ISS}) = 5500 pF

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$$i = i_{max} - \frac{\left(1.33 * V_{GS(th)}\right)}{2} = 15mA - \frac{1.33 * 3.1V}{2} = 12.93mA \tag{17}$$

$$C_{Total} = 20\mu s \frac{i}{V_{GS(th)}} = 20\mu s \frac{12.93mA}{3.1V} = 83.44nF \tag{18}$$

$$C_{FET} = C_{ISS} * 4 = 22000pF = 22nF \tag{19}$$

$$C_{GS} = C_{Total} - C_{FET} = 83.44nF - 22nF = 61.44nF \tag{20}$$

$$VCP = 10 * C_{Total} = 10 * 83.44nF = 834.4nF \tag{21}$$

Note: If the surge immunity protecton feature is not used, the VCP pin can be left open as specified in Table 3

6.5 Setting the Voltage at MODE1/0 pins in AADM

To set the desired voltage at the MODE1/0 pins, choose the resistor from corresponding pin to GND by dividing desired voltage over pin current (100 µA ± 7%).

Due to the wide voltage range, 5% tolerance resistors can be used:

Table 36 Setting MODEx pins voltage

Voltage (V)	MODE1/0 pin resistor (kΩ)
1.2	12
2.0	20

6.6 Setting the Voltage at ADDR1/0 pins

To set the voltage at the ADDR1/0 pins, choose the resistor from corresponding pin to GND by dividing desired voltage over pin current (100 µA ± 7%).

Due to the wide voltage range, 5% tolerance resistors can be used:

Table 37 Setting ADDRx pins voltage

Voltage (V)	ADDR1/0 pin resistor (kΩ)
1.2	12
2.0	20

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6.7 Handling external current at VREG pin

An internal LDO provides 5 V (typically) supply for the internal circuitry and could also be used as voltage reference for communication pull-up resistors.

Its current capability to supply external circuitry is 10 mA. Make sure not to exceed the package maximum power dissipation P_{PAK}.

To calculate the additional power due to external load:

$$P_{REG_EXT} = ABS(VDD_VIN - VREG) * i_{REG} \tag{22}$$

So, in the case of a 48 V input application (where VDD_VIN = 48 V with respect to GND), with a 10 mA load on VREG = 5 V:

$$P_{REG_EXT} = ABS(48V - 5V) * 10mA = 430mW \tag{23}$$

The rest of current consumption comes from controller's circuitry.

To keep the package power dissipation within the P_{PAK} limit and allow additional consumption due to external load of LDO, a shunt resistor may be required at the VDD_VIN pin in high input voltage applications. It helps not to exceed the P_{PAK} limit:

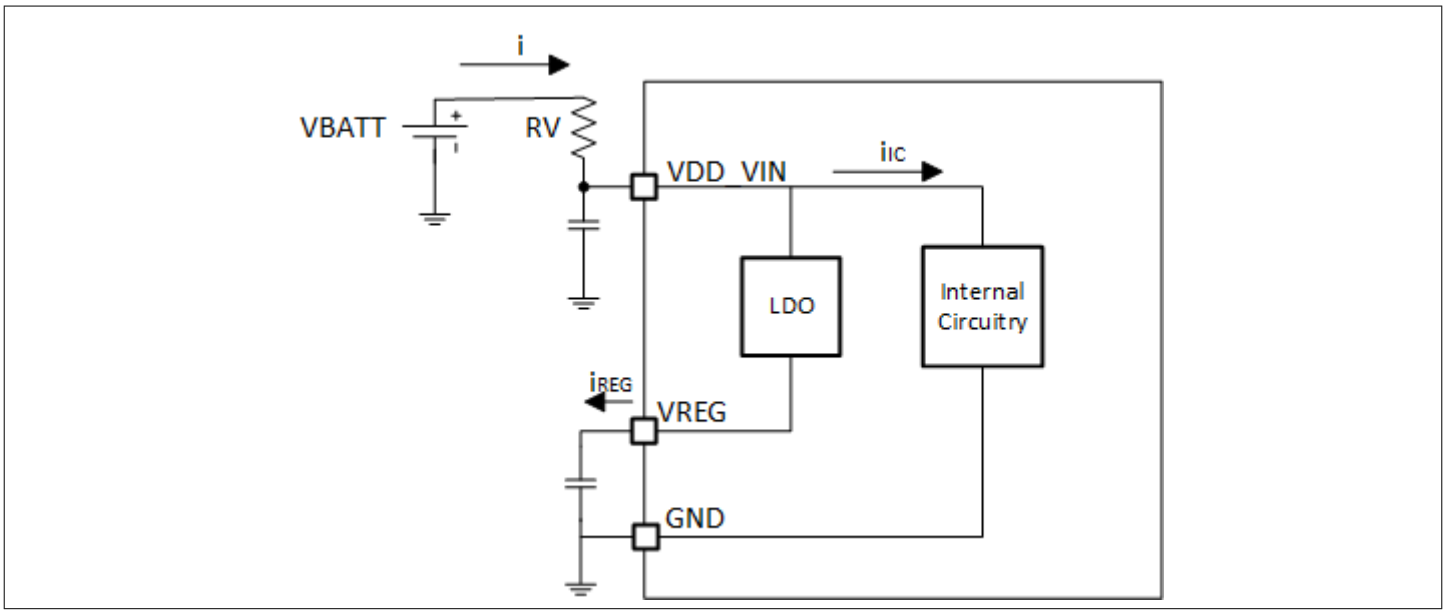

Figure 36 Handling external current at VREG pin

To calculate RV:

$$RV = \frac{P_{TOT} - P_{PAK}}{i^2} = \frac{VBATT}{i} - \frac{V_{REG} \times i_{REG} + P_{PAK}}{i^2} \tag{24}$$

where:

$$P_{TOT} = VBATT \times i - VREG \times i_{REG} \tag{25}$$

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and P_{PAK} = 0.8 W, V_{REG} = 5 V (typically), i_{REG} is the expected current consumption of the external circuitries supplied by *VREG* and *i* is the expected current consumption of the whole device supplied by *VBATT*.

So, for an expected maximum internal current consumption (i_{IC}) of 10 mA:

$$i = i_{IC} + i_{REG} = 10mA + 10mA = 20mA \tag{26}$$

$$RV = \frac{VBATT}{i} - \frac{VREG \times i_{REG} + P_{PAK}}{i^2} = \frac{48V}{20mA} - \frac{5V \times 10mA + 0.8W}{(20mA)^2} = 275\Omega \tag{27}$$

The power dissipated by the resistor is:

$$P_{RV} = i^2 \times RV = (20mA)^2 \times 275\Omega = 0.11W \tag{28}$$

Note: A negative result in the calculation of the resistance RV means that the total power dissipation of the package P_{PAK} is not being exceeded. In this case, RV is not needed.

To protect XDP711, if the die temperature goes above 163 ±10°C, VREG is turned off. Thus, communication is not possible and the status of FAULT, WARN, PWRGD and GPOs is not reliable.

Special considerations:

- RV must be limited to 1KΩ max.
- If RV is used, a 100nF cap from VDD_VIN to GND is mandatory.
- If it is desired to program OTP, care must be taken that the necessary voltage (20V) is applied directly at VDD_VIN pin, taking into account the voltage drop on RV.

6.8 ISNS input filter

In noisy or high dV/dt applications, an input filter from RSNS to ISNS_P and ISNS_N pins is recommended as shown in the following figure.

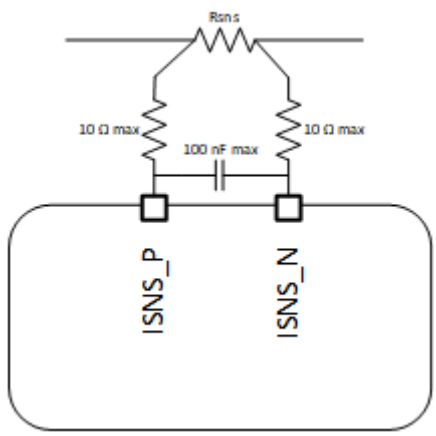

Figure 37 ISNS input filter

6.9 FET selection considerations

Due to the increased gate current of Infineon's Linear FET 1 over 125°C, its compatibility with XDP711 is limited to this temperature level. Make sure that the junction temperature of the Linear FET does not exceed this value and that the corresponding temperature protections are set accordingly. Infineon's Linear FET 2 does not have this limitation.

When selecting a FET, the following guidelines must be observed:

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- Plateau voltage of the FET must be lower than XDP711 detection level of enhancement (7.8 V typically).
- SOA of the FET and system input voltage will determine the current with which the output capacitor will be charged, thus, the start-up time. Wide SOA will translate into faster start-up time. If a specific start-up time is required, care must be taken to select a FET with an SOA that allows it.
- Control loop's absolute minimum current regulation capability in continuous SOA regulation start-up mode is 0.25 A. Any FET's target I_{SOA} values lower than this value will be rounded up. Therefore, the FET's SOA is violated. It is recommended for the FET to withstand the minimum current level at any point of its SOA. Alternatively, Boost Mode can be used to turn on weak FETs.
- If multiple FETs in parallel are used, their SOA must not be divided by the number of FETs, but single FET SOA must be programmed. Paralleling must be considered to reduce Rdson only.
- IREG feature must be disabled when using Linear FET 1 in the system. In other words, SOAR_TMR must be set to 0. Linear FET 2 does not have this limitation.
- At FET power up, the Vgs control by the loop might be affected by reaching FET's plateau level, but FET's current continues to be limited as well as SOA target follows FET's Vds. This can be more pronounced with LinearFETs. For LinearFETs, it is recommended to set start-up current limit IST in the way that Vgs is below plateau level at the end of regulation phase. It will ensure a smooth start-up behavior. The same is valid for OC level with standard FETs to ensure proper current regulation.
- Low Zthjc helps with power dissipation during linear mode.
- Low zero temperature coefficient (ZTC) point avoids staying in thermal instability region for too long.

6.10 Calculating PMBus direct format limits from "real world" values and vice-versa

6.10.1 Voltage

Voltage limits calculations are straight forward using the formulas and coefficients specified in Telemetry via PMBus. As an example, the VIN_OV_FAULT_LIMIT is taken.

System characteristics and configuration:

VTLM_RNG = 88 V

Based on VTLM_RNG value, from the coefficients table:

m = 4653

b = 0

R = -2

For a VIN_OV_FAULT_LIMIT of 64 V, the following formula is applied:

$$Y = \left(mX + b\right) * 10^{R} \tag{29}$$

$$Y = \left(4653 * 64 + 0\right) * 10^{-2} \tag{30}$$

$$Y = 2978 = 0xBA2 \tag{31}$$

So the value to be programmed in VIN_OV_FAULT_LIMIT is 0xBA2.

To convert from PMBus direct format to "real world" value, let's suppose the value from the ADC in the READ_VIN command is 0x8B9 = 2233 decimal. System characteristics, configuration and coefficients are the same as above. The following formula is applied:

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$$X = \frac{1}{m} * \left(Y * 10^{-R} - b\right) \tag{32}$$

$$X = \frac{1}{4653} * \left(2233 * 10^{2} - 0\right) \tag{33}$$

$$X = 48V \tag{34}$$

6.10.2 Current

Values in Table 33 are normalized to a 1 mΩ resistor. Therefore, to convert to a PMBus direct format value, result has to be divided over the value of the sense resistor in mΩ. And to convert to a "real world" value, the result must be multiplied. For example, if a value of 35 A is desired for IOUT_OC_WARN_LIMIT:

System characteristics and configuration:

Rsns = 0.5 mΩ

V_{SNS_CS} = 12.5 mV

Based on V_{SNS_CS} value, the coefficients are:

m = 23165

b = 0

R = -2

To get the limit value, the following formula is applied:

$$Y = \left(\left(mX + b\right) * 10^{R}\right) * Rsns\left(m\Omega\right) \tag{35}$$

$$Y = \left(\left(23165 * 35 + 0\right) * 10^{-2}\right) * 0.5 \tag{36}$$

$$Y = 4054 = 0xFD5 \tag{37}$$

So the value 0xFD5 must be programmed in IOUT_OC_WARN_LIMIT.

Similarly, to obtain the "real world" value from the ADC reading in READ_IOUT. Let's suppose the reading is 0x910 = 2320 decimal. The following formula is applied:

$$X = \frac{\frac{1}{m} * \left(Y * 10^{-R} - b\right)}{Rsns(m\Omega)} \tag{38}$$

$$X = \frac{\frac{1}{23165} * \left(2320 * 10^{2} - 0\right)}{0.5} \tag{39}$$

$$X = \frac{10}{0.5} = 20A \tag{40}$$

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READ_IOUT_RMS is a 16 bit field, so coefficients are different:
m = 20808
b = 0
R = -2
If the ADC reading is 0x1048 = 4168 decimal, the "real world" value is obtained as follows:

$$X = \frac{\frac{1}{20808} * \left(4168 * 10^{-2} - 0\right)}{0.5} \tag{41}$$

$$X = \frac{20}{0.5} = 40A \tag{42}$$

6.10.3 Power

Input power is the result of multiplying input voltage times the current. Power coefficients are also normalized to 1 mΩ, so it is also necessary to multiply or divide by the sense resistor value in mΩ to obtain direct format or "real world" values respectively.
If a 1100 W value is desired as PIN_OP_WARN_LIMIT:
System characteristics and configuration:
VTLM_RNG = 88 V
Rsns = 0.5 mΩ
V_{SNS_CS} = 12.5 mV
Based on these, coefficients are:
m = 4211
b = 0
R = -2
To obtain the limit, the following formula is applied:

$$Y = \left(\left(mX + b\right) * 10^{R}\right) * Rsns\left(m\Omega\right) \tag{43}$$

$$Y = \left(\left(4211 * 1100 + 0\right) * 10^{-2}\right) * 0.5 \tag{44}$$

$$Y = 23159 = 0x5A77 \tag{45}$$

So the value 0x5A77 must be programmed in PIN_OP_WARN_LIMIT.
The power reading can be 16 bits (READ_PIN) or 24 bits (READ_PIN_EXT). In the case of READ_PIN, coefficients are the same as specified for PIN_OP_WARN_LIMIT. So, if the reading of READ_PIN is 0xCD9A = 52634 decimal, the following formula is applied:

$$X = \frac{\frac{1}{m} * \left(Y * 10^{-R} - b\right)}{Rsns(m\Omega)} \tag{46}$$

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$$X = \frac{\frac{1}{4211} * \left(52634 * 10^2 - 0\right)}{0.5} \tag{47}$$

$$X = 2500W \tag{48}$$

If 24 bits power reading is desired (READ_PIN_EXT), corresponding coefficients based on the system characteristics and configuration specified above are:

m = 10780

b = 0

R = 0

For an example reading of 0xB4EE53 = 11857491 decimal, the formula becomes:

$$X = \frac{\frac{1}{10780} * \left(11857491 * 10^0 - 0\right)}{0.5} \tag{49}$$

$$X = 2200W \tag{50}$$

6.10.4 Temperature

Temperature calculation is straight forward too and it only requires to apply the coefficients to the formulas. If an OT_FAULT_LIMIT of 150°C is desired, the corresponding coefficients are:

m = 52

b = 14321

R = -1

By applying the direct format formula, the following is obtained:

$$Y = \left(mX + b\right) * 10^R \tag{51}$$

$$Y = \left(52 * 150 + 14321\right) * 10^{-1} \tag{52}$$

$$Y = 2212 = 0x8A4 \tag{53}$$

So the value 0x8A4 must be programmed in OT_FAULT_LIMIT.

Note: OT_FAULT_LIMIT can be programmed from -273°C (0x000) to 512°C (0xFFF). Care must be taken to program it within the FET operating temperature range.

The reading from READ_TEMPERATURE_1 is translated to "real world" by solving the equation for X. If the reading is 0x7A0 = 1952 decimal:

$$X = \frac{1}{m} * \left(Y * 10^{-R} - b\right) \tag{54}$$

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$$X = \frac{1}{52} * \left(1952 * 10^1 - 14321\right) \tag{55}$$

$$X = 100°C \tag{56}$$

6.10.5 Energy

Energy is calculated based on 16 bits power, therefore, the same coefficients shall be used. Two readings of the READ_EIN register are required. Since energy is power times time, it is also required to know the time between the samples.

In the following example, system characteristics and configuration are:
VTLM_RNG = 88 V
Rsns = 0.5 mΩ
V_{SNS_CS} = 12.5 mV
Based on these, from Table 33, coefficients are:
m = 4211
b = 0
R = -2

The samples read are:

Table 38 Energy read samples

	First Sample		Second Sample	
	Hex	**Dec**	**Hex**	**Dec**
SAMPLE_COUNT	1000	4096	3DC7	15815
ROLLOVER_COUNT	10	16	FF	255
ENERGY_COUNT	01FF	511	1FAC	8108

First, the power difference is calculated by substracting the ENERGY_COUNT of the first sample from the second sample. Note that the ENERGY_COUNT is concatenated with the ROLLOVER_COUNT:

$$Power \quad difference = 0xFF1FAC - 0x1001FF = 0xEF1DAD \tag{57}$$

Next step is to calculate the SAMPLE_COUNT difference by subtracting the SAMPLE_COUNT of both samples:

$$Sample \quad count \quad difference = 0x3DC7 - 0x1000 = 0x2DC7 = 11719d \tag{58}$$

Then the average power per sample is calculated by dividing the power difference over the sample count difference:

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$$Average \quad power = \frac{0xEF1DAD}{0x2DC7} = 0x539 = 1337d \tag{59}$$

Now X can be determined by using the PMBus direct format formula:

$$X = \frac{\frac{1}{m} * \left(Y * 10^{-R} - b\right)}{Rsns(m\Omega)} \tag{60}$$

$$X = \frac{\frac{1}{4211} * \left(1337 * 10^{2} - 0\right)}{0.5} \tag{61}$$

$$X = 63.5W \tag{62}$$

The time between samples can either be measured or calculated. XDP711 ADC conversion rate is 102.4µs. This is also the time it takes to get a sample of energy, so the time between samples can be determined by multiplying the SAMPLE_COUNT difference times 102.4µs:

$$11719 * 102.4\mu s = 1.2s \tag{63}$$

Finally, energy is determined by multiplying power times time:

$$E = 63.5W * 1.2s \tag{64}$$

$$E = 76.2J \tag{65}$$

Note: Extended energy (READ_EIN_EXT) is calculated in the same way, also using PMBus coefficients for 16 bits power, except ROLLOVER_COUNT is 24 bits in this command, instead of 8 bits.

6.11 Calculating AMON resulting current and power

Calculating AMON RC filter

If configured for current sensing, AMON outputs a current level of i_{AMON} = 2 mA at the maximum configured V_{SNS_CS}. To calculate the RC filter:

1. Define the maximum desired voltage drop on the resistor (V_{AMON}) taking into account the maximum voltage is 3.3V
2. Calculate R_{AMON} according to the following formula:

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$$R_{AMON} = \frac{V_{AMON}}{i_{IMON}} \tag{66}$$

3. Define the desired bandwidth (BW) between 80 and 100 KHz and calculate C_{AMON} according to the following formula:

$$C_{AMON} = \frac{1}{BW * 2 * \pi * R_{AMON}} \tag{67}$$

Calculating AMON current

If configured as a current monitor, AMON's output current level (I_{OUT}) can be calculated based on the voltage at the AMON pin (V_{DROP}):

$$I_{OUT} = V_{SNS_CS} * \frac{V_{DROP}/V_{AMON}}{R_{SNS}} \tag{68}$$

Where R_{SNS} is the populated sense resistor.

Calculating AMON power

If configured as a power monitor, the system input power can be calculated based on AMON's output current level (I_{OUT}) as follows:

$$i_{PMON} = \frac{V_{DROP}}{R_{AMON}} \tag{69}$$

The IDAC is designed so that a code of 0d361 = 2 mA of current at the output of the AMON. So to get the code:

$$IDAC \quad code = \frac{361 * i_{PMON}}{2mA} \tag{70}$$

Internally, the result of the power calculation, which consists on 24 bits, is truncated to 15 MSBs. In other words, it is divided by 2^{15}. Therefore, to determine the power, the inverse operation must be applied:

$$Power \quad calculation = IDAC \quad code * 2^{15} \tag{71}$$

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Once the power calculation is determined, the system input power can be determined by using the PMBus coefficients and formulas as specified in Calculating PMBus direct format limits from "real world" values and vice-versa.

Example:

V_{DROP} = 1.2 V
R_{AMON} = 900 Ω
VTLM_RNG = 88 V
Rsns = 0.5 mΩ
V_{SNS_CS} = 25 mV
Based on these and since the calculations are done based on 24 bits power, coefficients are:
m = 5390
b = 0
R = 0

$$i_{PMON} = \frac{V_{DROP}}{R_{AMON}} = \frac{1.2V}{900\Omega} = 1.33mA \tag{72}$$

$$IDAC \quad code = \frac{361 * i_{PMON}}{2mA} = \frac{361 * 1.33mA}{2mA} = 240.67 \tag{73}$$

$$Power \quad calculation = IDAC \quad code * 2^{15} = 240.67 * 32768 = 7886165 \tag{74}$$

$$X = \frac{\frac{1}{m} * \left(Y * 10^{-R} - b\right)}{Rsns(m\Omega)} = \frac{\frac{1}{5390} * \left(7886165 * 10^{0} - 0\right)}{0.5m\Omega} = 2926W \tag{75}$$

6.12 Layout guidelines

The following guidelines shall be followed when designing an XDP711 PCB:

- Maximum supply current of the XDP711 is 10mA. The traces at supply pin VDD_VIN don't need to be that thick.
- VREG capacitor must be placed right next to the VREG pin.
- I2C traces need a single-ended controlled impedance of 50 Ω. Therefore their width must be adjusted accordingly.
- TSNS filter capacitor must be placed right next to the TSNS pins.
- If used, TSNS BJT shall be placed right next to the FET or to the point to be sensed. It is best to place the sensor next to the hottest part of the FET package. In the case of our D2PAK FETs, the die is attached to the drain pad on bottom of the package, so this is the section that will get hotter in case of high power dissipation.
- Keep gate trace as short as possible in order to reduce parasitics. This trace and the source one must be able to handle 1.5 A current, which is the current that will flow through them in order to discharge the gate of the FET in case of a fast turn-off event.

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- ISNS filter capacitor also has to be placed right next to the ISNS pins.
- Exposed pad must have a solid connection to GND through many vias.
- The path that will need to handle the highest amount of current goes from the input voltage source, through the sense resistor, FET and output capacitor to the load, including its corresponding return path to ground. Make sure this path is robust enough to support the current level required by the system.
- ISNS lines must be connected directly to sense pins of the sense resistor, separately from the power plane.
- Connect VOUT pin directly to the source of the FET.

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7 Package information

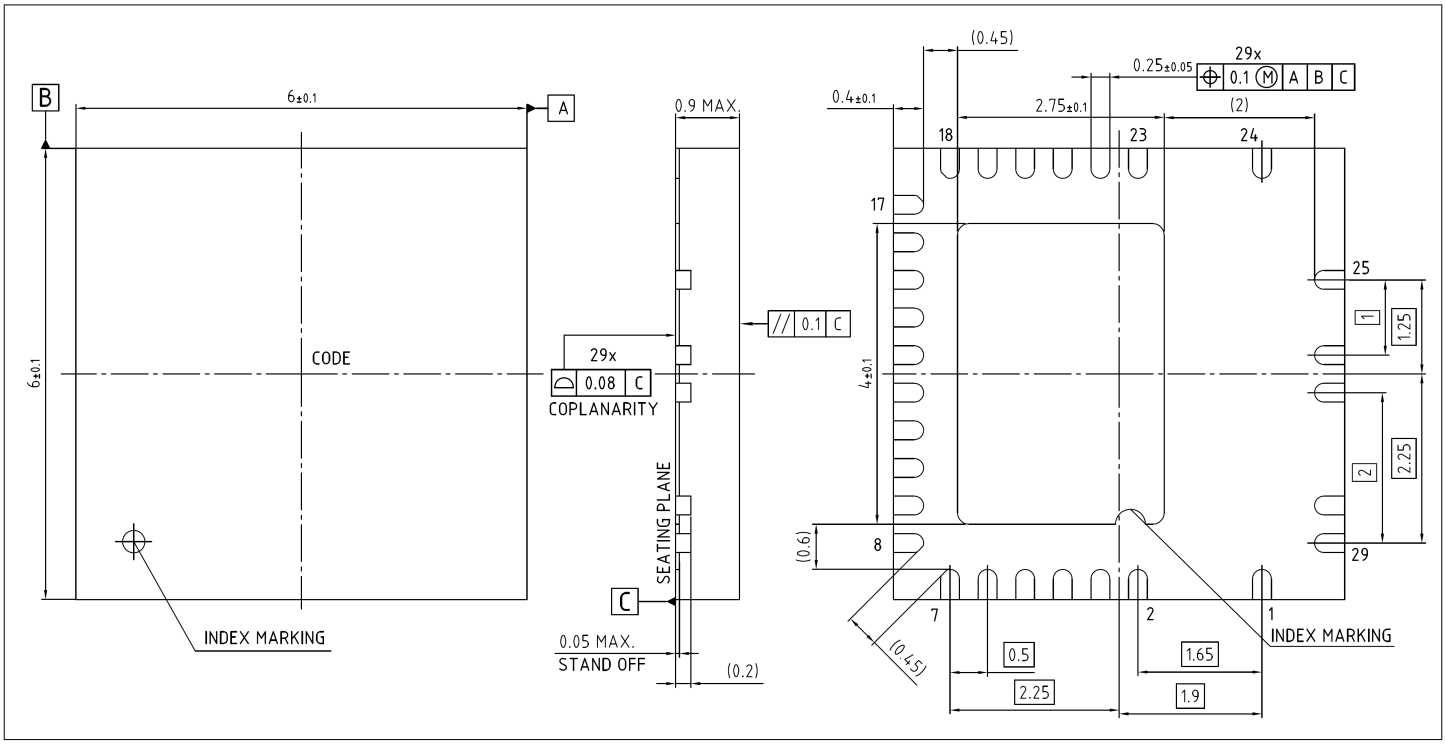

Figure 38 Package dimensions

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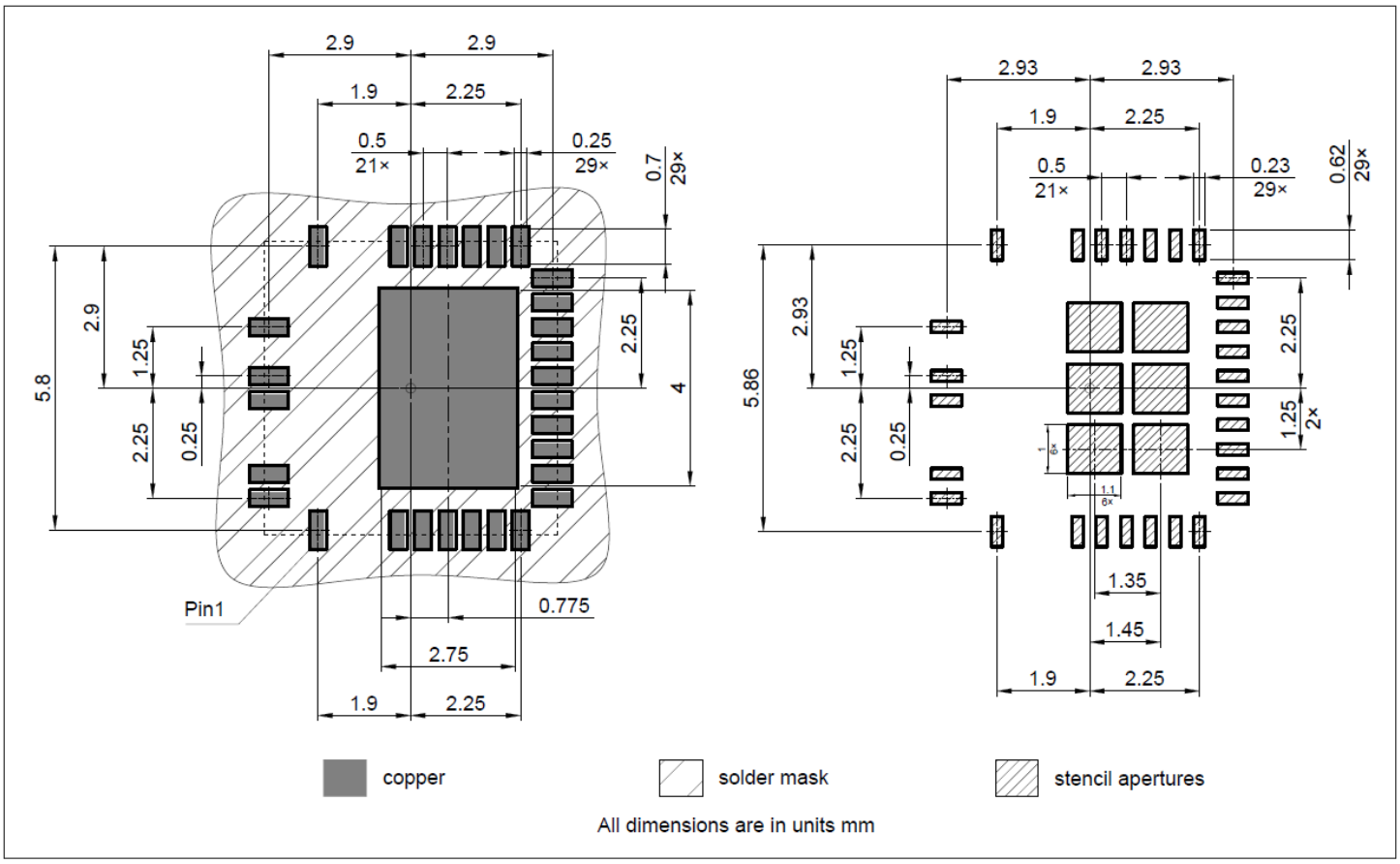

Figure 39 **Recommended footprint**

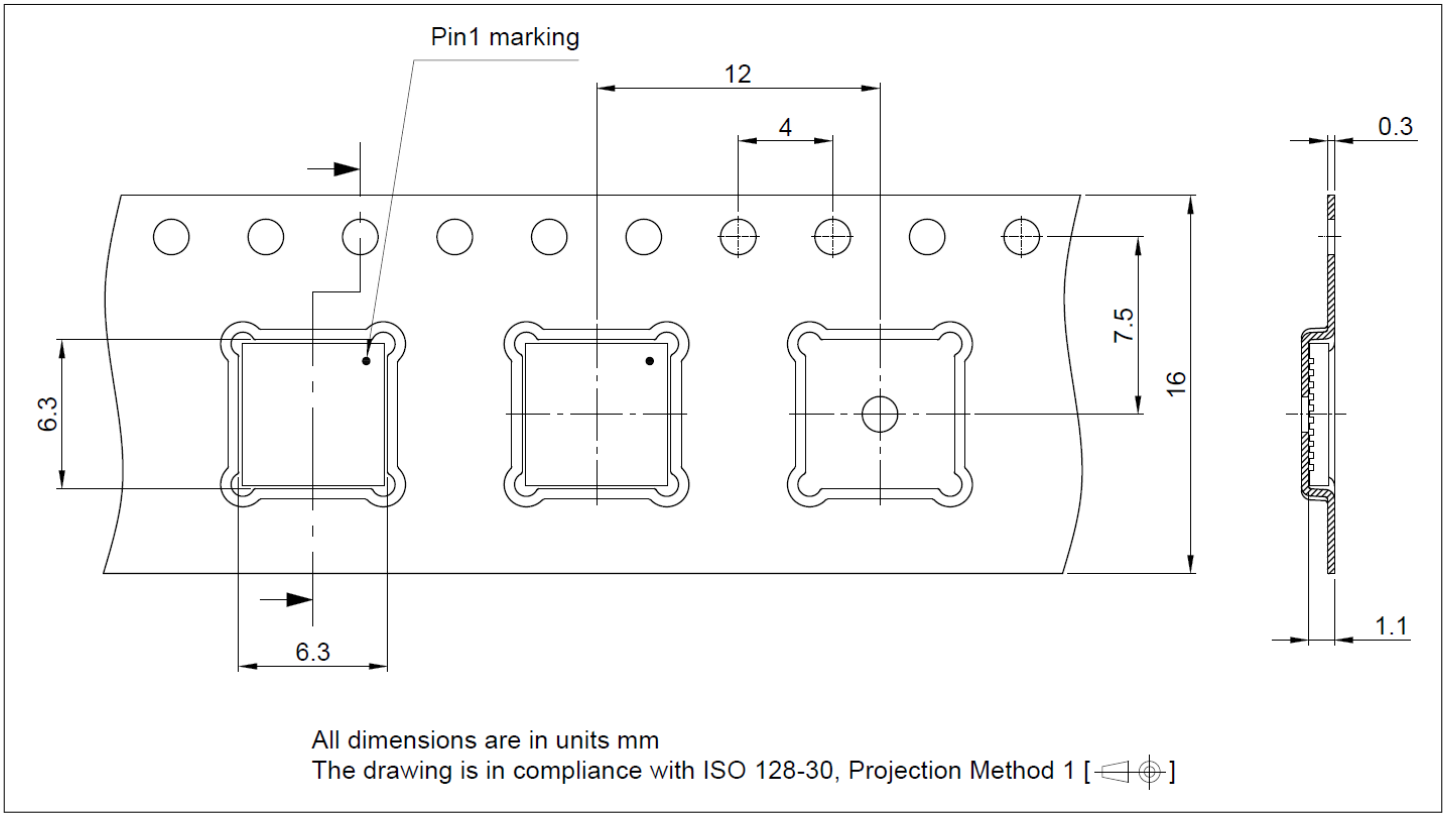

Figure 40 **Tape and reel dimensions**

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Table 39 Ordering information

Basic part number	Orderable part number	Description
XDP711-001	XDP711001XUMA1	Positive input voltage hot-swap controller

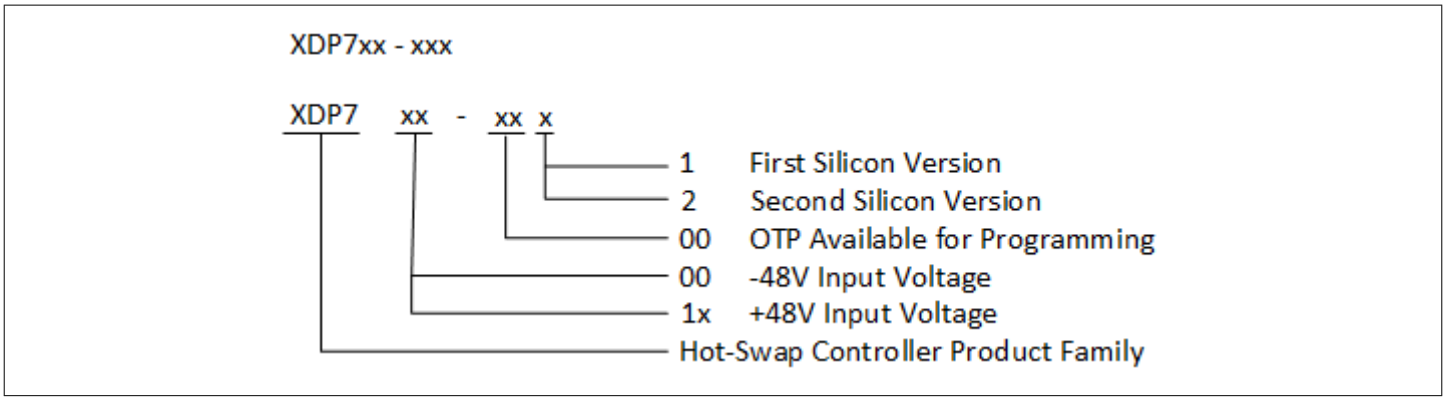

Figure 41 Ordering information

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Revision history

Document version	Date of release	Description of changes
Rev.1.00	2025-06-30	Datasheet release

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