

MOSFET - Power, Single N-Channel 100 V, 12.2 mΩ, 47.1 A

NVMFS015N10MCL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFWS015N10MCL – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	100	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	47.1	
			I_D	29.8	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	59.5	
			P_D	23.8	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	10.7	
			I_D	6.8	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.1	
			P_D	1.2	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	259	A	
Operating Junction and Storage Temperature Range		T_J , T_{Stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	49.6	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{AS} = 2.6\text{ A}$)		E_{AS}	469	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

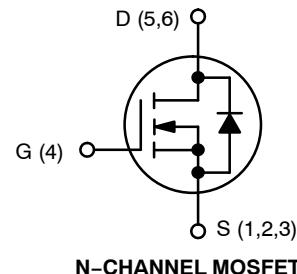
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
100 V	12.2 mΩ @ 10 V	47.1 A
	18.3 mΩ @ 4.5 V	



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS015N10MCL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				60		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25 °C			1.0	μA
			T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 77 μA		1	1.5	3	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.0		mV/°C
Drain-to-Source On Resistance	R _{DSS(on)}	V _{GS} = 10 V	I _D = 14 A		9.7	12.2	mΩ
		V _{GS} = 4.5 V	I _D = 11 A		13.3	18.3	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 14 A			51		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V			1338		pF
Output Capacitance	C _{OSS}				521		
Reverse Transfer Capacitance	C _{RSS}				9.0		
Total Gate Charge	Q _{G(TOT)}		V _{GS} = 4.5 V, V _{DS} = 50 V; I _D = 14 A		9.0		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 14 A	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 14 A		19		nC
Threshold Gate Charge	Q _{G(TH)}				2.0		nC
Gate-to-Source Charge	Q _{GS}				3.0		
Gate-to-Drain Charge	Q _{GD}				3.0		
Plateau Voltage	V _{GP}				2.7		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 14 A, R _G = 6.0 Ω			8.4		ns
Rise Time	t _r				2.7		
Turn-Off Delay Time	t _{d(OFF)}				23.8		
Fall Time	t _f				4.6		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Source to Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2 A			0.7	1.2	V
		V _{GS} = 0 V, I _S = 14 A			0.83	1.3	
Reverse Recovery Time	t _{rr}	I _F = 7 A, di/dt = 300 A/μs			20		ns
Reverse Recovery Charge	Q _{rr}				33		nC
Reverse Recovery Time	t _{rr}	I _F = 7 A, di/dt = 1000 A/μs			14		ns
Reverse Recovery Charge	Q _{rr}				76		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

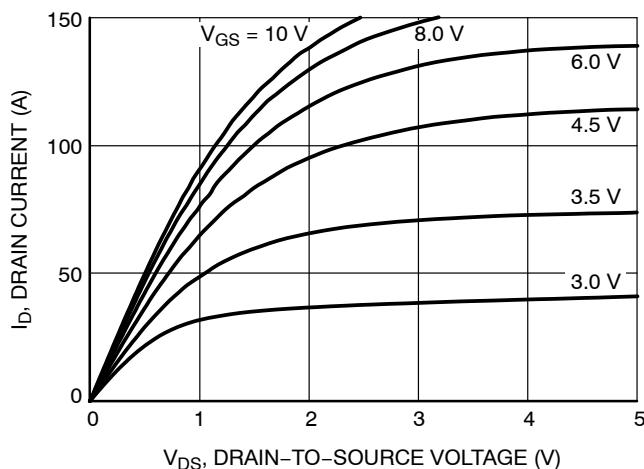


Figure 1. On-Region Characteristics

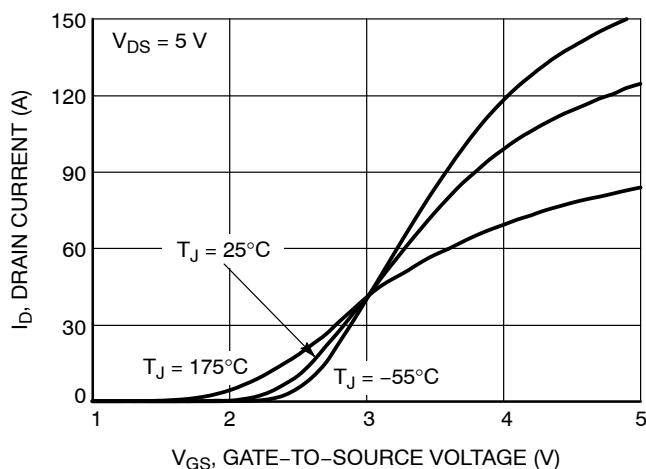


Figure 2. Transfer Characteristics

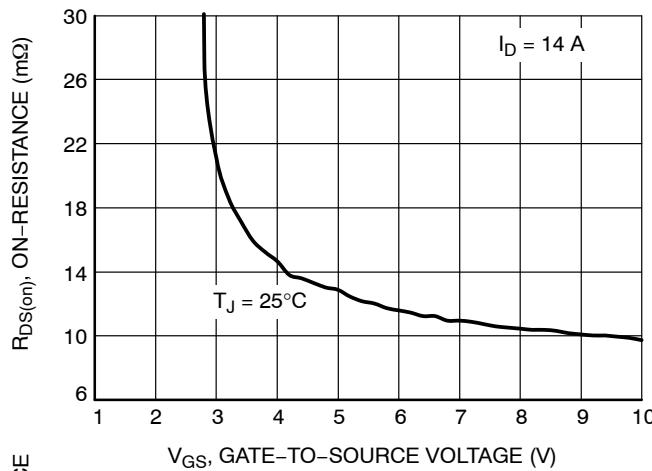


Figure 3. On-Resistance vs. Gate-to-Source Voltage

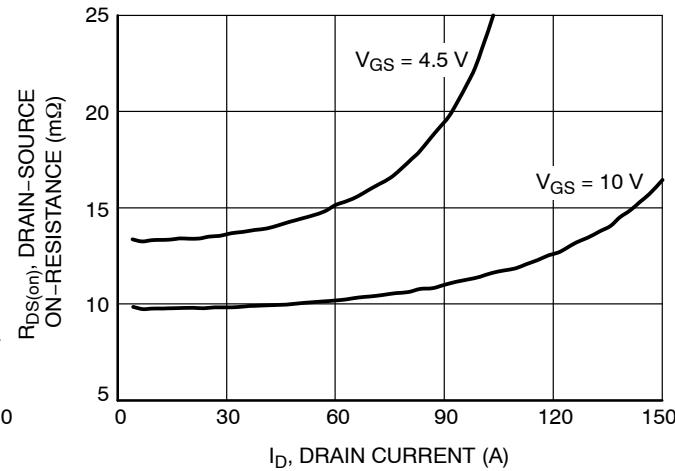


Figure 4. On-Resistance vs. Drain Current

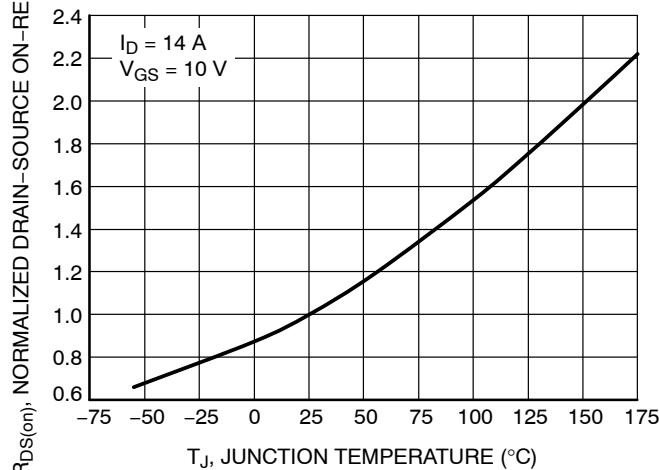


Figure 5. On-Resistance Variation with Temperature

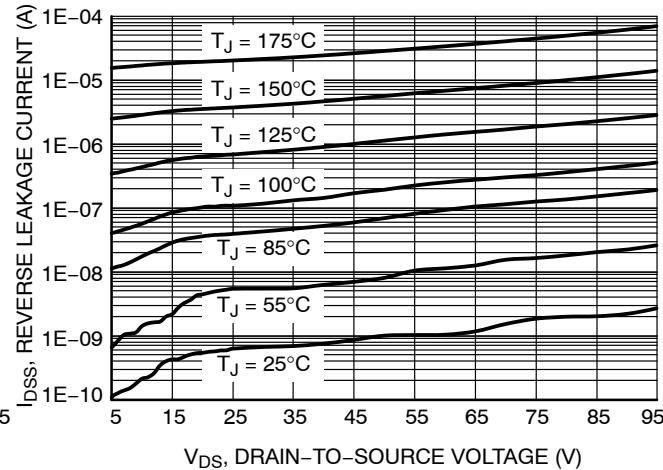
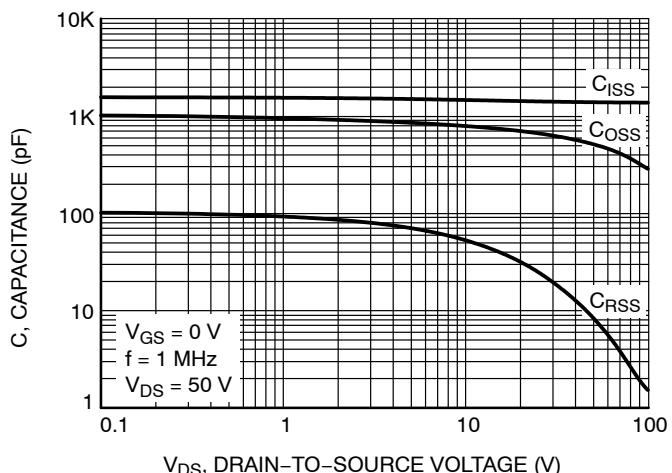
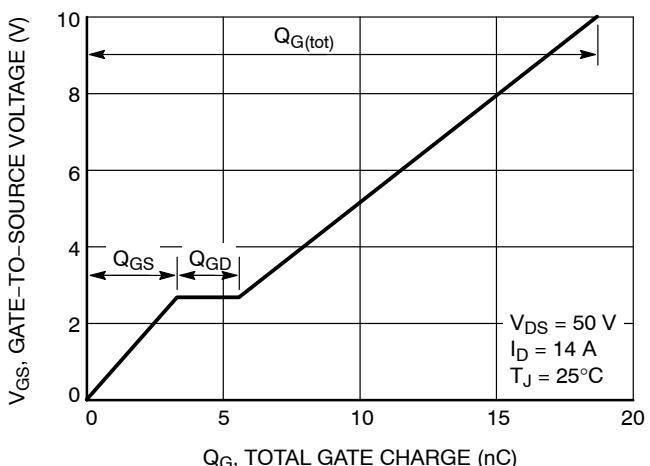
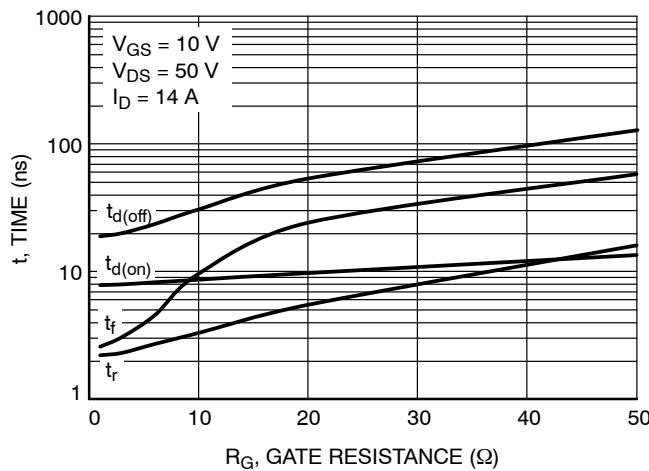
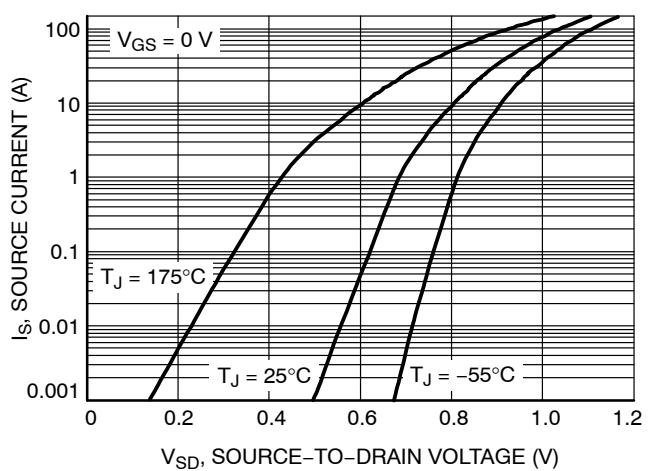
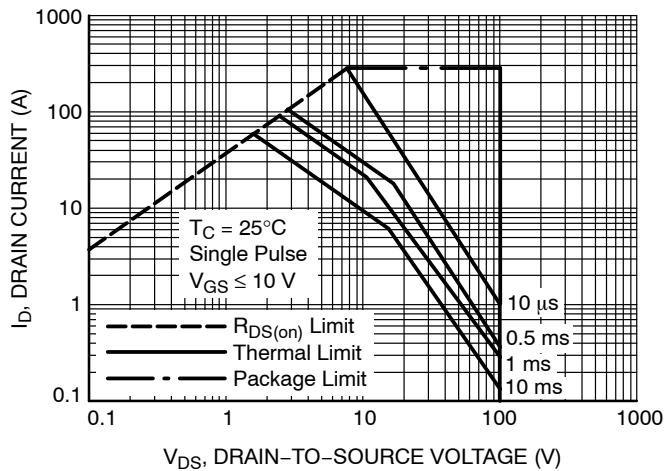
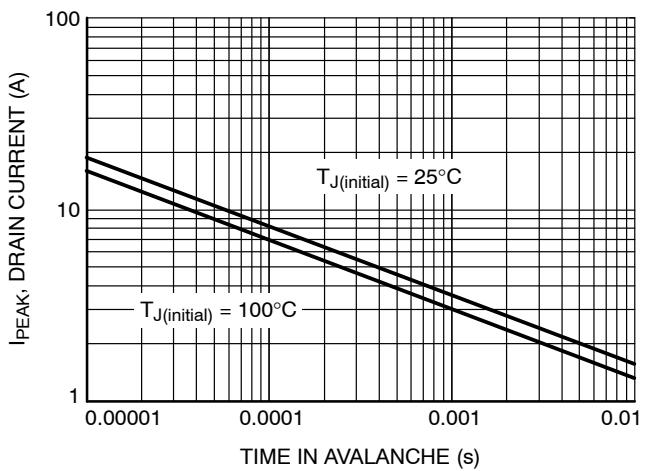


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

Figure 11. Safe Operating Area

Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

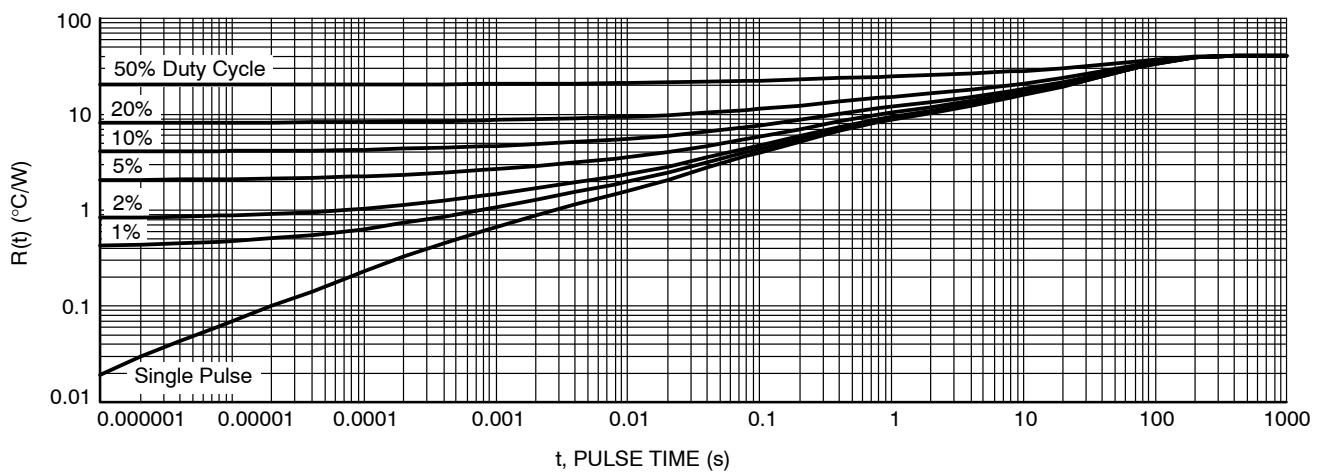
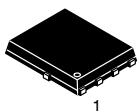


Figure 13. Junction-to-Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS015N10MCLT1G	015L10	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFWS015N10MCLT1G	015W10	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

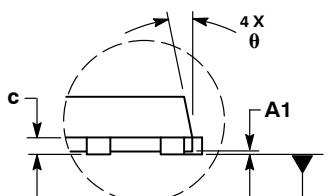
DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:

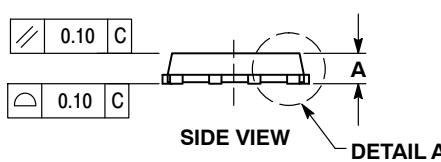
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	----	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	----	12 °

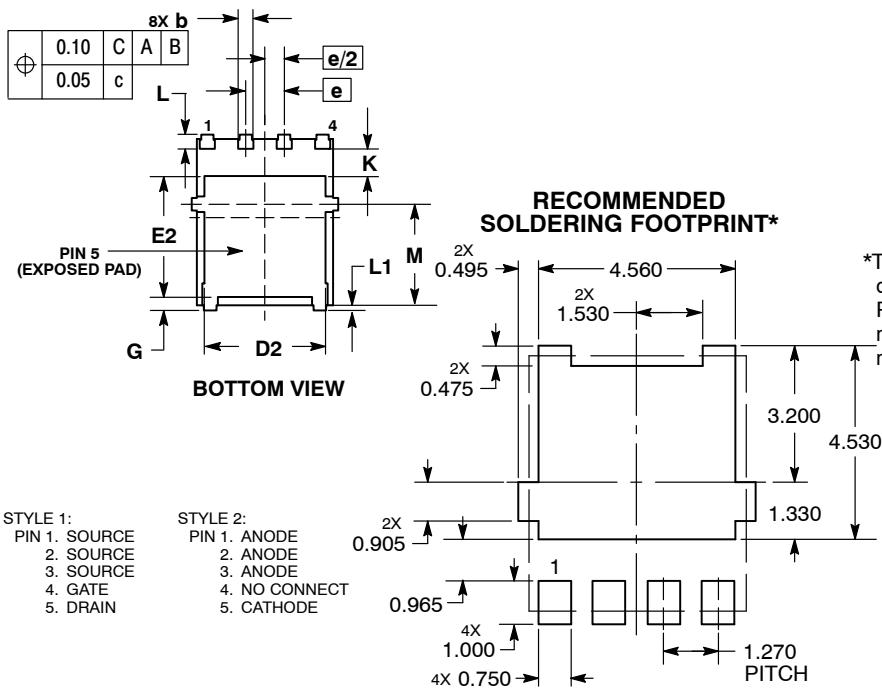


DETAIL A

SEATING PLANE



DETAIL A



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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