RoHS Compliant

# P-CHANNEL MOSFET

***Qualified per MIL-PRF-19500/564***

*Qualified Levels:*
*JAN, JANTX, JANTXV and JANS*

## DESCRIPTION

This 2N6849U switching transistor is military qualified up to the JANS level for high-reliability applications. This device is also available in a thru hole TO-205AF package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

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**U-18 LCC Package**

## FEATURES

- Surface mount equivalent of JEDEC registered 2N6849 number.
- JAN, JANTX, JANTXV and JANS qualifications are available per MIL-PRF-19500/564. (See part nomenclature for all available options.)
- RoHS compliant by design.

## APPLICATIONS / BENEFITS

- Low profile surface mount for crowded areas.
- Military and other high-reliability applications.

Also available in:

**TO-205AF (TO-39) package**
(Leaded Top Hat)
2N6849

## MAXIMUM RATINGS @ $T_A$ = +25 ºC unless otherwise stated

| Parameters / Test Conditions | Symbol | Value | Unit |
|---|---|---|---|
| Operating & Storage Junction Temperature Range | $T_J$ & $T_{stg}$ | -55 to +150 | °C |
| Thermal Resistance Junction-to-Case | $R_{\Theta JC}$ | 5.0 | °C/W |
| Total Power Dissipation @ $T_A$ = +25 °C<br>@ $T_C$ = +25 °C (1) | $P_T$ | 0.8<br>25 | W |
| Drain-Source Voltage, dc | $V_{DS}$ | -100 | V |
| Gate-Source Voltage, dc | $V_{GS}$ | ± 20 | V |
| Drain Current, dc @ $T_C$ = +25 ºC (2) | $I_{D1}$ | -6.5 | A |
| Drain Current, dc @ $T_C$ = +100 ºC (2) | $I_{D2}$ | -4.1 | A |
| Off-State Current (Peak Total Value) (3) | $I_{DM}$ | -25 | A (pk) |
| Source Current | $I_S$ | -6.5 | A |

**Notes:**
1. Derate linearly 0.2 W/°C for $T_C$ > +25 °C.
2. The following formula derives the maximum theoretical $I_D$ limit. $I_D$ is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J\,(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J\,(max)}}$$

3. $I_{DM}$ = 4 x $I_{D1}$ as calculated in note 2.

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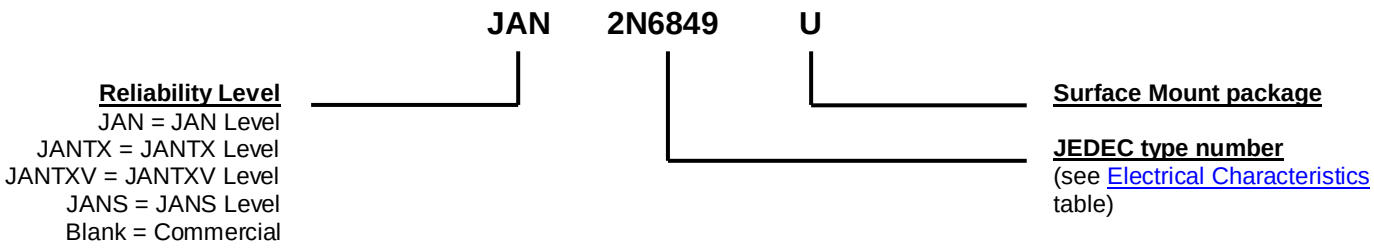
## MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See Package Dimensions on last page.

## PART NOMENCLATURE




## SYMBOLS & DEFINITIONS

| Symbol | Definition |
|---|---|
| di/dt | Rate of change of diode current while in reverse-recovery mode, recorded as maximum value. |
| $I_F$ | Forward current |
| $R_G$ | Gate drive impedance |
| $V_{DD}$ | Drain supply voltage |
| $V_{DS}$ | Drain source voltage, dc |
| $V_{GS}$ | Gate source voltage, dc |

## ELECTRICAL CHARACTERISTICS @ $T_A$ = +25 °C, unless otherwise noted

| Parameters / Test Conditions | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Drain-Source Breakdown Voltage<br>$V_{GS}$ = 0 V, $I_D$ = -1.0 mA | $V_{(BR)DSS}$ | -100 | | V |
| Gate-Source Voltage (Threshold)<br>$V_{DS} \geq V_{GS}$, $I_D$ = -0.25 mA<br>$V_{DS} \geq V_{GS}$, $I_D$ = -0.25 mA, $T_J$ = +125°C<br>$V_{DS} \geq V_{GS}$, $I_D$ = -0.25 mA, $T_J$ = -55°C | <br>$V_{GS(th)1}$<br>$V_{GS(th)2}$<br>$V_{GS(th)3}$ | <br>-2.0<br>-1.0 | <br>-4.0<br><br>-5.0 | V |
| Gate Current<br>$V_{GS}$ = ± 20 V, $V_{DS}$ = 0 V<br>$V_{GS}$ = ± 20 V, $V_{DS}$ = 0 V, $T_J$ = +125°C | <br>$I_{GSS1}$<br>$I_{GSS2}$ | | <br>±100<br>±200 | nA |
| Drain Current<br>$V_{GS}$ = 0 V, $V_{DS}$ = -80 V | $I_{DSS1}$ | | -25 | µA |
| Drain Current<br>$V_{GS}$ = 0 V, $V_{DS}$ = -80 V, $T_J$ = +125 °C | $I_{DSS2}$ | | -0.25 | mA |
| Static Drain-Source On-State Resistance<br>$V_{GS}$ = -10 V, $I_D$ = -4.1 A pulsed | $r_{DS(on)1}$ | | 0.30 | Ω |
| Static Drain-Source On-State Resistance<br>$V_{GS}$ = -10 V, $I_D$ = -6.5 A pulsed | $r_{DS(on)2}$ | | 0.32 | Ω |
| Static Drain-Source On-State Resistance<br>$T_J$ = +125°C<br>$V_{GS}$ = -10 V, $I_D$ = -4.1 A pulsed | $r_{DS(on)3}$ | | 0.54 | Ω |
| Diode Forward Voltage<br>$V_{GS}$ = 0 V, $I_D$ = -6.5 A pulsed | $V_{SD}$ | | -4.3 | V |

### DYNAMIC CHARACTERISTICS

| Parameters / Test Conditions | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Gate Charge: | | | | |
| On-State Gate Charge<br>$V_{GS}$ = -10 V, $I_D$ = -6.5 A, $V_{DS}$ = -50 V | $Q_{g(on)}$ | | 34.8 | nC |
| Gate to Source Charge<br>$V_{GS}$ = -10 V, $I_D$ = -6.5 A, $V_{DS}$ = -50 V | $Q_{gs}$ | | 6.8 | nC |
| Gate to Drain Charge<br>$V_{GS}$ = -10 V, $I_D$ = -6.5 A, $V_{DS}$ = -50 V | $Q_{gd}$ | | 23.1 | nC |

**ELECTRICAL CHARACTERISTICS** @ $T_A$ = +25 °C, unless otherwise noted (continued)

## SWITCHING CHARACTERISTICS

| Parameters / Test Conditions | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Turn-on delay time<br>$I_D$ = -6.5 A, $V_{GS}$ = -10 V, $R_G$ = 7.5 Ω, $V_{DD}$ = -40 V | $t_{d(on)}$ | | 60 | ns |
| Rinse time<br>$I_D$ = -6.5 A, $V_{GS}$ = -10 V, $R_G$ = 7.5 Ω, $V_{DD}$ = -40 V | $t_r$ | | 140 | ns |
| Turn-off delay time<br>$I_D$ = -6.5 A, $V_{GS}$ = -10 V, $R_G$ = 7.5 Ω, $V_{DD}$ = -40 V | $t_{d(off)}$ | | 140 | ns |
| Fall time<br>$I_D$ = -6.5 A, $V_{GS}$ = -10 V, $R_G$ = 7.5 Ω, $V_{DD}$ = -40 V | $t_f$ | | 140 | ns |
| Diode Reverse Recovery Time<br>di/dt ≤ -100 A/µs, $V_{DD}$ ≤ -50 V, $I_F$ = -6.5 A | $t_{rr}$ | | 250 | ns |

## GRAPHS

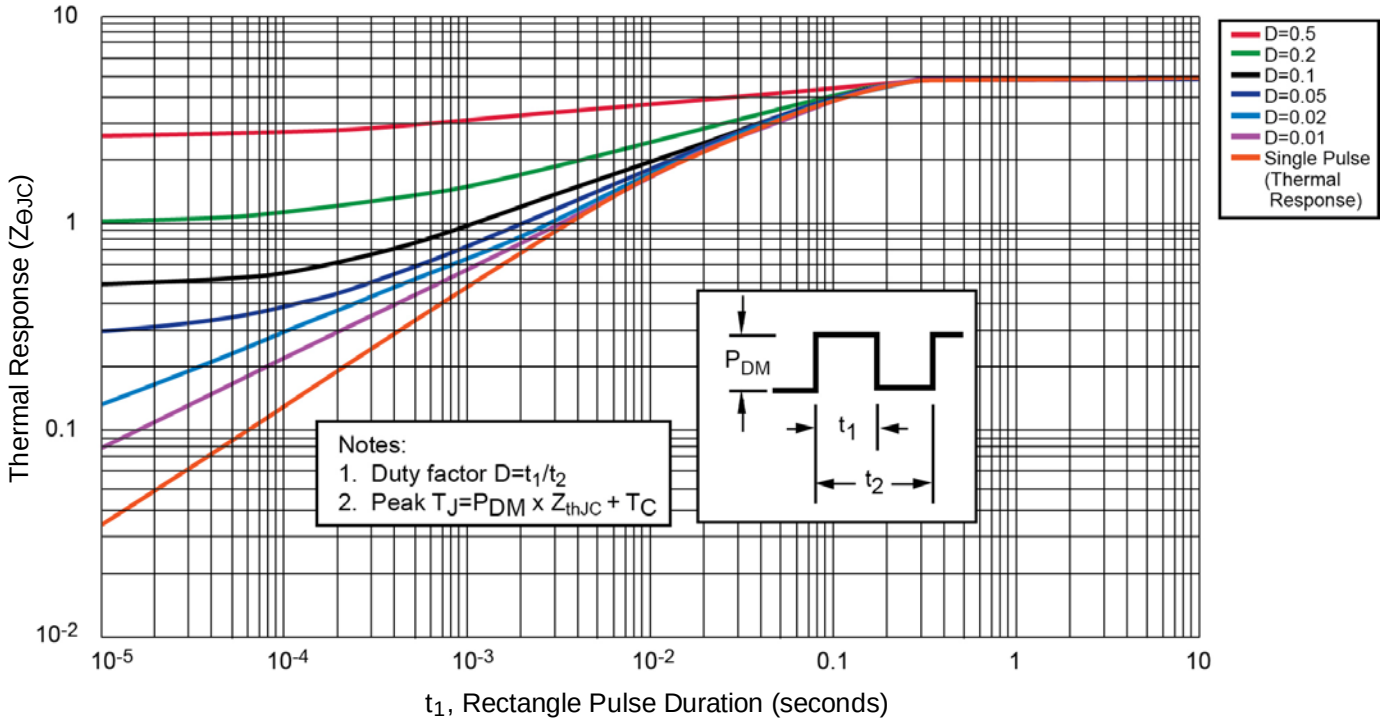



**FIGURE 1** – Normalized Transient Thermal Impedance

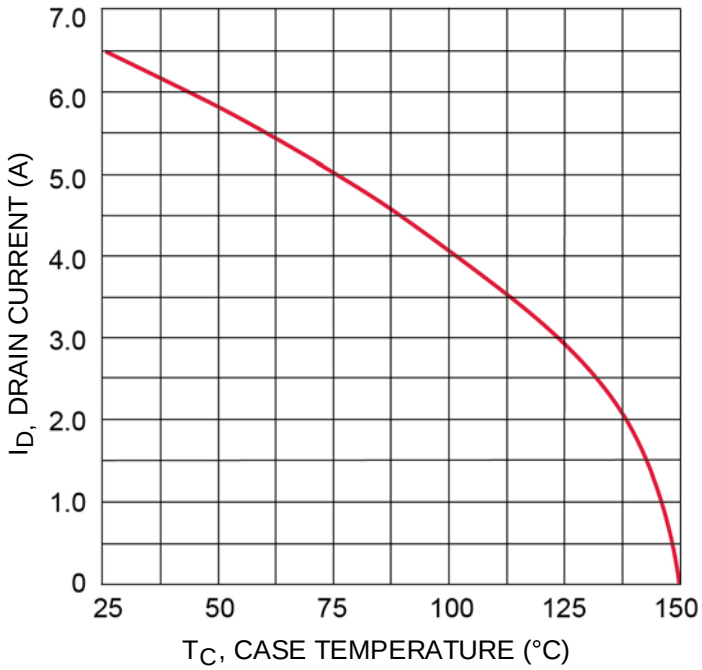



**FIGURE 2** – Maximum Drain Current vs Case Temperature

## GRAPHS (continued)

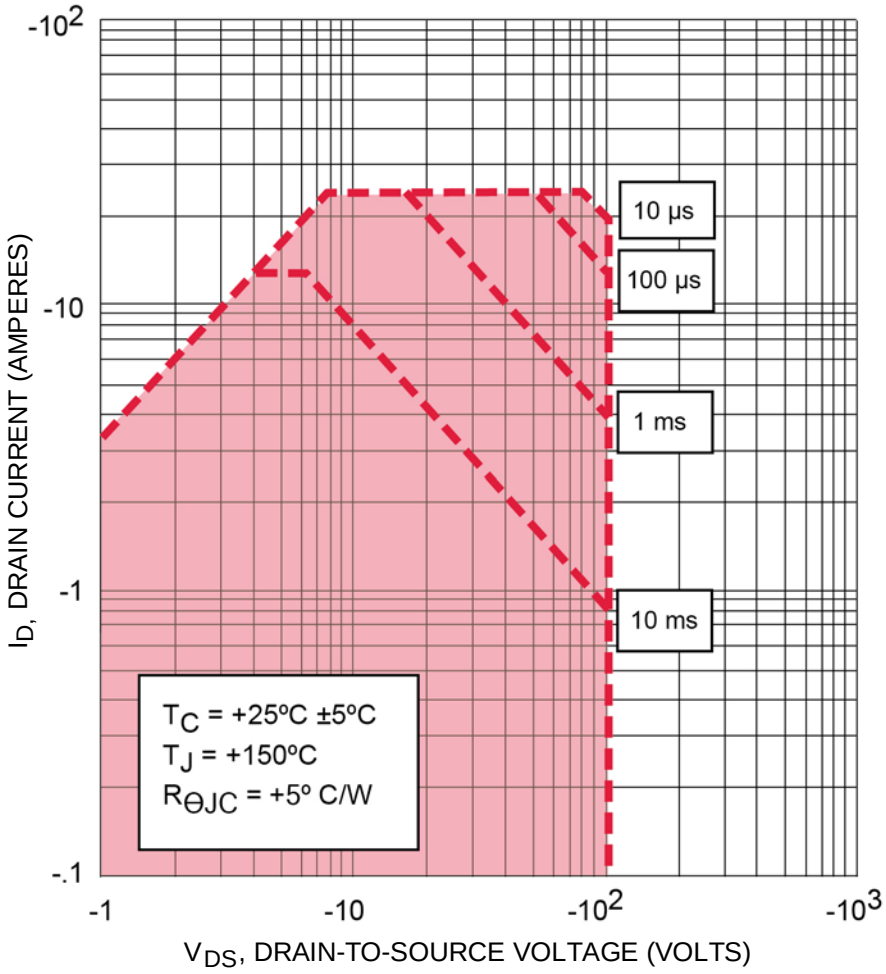
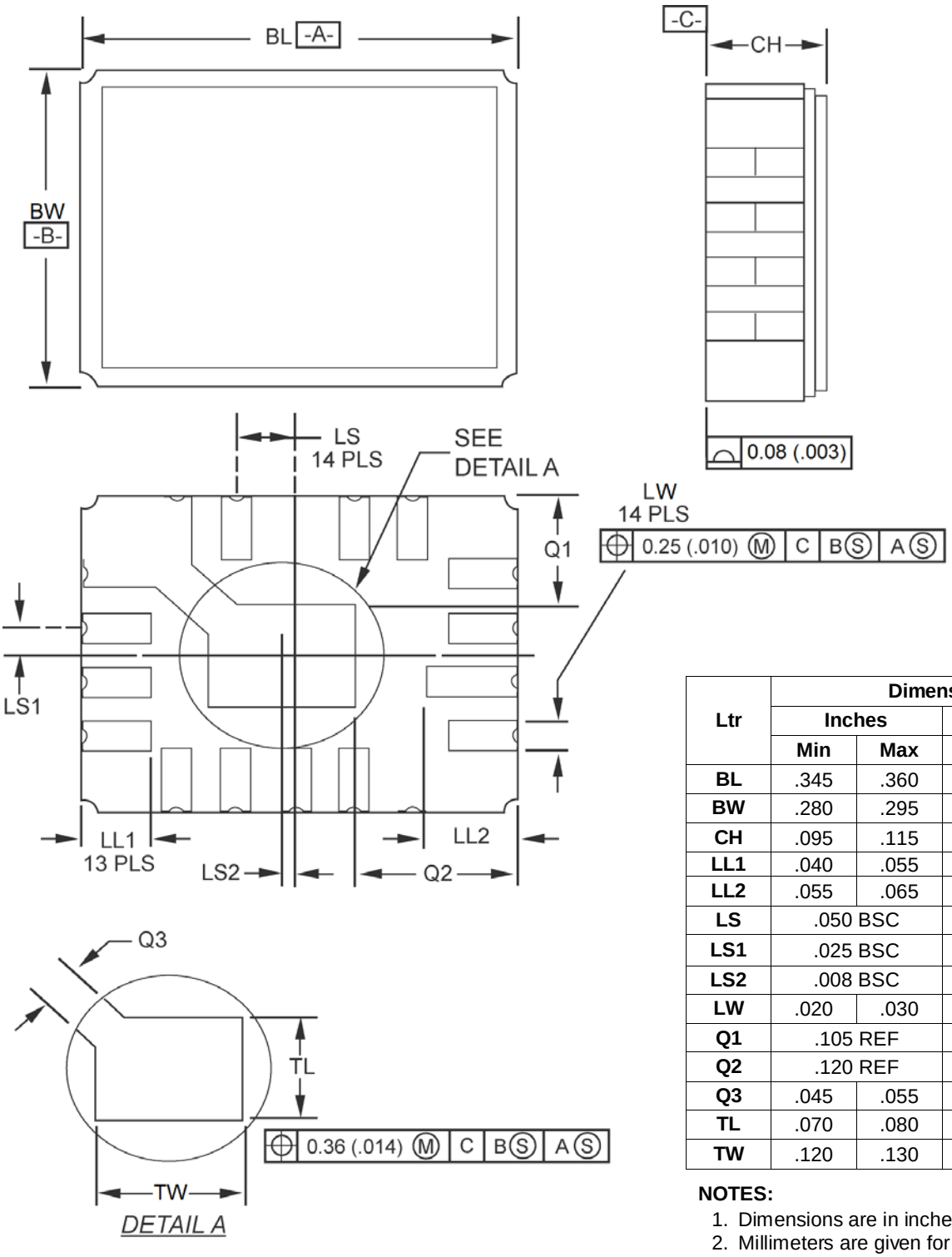



**FIGURE 3** – Maximum Safe Operating Area

## PACKAGE DIMENSIONS

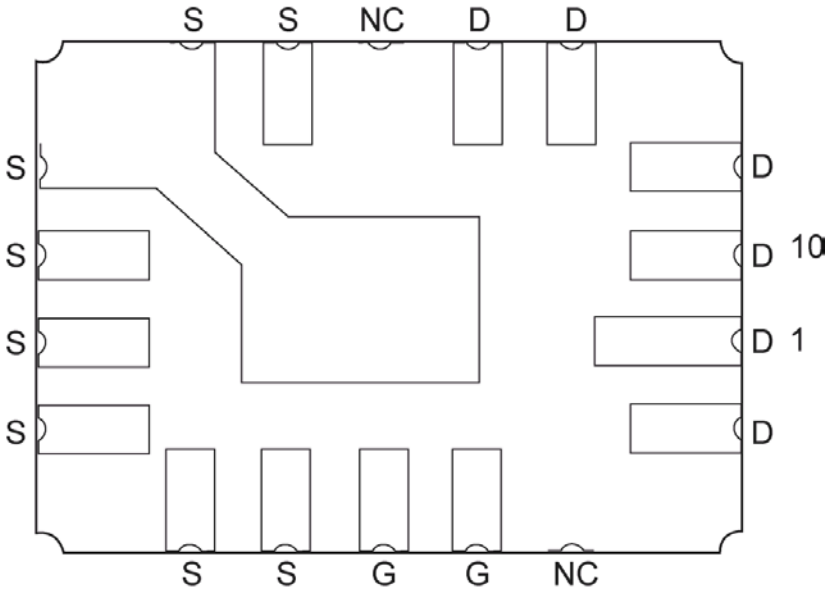



| Ltr | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| BL | .345 | .360 | 8.77 | 9.14 |
| BW | .280 | .295 | 7.12 | 7.49 |
| CH | .095 | .115 | 2.42 | 2.92 |
| LL1 | .040 | .055 | 1.02 | 1.39 |
| LL2 | .055 | .065 | 1.40 | 1.65 |
| LS | .050 BSC | | 1.27 BSC | |
| LS1 | .025 BSC | | 0.635 BSC | |
| LS2 | .008 BSC | | 0.203 BSC | |
| LW | .020 | .030 | 0.51 | 0.76 |
| Q1 | .105 REF | | 2.67 REF | |
| Q2 | .120 REF | | 3.05 REF | |
| Q3 | .045 | .055 | 1.14 | 1.40 |
| TL | .070 | .080 | 1.78 | 2.03 |
| TW | .120 | .130 | 3.05 | 3.30 |

**NOTES:**

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
4. Ceramic package only.

## PAD LAYOUT




**PAD ASSIGNMENTS**