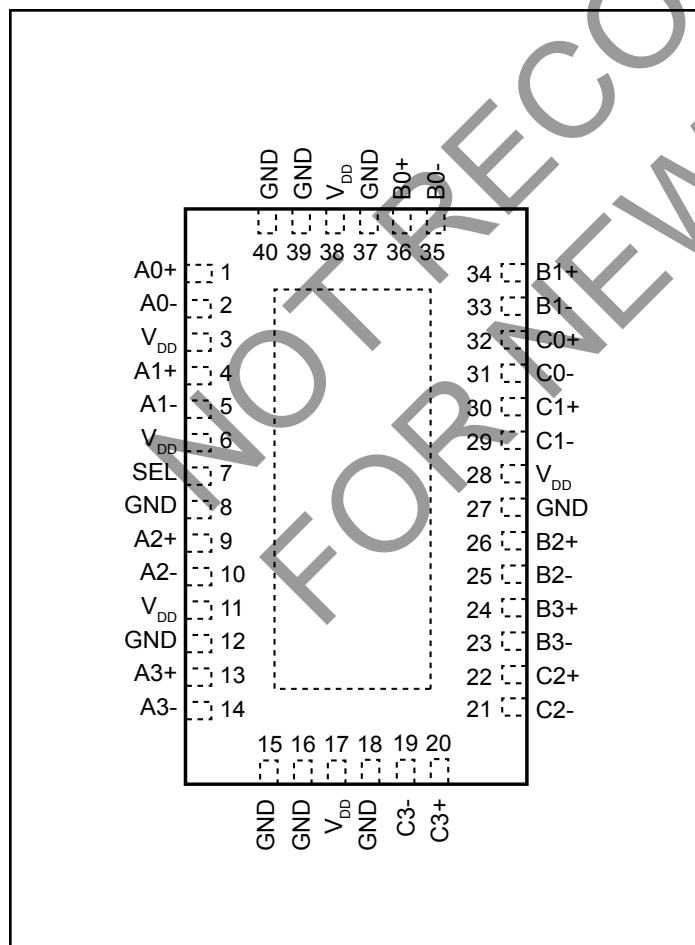


3.3V, PCI Express® 3.0 2-Lane, 2:1 Mux/DeMux Switch, with Single Enable
Features

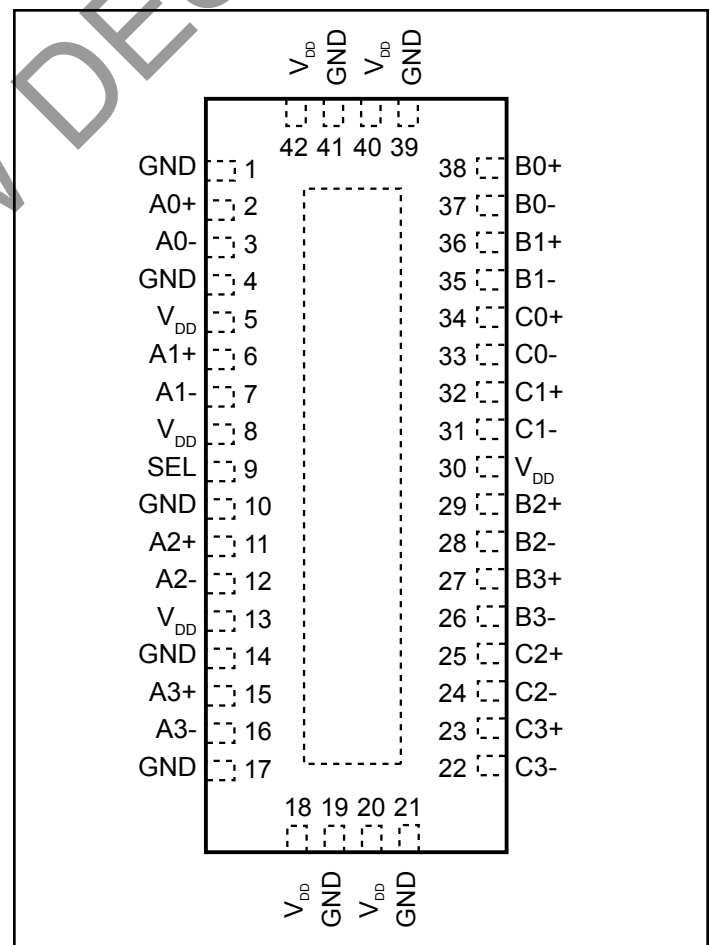
- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express® 3.0 Performance, 8.0Gbps
- Bi-directional Operation
- Low Bit-to-Bit Skew, 10ps max
- Low channel-to-channel skew, 20ps max
- Low Crosstalk: -35dB@4 GHz
- High Off Isolation: -22dB@4 GHz (8.0Gbps)
- Low insertion loss: -1.3dB@4 GHz (8.0Gbps)
- Return loss: -21dB@4 GHz
- Support for DP1.2 - HBR2, HBR, RBR
- Supply Voltage 3.3V
- Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
 - 42-contact, TQFN (ZH42), 3.5 x 9mm
 - 40-contact, TQFN (ZL40), 3 x 6mm

Pin Configuration - 40- Contact TQFN

Description

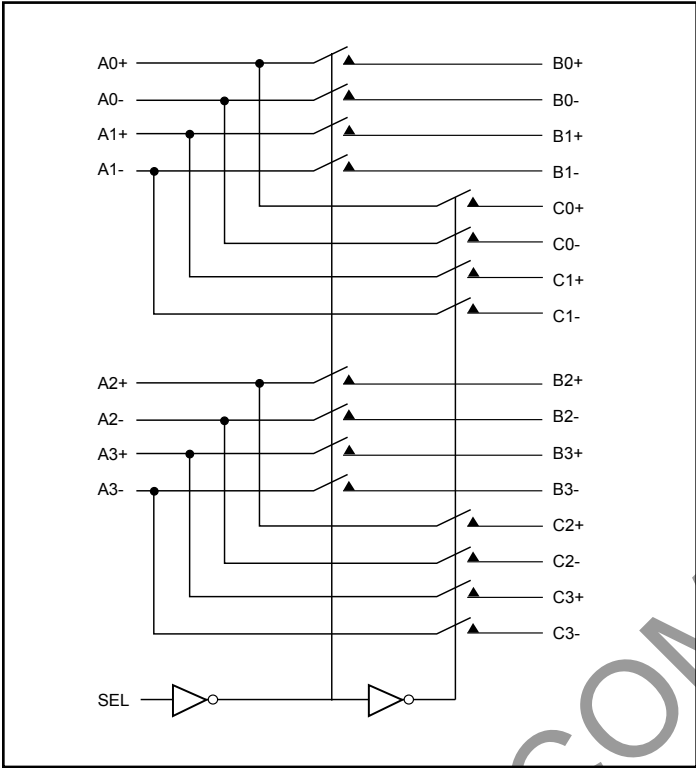
The PI3PCIE3412 is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express® 3.0, lanes to one of two locations. Using a unique design technique, Diodes has been able to minimize the impedance of the switch such that the attenuation observed through the switch is minimal. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification. PI3PCIE3412 can also be used for application up to 12Gbps

Application

Routing of PCI Express 3.0, DP1.2, USB3.0, SAS2.0, SATA3.0, XAUI, RXAUI signals with low signal attenuation.

Pin Configuration - 42- Contact TQFN


Block Diagram



Truth Table

Function	SEL
A_N to B_N	L
A_N to C_N	H



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PI3PCIE3412

Pin Description

Pin #		Pin Name	I/O	Description
42-TQFN	40-TQFN			
2	1	A0+	I/O	Signal I/O, Channel 0, Port A
3	2	A0-		
6	4	A1+	I/O	Signal I/O, Channel 1, Port A
7	5	A1-		
11	9	A2+	I/O	Signal I/O, Channel 2, Port A
12	10	A2-		
15	13	A3+	I/O	Signal I/O, Channel 3, Port A
16	14	A3-		
38	36	B0+	I/O	Signal I/O, Channel 0, Port B
37	35	B0-		
36	34	B1+	I/O	Signal I/O, Channel 1, Port B
35	33	B1-		
29	26	B2+	I/O	Signal I/O, Channel 2, Port B
28	25	B2-		
27	24	B3+	I/O	Signal I/O, Channel 3, Port B
26	23	B3-		
34	32	C0+	I/O	Signal I/O, Channel 0, Port C
33	31	C0-		
32	30	C1+	I/O	Signal I/O, Channel 1, Port C
31	29	C1-		
25	22	C2+	I/O	Signal I/O, Channel 2, Port C
24	21	C2-		
23	20	C3+	I/O	Signal I/O, Channel 3, Port C
22	19	C3-		
9	7	SEL	I	Operation mode Select (when SEL=0: A→B, when SEL=1: A→C)
5, 8, 13, 18, 20, 30, 40, 42	3, 6, 11, 17, 28, 38	V _{DD}	Pwr	3.3V ±10% Positive Supply Voltage
1, 4, 10, 14, 17, 19, 21, 39, 41, Center Pad	8, 12, 15, 16, 18, 27, 37, 39, 40	GND	Pwr	Power ground



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PI3PCIE3412

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +4.6V
Channel DC Input Voltage	-0.5V to 1.5V
DC Output Current	120mA
Power Dissipation	0.5W
SEL DC Input Voltage	-0.5V to 4.6V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I _{DD}	Total current from V _{DD} 3.3V supply	SEL = 0V or V _{DD}		0.15	1	mA
V _{I/O-DIF}	Differential Voltage (differential pins)				1.6	V _{ppd}
V _{I/O-CM}	Common Mode Voltage (differential pins)		0		0.8	v
T _A	Operating temperature range		-40		85	°C

DC Electrical Characteristics for Switching over Operating Range

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽¹⁾	Max.	Units
V _{IH} - SEL	Input HIGH Voltage, SEL Input		2		3.6	V
V _{IL} - SEL	Input LOW Voltage, SEL Input		0		0.8	
V _{IK}	Clamp Diode Voltage	V _{DD} = Max., I _{IN} = -18mA		-0.7	-1.2	
I _{IH}	Input HIGH Current, SEL	V _{DD} = Max., V _{IN} = V _{DD}			±5	μA
I _{IL}	Input LOW Current, SEL	V _{DD} = Max., V _{IN} = 0V			±5	
I _{IN} - SEL	Input Leakage Current, SEL Input	V _{IN} = V _{IH} - SEL Max or V _{IL} - SEL Min	-10		+10	
I _{IH}	Input HIGH Current, A _X , B _X , C _X	V _{DD} = Max., V _{IN} = 1.5V	-10		+10	μA
I _{IL}	Input LOW Current, A _X , B _X , C _X	V _{DD} = Max., V _{IN} = 0V	-10		+10	
I _{OZH}	HighZ HIGH Current, B _X , C _X	V _{DD} = Max., V _{IN} = 1.5V	-10		+10	
I _{OZL}	HighZ LOW Current, B _X , C _X	V _{DD} = Max., V _{IN} = 0V	-10		+10	μA
C _{I/O-ON}	ON state I/O capacitance			1.5		pF
R _{ON}	ON state resistance	V _{DD} = 3.3V, I _O = 8mA, V _{IN} = 0.8V		5		Ω

Note:

1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics

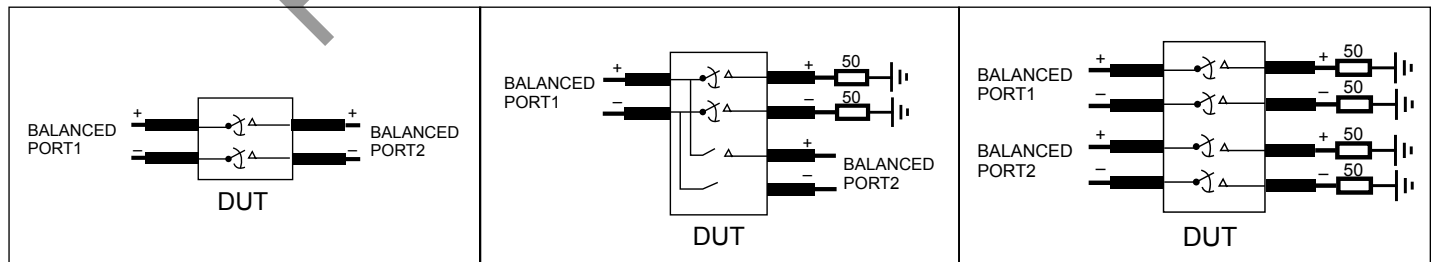
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PZH} , t _{PZL}	Line Enable Time - SEL to A _N , B _N , C _N		2	20	25	ns
t _{PHZ} , t _{PLZ}	Line Disable Time - SEL to A _N , B _N , C _N		0.5	5	25	
t _{b-b}	Bit-to-bit skew within the same differential pair			5	10	ps
t _{ch-ch}	Channel-to-channel skew				20	ps

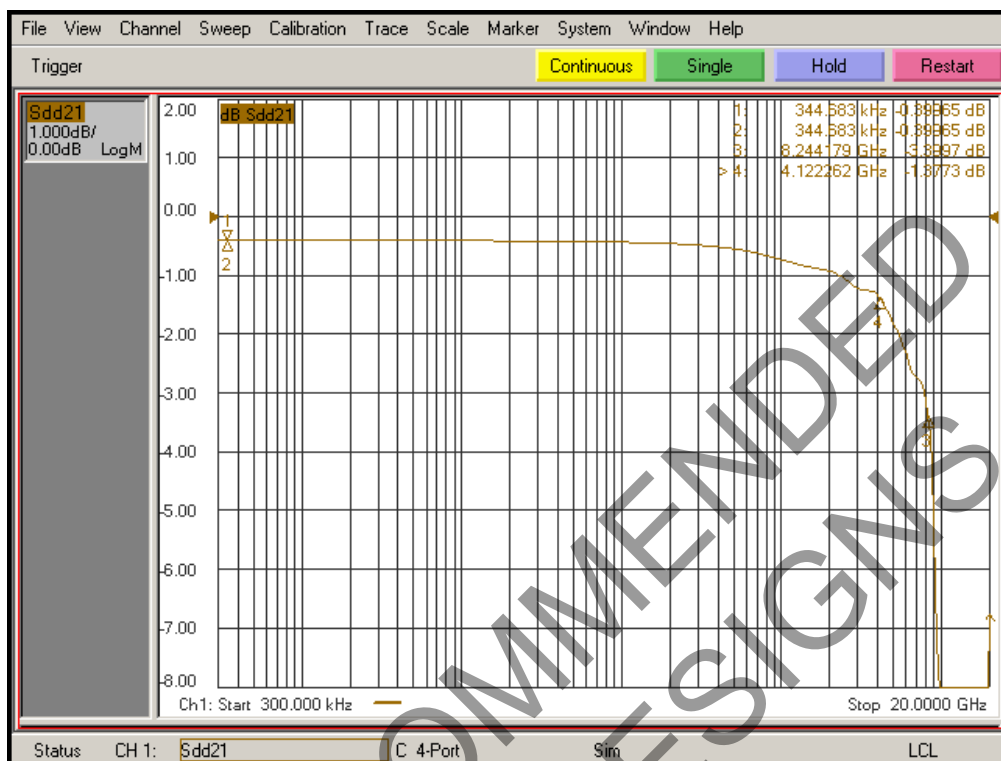
Dynamic Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
DDIL	Differential Insertion Loss ($V_{IN} = -10\text{dBm}$, DC = 0V)	$f = 50\text{MHz} - 1.25\text{GHz}$ $f = 1.25\text{GHz} - 2.5\text{GHz}$ $f = 2.5\text{GHz} - 4\text{GHz}$ $f = 5\text{GHz}$		-0.8 -1.0 -1.3 -1.8	-1 -1.2 -1.6 -2.2	dB
DDIL _{OFF}	Differential Off Isolation	$f = 50\text{MHz} - 1.25\text{GHz}$ $f = 1.25\text{GHz} - 2.5\text{GHz}$ $f = 2.5\text{GHz} - 4\text{GHz}$ $f = 5\text{GHz}$	-26.3 -21.4 -17.6 -16	-32.9 -26.7 -22 -20		dB
DDRL	Differential Return Loss	$f = 50\text{MHz} - 1.25\text{GHz}$ $f = 1.25\text{GHz} - 2.5\text{GHz}$ $f = 2.5\text{GHz} - 4\text{GHz}$ $f = 5\text{GHz}$	-20 -18.4 -16.8 -9.6	-25 -23 -21 -12		dB
DDNEXT	Near End Crosstalk	$f = 50\text{MHz} - 1.25\text{GHz}$ $f = 1.25\text{GHz} - 2.5\text{GHz}$ $f = 2.5\text{GHz} - 4\text{GHz}$ $f = 5\text{GHz}$	-34.1 -30.5 -28.1 -27.2	-42.6 -38.1 -35.1 -34		dB
V _{IF}	Max Signal Frequency Range	Insertion loss 1.5dB, $V_{IN} = 0.623\text{Vpp}$, DC=0V		4.0		GHz
		Insertion loss 1.5dB, $V_{IN} = 0.623\text{Vpp}$, DC=0.9V		4.0		
		Insertion loss 3dB, $V_{IN} = 0.623\text{Vpp}$, DC=0V		8.0		
		Insertion loss 3dB, $V_{IN} = 0.623\text{Vpp}$, DC=0.9V		8.0		
BW	-3dB Bandwidth			8.2		GHz

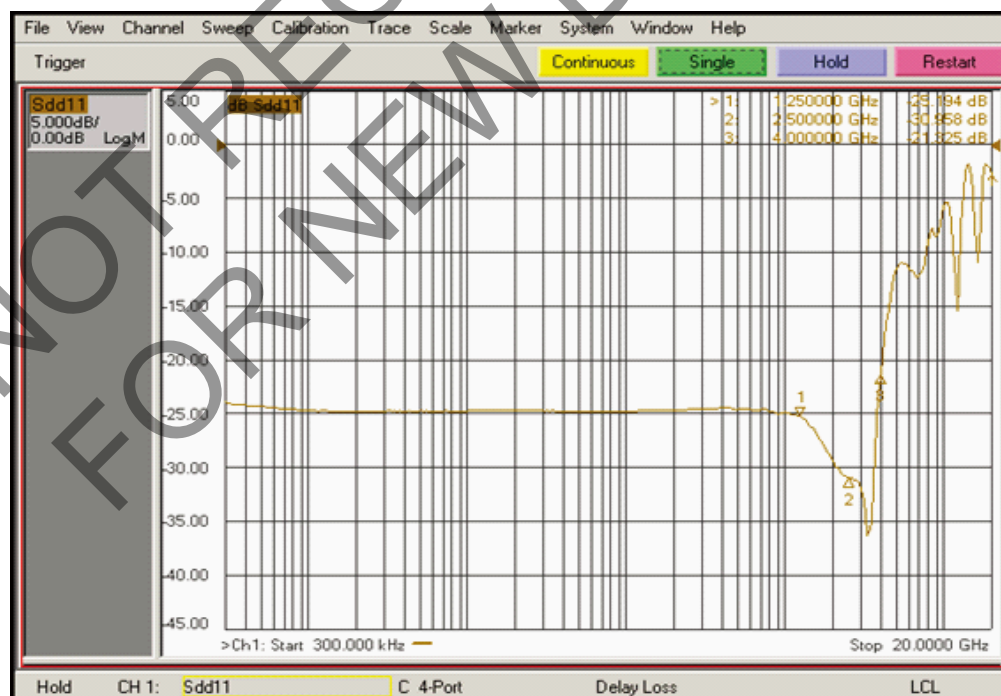
Notes:

1. Guaranteed by design. Typical values are at $V_{DD} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.

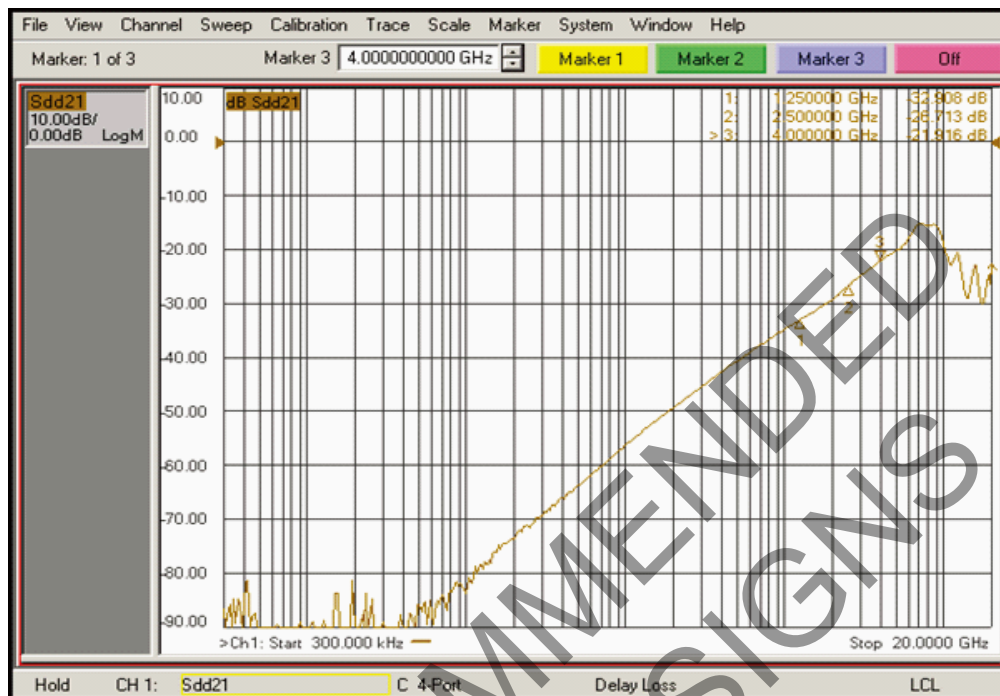

Diff. Insertion Loss and Return Test Circuit
Diff. Off Isolation Test Circuit
Diff. Near End Xtalk Test Circuit



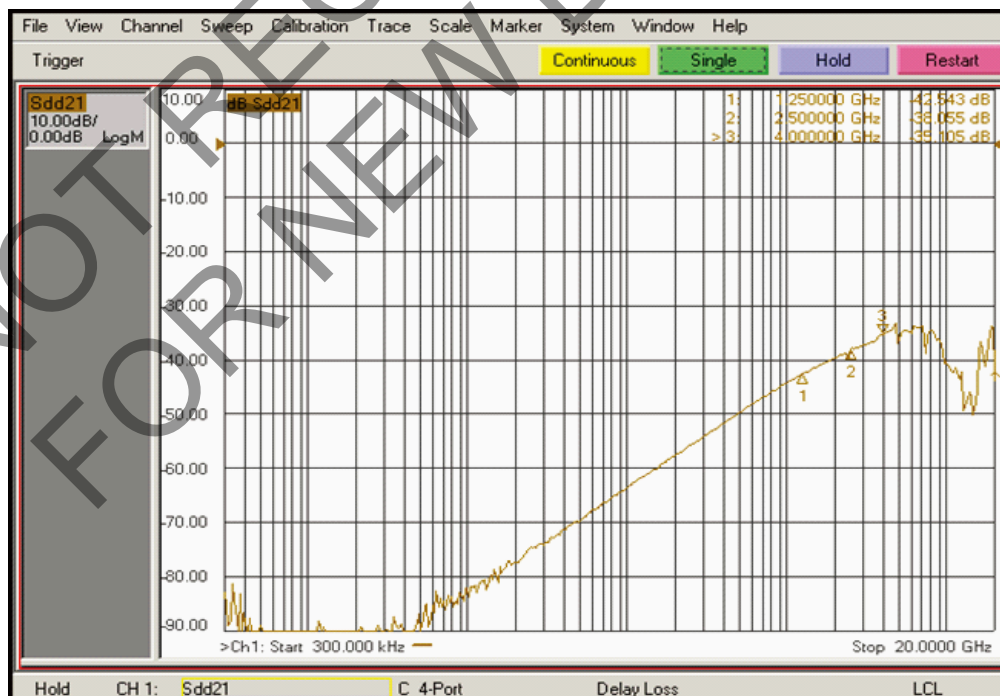
Differential Insertion Loss



Differential Return Loss

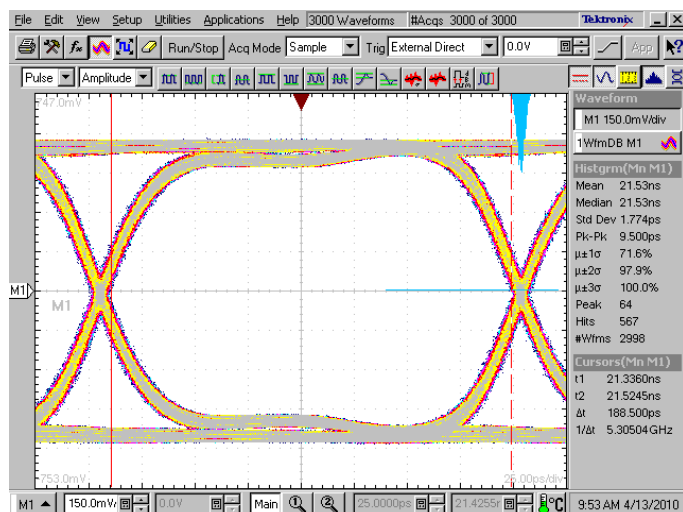


Differential Off Isolation

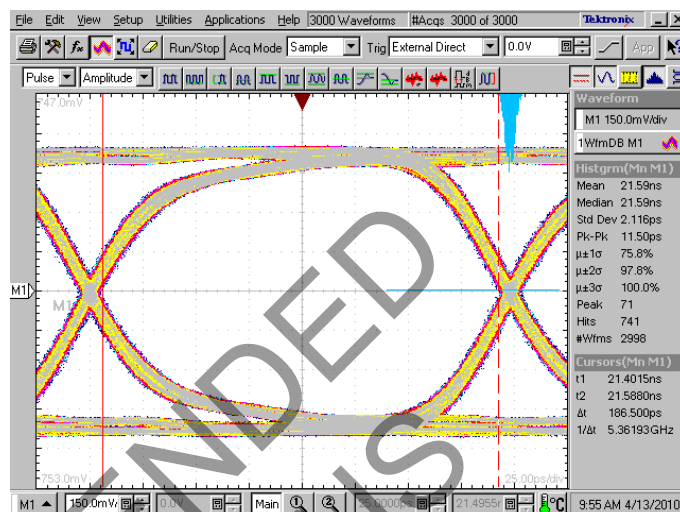


Differential Crosstalk

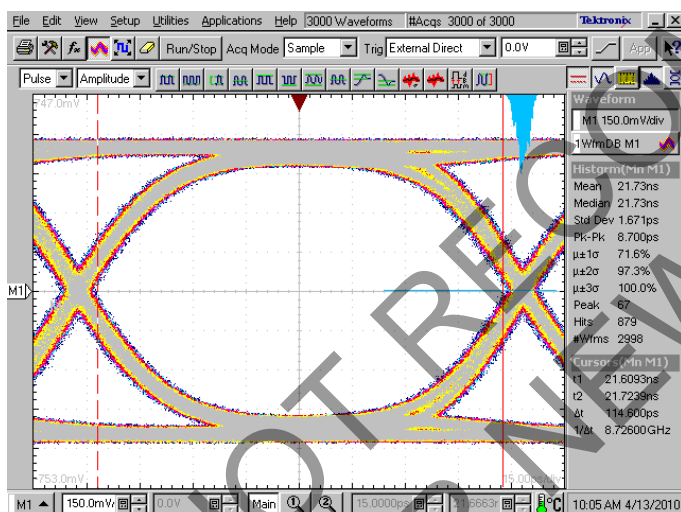
PI3PCIE3412



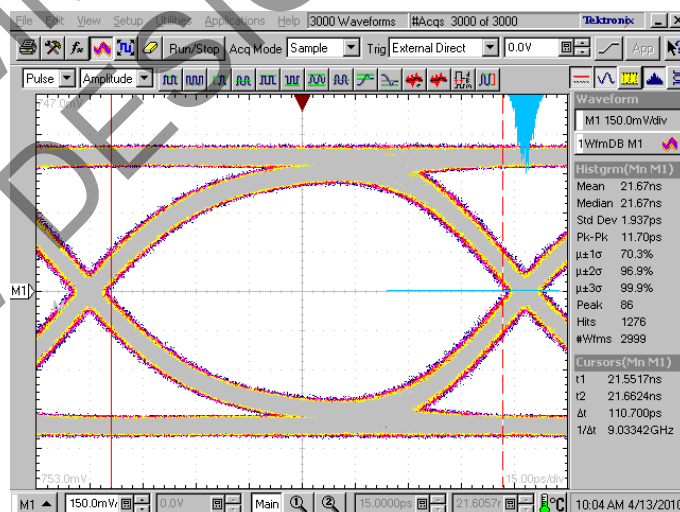
5.0 Gbps RX signal eye without PI3PCIE3412



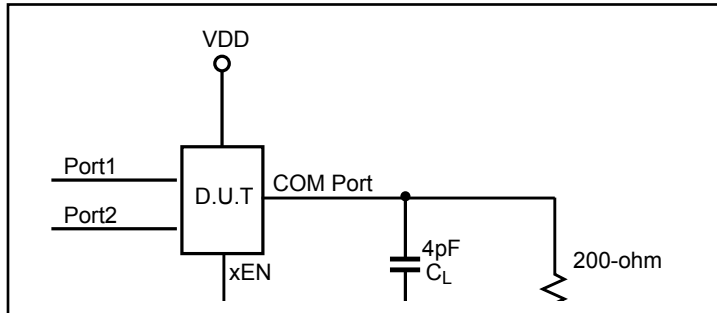
5.0 Gbps RX signal eye with PI3PCIE3412



8.0 Gbps RX signal eye without PI3PCIE3412



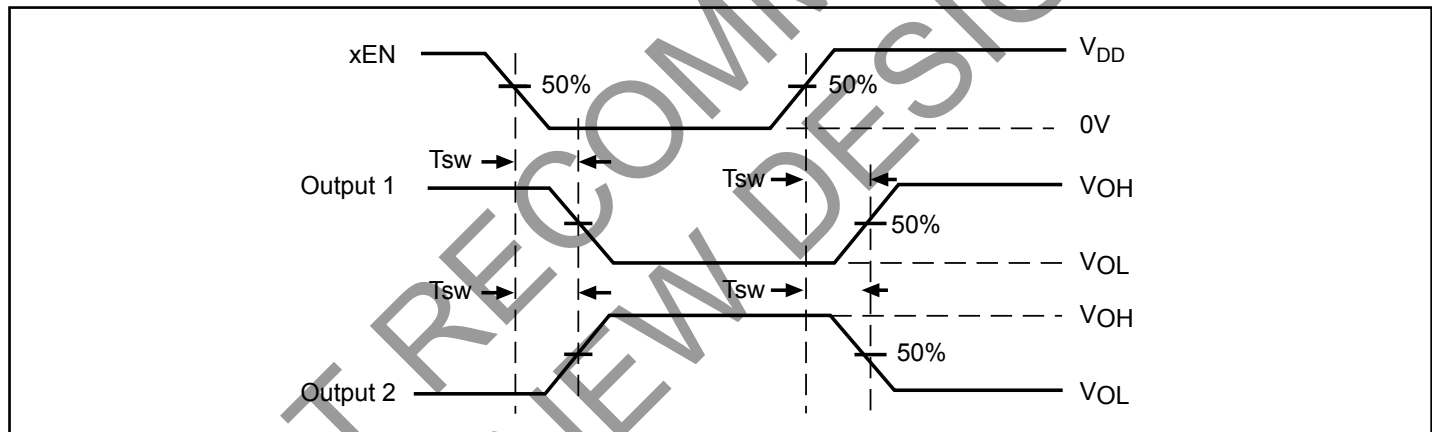
8.0 Gbps RX signal eye with PI3PCIE3412

Test Circuit for Electrical Characteristics⁽¹⁻⁵⁾

Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ} , t_{PZL}	3.0V
t_{PHZ} , t_{PZH}	GND
Prop Delay	Open

Switching Waveforms

Voltage Waveforms Enable and Disable Times

DP Source 1

DP Source 2

DP Source 3

DP_LANEx

DP_LANEx#

DP_AUX

DP_AUX#

DP_HPDP

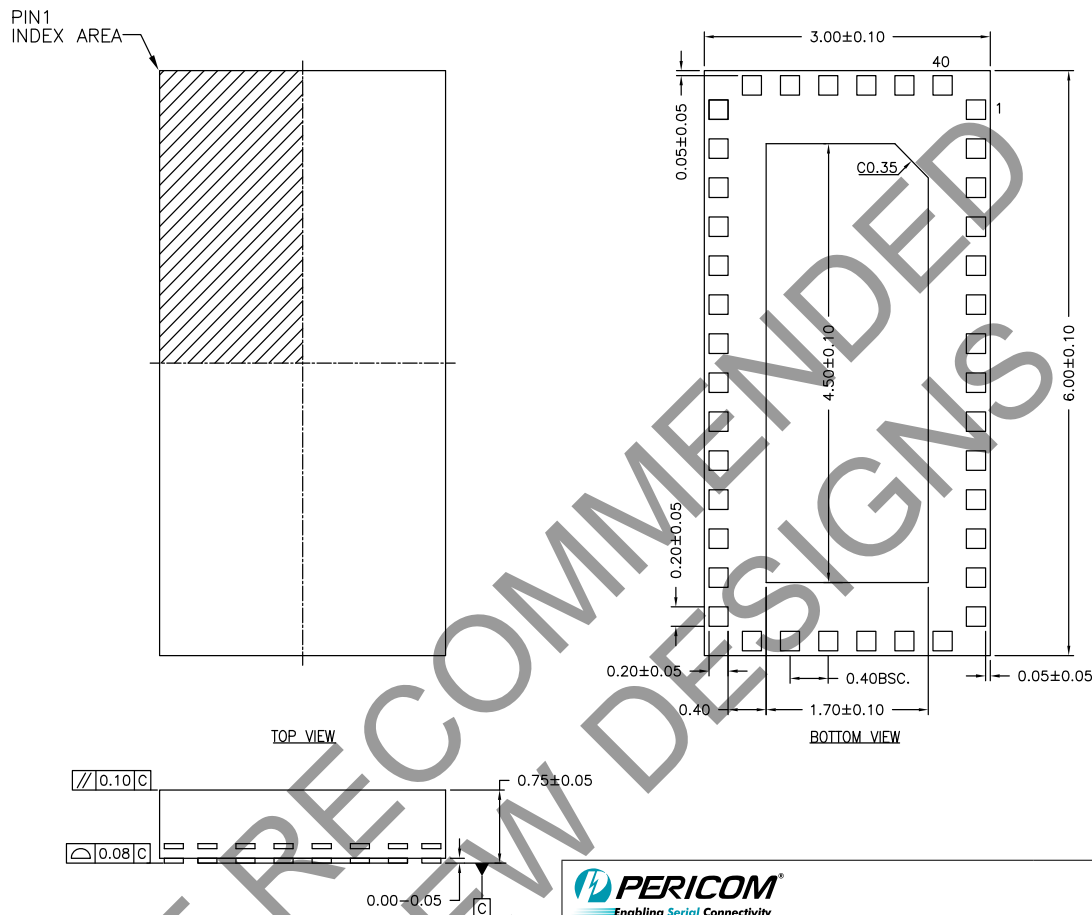
SEL_GPIO1

At least 1pc 4.7uF and 4pc 0.1uF decoupling capacitors are recommended. Each decoupling capacitor should be connected to PCB power plane via shortest path.

4Lane eDP Source Receptacle

4Lane eDP Source Receptacle

Packaging Information



Notes:

1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220



DATE: 07/11/13

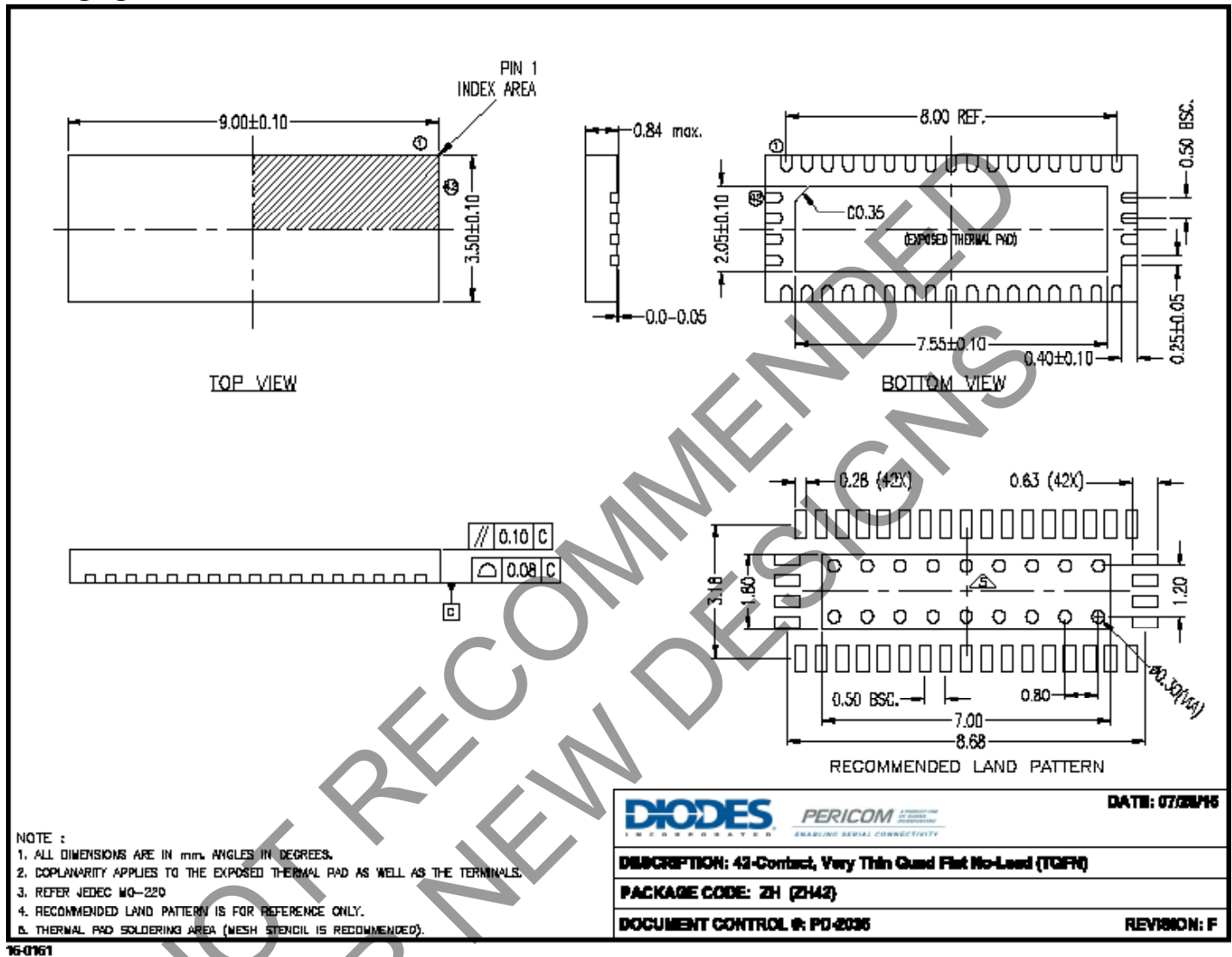
DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZL (ZL40)

DOCUMENT CONTROL #: PD-2165

REVISION: --

Packaging Information



Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE3412ZLE	ZL	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PI3PCIE3412ZLEX	ZL	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN), Tape & Reel
PI3PCIE3412ZHE	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN)
PI3PCIE3412ZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN), Tape & Reel

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging



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PI3PCIE3412

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