# S-19720 Series

## AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 50 mA VOLTAGE TRACKER WITH REVERSE CURRENT PROTECTION

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This IC, developed by using high-withstand voltage CMOS process technology, is a voltage tracker with a reverse current protection function, which has high-withstand voltage and low current consumption.
Since the maximum operating voltage is as high as 36 V and the current consumption is as low as 30 µA typ., it contributes to the reduction of standby current.
This IC operates stably due to the internal phase compensation circuit so that users are able to use low ESR ceramic capacitor as the output capacitor.
This IC includes an overcurrent protection circuit that prevents the load current from exceeding the current capacity of the output transistor and a thermal shutdown circuit that prevents damage because of overheating.
Due to the built-in reverse current protection function, the reverse current flowing from the VOUT pin to the VIN pin can be controlled as the small value –5 µA min. Therefore, IC protection diode is not needed.

ABLIC Inc. offers a "thermal simulation service" which supports the thermal design in conditions when our power management ICs are in use by customers. Our thermal simulation service will contribute to reducing the risk in the thermal design at customers' development stage.
ABLIC Inc. also offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
Contact our sales representatives for details.

**Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

## ■ Features

- Input voltage: 4.0 V to 36.0 V
- Offset voltage: ±5 mV (0.1 mA ≤ $I_{OUT}$ ≤ 50 mA)
- Dropout voltage: 160 mV typ. ($V_{ADJ / EN}$ = 4.0 V, $I_{OUT}$ = 10 mA)
- Current consumption: During operation: 30 µA typ.
  During power-off: 4.0 µA typ.
- Output current: Possible to output 50 mA ($V_{IN}$ = $V_{ADJ / EN}$ + 2.0 V)*1
- Input capacitor: A ceramic capacitor can be used. (1.0 µF or more)
- Output capacitor: A ceramic capacitor can be used. (1.0 µF to 1000 µF)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.
- Built-in thermal shutdown circuit: Detection temperature 175°C typ.
- Reverse current protection function: $I_{REV}$ = –5 µA min. ($V_{IN}$ = 0 V, $V_{ADJ / EN}$ = 5.0 V, $V_{OUT}$ = 16.0 V)
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*2

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
***2.** Contact our sales representatives for details.

## ■ Applications

- Power supply for automotive off-board sensors
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

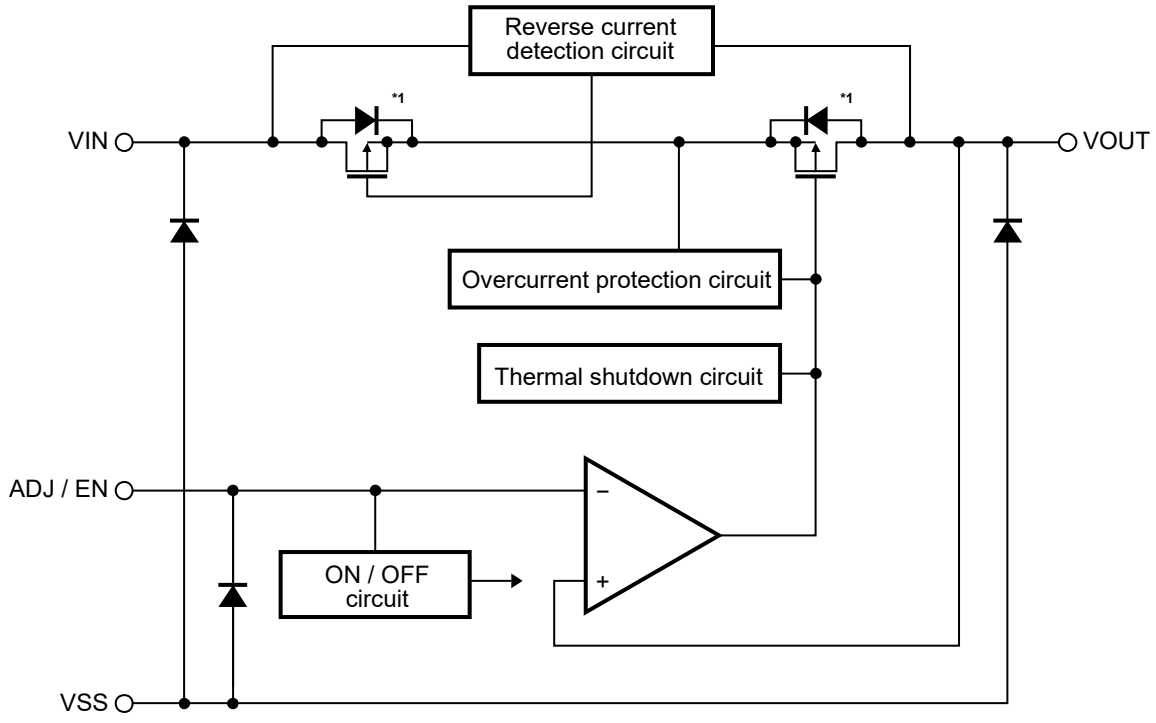
## ■ Packages

- SOT-23-5
- HSNT-6(2025)



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## ■ Block Diagram




***1.** Parasitic diode

**Figure 1**



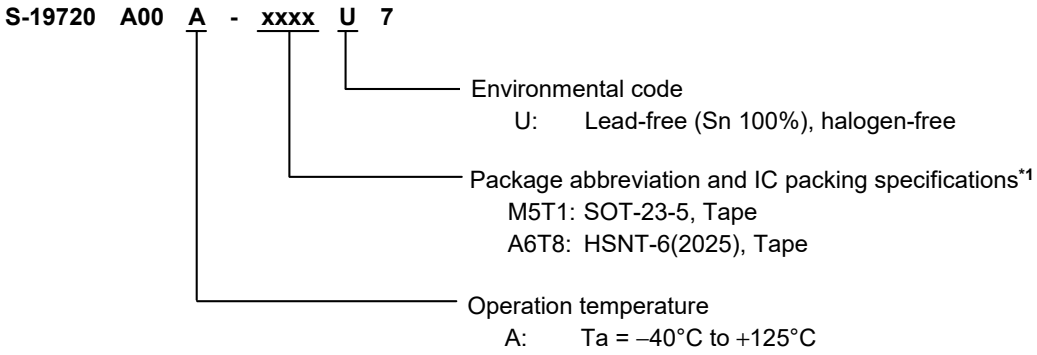
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## ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

## ■ Product Name Structure

### 1. Product name




***1.** Refer to the tape drawing.

### 2. Packages

**Table 1 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD | – |
| HSNT-6(2025) | PJ006-B-P-SD | PJ006-B-C-SD | PJ006-B-R-SD | PJ006-B-LM-SD |

### 3. Product name list

**Table 2**

| Product Name | Package |
|---|---|
| S-19720A00A-M5T1U7 | SOT-23-5 |
| S-19720A00A-A6T8U7 | HSNT-6(2025) |



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## ■ Pin Configurations

### 1. SOT-23-5

Top view

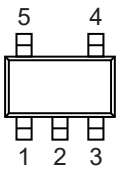



**Figure 2**

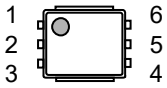
**Table 3**

| Pin No. | Symbol | Description | |
|---|---|---|---|
| 1 | ADJ / EN | ADJ | Output voltage adjustment pin |
| | | EN | Enable pin |
| 2 | VSS*1 | GND pin | |
| 3 | VIN | Input voltage pin | |
| 4 | VOUT | Output voltage pin | |
| 5 | VSS*1 | GND pin | |

***1.** Be sure to short the VSS pins.

### 2. HSNT-6(2025)

Top view




Bottom view

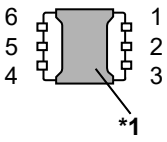



**Figure 3**

**Table 4**

| Pin No. | Symbol | Description | |
|---|---|---|---|
| 1 | VIN | Input voltage pin | |
| 2 | NC*2 | No connection | |
| 3 | ADJ / EN | ADJ | Output voltage adjustment pin |
| | | EN | Enable pin |
| 4 | VSS | GND pin | |
| 5 | NC*2 | No connection | |
| 6 | VOUT | Output voltage pin | |

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.



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## ■ Absolute Maximum Ratings

**Table 5**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|
| Input voltage | $V_{IN}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 45.0 | V |
| | $V_{ADJ / EN}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 45.0 | V |
| Output voltage | $V_{OUT}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 45.0 | V |
| Output current | $I_{OUT}$ | 65 | mA |
| Junction temperature | $T_j$ | –40 to +150 | °C |
| Operation ambient temperature | $T_{opr}$ | –40 to +125 | °C |
| Storage temperature | $T_{stg}$ | –40 to +150 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Recommended Operation Conditions

**Table 6**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VIN pin voltage | $V_{IN}$ | – | 4.0 | – | 36 | V |
| ADJ / EN pin voltage | $V_{ADJ / EN}$ | – | 2.0 | – | 18 | V |
| Output current*1 | $I_{OUT}$ | – | 0.1 | – | 50 | mA |
| Input capacitor | $C_{IN}$ | – | 1.0 | – | – | µF |
| Output capacitor | $C_L$ | – | 1.0 | – | 1000 | µF |
| | ESR | – | – | – | 3 | Ω |

***1.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.

## ■ Thermal Resistance Value

**Table 7**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance*1 | $\theta_{JA}$ | SOT-23-5 | Board A | – | 192 | – | °C/W |
| | | | Board B | – | 160 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |
| | | HSNT-6(2025) | Board A | – | 180 | – | °C/W |
| | | | Board B | – | 128 | – | °C/W |
| | | | Board C | – | 43 | – | °C/W |
| | | | Board D | – | 44 | – | °C/W |
| | | | Board E | – | 36 | – | °C/W |

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "**■ Power Dissipation**" and "**Test Board**" for details.



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## ■ Electrical Characteristics

**Table 8**

($V_{IN}$ = 13.5 V, $T_j$ = −40°C to +150°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Offset voltage*1 | $\Delta V_{OUT}$ | 2.0 V ≤ $V_{ADJ / EN}$ ≤ $V_{IN}$ − 2.0 V, $V_{ADJ / EN}$ ≤ 18.0 V | 4.0 V ≤ $V_{IN}$ ≤ 24.0 V, 0.1 mA ≤ $I_{OUT}$ ≤ 50 mA | −5 | – | +5 | mV | 1 |
| | | | 4.0 V ≤ $V_{IN}$ ≤ 36.0 V, 0.1 mA ≤ $I_{OUT}$ ≤ 25 mA | −5 | – | +5 | mV | 1 |
| Dropout voltage*2 | $V_{drop}$ | $V_{ADJ / EN}$ ≥ 4.0 V, $I_{OUT}$ = 10 mA | | – | 160 | 300 | mV | 2 |
| Line regulation*3 | $\Delta V_{OUT1}$ | 6.0 V ≤ $V_{IN}$ ≤ 36.0 V, $I_{OUT}$ = 10 mA, $V_{ADJ / EN}$ = 5.0 V | | – | – | 5 | mV | 2 |
| Load regulation*4 | $\Delta V_{OUT2}$ | 0.1 mA ≤ $I_{OUT}$ ≤ 50 mA, $V_{ADJ / EN}$ = 5.0 V | | – | – | 5 | mV | 2 |
| Input voltage | $V_{IN}$ | – | | 4.0 | – | 36.0 | V | – |
| Current consumption during operation | $I_{SS1}$ | $V_{ADJ / EN}$ = 5.0 V, $I_{OUT}$ = 0.01 mA | | – | 30 | 50 | µA | 3 |
| Reverse current | $I_{REV}$ | $V_{IN}$ = 0 V, $V_{ADJ / EN}$ = 5.0 V, $V_{OUT}$ = 16.0 V | | −5 | 0 | – | µA | 4 |
| Current consumption during power-off | $I_{SS2}$ | $V_{ADJ / EN}$ = 0 V | | – | 4.0 | 15.0 | µA | 5 |
| ADJ / EN pin input voltage "H" | $V_{ADJH}$ | Determined by $V_{OUT}$ output level | | 2.0 | – | – | V | 6 |
| ADJ / EN pin input voltage "L" | $V_{ADJL}$ | Determined by $V_{OUT}$ output level | | – | – | 0.5 | V | 6 |
| ADJ / EN pin input current "H" | $I_{ADJH}$ | $V_{ADJ / EN}$ = 5.0 V | | −0.1 | – | 2 | µA | 6 |
| ADJ / EN pin input current "L" | $I_{ADJL}$ | $V_{ADJ / EN}$ = 0 V | | −0.1 | – | 0.1 | µA | 6 |
| Ripple rejection | \|RR\| | f = 100 Hz, $\Delta V_{rip}$ = 0.5 $V_{pp}$, $I_{OUT}$ = 5 mA | | – | 80 | – | dB | 7 |
| Limit current | $I_{LIM}$ | $V_{IN}$ = 7.0 V, $V_{ADJ / EN}$ = 5.0 V, $V_{OUT}$ = $V_{ADJ / EN}$ × 0.85 | | 80 | 180 | 330 | mA | 8 |
| Short-circuit current | $I_{short}$ | $V_{IN}$ = 7.0 V, $V_{ADJ / EN}$ = 5.0 V, $V_{OUT}$ = 0 V | | 80 | 180 | 330 | mA | 8 |
| Thermal shutdown detection temperature | $T_{SD}$ | Junction temperature | | – | 175 | – | °C | – |
| Thermal shutdown release temperature | $T_{SR}$ | Junction temperature | | – | 165 | – | °C | – |

***1.** Indicates the difference between output voltage ($V_{OUT}$) and ADJ / EN pin voltage ($V_{ADJ / EN}$).
The accuracy is guaranteed when the input voltage, output current, and temperature satisfy the conditions listed above.
$\Delta V_{OUT} = V_{OUT} - V_{ADJ / EN}$

***2.** Indicates the difference between input voltage ($V_{IN1}$) and the output voltage when the output voltage becomes 98% of the output voltage value ($V_{OUT3}$) after the input voltage ($V_{IN}$) is decreased gradually.
$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$
$V_{OUT3}$: Output voltage value at $V_{IN} = V_{ADJ / EN} + 2.0$ V, and $I_{OUT}$ = 10 mA

***3.** Indicates the dependency of the output voltage against the input voltage. The value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

***4.** Indicates the dependency of the output voltage against the output current. The value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.



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## ■ Test Circuits

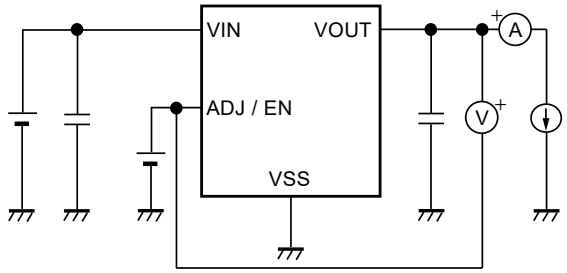



Figure 4 Test Circuit 1

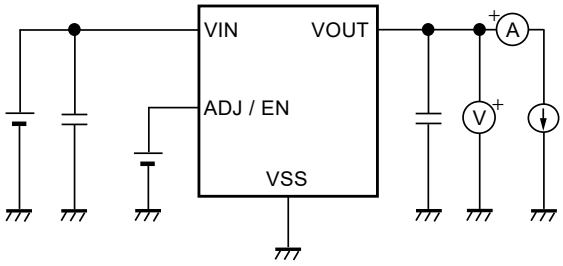



Figure 5 Test Circuit 2

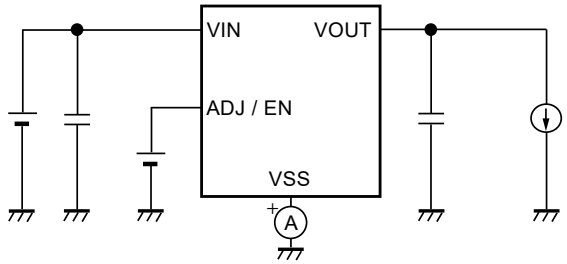



Figure 6 Test Circuit 3

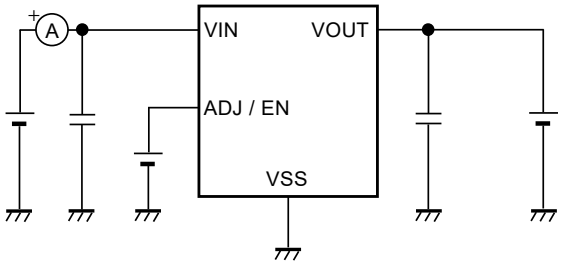



Figure 7 Test Circuit 4

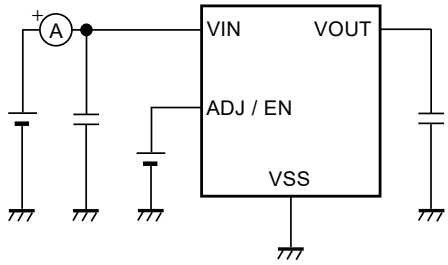



Figure 8 Test Circuit 5

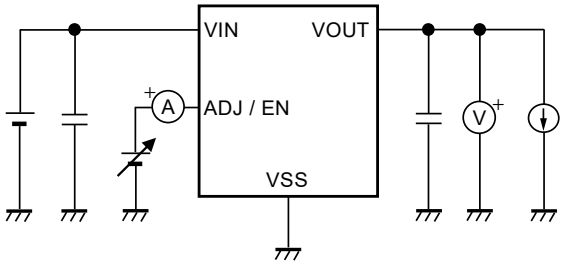



Figure 9 Test Circuit 6

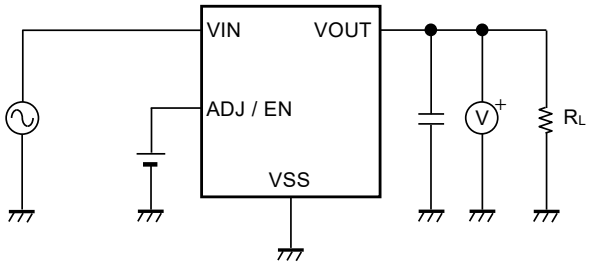



Figure 10 Test Circuit 7

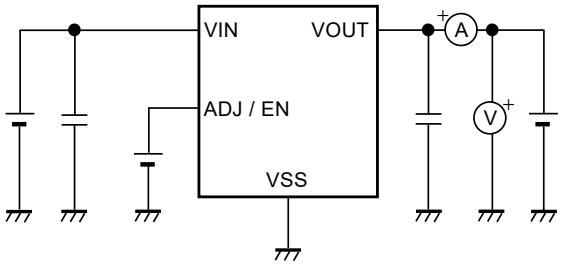
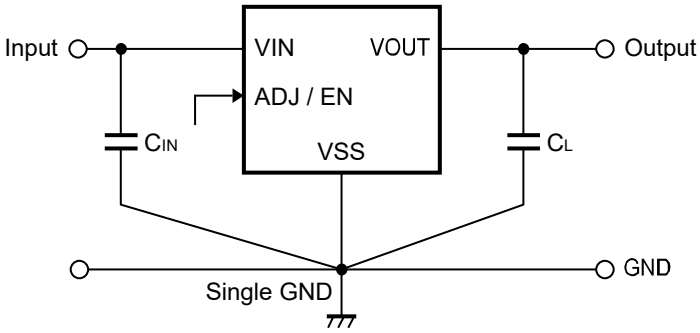



Figure 11 Test Circuit 8



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## ■ Standard Circuit




***1.** $C_{IN}$ is a capacitor for stabilizing the input.
***2.** $C_L$ is a capacitor for stabilizing the output.

**Figure 12**

**Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.**

## ■ Condition of Application

Input capacitor ($C_{IN}$): A ceramic capacitor with capacitance of 1.0 µF or more is recommended.
Output capacitor ($C_L$): A ceramic capacitor with capacitance of 1.0 µF to 1000 µF is recommended.

**Caution Generally, in a voltage tracker, an oscillation may occur depending on the selection of the external parts. Perform thorough evaluation including the temperature characteristics with an actual application using the above capacitors to confirm no oscillation occurs.**

## ■ Selection of Input Capacitor ($C_{IN}$) and Output Capacitor ($C_L$)

This IC requires $C_L$ between the VOUT pin and the VSS pin for phase compensation. The operation is stabilized by a ceramic capacitor with capacitance of 1.0 µF to 1000 µF over the entire temperature range. When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance also must be 1.0 µF to 1000 µF. However, an oscillation may occur depending on the equivalent series resistance (ESR).
Moreover, this IC requires $C_{IN}$ between the VIN pin and the VSS pin for a stable operation.
Generally, an oscillation may occur when a voltage tracker is used under the condition that the impedance of the power supply is high.
Note that the output voltage transient characteristics varies depending on the capacitance of $C_{IN}$ and $C_L$ and the value of ESR.

**Caution Perform thorough evaluation including the temperature characteristics with an actual application to select $C_{IN}$ and $C_L$.**



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# ■ Operation

## 1. Basic operation

**Figure 13** shows the block diagram of this IC to describe the basic operation.
The error amplifier compares the output voltage ($V_{OUT}$) with the ADJ / EN pin voltage ($V_{ADJ / EN}$).
The error amplifier controls the output transistor to keep $V_{OUT}$ equal to $V_{ADJ / EN}$ without being affected by the input voltage ($V_{IN}$), that is, the tracking operation is performed.

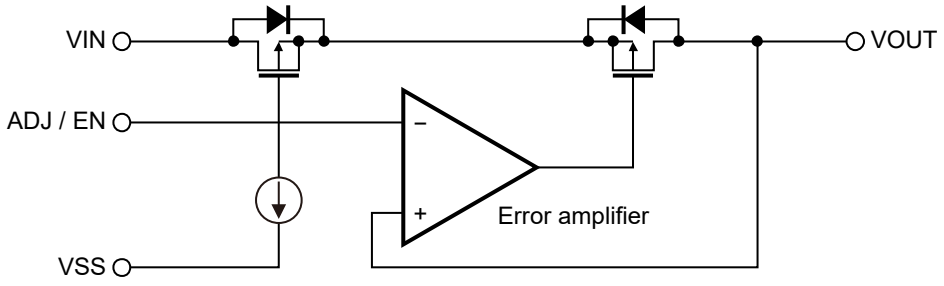



**Figure 13**

## 2. Output transistor

In this IC, a low on-resistance P-channel MOS FET is used between the VIN pin and the VOUT pin as the output transistor. In order to maintain the tracking operation of $V_{ADJ / EN}$ and $V_{OUT}$, the on-resistance of the output transistor varies appropriately according to the output current ($I_{OUT}$).
Also, the reverse current prevention transistor is connected in series with the output transistor.

## 3. ADJ / EN pin

The ADJ / EN pin controls the internal circuit and the output transistor in order to start and stop the tracker.
When the ADJ / EN pin is set to ON ($V_{ADJ / EN} \geq V_{ADJH}$), the tracking operation starts and $V_{OUT}$ is adjusted so that it becomes equal to $V_{ADJ / EN}$.
When the ADJ / EN pin is set to OFF, the internal circuit stops operating and the output transistor between the VIN pin and the VOUT pin is turned off, reducing current consumption significantly.
The ADJ / EN pin is internally pulled down to the VSS pin in the floating status, so the VOUT pin is set to the $V_{SS}$ level.

**Table 9**

| ADJ / EN Pin | Internal Circuit | $V_{OUT}$ | Current Consumption |
|---|---|---|---|
| "H": ON | Operate | $\cong V_{ADJ / EN}$ | $I_{SS1}$ |
| "L": OFF | Stop | $V_{SS}$*1 | $I_{SS2}$ |

***1.** The VOUT pin is not pulled down internally. The VOUT pin voltage changes to $V_{SS}$ level by the load connected to the VOUT pin.



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### 4. Overcurrent protection circuit

This IC includes an overcurrent protection circuit which having the characteristics shown in "**1. Output voltage vs. Output current (When load current increases) (Ta = +25°C)**" in "**■ Characteristics (Typical Data)**", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin.
When the load current increases and reaches the limit current ($I_{LIM}$), the overcurrent protection circuit operates, and the output current is limited based on $I_{LIM}$. When the output is short-circuited (the VOUT pin is shorted to the VSS pin), the output current is limited to short-circuit current ($I_{short}$). $I_{LIM}$ and $I_{short}$ are internally set at 180 mA typ.
This IC restarts the tracking operation over $V_{OUT}$ and $V_{ADJ\,/\,EN}$ when the output transistor is released from the overcurrent status.

**Caution** **This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting inside, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation of the package.**

### 5. Thermal shutdown circuit

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 175°C typ., the thermal shutdown circuit becomes the detection status, and the tracking operation is stopped. When the junction temperature decreases to 165°C typ., the thermal shutdown circuit becomes the release status, and the tracking operation is restarted.
If the thermal shutdown circuit becomes the detection status due to self-heating, the tracking operation is stopped and $V_{OUT}$ decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the tracking operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of $V_{OUT}$ into a pulse-like form. This phenomenon continues unless decreasing either or both of $V_{IN}$ and $I_{OUT}$ in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

**Caution** **If a large load current flows during the restart process of the tracking operation after the thermal shutdown circuit changes to the release status from the detection status, the thermal shutdown circuit becomes the detection status again due to self-heating, and a problem may happen in the restart of the tracking operation. A large load current, for example, occurs when charging to the $C_L$ whose capacitance is large.**
**Perform thorough evaluation including the temperature characteristics with an actual application to select $C_L$.**

**Table 10**

| Thermal Shutdown Circuit | $V_{OUT}$ |
|---|---|
| Release: 165°C typ.*1 | $\cong V_{ADJ\,/\,EN}$ |
| Detection: 175°C typ.*1 | $V_{SS}$*2 |

***1.** Junction temperature
***2.** The VOUT pin is not pulled down internally.
The VOUT pin voltage changes to $V_{SS}$ level by the load connected to the VOUT pin.



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## 6. Reverse current protection function

The reverse current protection function compares values of $V_{IN}$ and $V_{OUT}$, and prevents the current from flowing to the VIN pin from the VOUT pin.
During the reverse current protection mode, the reverse current detection circuit turns off the reverse current protection transistor between the VIN pin and the output transistor and blocks the reverse current from the VOUT pin.
In the case of $V_{OUT} - V_{IN} < V_{REVD}$, this IC is in normal operation mode (refer to **Figure 14**). The reverse current protection mode is detected when $V_{OUT} - V_{IN} \geq V_{REVD}$ (refer to **Figure 15**). In order to insure the stable operation, there is also a hysteresis for detection and release of the reverse current protection mode. Therefore, the reverse current protection mode is released when $V_{OUT} - V_{IN} \leq V_{REVR}$.
The reverse current protection function also operates when the ADJ / EN pin is set to OFF level.

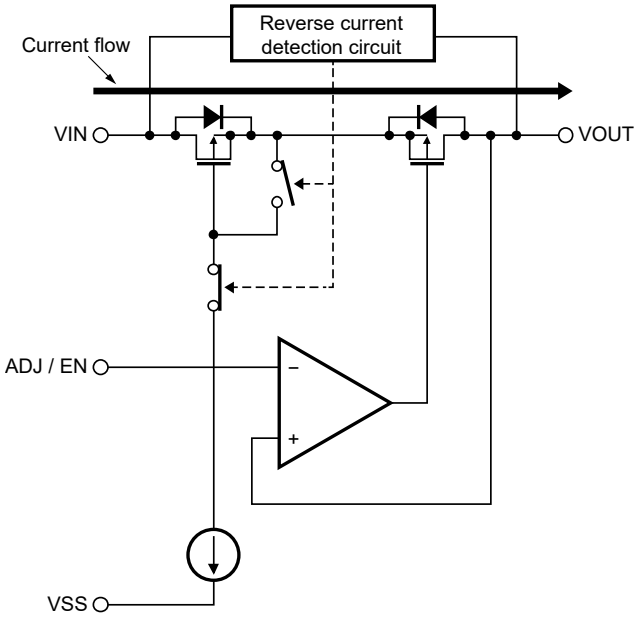



**Figure 14 Normal Operation Mode**

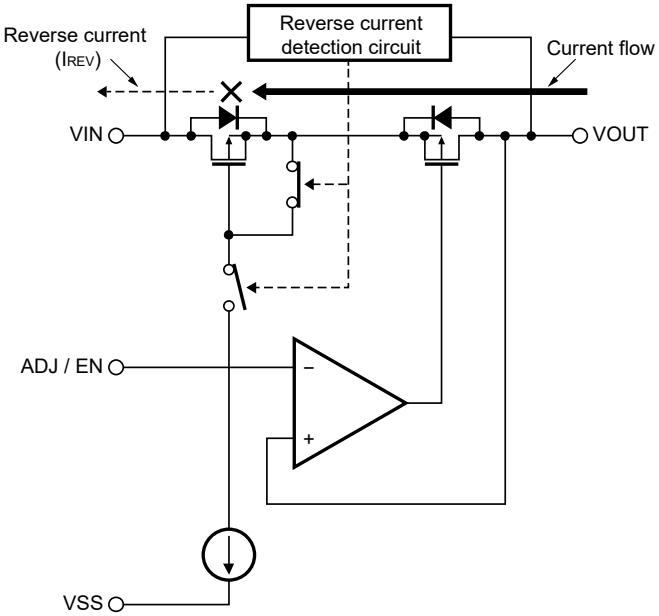



**Figure 15 Reverse Current Protection Mode**

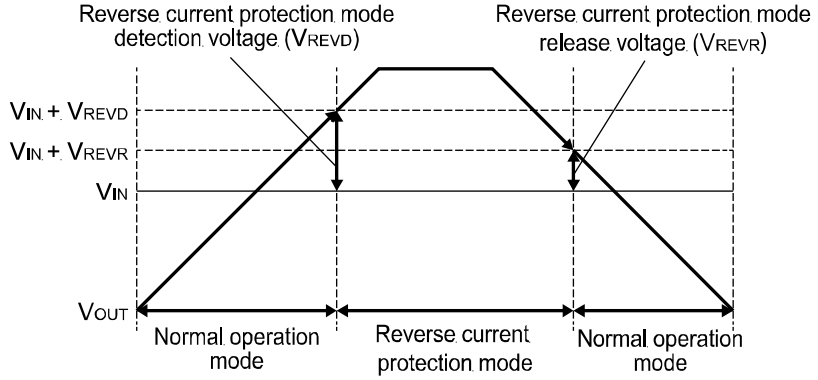



**Figure 16**

**Table 11**

| Reverse current protection mode detection voltage ($V_{REVD}$) | Reverse current protection mode release voltage ($V_{REVR}$) |
|---|---|
| 0.50 V typ. | 0.33 V typ. |



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## ■ Precautions

- Generally, when a voltage tracker is used under the condition that the load current value is small (0.1 mA or less), the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage tracker is used under the condition that the temperature is high, the output voltage may increase due to the leakage current of an output transistor.
- Generally, when the ADJ / EN pin of a voltage tracker is used under the condition of OFF, the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage tracker is used under the condition that the impedance of the power supply is high, an oscillation may occur. Perform thorough evaluation including the temperature characteristics with an actual application to select $C_{IN}$.
- Generally, in a voltage tracker, an oscillation may occur depending on the selection of the external parts. The following use conditions are recommended in this IC, however, perform thorough evaluation including the temperature characteristics with an actual application to select $C_{IN}$ and $C_L$.
  Input capacitor ($C_{IN}$): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
  Output capacitor ($C_L$): A ceramic capacitor with capacitance of 1.0 μF to 1000 μF is recommended.
- Generally, in a voltage tracker, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage start-up, input voltage fluctuation and load fluctuation etc., or the capacitance of $C_{IN}$ or $C_L$ and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select $C_{IN}$ and $C_L$.
- Generally, in a voltage tracker, an overshoot may occur in the output voltage momentarily if the input voltage steeply changes when the input voltage is started up or the input voltage fluctuates etc. Perform thorough evaluation including the temperature characteristics with an actual application to confirm no problems happen.
- Generally, in a voltage tracker, if the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including $C_L$ on the application. The resonance phenomenon is expected to be weakened by inserting a series resistor into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- If the input voltage is started up steeply under the condition that the capacitance of $C_L$ is large, the thermal shutdown circuit may be in the detection status by self-heating due to the charge current to $C_L$.
- Make sure of the conditions for the input voltage, output voltage and the load current so that the internal loss does not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- When considering the output current value that this IC is able to output, make sure of the output current value specified in **Table 6** in "**■ Recommended Operation Conditions**" and footnote ***1** of the table.
- Wiring patterns on the application related to the VIN pin, the VOUT pin and the VSS pin should be designed so that the impedance is low. When mounting $C_{IN}$ between the VIN pin and the VSS pin and $C_L$ between the VOUT pin and the VSS pin, connect the capacitors as close as possible to the respective destination pins of this IC.
- In the package equipped with heat sink of backside, mount the heat sink firmly. Since the heat radiation differs according to the condition of the application, perform thorough evaluation with an actual application to confirm no problems happen.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

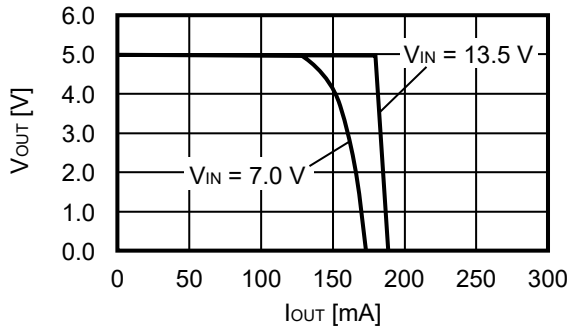


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## ■ Characteristics (Typical Data)

### 1. Output voltage vs. Output current (When load current increases) (Ta = +25°C)

#### 1. 1 $V_{ADJ / EN}$ = 5.0 V

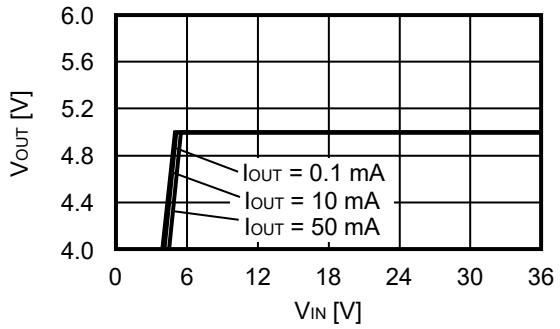



**Remark** In determining the output current, attention should be paid to the following.

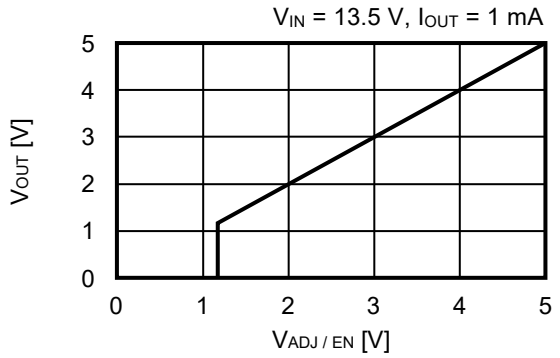
1. The output current value and footnote ***1** of **Table 6** in "■ **Recommended Operation Conditions**"
2. Power dissipation

### 2. Output voltage vs. Input voltage (Ta = +25°C)

#### 2. 1 $V_{ADJ / EN}$ = 5.0 V




### 3. Output voltage vs. ADJ / EN pin input voltage (Ta = +25°C)

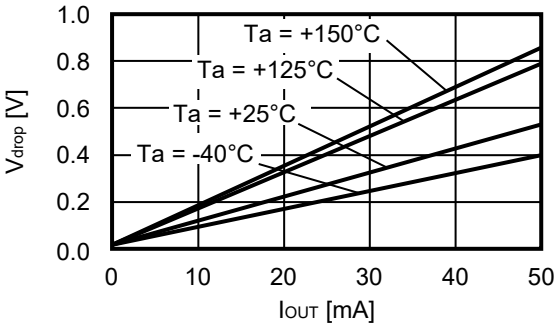





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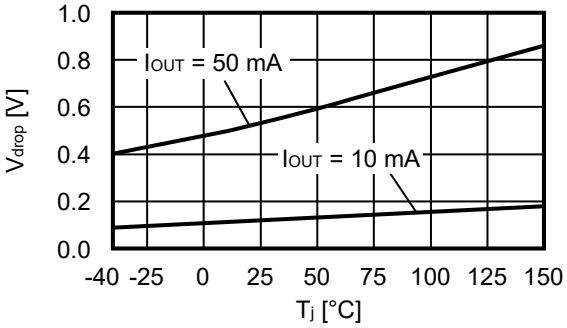
### 4. Dropout voltage vs. Output current

#### 4. 1 $V_{ADJ / EN}$ = 5.0 V

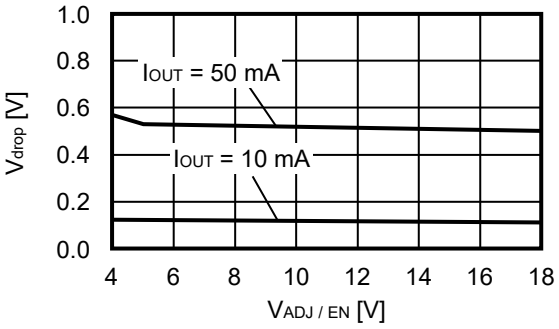



### 5. Dropout voltage vs. Junction temperature

#### 5. 1 $V_{ADJ / EN}$ = 5.0 V

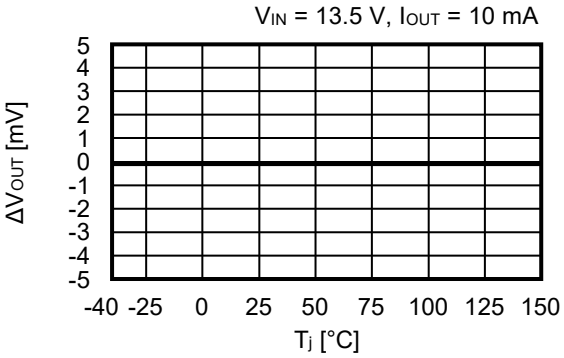



### 6. Dropout voltage vs. Set output voltage (Ta = +25°C)



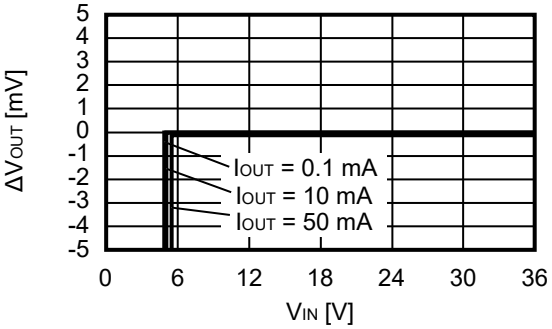

### 7. Offset voltage vs. Junction temperature

#### 7. 1 $V_{ADJ / EN}$ = 5.0 V



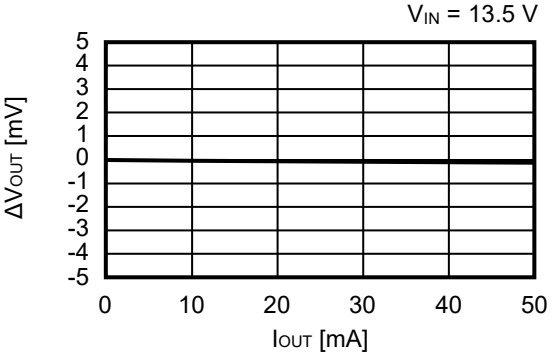

### 8. Offset voltage vs. Input voltage (Ta = +25°C)

#### 8. 1 $V_{ADJ / EN}$ = 5.0 V




### 9. Offset voltage vs. Output current (Ta = +25°C)

#### 9. 1 $V_{ADJ / EN}$ = 5.0 V

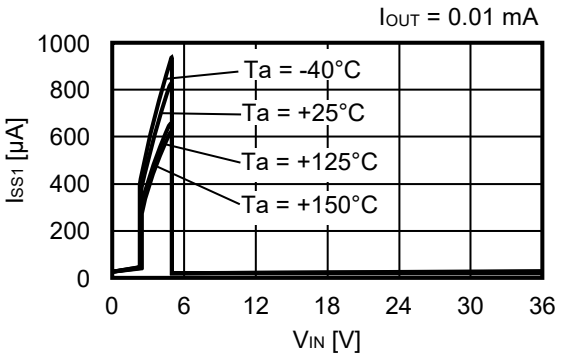


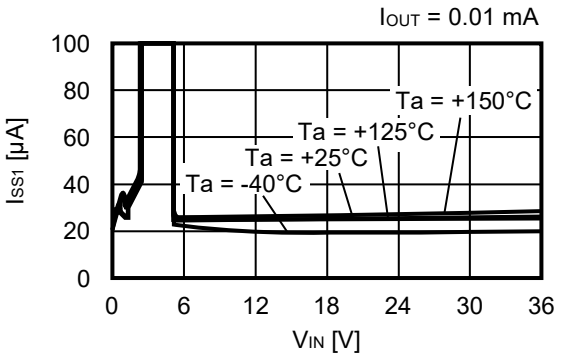



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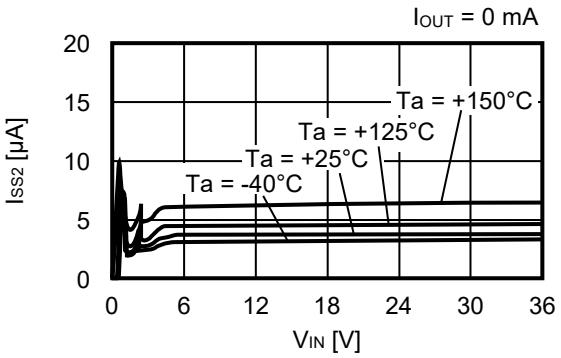
## 10. Current consumption vs. Input voltage

### 10. 1 $V_{ADJ / EN}$ = 5.0 V (during operation)



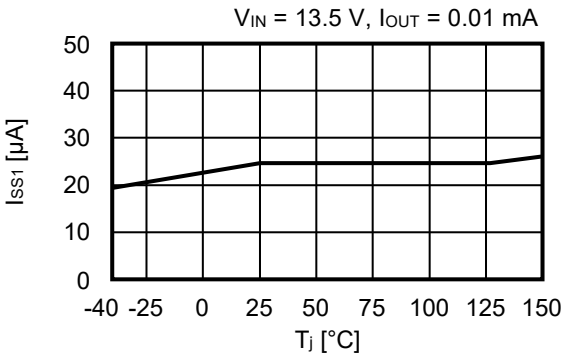




### 10. 2 $V_{ADJ / EN}$ = 0.0 V (Power-off)

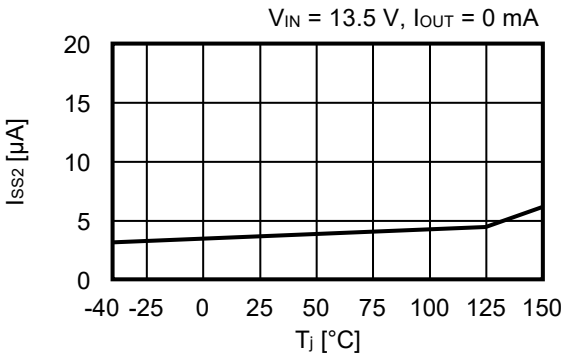



## 11. Current consumption vs. Junction temperature

### 11. 1 $V_{ADJ / EN}$ = 5.0 V (during operation)

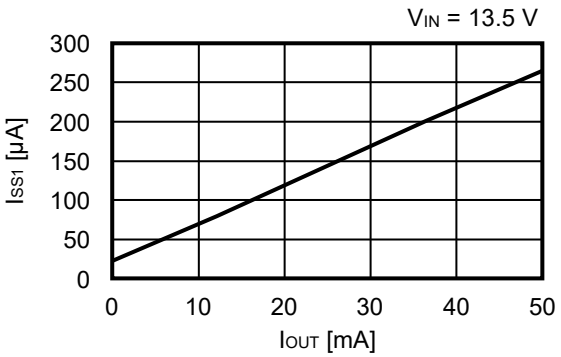



### 11. 2 $V_{ADJ / EN}$ = 0.0 V (Power-off)




## 12. Current consumption during operation vs. Output current (Ta = +25°C)

### 12. 1 $V_{ADJ / EN}$ = 5.0 V

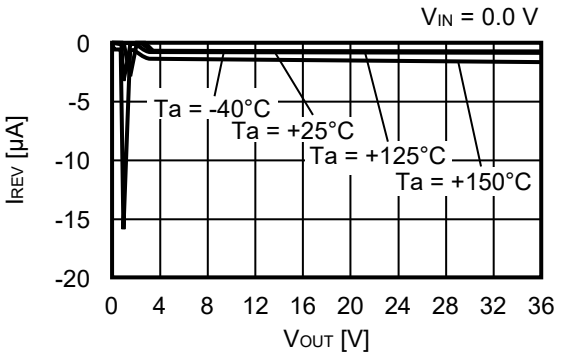


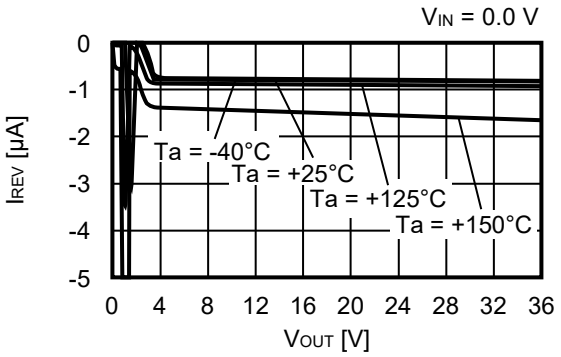



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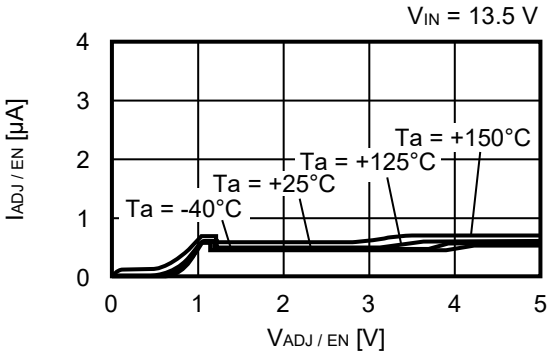
## 13. Reverse current vs. VOUT pin voltage

### 13. 1 $V_{ADJ / EN}$ = 5.0 V



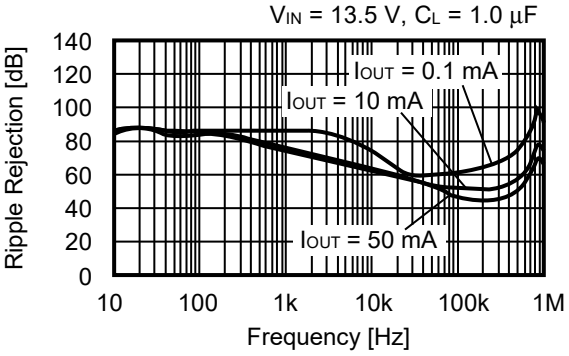




## 14. ADJ / EN pin current vs. ADJ / EN pin voltage




## 15. Ripple rejection (Ta = +25°C)

### 15. 1 $V_{ADJ / EN}$ = 5.0 V



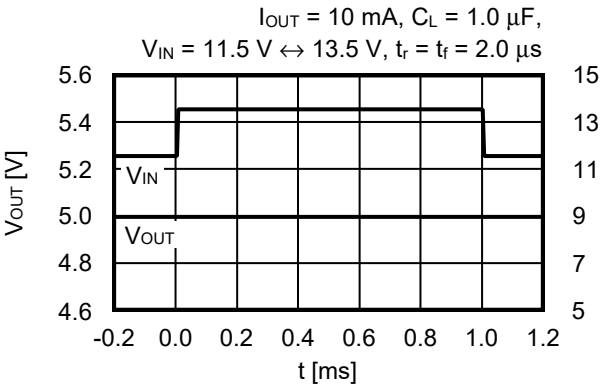



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## ■ Reference Data

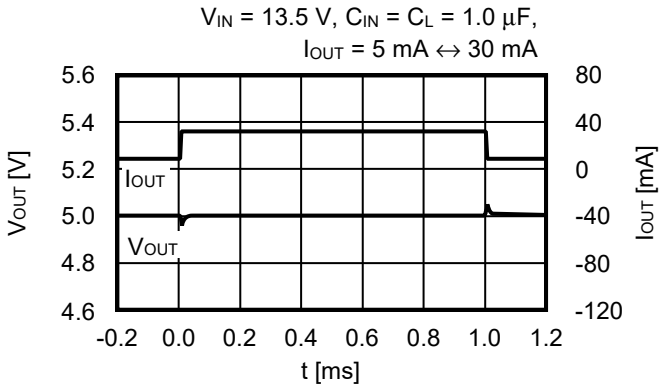
### 1. Characteristics of input transient response (Ta = +25°C)

#### 1. 1 $V_{ADJ / EN}$ = 5.0 V



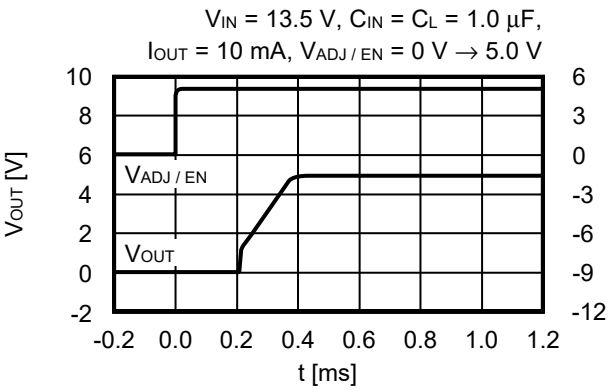

### 2. Characteristics of load transient response (Ta = +25°C)

#### 2. 1 $V_{ADJ / EN}$ = 5.0 V



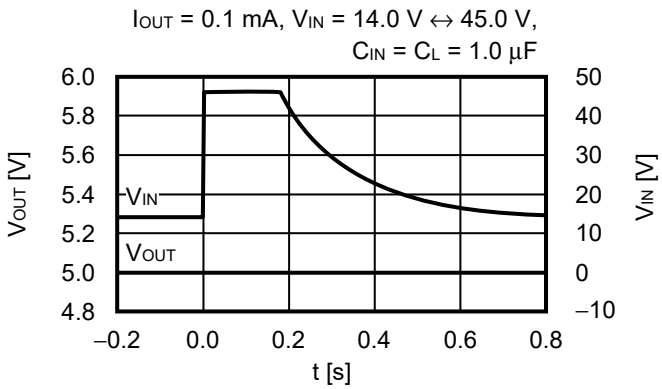

### 3. Transient response characteristics of ADJ / EN pin (Ta = +25°C)

#### 3. 1 $V_{ADJ / EN}$ = 5.0 V




### 4. Load dump characteristics (Ta = +25°C)

#### 4. 1 $V_{ADJ / EN}$ = 5.0 V




### 5. Example of equivalent series resistance vs. Output current characteristics (Ta = –40°C to +125°C)

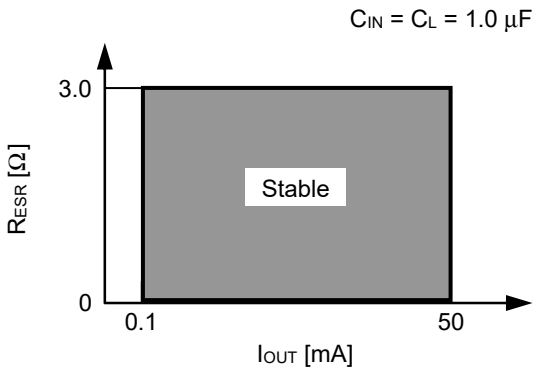
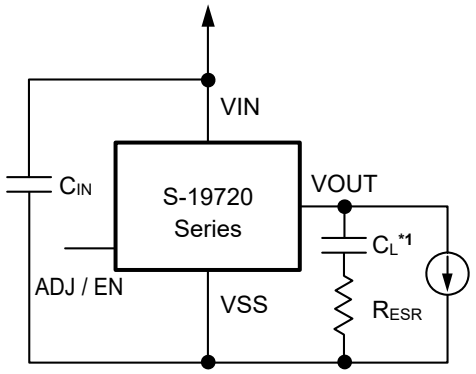



Figure 17




*1. CL: TDK Corporation CGA5L3X8R1H105K (1.0 µF)

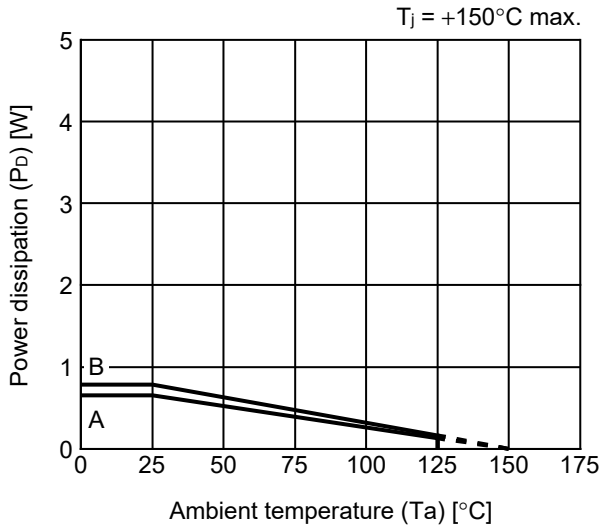
Figure 18



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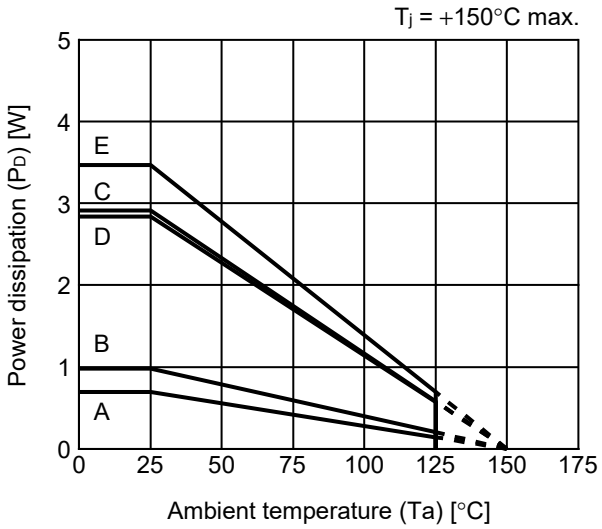
## ■ Power Dissipation

**SOT-23-5**




| Board | Power Dissipation ($P_D$) |
|---|---|
| A | 0.65 W |
| B | 0.78 W |
| C | – |
| D | – |
| E | – |

**HSNT-6(2025)**




| Board | Power Dissipation ($P_D$) |
|---|---|
| A | 0.69 W |
| B | 0.98 W |
| C | 2.91 W |
| D | 2.84 W |
| E | 3.47 W |

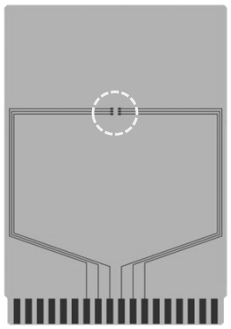


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# SOT-23-3/3S/5/6 Test Board

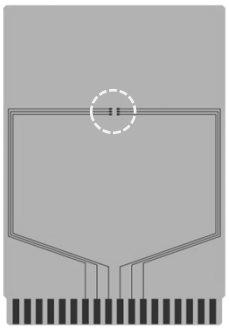
IC Mount Area

**(1) Board A**



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(2) Board B**



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. SOT23x-A-Board-SD-2.0

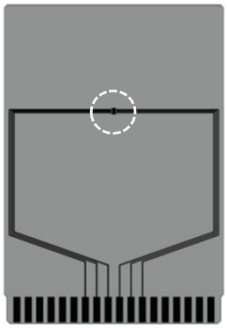


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# HSNT-6(2025) Test Board

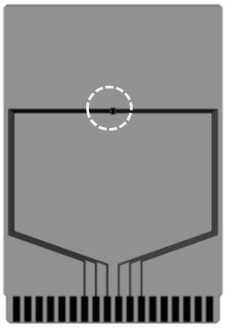
IC Mount Area

### (1) Board A



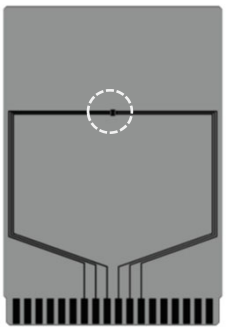
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

### (2) Board B



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

### (3) Board C



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | Number: 4<br>Diameter: 0.3 mm |



enlarged view

No. HSNT6-B-Board-SD-1.0

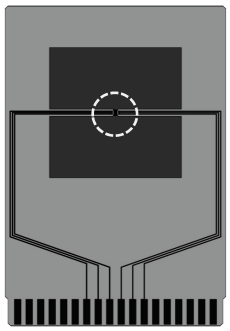


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# HSNT-6(2025) Test Board

IC Mount Area

**(4) Board D**

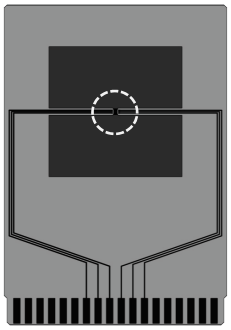




enlarged view

| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Pattern for heat radiation: 2000mm$^2$ t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(5) Board E**





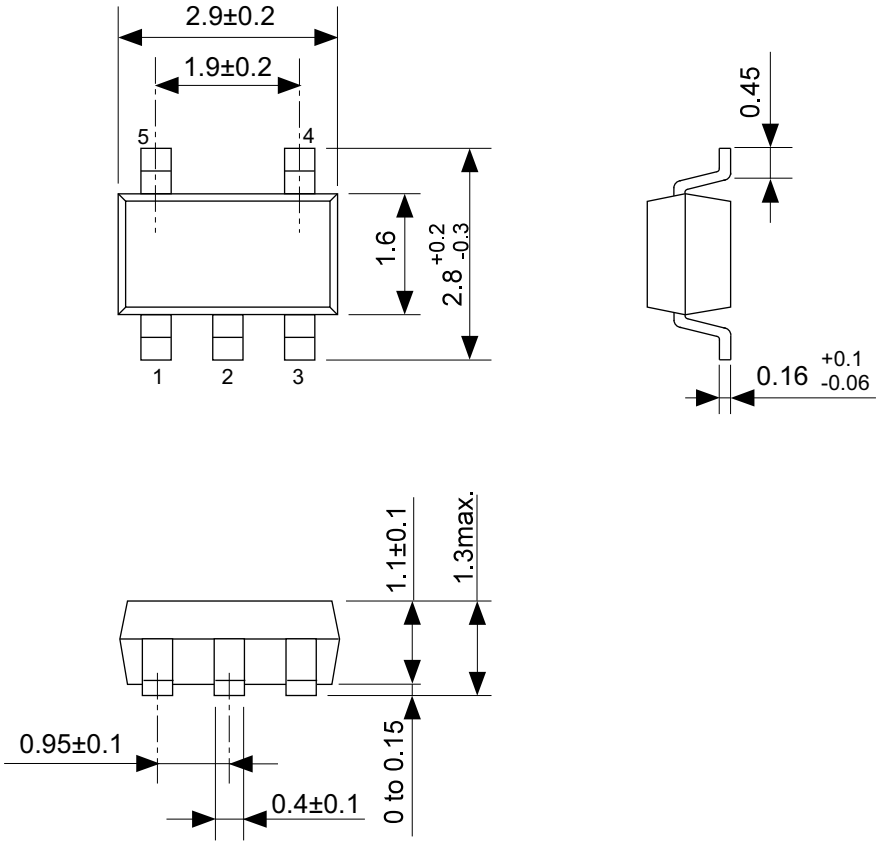
enlarged view

| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Pattern for heat radiation: 2000mm$^2$ t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | Number: 4<br>Diameter: 0.3 mm |

No. HSNT6-B-Board-SD-1.0



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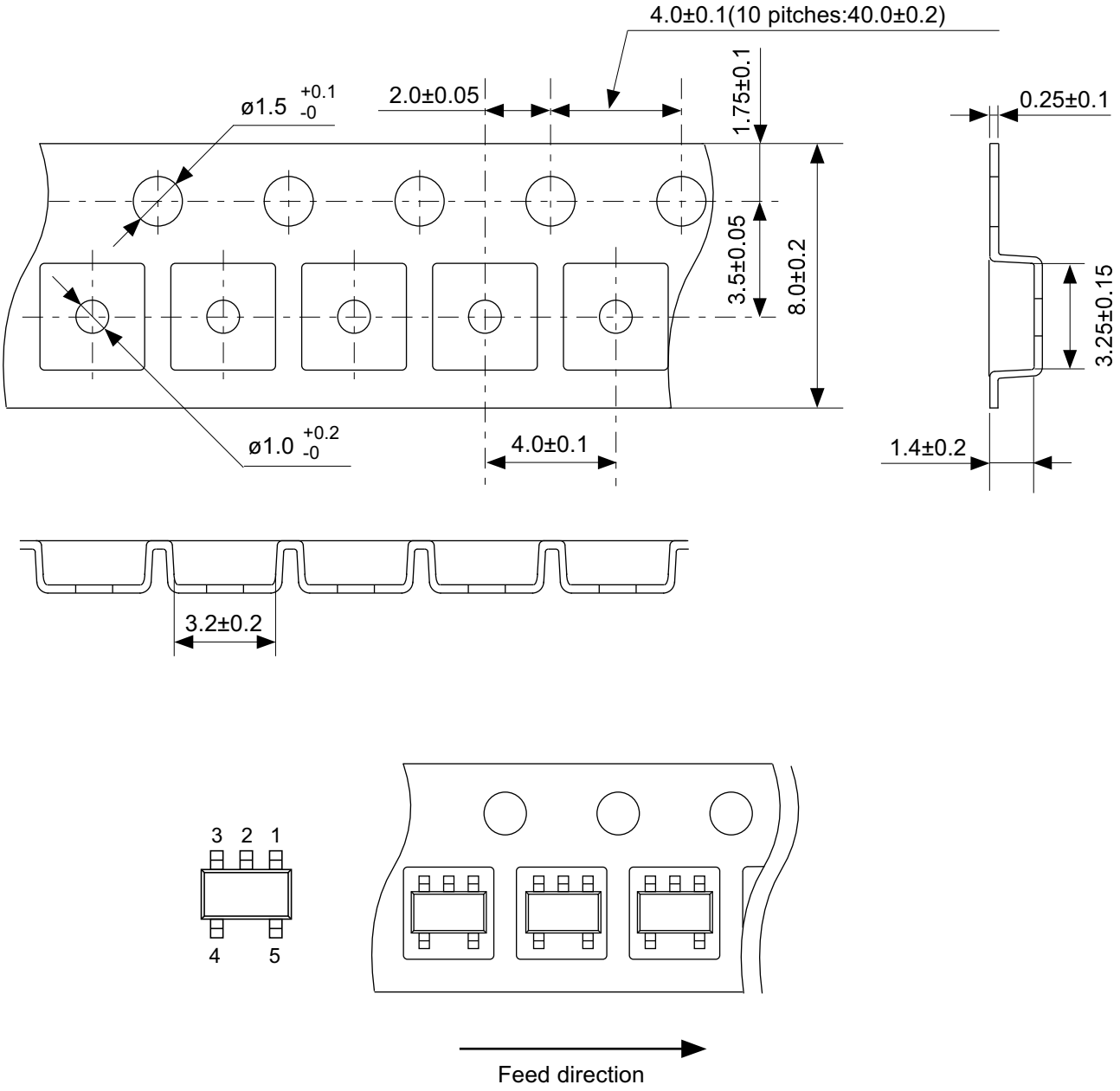



No. MP005-A-P-SD-1.3

| | |
|---|---|
| TITLE | SOT235-A-PKG Dimensions |
| No. | MP005-A-P-SD-1.3 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

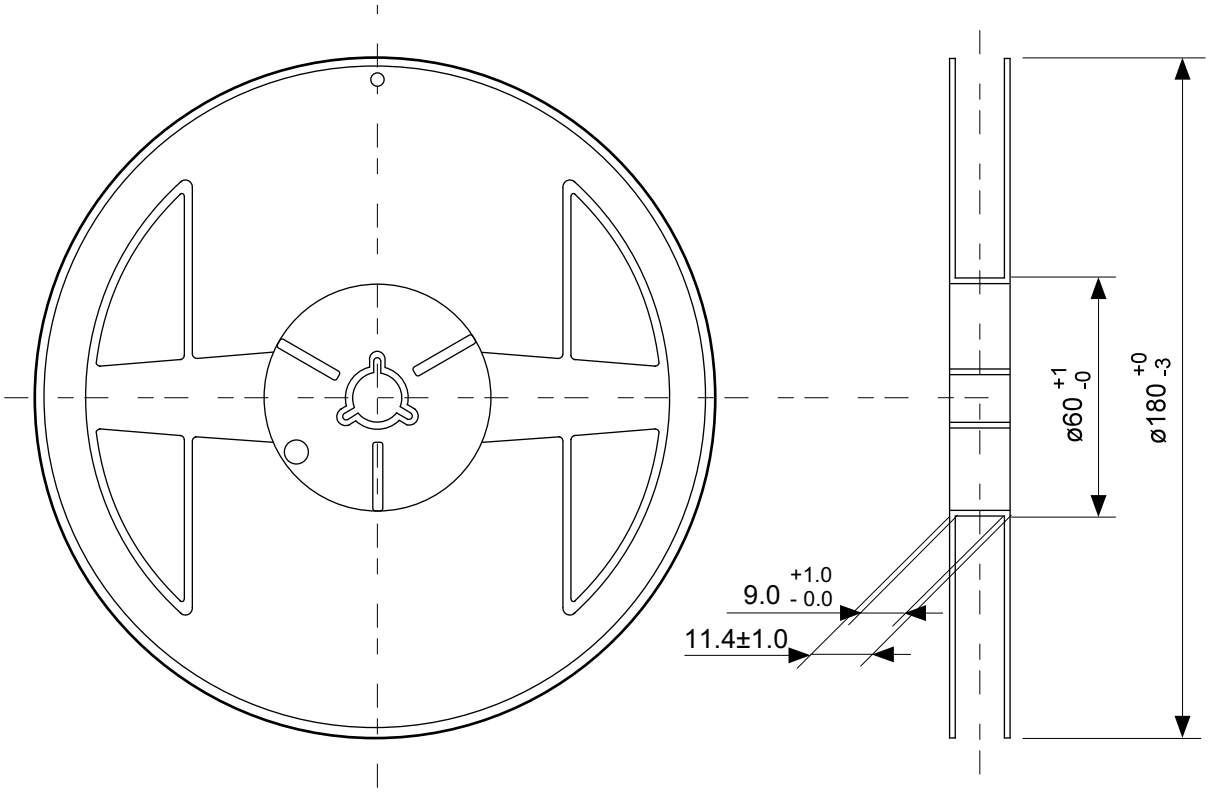
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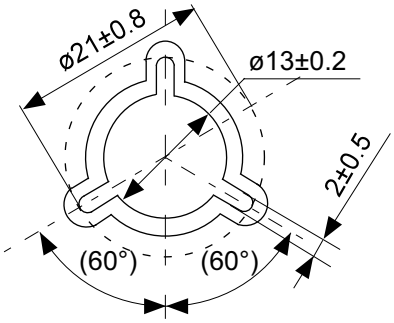

No. MP005-A-C-SD-2.1

| | |
|---|---|
| TITLE | SOT235-A-Carrier Tape |
| No. | MP005-A-C-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

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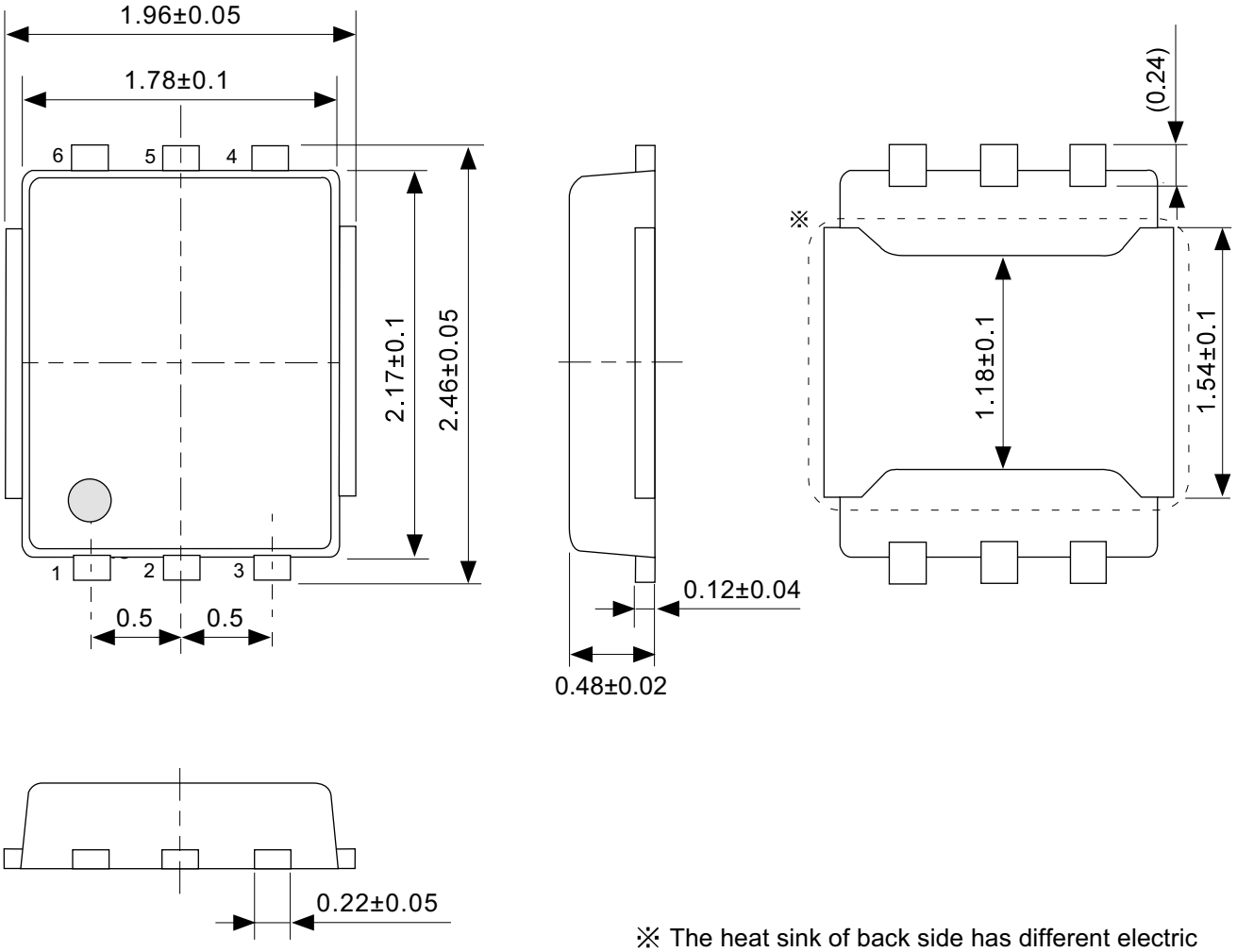

Enlarged drawing in the central part




No. MP005-A-R-SD-2.0

| | | | |
|---|---|---|---|
| TITLE | SOT235-A-Reel | | |
| No. | MP005-A-R-SD-2.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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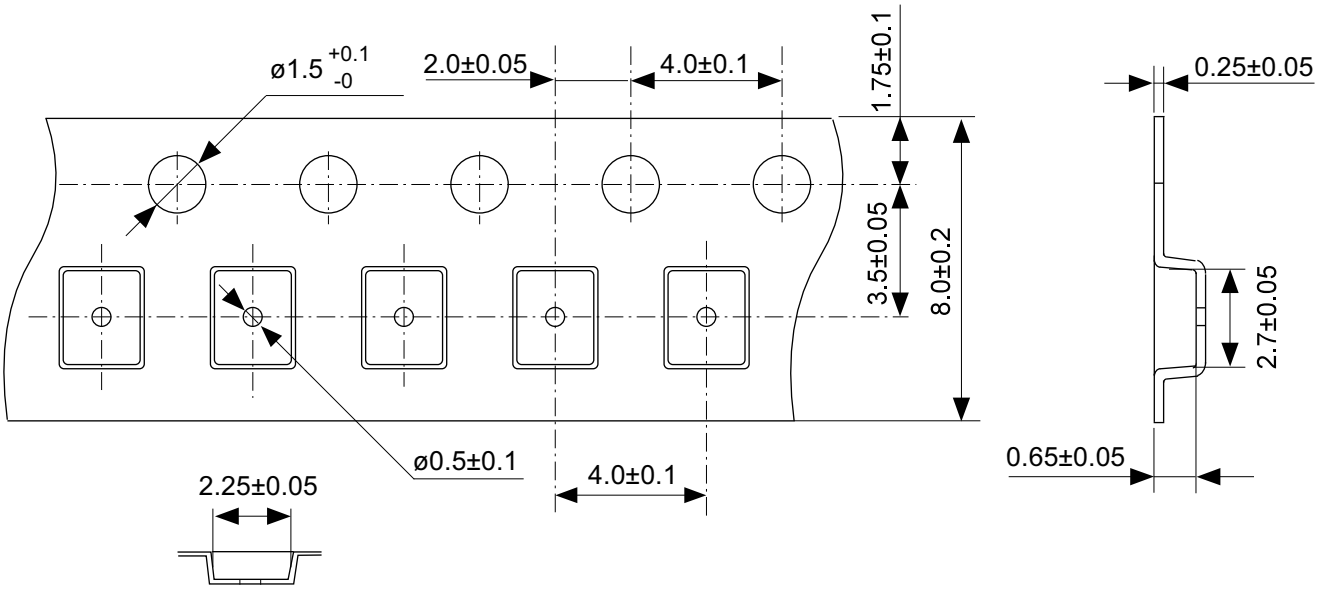


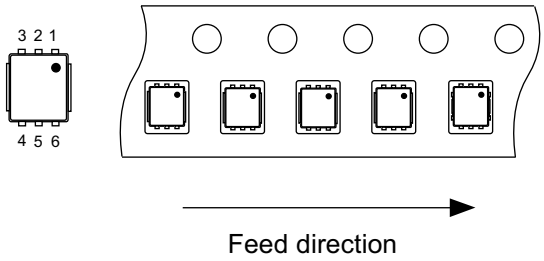

※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PJ006-B-P-SD-1.0

| | |
|---|---|
| TITLE | HSNT-6-C-PKG Dimensions |
| No. | PJ006-B-P-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| | **ABLIC Inc.** |

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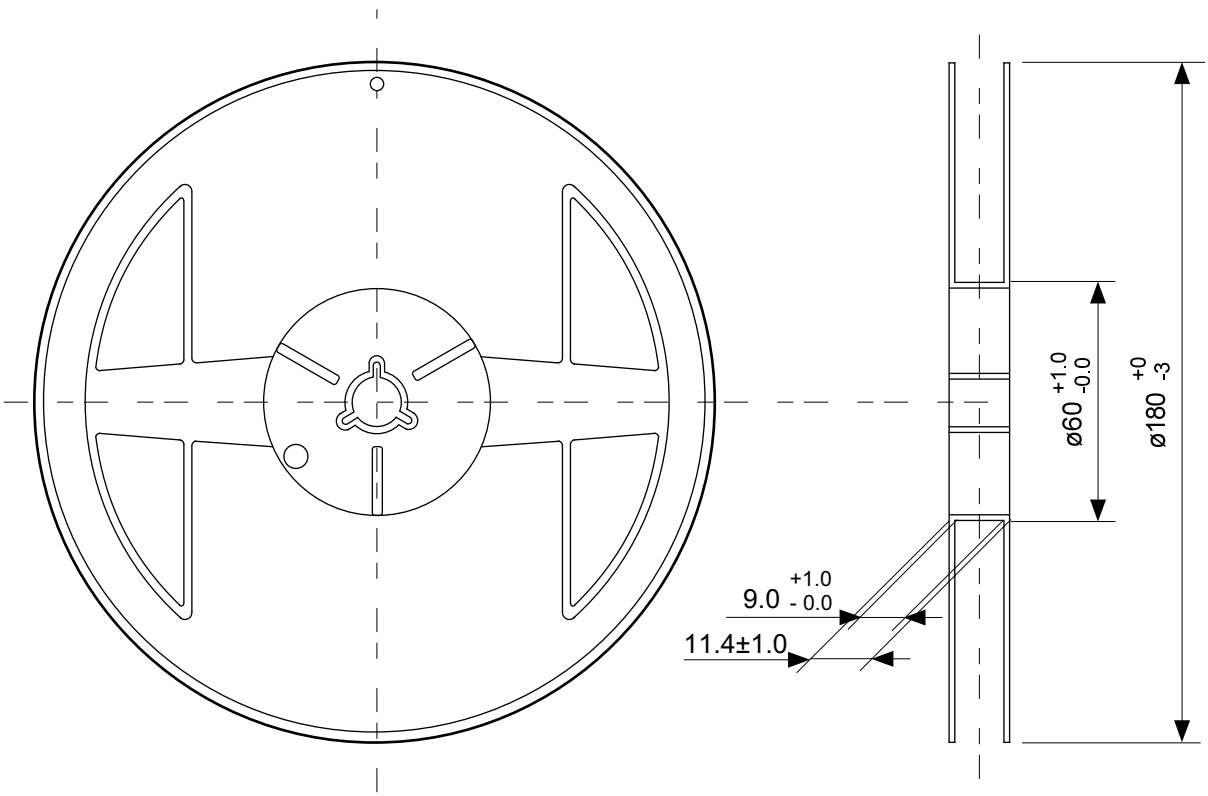


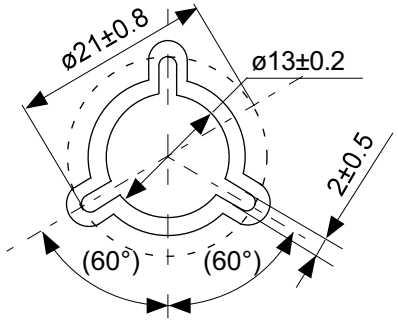

No. PJ006-B-C-SD-1.0

| | |
|---|---|
| TITLE | HSNT-6-C-Carrier Tape |
| No. | PJ006-B-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

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Enlarged drawing in the central part

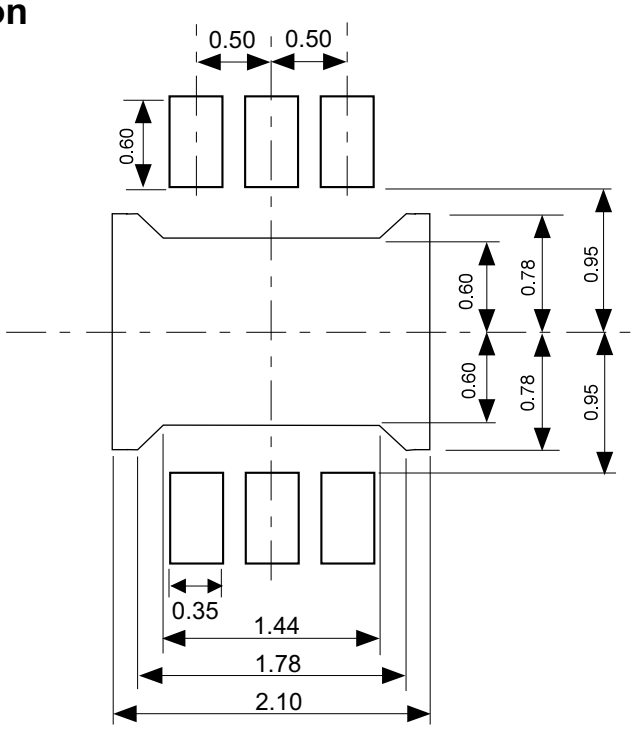



No. PJ006-B-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | HSNT-6-C-Reel | | |
| No. | PJ006-B-R-SD-1.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |

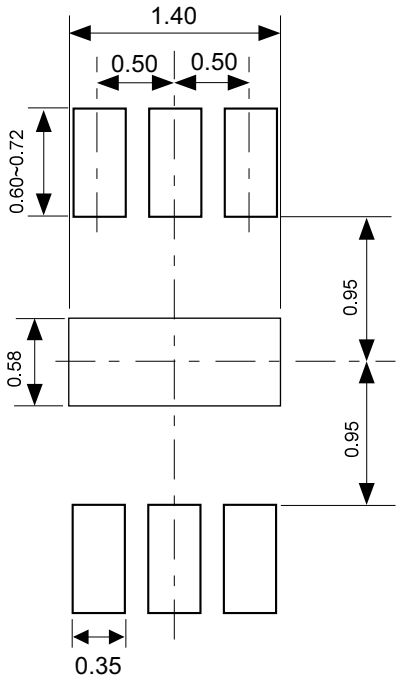
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## Land Recommendation




Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.
注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

## Stencil Opening




No. PJ006-B-LM-SD-1.0

Caution
① Mask aperture ratio of the lead mounting part is 100~120%.
② Mask aperture ratio of the heat sink mounting part is 30%.
③ Mask thickness: t0.12 mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意
①リード実装部のマスク開口率は100~120%です。
②放熱板実装のマスク開口率は30%です。
③マスク厚み：t0.12 mm
④リフロー雰囲気・窒素雰囲気（酸素濃度1000ppm以下）推奨

| | |
|---|---|
| TITLE | HSNT-6-C<br>-Land &Stencil Opening |
| No. | PJ006-B-LM-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |

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