UM11792

KITPF5103FRDMEVM evaluation board

Rev. 2.1 — 6 March 2026 **User manual**

Document information

Information	Content
Keywords	PF5103, FRDM-KL25Z, PF5103 NXP GUI, PMIC, mirror register, one time programming, try before buy, test mode
Abstract	The KITPF5103FRDMEVM evaluation board user guide is intended for engineers involved in the evaluation, design, implementation, and validation of PF5103 fail-safe system basis chips with multiple SMPSs.

Downloaded from Arrow.com.

1 Introduction

IMPORTANT NOTICE

For engineering development or evaluation purposes only



NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

The KITPF5103FRDMEVM evaluation board user guide is intended for engineers involved in the evaluation, design, implementation, and validation of PF5103 fail-safe system basis chip with multiple SMPSes (switch mode power supplies).

This document contains all of the information required to evaluate the PF5103 fail-safe system basis chip with two SMPSes connected in single- or multiphase mode, and two LDOs.

The document covers connecting the hardware, installing the software and tools, configuring the environment, and using the kit.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for the KITPF5103FRDMEVM evaluation board is at http://www.nxp.com/KITPF5103FRDMEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITPF5103FRDMEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate with the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

3 Getting ready

Working with the KITPF5103FRDMEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

The KITPF5103FRDMEVM kit contains the following items:

- An assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- A 3.0 ft USB-STD A to USB-C-minicable
- Jumpers mounted onboard
- Mating Phoenix connectors
- Assembled and tested evaluation board in an antistatic bag
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary.

- A power supply with a range of 3.3 V to 5.0 V

3.3 Assumptions

Familiarity with the I^2C-bus is helpful but not required.

3.4 Static handling requirements

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling. You must use a ground strap or touch the PC case or other grounded source before unpacking or handling the hardware.

3.5 Minimum system requirements

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- A USB-enabled computer with Windows 7 or Windows10

3.6 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/KITPF5103FRDMEVM or from the provided link.

- PF5103 NXP GUI installation package
- Flexera

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

4 Getting to know the hardware

4.1 Kit overview

The KITPF5103FRDMEVM kit provides an integrated platform for evaluating designs based on NXP's PF5103 PMIC. All PF5103 features can be accessed and monitored in a test environment.

The kit hardware consists of the KITPF5103FRDMEVM evaluation board, a FRDM-KL25Z microcontroller board, and the USB cable required to connect the FRDM-KL25Z to the PC.

The KITPF5103FRDMEVM evaluation board features an individual PF5103 soldered on board. Connectors, jumpers, and switches on the board can be used to configure an evaluation environment that meets specific design requirements. The board also contains LEDs and test points that provide a means of monitoring performance in real time.

The FRDM-KL25Z is mounted to Arduino connectors on the bottom of the KITPF5103FRDMEVM board. The role of the FRDM-KL25Z is to manage serial peripheral interface (SPI) communication between the KITPF5103FRDMEVM board and the GUI installed on the PC. The FRDM- KL25Z draws power from the USB cable connected to the PC.

4.2 Board features

- Phoenix (3.81mm) male connectors for switches and LDOs
- Selectable Debug mode, Normal mode, and Test mode
- VDDOTP and PWRON to power up the device in different modes
- PGOOD, INTB/RSTB, SYNC and XFAIL pins
- USB to I^2C protocol for easy connection to software GUI
- LEDs, green and red, indicate signal or regulator status
- LED blue to indicate VDDOTP pin is set to 8 V (OTP burning voltage)
- Header connectors for monitoring outputs
- Advance system monitoring via KL25 MCU ADC

4.3 Block diagram

Figure 1 shows the default jumper and switch configurations for the use of the KITPF5103FRDMEVM board, and placement of connectors, monitoring headers and LEDs signaling.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

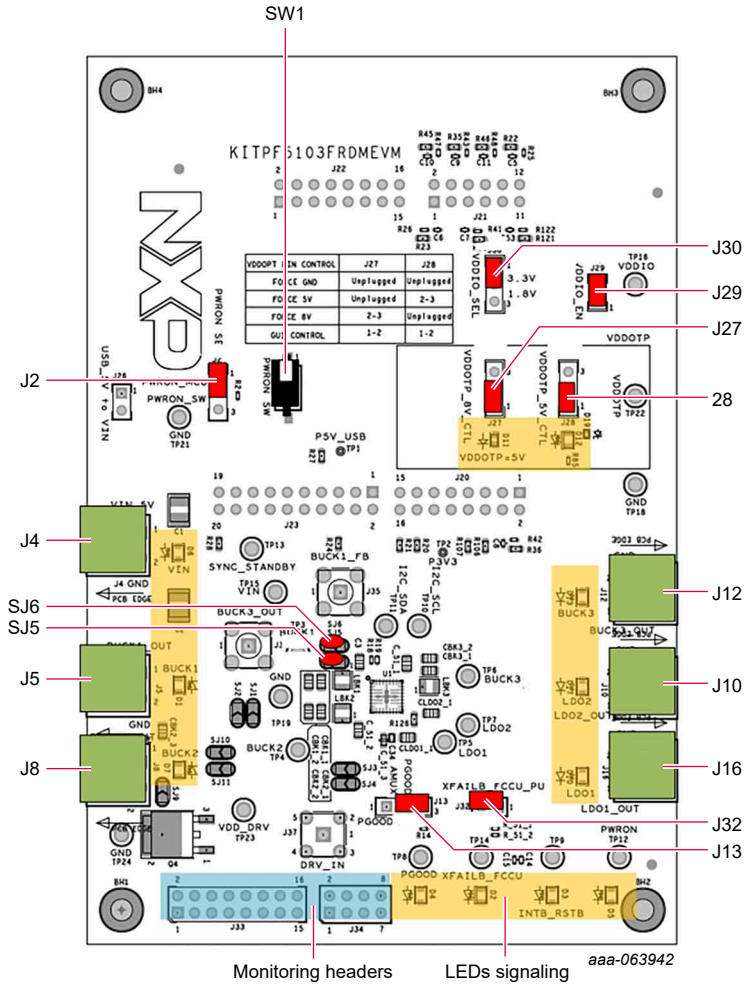


Figure 1. Board image with callouts

4.4 Kit featured components

Table 1. Jumper or switches functions

Position	Function	Description
J4	VIN	Input voltage (3.3 V min / 5.5 V max)
J5	BUCK1_OUT	Output for Buck 1
J8	BUCK2_OUT	Output for Buck 2
J12	BUCK3_OUT	Output for Buck 3
J16	LDO1_OUT	Output for LDO 1
J10	LDO2_OUT	Output for LDO 2
J2	PWRON_SEL	PWRON controlled either by MCU or manually with PWRON_SW
SW1	PWRON_SW	PWRON manual control (assume J2 on PWRON_SW position).
J26	USB_5V_TO_VIN	Supply VIN with 5 V from USB (Current limited to 1A)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Table 1. Jumper or switches functions*...continued*

Position	Function	Description
J30	VDDIO_SEL	VDDIO set to either 1.8 V or 3.3 V
J29	VDDIO_EN	Apply VDDIO to VDDIO pin
J13	PGOOD_SEL	PGOOD setting either PGOOD/GPO or output of temperature junction analog voltage
J27	VDDOTP_8V_CTL	8 V on VDDOTP controlled either manually or by MCU
J28	VDDOTP_5V_CTL	5 V on VDDOTP controlled either manually or by MCU
J32	XFAILB_PU	Pull-up XFAILB to VDDIO
J33/J34	Monitoring headers	I/O pins and regulator outputs for monitoring purpose
SJ5	-	Solder blob jumper to connect BUCK1_OUT and BUCK1_FB
SJ6	-	Solder blob jumper to connect BUCK1_LX and BUCK3_OUT

4.4.1 Connectors

4.4.1.1 VIN connectors

Nominal VIN voltage is 3.3 V minimum to 5.5 V maximum.

Table 2. VIN connector (J4)

Schematic label	Signal name	Description
J4-1	VIN	VIN supply input
J4-2	GND	Ground

4.4.1.2 BUCK1, BUCK2, and BUCK3 connectors

Each buck can be controlled between 0.5 V / 3.3 V.

Current capability is up to 3.5 A, assuming current limit is correctly set.

Voltage and current limit are set by OTP.

Configurable as multiphase regulators.

Table 3. BUCK1, BUCK2 and BUCK3 connectors

Schematic label	Signal name	Description
J5-1	BUCK1_OUT	BUCK1 output power supply
J5-2	GND	Ground
J8-1	BUCK2_OUT	BUCK2 output power supply
J8-2	GND	Ground
J12-1	BUCK3_OUT	BUCK3 output power supply
J12-2	GND	Ground

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

4.4.1.3 LDO1 and LDO2 connectors

LDO1 can be controlled between 0.75 V to 3.3 V, up to 200 mA.

LDO2 can be controlled between 0.75 V to 3.3 V, up to 500 mA.

Table 4. LDO1 and LDO2 connectors

Schematic label	Signal name	Description
J16-1	LDO1_OUT	LDO1 output power supply
J16-2	GND	Ground
J10-1	LDO2_OUT	LDO2 output power supply
J10-2	GND	Ground

4.4.2 Test points

The KITPF5103FRDMEVM board has several test points, see Figure 2, that facilitate access and measurements. This section summarizes the available test points, how they are color-coded, and whether they are a test-point component with a part number or a through-hole test point with no part number.

Yellow: Test loop access to safety outputs and analog signals

Red: Test loop access for power supplies

Black: Test loop access to GND

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

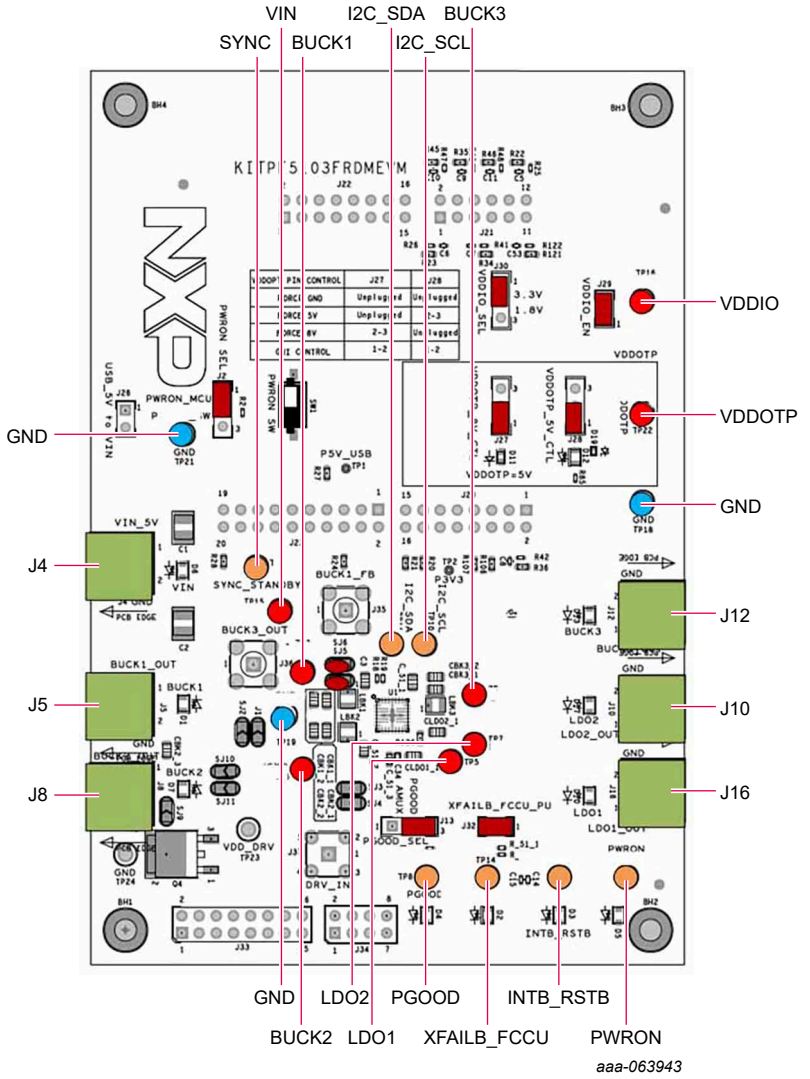


Figure 2. Test points

4.4.3 Jumpers

4.4.3.1 PWRON_SEL Jumper (J2)

PWRON_SEL selects PWRON control from MCU or manually via PWRON_SW switch. MCU controlled is the default configuration as it eases the use of the board when connected to the GUI.

Table 5. PWRON_SEL Jumper (J2)

Schematic label	Signal name	Description
J2-1-2	PWRON_MCU	PWRON is controlled from MCU
J2-2-3	PWRON_SW	PWR is manually controlled via PWRON_SW switch

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

4.4.3.2 USB_5V_TO_VIN Jumper (J26)

USB_5V_TO_VIN provides power from USB 5 V. In this case, do not supply via J4. Be careful to use this mode only without load connected to the board.

Table 6. USB_5V_TO_VIN jumper (J26)

Schematic label	Signal name	Description
J26-1	VIN	Connected to VIN
J26-2	P5V_USB	Connected to 5 V from USB

4.4.3.3 VDDIO_SEL Jumper (J30)

VDDIO_SEL selects 1.8 V or 3.3 V for VDDIO.

Table 7. VDDIO_SEL jumper (J30)

Schematic label	Signal name	Description
J30-1-2	3.3 V	Set VDDIO to 3.3 V with external LDO
J30-2-3	1.8 V	Set VDDIO to 1.8 V with external LDO

4.4.3.4 VDDIO_EN Jumper (J29)

VDDIO_EN enables VDDIO from the external LDO to the VDDIO pin of the device.

Table 8. VDDIO_EN jumper (J29)

Schematic label	Signal name	Description
J29-1	VDDIO ext	VDDIO voltage from external LDO
J29-2	VDDIO PF510300	VDDIO connected to PF510300

4.4.3.5 PGOOD_SEL Jumper (J13)

PGOOD_SEL selects either PGOOD/GPO or temperature sensor.

The PGOOD pin must be configured correctly through I^2C using the GUI.

Table 9. PGOOD_SEL jumper (J13)

Schematic label	Signal name	Description
J13-2-3	PGOOD/GPO	PGOOD/GPO mode; apply an external pull up to PGOOD pin
J13-1-2	AMUX	Temperature sensor mode; no pull-up connected to PGOOD pin

4.4.3.6 VDDOTP_8V_CTL Jumper (J27)

8 V on VDDOTP can be controlled either by the FRDM-KL25Z MCU, allowing control by script, or manually forced.

Table 10. VDDOTP_8V_CTL jumper (J27)

Schematic label	Signal name	Description
J27-1-2	VDDOTP_MCU_8V	8 V on VDDOTP controlled by MCU

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Table 10. VDDOTP_8V_CTL jumper (J27)...*continued*

Schematic label	Signal name	Description
J27-2-3	VDDOTP_FORCE_8V	8 V on VDDOTP manually forced

4.4.3.7 VDDOTP_5V_CTL Jumper (J28)

5 V on VDDOTP can be controlled either by the FRDM-KL25Z MCU, allowing control by script, or manually forced.

Table 11. VDDOTP_5V_CTL jumper (J28)

Schematic label	Signal name	Description
J28-1-2	VDDOTP_MCU_5V	5 V on VDDOTP controlled by MCU
J28-2-3	VDDOTP_FORCE_5V	5 V on VDDOTP manually forced

4.4.3.8 XFAILB_FCCU_PU Jumper (J32)

This jumper pulls up XFAILB_FCCU to VDDIO.

Table 12. XFAILB_FCCU_PU jumper (J32)

Schematic label	Signal name	Description
J32-1	VDDIO	VDDIO through 5.1 K Ohms resistor
J32-2	XFAILB_FCCU	XFAILB_FCCU signal from PF5103

4.4.4 LED

The LED signaling displays the state of the following signals:

- **Signals:** PWRON, PGOOD, INTB_RSTB and XFAILB_FS0B
- **Power:** BUCKx regulators outputs and LDOx regulator outputs
- **Power Supply:** VIN
- **OTP control:** VDDOTP_5V_CTL, VDDOTP_8V_CTL

4.4.5 Switches

4.4.5.1 PWRON_SW (SW1)

This switch gets control only if the PWRON_SEL jumper is in the PWRON_SW position. Otherwise, SW1 has no effect.

Table 13. PWRON_SEL switch (SW1)

Schematic label	Description
SW1 ON	PWRON set to 1
SW1 OFF	PWRON set to 0

4.4.6 Monitoring headers (J33 and J34)

J33 and J34 headers allow you to monitor each I/O pin and power supply output.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

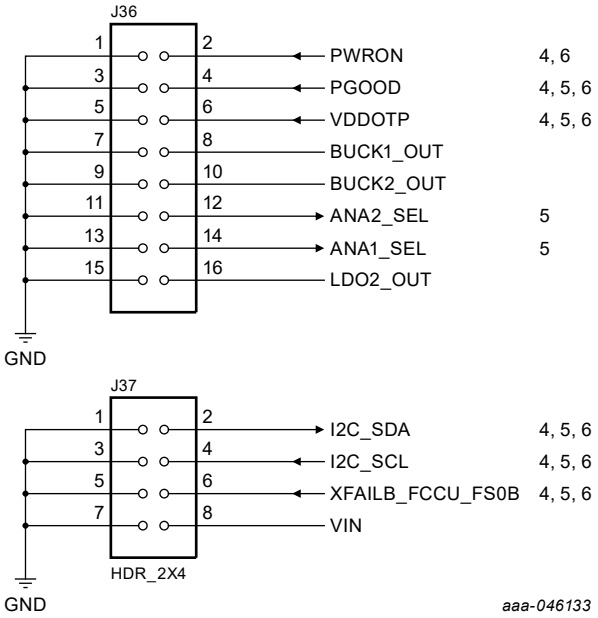


Figure 3. Monitoring headers (J33 and J34)

4.5 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for theKITPF5103FRDMEVM evaluation board are available at http://www.nxp.com/KITPF5103FRDMEVM.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

5 Installing and configuring software tools

5.1 Flashing the FRDM-KL25Z firmware – Windows 7

If BOOTLOADER is already on the FRDM-KL25Z board, skip Step 1 and Step 2 and begin with Step 3.

1. Plug the USB cable into the USB port of your computer. Press the RST push button of the FRDM-KL25Z board and plug the USB cable into the SDA port on the FRDM-KL25Z board. Once connected, release the RST button.
   - A new BOOTLOADER, see Figure 4, device should appear on the left panel of the Windows File Explorer.

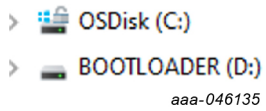


Figure 4. Bootloader – FRDM-KL25Z firmware – Windows 7

2. Locate the file MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA from the package. Drag and drop it into the BOOTLOADER device.
   Note: *Allow enough time for the firmware to be saved in the bootloader.*
3. Disconnect and reconnect the USB cable into the SDA port, this time without pressing the RST push button.
   - The FRDM-KL25Z device should appear on the left pane of the File explorer as shown in Figure 5.

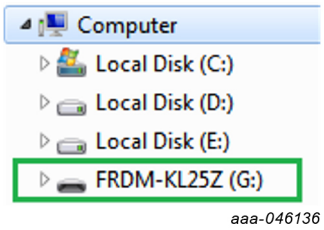


Figure 5. Locate debug for FRDM-KL25Z

4.
5. Locate the file nxp-gui-fw-frdmkl25z-usb_hid-pf5103_v0.4.bin from the package. Drag and drop the file into the FRDM-KL25Z device.
   Note: *Make sure to allow enough time for the firmware to be saved.*
6. Freedom board Firmware is successfully loaded. Disconnect the USB cable from the SDA port and reconnect it into the FRDM-KL25Z USB port.

5.2 Flashing the FRDM-KL25Z firmware – Windows 10

1. **Disable the storage services:** Run the services, double click on the storage service from the list and press the Stop button.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

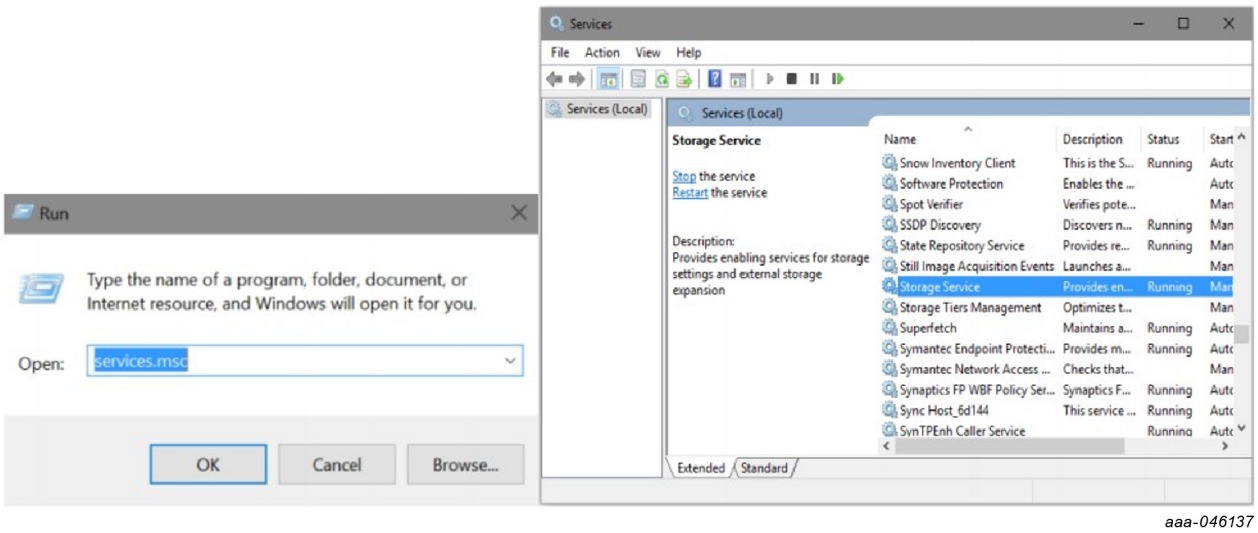


Figure 6. Disabling storage services

If BOOTLOADER is already on the FRDM-KL25Z board, skip Step 2 and Step 3 and begin with Step 4.

2. Plug the USB cable into the computer's USB port, press the RST push button on the FRDM-KL25Z board and plug the USB cable into the SDA port on the FRDM-KL25Z board. Once connected, release the RST button.
   - A new BOOTLOADER device, see Figure 7, should appear on the left panel of the Windows File explorer.

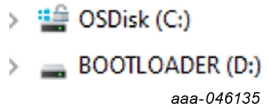


Figure 7. Bootloader – FRDM-KL25Z firmware – Windows 10

3. Locate the file MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA from the package. Drag and drop it into the BOOTLOADER device.
   Note: *Allow enough time for the firmware to be saved in the Bootloader.*
4. Disconnect and reconnect the USB cable into the SDA port, this time without pressing the RST push button.
   - The FRDM_KL25Z device, see Figure 8, should appear on the left pane of the File Explorer.

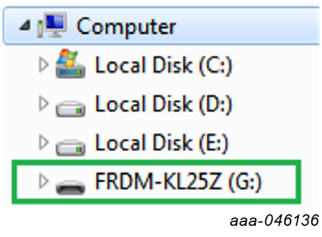


Figure 8. Locate debug for FRDM-KL25Z

5. Locate the file nxp-gui-fw-frdmkl25z-usb_hid-pf5103_v0.4.bin from the package. Drag and drop the file into the FRDM_KL25Z device.
   Note: *Allow enough time for the firmware to be saved.*
6. After the Freedom board firmware is loaded, disconnect the USB cable from the SDA port and reconnect it to the KL25Z USB port.

5.3 Flashing or updating the GUI firmware

The KITPF51SKTEVM is delivered with the GUI firmware already flashed. If the MCU firmware is already flashed, ignore this section. If the firmware needs to be updated or it is malfunctioning, follow these instructions:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Note: *This section uses the PF5103 as an example to explain software installation, configuration, and use. Specific explanations for PF5100, PF5101, or PF5104 are provided if necessary. Otherwise, the method is general to PF510x.*

5.4 PF51 NXP GUI

5.4.1 Installing the GUI software package

To install the PF510x NXP GUI, download or obtain the NXP GUI package, then follow the instructions listed:

1. Open the NXP GUI package. Unzip and open "1 - NXP_GUI_Setup folder".

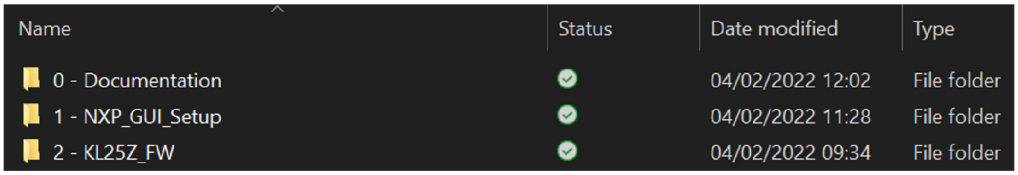


Figure 9. Open NXP GUI package

2. Double click on NXP_GUI-version-Setup.exe to launch the application and follow the instructions.



Figure 10. Launch NXP_GUI setup

3. Click Next when the initial application setup window appears.

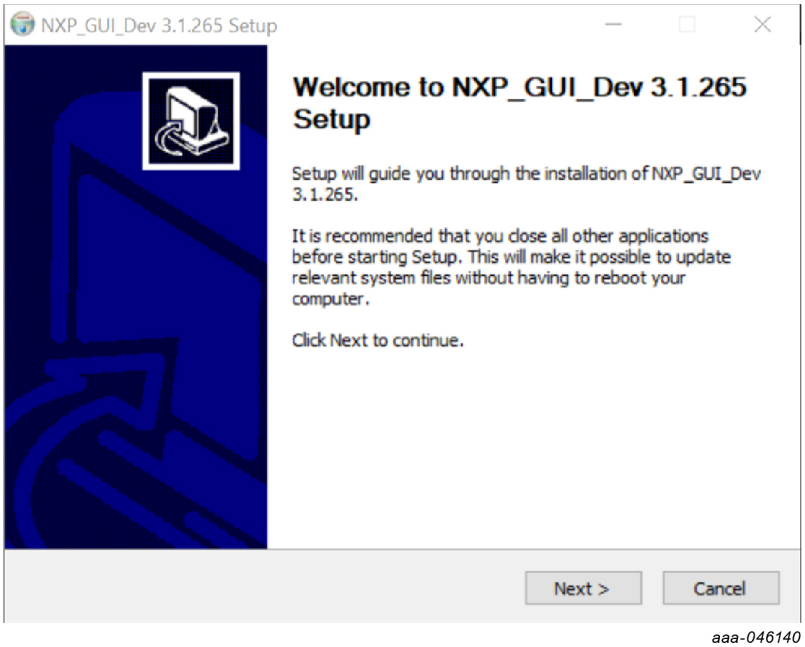


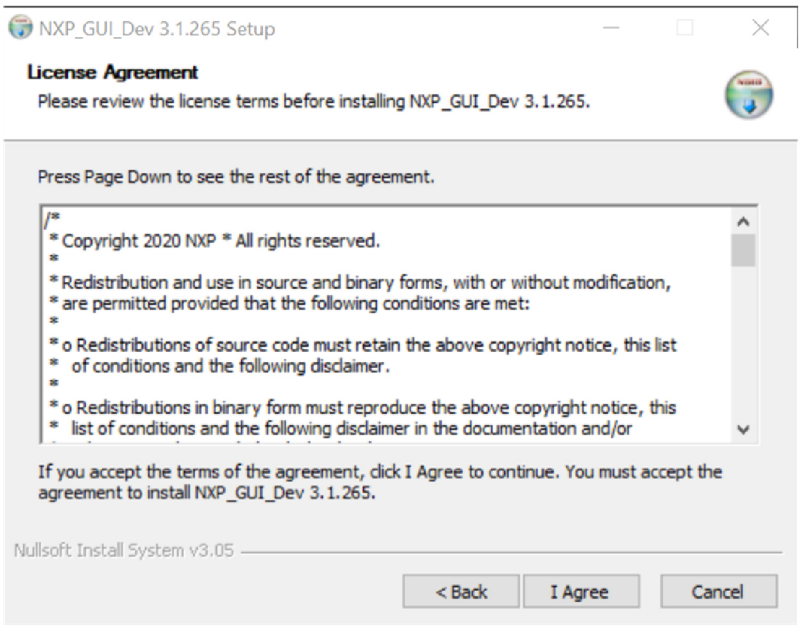
Figure 11. Initial application setup window

4. On the License Agreement window, read the license information and click I Agree.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

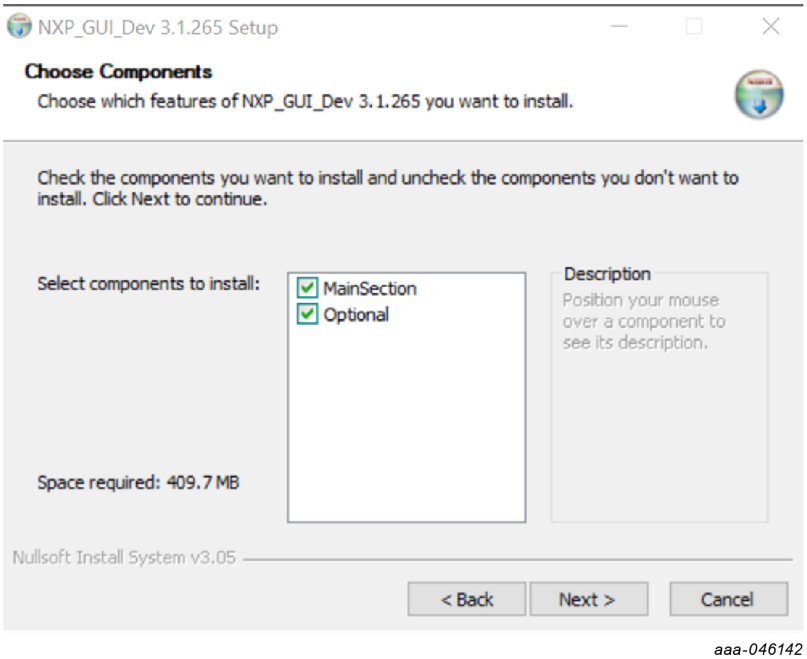
Downloaded from Arrow.com.



aaa-046141

Figure 12. License Agreement window

5. In the Choose Components window, select the appropriate GUI components. Then click Next.



aaa-046142

Figure 13. Choose Components window

6. In the Choose Install Location window, choose the appropriate folder for the GUI installation.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

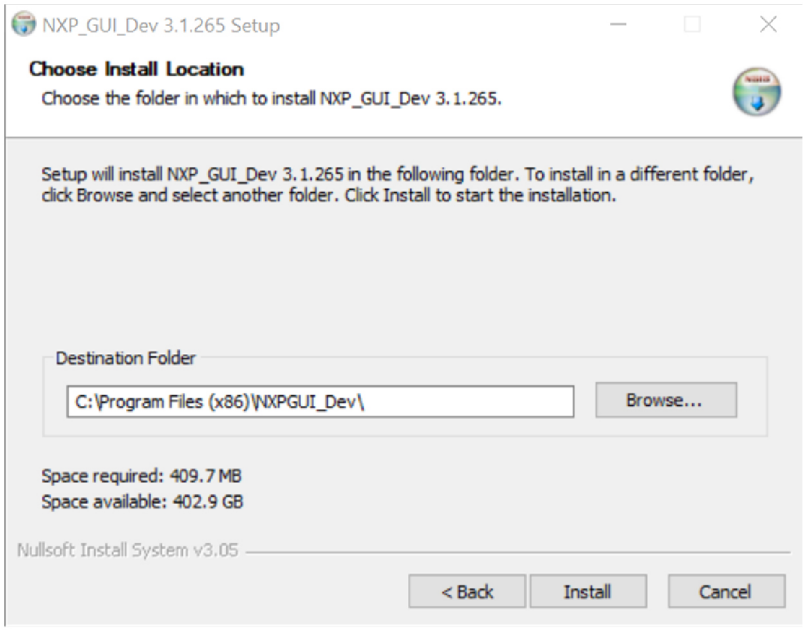


Figure 14. Choose Install Location window

7. In the Completing Setup window, select the following options:
   - Run NXP_GUI
   - Show Readme

   Click Finish to complete the installation.

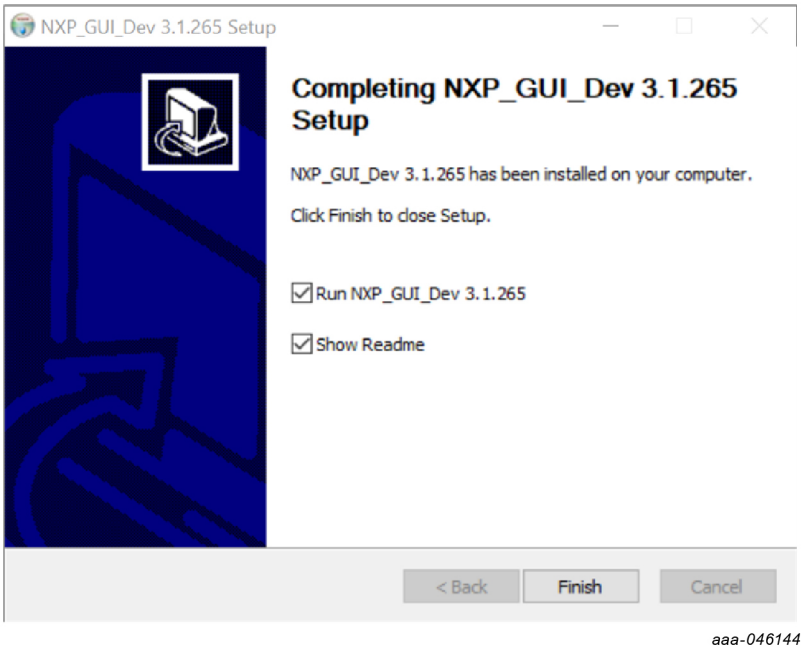


Figure 15. Completing setup window

5.4.2 Launching the PF51 NXP GUI

When the KITPF51SKTEVM kit is set up and the GUI is installed, follow the steps below to launch the GUI:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

1. Click the Windows icon (bottom left corner), locate the NXPGUI in the Windows All Apps bar, then click the NXPGUI icon to launch the GUI.

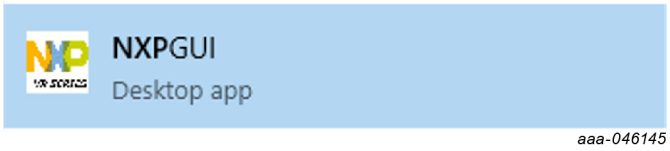


Figure 16. NXPGUI app

2. When the GUI opens, the first window to appear is the Kit Selection window. In the Kit Selection window, select the settings shown in Figure 17. To avoid the Kit Selection window on every launch, check “Use this configuration and do not ask again". (The Kit Selection window can be disabled through the File main menu item.) When finished selecting the settings, click OK.

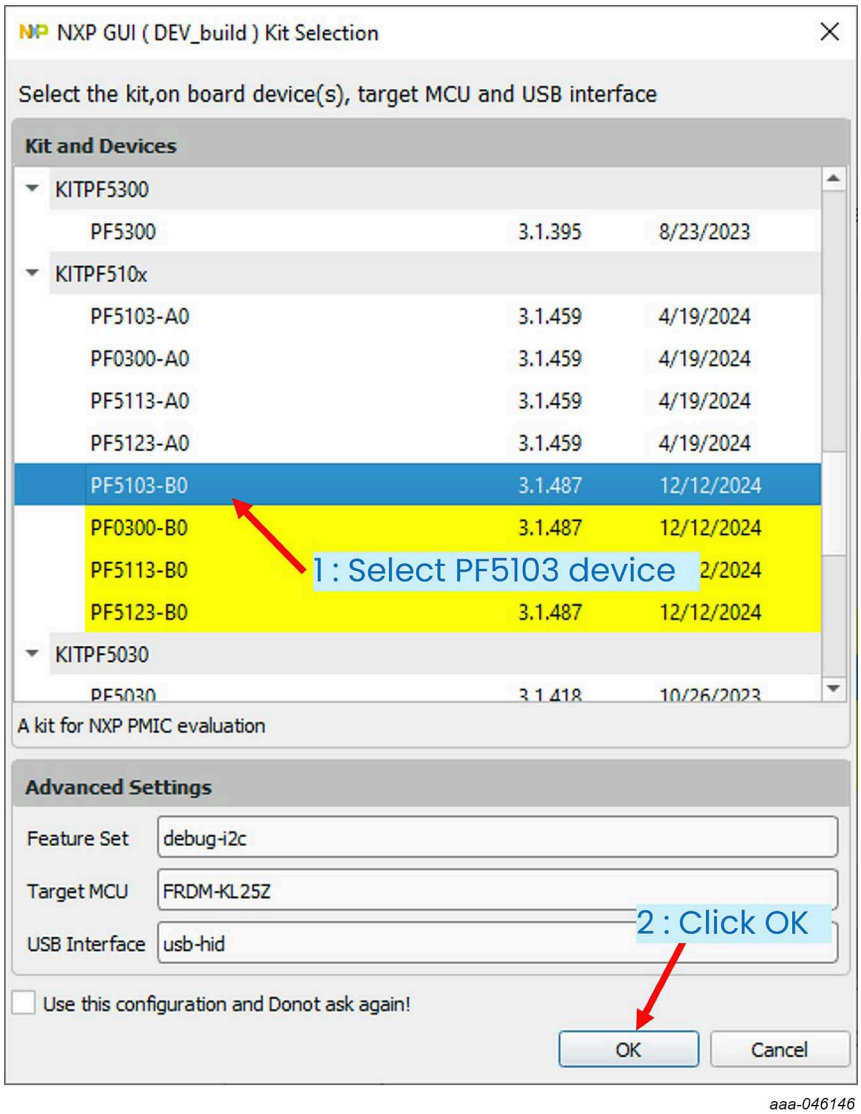


Figure 17. Kit selection window

Note: *For PF51x3 devices, select the corresponding device name.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

5.4.3 The Framework window

The Framework window consists of the following sections:

- **Device Manager:** Used to start communication with the device, enter or exit test mode, enable I^2C CRC and I^2C secure access, enable watchdog.
- **Framework settings:** Manage file import/export and Framework configuration.
- **Window log:** Reports USB and Device communication events.
- **USB and Device status:** Indicates if a USB or device is connected or disconnected, shows firmware and GUI version, displays current state of functional safety state machine. It should indicate if everything is safe states, failing states, or a debug mode. (Click the display button to refresh.)

Tools access bar: Provides quick access to the PF51 evaluation tools and features.

Note: *Power tool is currently not available.*

- **Tab content:** Shows the content of each tool or tab. (There may be more tabs, boxes, or windows inside.)

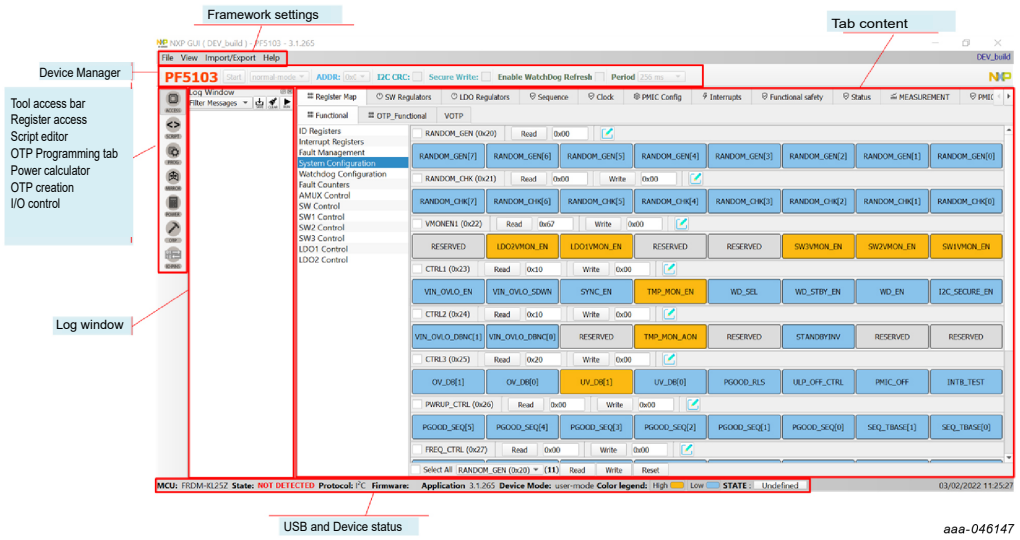


Figure 18. Framework window

If Log Window, Tools access bar or Device Manager do not appear on the screen, right-click on the Framework settings bar. This action displays three selection boxes (checked if display is active):

- Log window
- Tabs, which corresponds to the Tools access bar
- ConnectionMgr, which corresponds to Device Manager

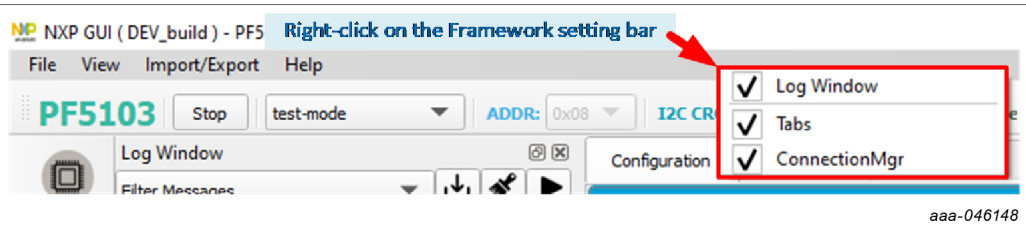


Figure 19. Framework bar

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

5.4.3.1 Framework settings

The Framework settings section, see Figure 20, appears at the top left corner of the Framework. It consists of four items:

- File
- View
- Import/Export
- Help

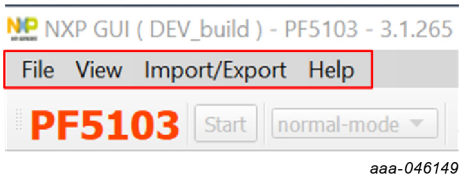


Figure 20. Framework settings

5.4.3.1.1 File menu item

Choose to display or not the GUI Kit selection at start or Exit the application.

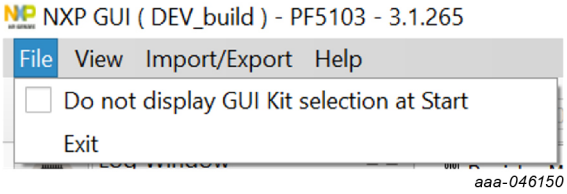


Figure 21. GUI Kit selection display settings

- **Do not display GUI Kit selection at start:** When starting the GUI, this option allows the user to enable or disable the Kit Selection window.
- **Exit:** Exits the NXP GUI application.

5.4.3.1.2 View menu item

The View menu contains the following options:

1. Display
2. Show
3. Naming conventions
4. OTP sequence diagram mode
   - **Display:** Enables and disables the Connection Tool Bar option. This is enabled by default.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

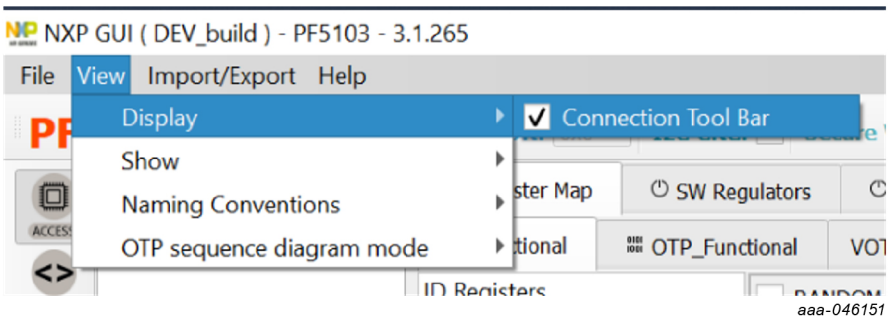


Figure 22. GUI kit display

- **Show:** This option can be used to access various sections of the GUI as shown below:

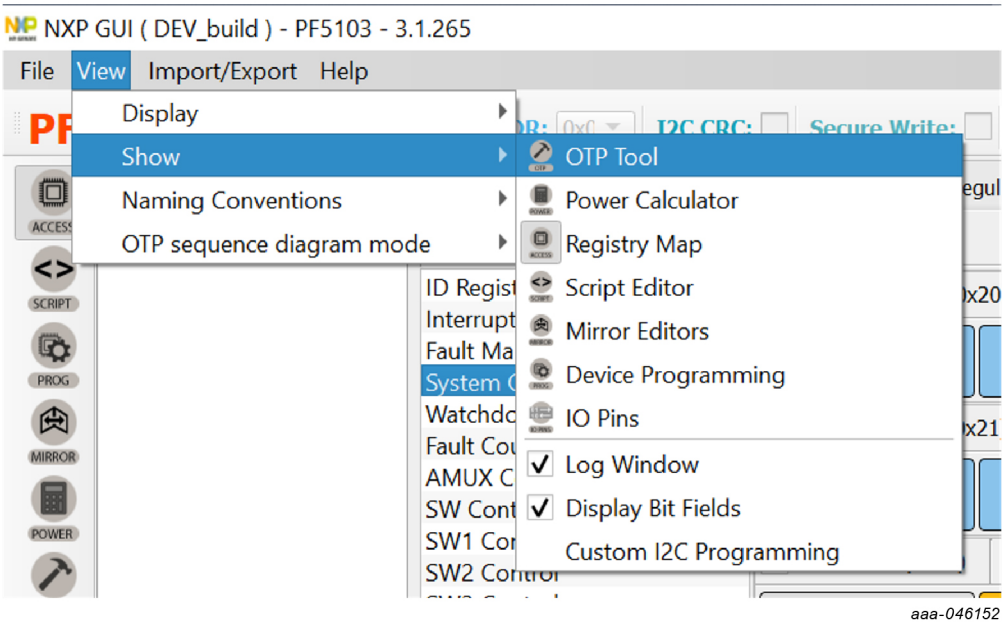


Figure 23. GUI kit Show view

Enabling Display Bit Fields provides a binary bit value next to a corresponding field.

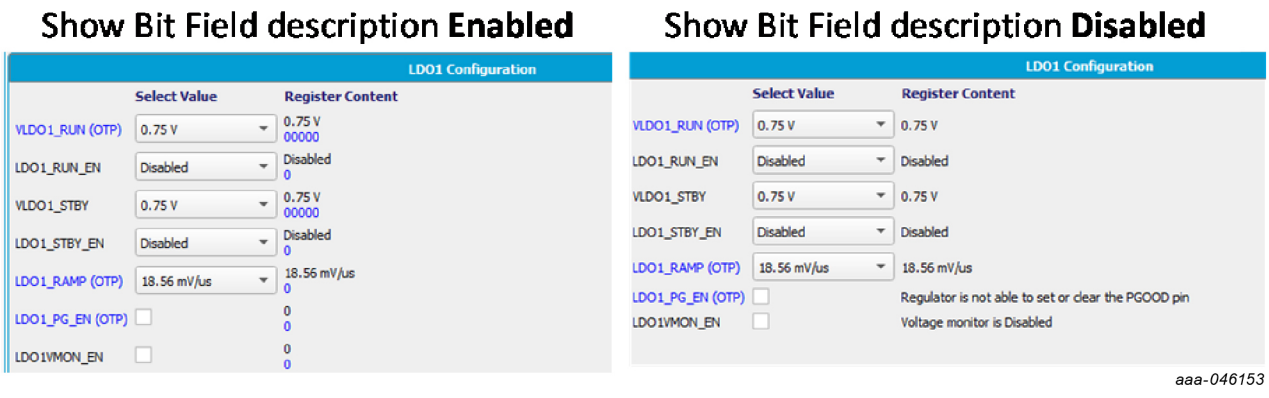


Figure 24. GUI kit Show View Enabled and Disabled

- **Naming Conventions:** Selects Friendly or Register name display for OTP tool. This option is enabled only when OTP tool is active.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

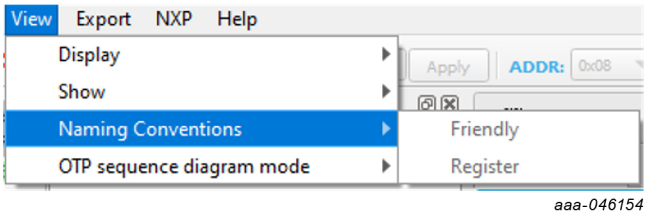


Figure 25. GUI kit View Naming conventions

The naming convention options are:

- **Friendly:** Causes register names to be displayed as user-friendly names throughout the OTP tool.
- **Register:** Causes register names to be displayed as the register's technical names throughout the OTP tool.

- **OTP sequence diagram mode:** Sets the x-axis in the Sequence Diagram (Sequencer tab) to display in either Time Mode, which displays the sequence in increments of time, or in Slot Mode, which displays the sequence in terms of the assigned slots.

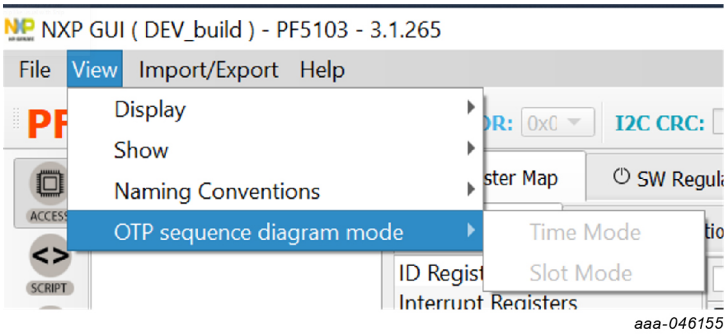


Figure 26. GUI kit View OTP sequence diagram mode

5.4.3.1.3 Import/Export menu

The Import/Export menu item allows the user to manage all of the files needed for emulation, for use with the OTP PROG tool, and for GUI configuration. This menu item is only active when the OTP tool has been selected. See Section 7.6 for details.

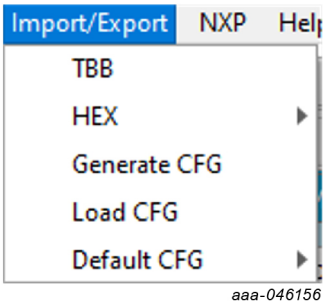


Figure 27. GUI kit Import/Export

The Import/Export menu consists of the following items:

- **TBB:** Exports an OTP configuration into a TBB script file that can be used to load the Mirror registers. The same file can be used by the PROG tool to burn OTP fuses.
- **HEX:** Outputs the script in HEX format. A drop-down menu allows the user to select the type of HEX format to be exported.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

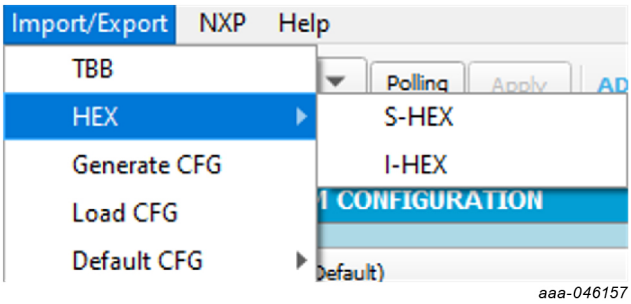


Figure 28. GUI kit Import/Export HEX

- **I-HEX:** Exports as an Intel Hex script file.
- **S-HEX:** Exports as a Simple Hex script file.

- **Generate CFG:** Generates a configuration file (.cfg) used by the GUI.
- **Load CFG:** Loads an existing configuration file.
- **Default CFG:** Loads a predefined configuration in QM or ASIL B to use as a starting point.

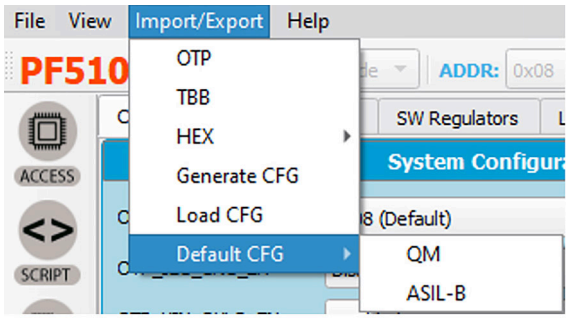


Figure 29. GUI kit Import/Export Default CFG

5.4.3.1.4 Help menu item

This menu item contains links to additional information and displays the version number of the installed GUI.

- **Documentation:** Lists online NXP documentation related to using the PF510x GUI.
- **About:** Displays the version number of the GUI currently installed.

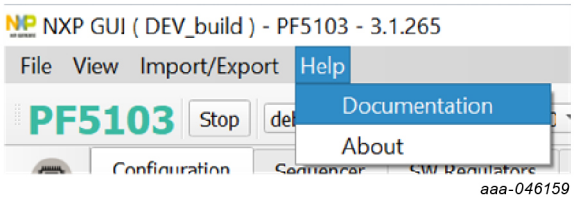


Figure 30. GUI kit Help

5.4.4 Device manager

The Device Manager menu is located directly below the Framework settings menu in the top left corner of the Framework window. See Figure 18.

Note: *The Device Manager is not displayed if the Connection Tool Bar is not selected in the Frameworks setting>View>Display menu item.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

The device manager allows the user to start or stop communication with the device, enter or exit the test mode, manage I^2C communications, and enableor disable the Watchdog Refresh.

The Device Manager consists of the following items:

- **Start/Stop** :Opens or closes communication with the device
- **Mode:** Selects between Debug mode, Test mode, and Normal mode
- **ADDR:** Sets the I^2C address assigned to the device
- **I2CCRC:** Indicates whether an extra CRC byte has been enabled by OTP programming
- **Secure Write:** Enables/disables I^2C secure write
- **Enable Watchdog Refresh:** Enables/disables a watchdog refresh
- **Period:** Sets the watchdog period
- **Type:** Sets watchdog type, either simple, or challenger



aaa-046160

Figure 31. Set watchdog type

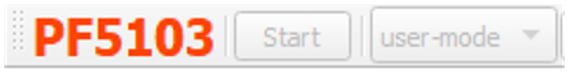
5.4.4.1 Device connection

A device connection box appears immediately below the Device Manager. When the FRDM-KL25Z is not connected through the USB port, the State indicator in the bottom bar shows Not Detected, the PF5103 header text appears red, and the Start button is not available.



aaa-046160

Figure 32. GUI kit Device Manager bar



aaa-046161

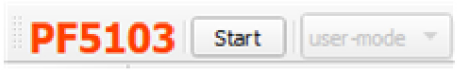
Figure 33. PF5103 no start no user-mode



aaa-046162

Figure 34. Device connection State: Not detected

After the USB cable is connected, the State indicator displays Connected and the Start button becomes available.



aaa-046321

Figure 35. Device connection Start



aaa-046322

Figure 36. Device connection State: Disconnected

Click on the Start button to start communication with the PF5103.

At this point, the State indicator will display Connected and PF5103 header text changes from red to green.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.



Figure 37. Device connection State: Connected

Usually, when connected, the next step is to load a script that is written to the Mirror register. This will be done in debug mode.

5.4.4.2 I²C address selection

The I²C address assigned to the device is selected via the ADDR selection box. The range of available values is from 0x08 to 0x0F.



Figure 38. I²C address selection

5.4.4.3 I²C CRC enablement

The PF5103 I²C communication bus can be configured to manage an extra CRC byte. This option is selected during OTP configuration by setting the OTP_I2C_CRC_EN bit. The FRDM-KL25Z must be notified when the OTP_I2C_CRC_EN is enabled in order to correctly manage the I²C communication. That notification is provided by an I2C CRC checkbox in the Device Manager.

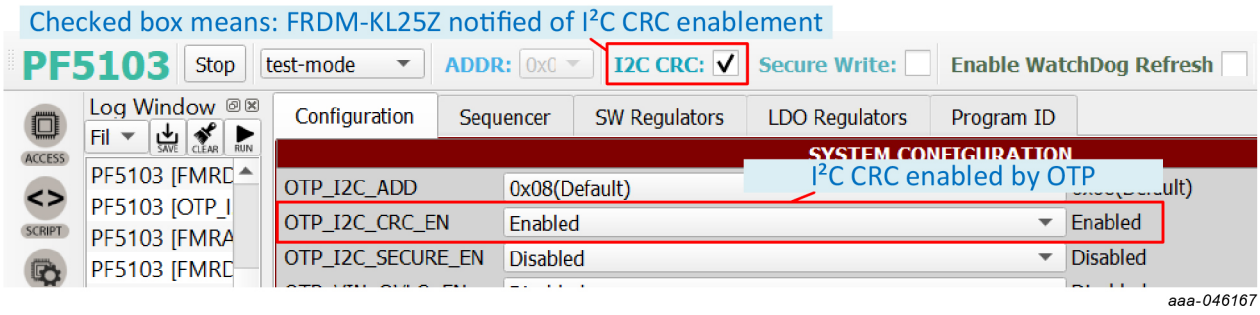


Figure 39. I²C CRC enablement notification

The configuration cases are:

- If OTP_I2C_CRC_EN is not enabled by OTP in the PF5103, no action is required by the user and the I2C CRC box can be left unchecked.
- If OTP_I2C_CRC_EN is enabled by OTP in the PF5103, the user must select test-mode in the Mode box and check the I2C CRC box in the Device Manager section.

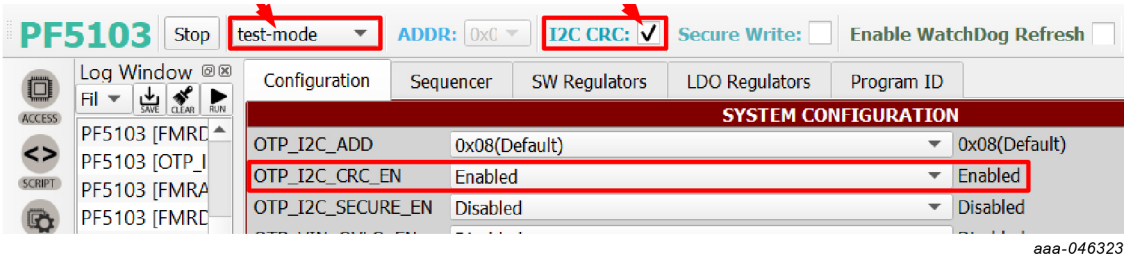


Figure 40. I²C test-mode

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

The GUI checks whether the PF5103 OTP_I2C_CRC_EN bit is enabled or not:

- If the OTP_I2C_CRC_EN bit is enabled, the selection is valid and the FRDM-KL25Z is notified and able to manage the I²C CRC.
- If the OTP_I2C_CRC_EN bit is not enabled, the PF5103 is not able to manage the I2C CRC, the FRDM-KL25Z is not notified and the following error message is displayed as a pop-up window.

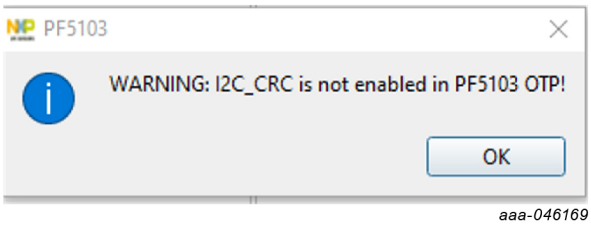


Figure 41. Warning I2C_CRC is not enabled

5.4.4.4 Secure Write mode enablement

PF5103 provides a Secure Write mechanism for specific bits that are critical to the functional safety of the device. The Secure Write sequence requests actions from both PMIC and MCU. PMIC actions are enabled by OTP_I2C_SECURE_EN. MCU actions are enabled by the Secure Write checkbox. This mechanism is fully operative when both PMIC and MCU actions are enabled.

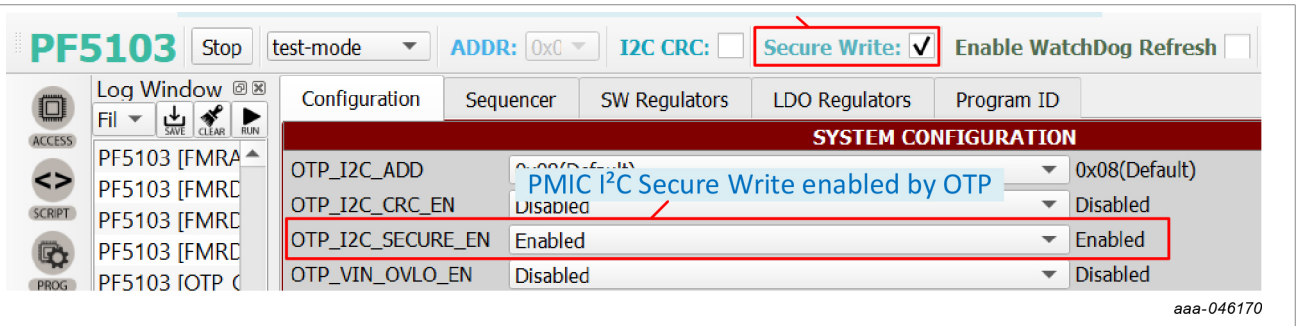


Figure 42. I²C Secure Write enabled by OTP

The configuration cases are:

- If OTP_I2C_SECURE_EN is not enabled by OTP in the PF5103, no action is required by the user and the Secure Write box can be left unchecked.
- If OTP_I2C_SECURE_EN is enabled by OTP in the PF5103, the user must select test-mode in the Mode box and check the Secure Write box in the Device Manager section.

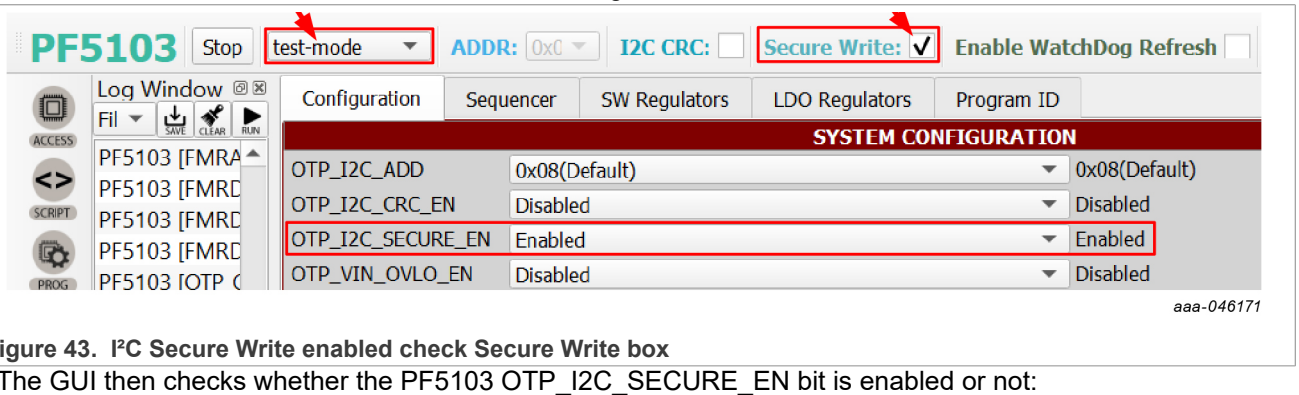


Figure 43. I²C Secure Write enabled check Secure Write box

The GUI then checks whether the PF5103 OTP_I2C_SECURE_EN bit is enabled or not:

- If the OTP_I2C_SECURE_EN bit is enabled, the selection is valid and the FRDM-KL25Z is now able to do I²C Secure Write actions.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

– If the OTP_I2C_SECURE_EN bit is not enabled, the PF5103 is not able to manage the Secure Write, therefore Secure Write is not enabled on FRDM-KL25Z and the following error message is displayed as a pop-up window.

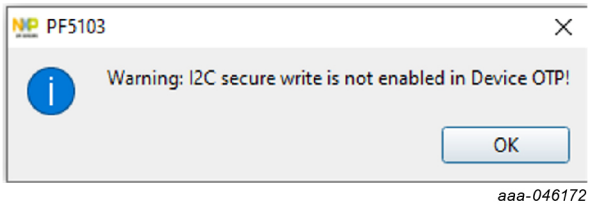


Figure 44. I²C Secure Write not enabled warning

5.4.4.5 Watchdog management

The PF5103 provides watchdog monitoring of Simple type or Challenger type as a functional safety feature. Watchdog monitoring requests synchronized actions from PMIC and MCU. Notice the Watchdog timer start as soon PGOOD is released. For the PF5103, the Watchdog monitoring default configuration is done by OTP, and additional Watchdog configuration is done via I²C.

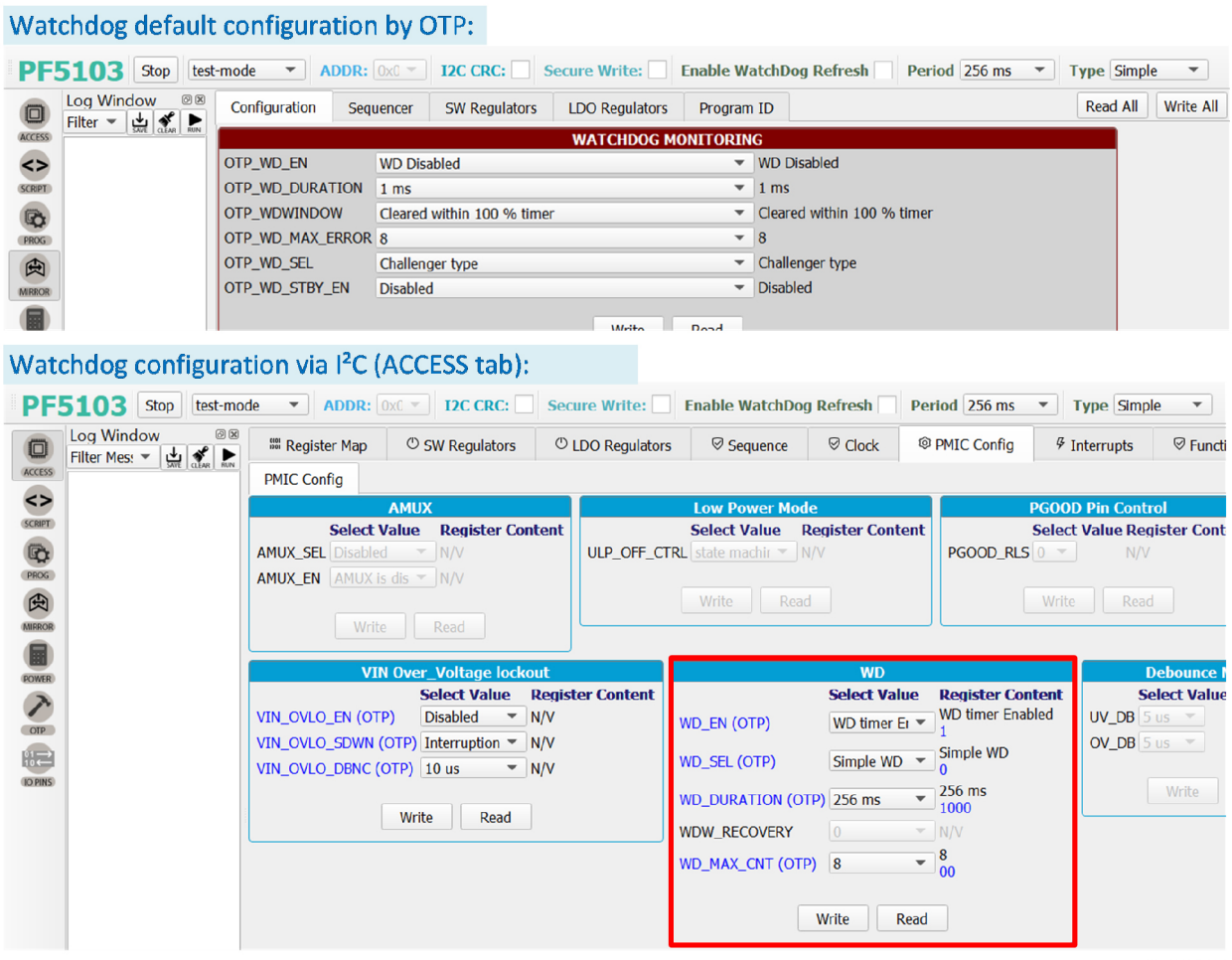


Figure 45. Watchdog default configuration window

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

MCU actions are configured with Period and Type selection boxes, and enabled by the Enable Watchdog Refresh checkbox in debug mode.



Figure 46. Watchdog configuration bar

The mechanism is fully operative when both PMIC and MCU actions are enabled and have matching configurations.

The steps for Watchdog enablement are described by Figure 47 and the following instructions:

1. Select Watchdog period via the Period selection box in the Device Manager.
2. Select Watchdog type (Simple or Challenger) via the Type selection box in the Device Manager.
3. Enable Watchdog refresh by checking the corresponding box to enable Watchdog monitoring on the MCU side.
4. A message is displayed in the Log Window with the selected period and type values.

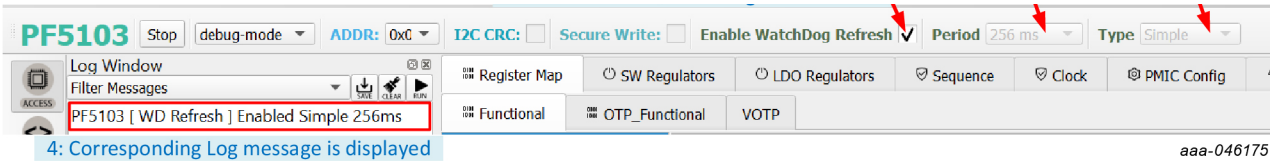


Figure 47. Watchdog configuration bar WD Refresh

If the Period and Type selection boxes are unavailable, please verify that Enable Watchdog Refresh is unchecked.

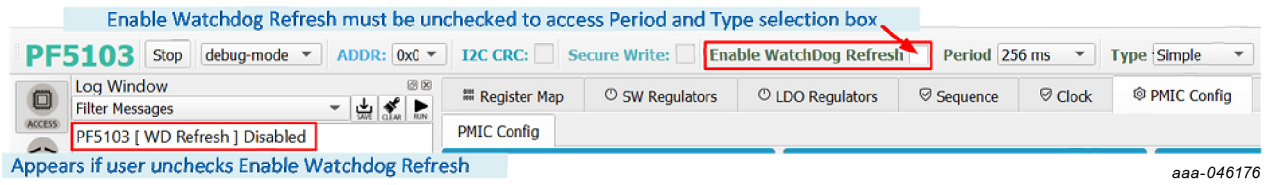


Figure 48. Watchdog configuration bar WD Refresh Disabled

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

6 Configuring the hardware

6.1 Setting up the KITPF5103FRDMEVM

The procedure for setting up the KITPF5103FRDMEVM board is as follows:

1. Make sure the board has the jumpers configured in their default position as shown in Figure 49. The default configuration enables the board to be fully controlled by the FRDM-KL25Z and the GUI.

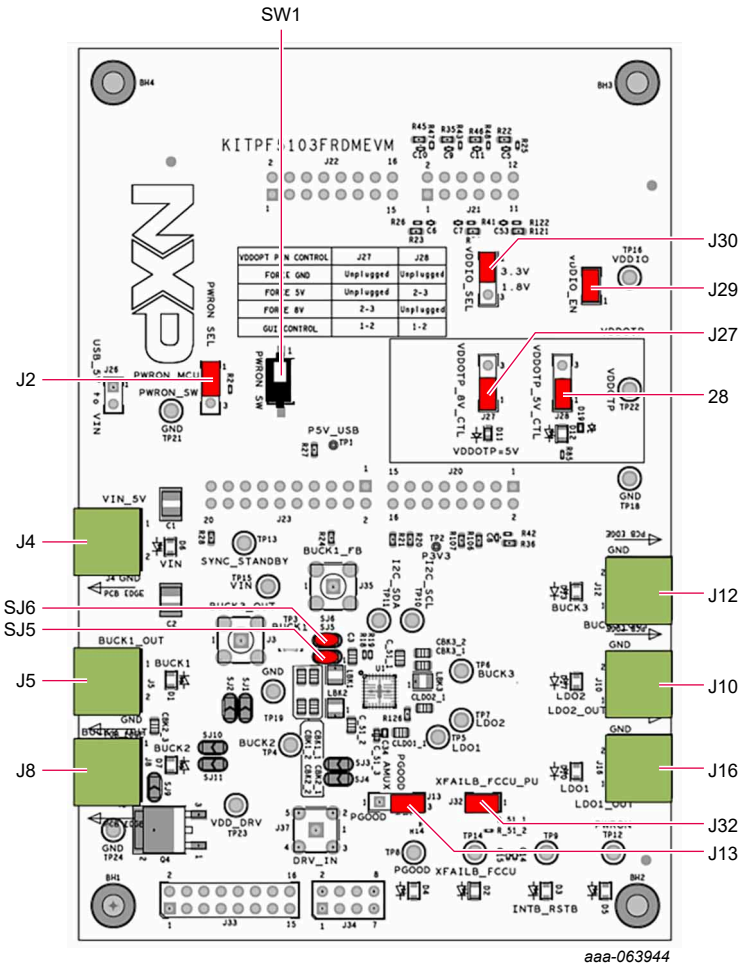


Figure 49. KITPF5103FRDMEVM board setup

2. Connect the power supply to J4 (Phoenix connector - 3.81 mm). The power supply should be set to an initial value of 5.0 V.
   Note: *Please check that J26 jumper is OFF, the USB_TO_5V supply mode cannot be used at the same time as J4 and cannot be used when loads are connected to the board.*
3. Verify that the FRDM-KL25Z board is firmly mounted to the KITPF5103FRDMEVM board. Also, make sure that the USB cable between the FRDM-KL25Z and the PC is securely connected. This connection is critical because the USB port serves as a communication channel between the PC and the FRDM-KL25Z board, provides voltages and references to some onboard circuits, and generates the VDDIO reference for the integrated circuit (IC).

6.2 Connecting the KITPF5103FRDMEVM to the GUI

The procedure for connecting the KITPF5103FRDMEVM to the GUI is:

All information provided in this document is subject to legal disclaimers.

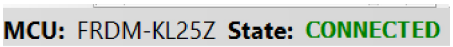
© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

1. Click the Windows icon at the bottom left of the screen to open the All Apps panel. Find the NXPGUI icon in the All Apps panel and click on it to open the GUI.
2. When the GUI opens, the Kit Selection window appears. Select PF5103 device and click on the OK button. ***Note:*** *If the File menu shows a checkmark next to the "Do not display GUIKit selection at Start" item, the Kit Selection window does not appear at start-up.*
3. In the bar at the bottom of the window, the State message should display DISCONNECTED. This indicates the USB cable is plugged in but communication has not been established between the FRDM-KL25Z and the PF5103.

USB cable plugged in, communication not established yet	 aaa-046221 **Figure 50. State: Disconnected**
USB cable not plugged in	 aaa-046222 **Figure 51. State: Not detected**

4. To establish communication between the FRDM- KL25Z and the PF5103 and allow the GUI to take control, click on the Start button in the upper left corner.

USB cable plugged in, communication established	 aaa-046223 **Figure 52. Connected**

6.3 Operation modes

GUI provides three distinct modes that have direct impact on device functionalities.

Understanding those mode will with using the GUI properly.

6.3.1 Debug mode

Debug is the default mode when GUI is started.

This mode requires PWRON = HIGH and VDDOTP = 5 V.

When this mode is active, the device runs with limited functionalities where some functions are disabled.

Note: *Functions CRC, Secure Write, Watchdog are disabled and default I²C address is 0x08.*

Debug mode is helpful during software development if the device has those functions enabled by OTP.

6.3.2 Test mode

Test mode requires PWRON = LOW and VDDOTP = 8 V and valid test-mode keys to be sent by I^2C.

When entering test mode, the device goes in the LP_OFF state, and the GUI will automatically send keys to PMIC to have full mirror register access.

When the configuration is done, the user can move either in normal mode or debug mode to power up the device with the given configuration.

6.3.3 Normal mode

The normal-mode operation is the one used for final product in an automotive environment.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

This mode requires PWRON = HIGH and VDDOTP = GND.

When this mode is active, the device operates with full functionalities regarding the loaded OTP configuration.

Note: *When going in normal mode, test mode is exited.*

6.3.4 Debug-mode operation

With GUI using Mode selection (Recommended) :

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and your computer.
3. Apply VIN.
4. Open the GUI and start the connection.
5. Select debug-mode from Device Manager:

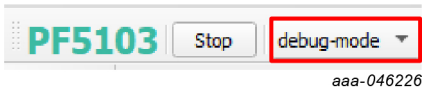


Figure 53. GUI using Mode selection debug-mode

6. Debug mode is now set.

With GUI using I/O Pins (Advanced):

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN.
4. Open the GUI and start the connection.
5. Go to I/O Pins tab:

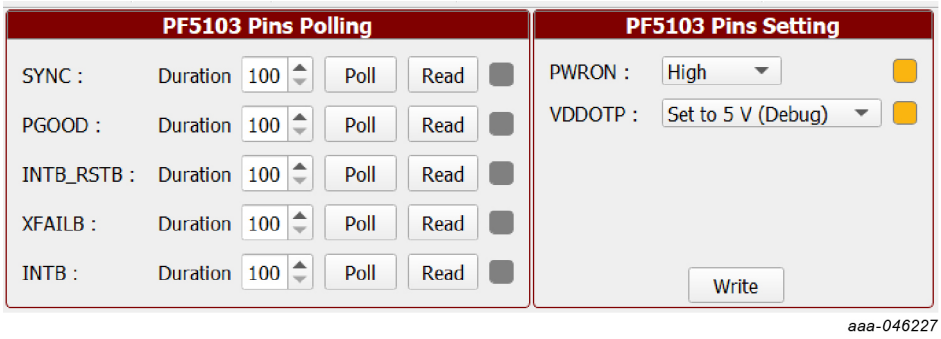


Figure 54. GUI using I/O Pins debug-mode

6. Set PWRON to HIGH and VDDOTP to Set to 5 V (debug).
7. Click on Write.
8. Debug mode is now set.

With Hardware (Without GUI) :

From the default jumper configuration. See Section 6.1.

1. Place J2 jumper between in position 2-3 (PWRON controlled by SW1).
2. Open J27 jumper and place jumper J28 in position 2-3 (Force VDDOTP to 5 V).
3. Set SW1 to ON state (PWRON=HIGH).
4. Apply VIN.
5. The device will power up and operate in debug mode.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

6.3.5 Test-mode operation

The test-mode operation allows the user to create and test a preliminary version of a desired configuration in the mirror registers, prior to submitting the configuration to the OTP fuse burning process.

The loaded configuration is activated in the PF5103 as soon as PWRON goes active (assuming VIN is above VIN_UV).

There are two ways to load mirror register:

- With a TBB script via Script tool
- With the Mirror tool

Those ways are functional with an empty or burned part.

6.3.5.1 Modify mirror registers with a TBB Script

One way to configure the mirror registers is to use the Script tool. See Section 7.2.

In order to start the device with a configuration loaded in the mirror registers, follow the instructions below:

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN. This action loads the mirror registers with burned OTP configuration if present.
4. Set the connection with the GUI.
5. Switch to test-mode.
6. In the Script Tool, click Open in the Script bar to load the TBB script file into the Script Command window.
   Note: *The script file must have a "PF5103" prefix.*



Figure 55. Open

7. To execute the TBB script, click on Run in the bar at the bottom of the Script Command Window:



Figure 56. Run

8. Switch to normal mode or debug mode to start the device with the given configuration. This action loads the I²C functional registers with the mirror registers content

At this point, the PWRON LED should be lit on the KITPF5103FRDMEVM board, indicating the device is now running with the given configuration in the chosen mode.

To verify, open the Access tool and check the fields in the SW Regulators tab. If the operation completed without problems, all fields should display expected configuration.

6.3.5.2 Modify Mirror with the Mirror tool

To configure the mirror registers, Mirror tool can be used to write/read directly into mirror registers. See Section 7.4. For this operation, test mode must be activated.

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

3. Apply VIN. This action loads the mirror registers with burned OTP configuration if present.
4. Set the connection with the GUI.
5. Switch to test-mode.
6. Go to Mirror tool from the Tools access bar:

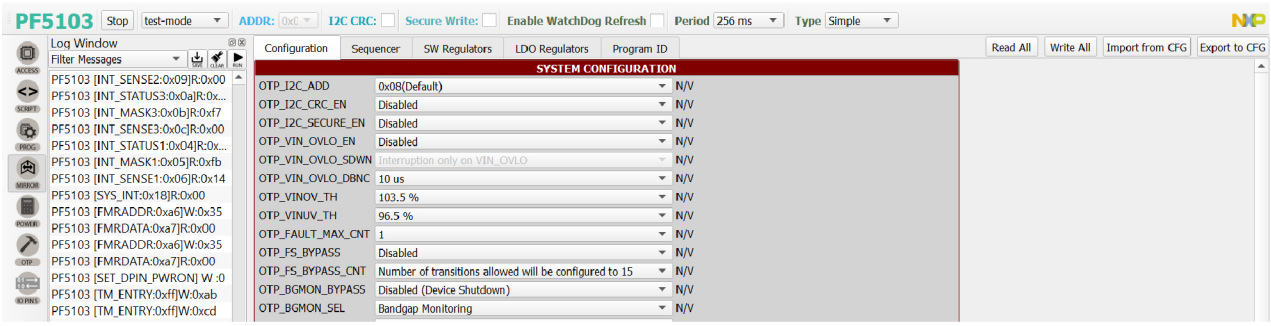


Figure 57. Test-mode mirror configuration

7. Configure appropriate mirror registers to fit the application.
8. Once done, click on Write All.
9. Switch to normal mode or debug-mode to load the mirror registers with the given configuration.
   - It is possible to load a configuration from a previously made configuration saved as a CFG file, using the Import from CFG button in the top-right corner of the Mirror tool.
   - It is possible to save a current mirror registers configuration as a .cfg file. Use the Export from CFG button in the top right corner of the Mirror tool.

6.3.6 Normal-mode operation

There are two ways to activate normal mode:

With GUI using Mode selection (Recommended) :

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN.
4. Open the GUI and start the connection.
5. Select normal mode from Device Manager:

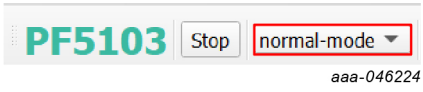


Figure 58. GUI using Mode selection normal-mode

6. Normal mode is automatically set.

With GUI using I/O Pins (Advanced):

1. Set the default jumper configuration. See Section 6.1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN.
4. Open the GUI and start the connection.
5. Go to I/O Pins tab:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

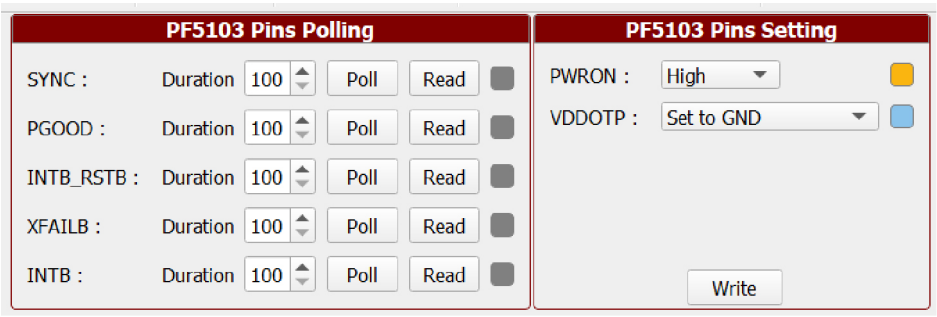


Figure 59. GUI using I/O pins

6. Set PWRON to HIGH and VDDOTP to Set to GND.
7. Click on Write.
8. Normal mode is now set.

With hardware (Without GUI):

1. From the default jumper configuration. See Section 6.1.
2. Place J2 jumper between in position 2-3 (PWRON controlled by SW1).
3. Open jumper J27 and jumper J28 (Force VDDOTP to GND).
4. Set SW1 to ON state (PWRON=HIGH).
5. Apply VIN.
6. The device will power up and operate in normal mode.

6.4 Generate a TBB script

A TBB file is needed to burn an OTP fuse or to emulate an OTP configuration by filling the mirror registers through the Script tool.

Follow the prodecure below to generate a TBB file:

1. Go to the OTP tool from the Tools access bar:

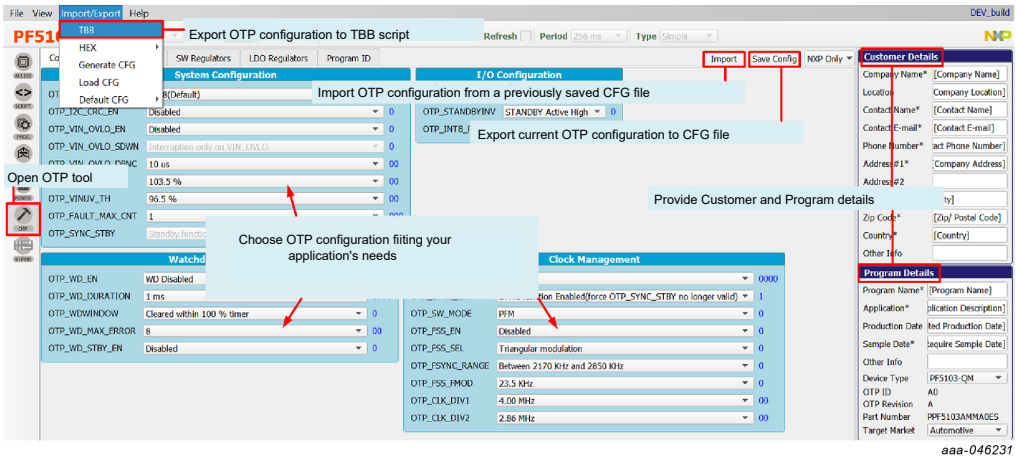


Figure 60. Generate TBB script

2. Configure the OTP parameters to fit the application’s needs.
3. Enter Customer and Program details in the window on the right side.
4. When done, directly export the OTP configuration to a TBB script by clicking on Import/Export in the Framework settings bar and choosing TBB:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

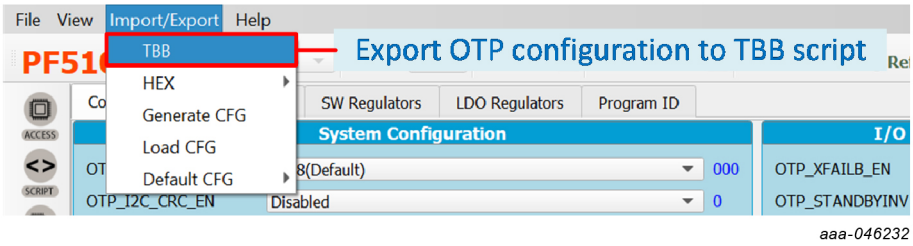


Figure 61. Export OTP to TBB script window

5. Select the desired folder to save the TBB script:

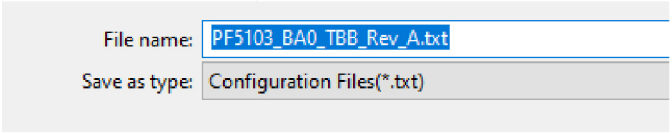


Figure 62. Export OTP to TBB script destination

Note: *The Script file must have a "PF5103" prefix.*

6. The TBB script is now generated and saved. See Section 6.6 for a TBB script example.

6.5 Programming an OTP operation

The Prog tool, see Section 7.3, is used to burn the PF5103 fuses with the user's OTP configuration from a TBB script file.

The TBB script can be generated from an OTP configuration. See Section 6.4 for instructions.

The TBB file must have PF5103 as a prefix.

Note: *A PF5103 device can be burned only once.*

Requirement: Make sure the socket contains a device that has not yet been burned before starting the burning process.

To verify the part is empty:

1. Set the default jumper configuration. See Figure 1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN. This action loads the mirror registers with burned OTP configuration if present.
4. Set the connection with the GUI and switch to test mode.
5. Open the Prog tool from the Tools access bar.
6. Check the flags in the Sector Flags section of the Fuse Box Status window. See Section 7.3.1.
7. The device is empty and capable of being burned if the three conditions are fulfilled:
   a. SECT_BE0, SECT_WP0 flags are set to 1 (orange).
   b. SECT_BE1, SECT_WP1 flags are set to 1 (orange).
   c. SECT_BE2, SECT_WP2 flags are set to 0 (blue).

Figure 63 shows the Sector Flags status in the PF5103 Programming interface for an empty part.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

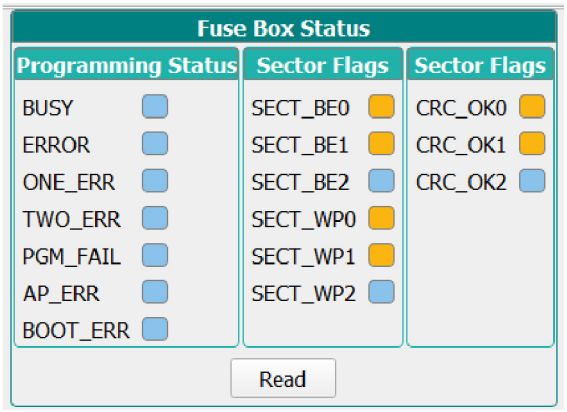


Figure 63. Programming an OTP operation Fuse Box Status

All sectors flags are set to 1 (orange) once the part is burned.

Programming procedure:

1. Set the default jumper configuration. See Figure 1.
2. Plug the USB cable between the board (USB port of KL25Z) and the computer.
3. Apply VIN.
4. Set the connection with the GUI and switch to test-mode.
5. Open the Prog tool from the Tools access bar.

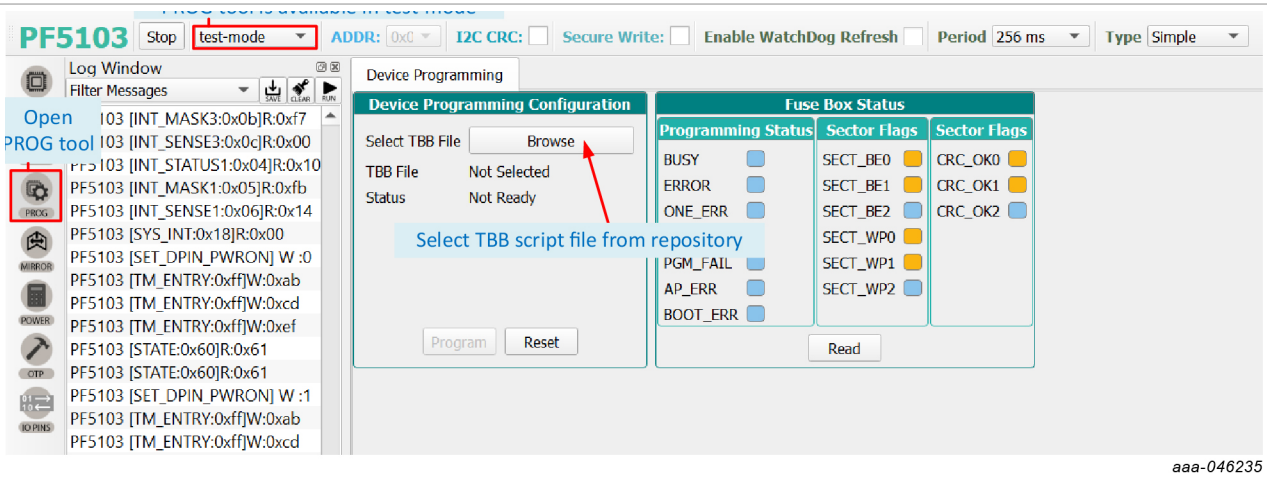


Figure 64. Load TBB file

6. Load the TBB file.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

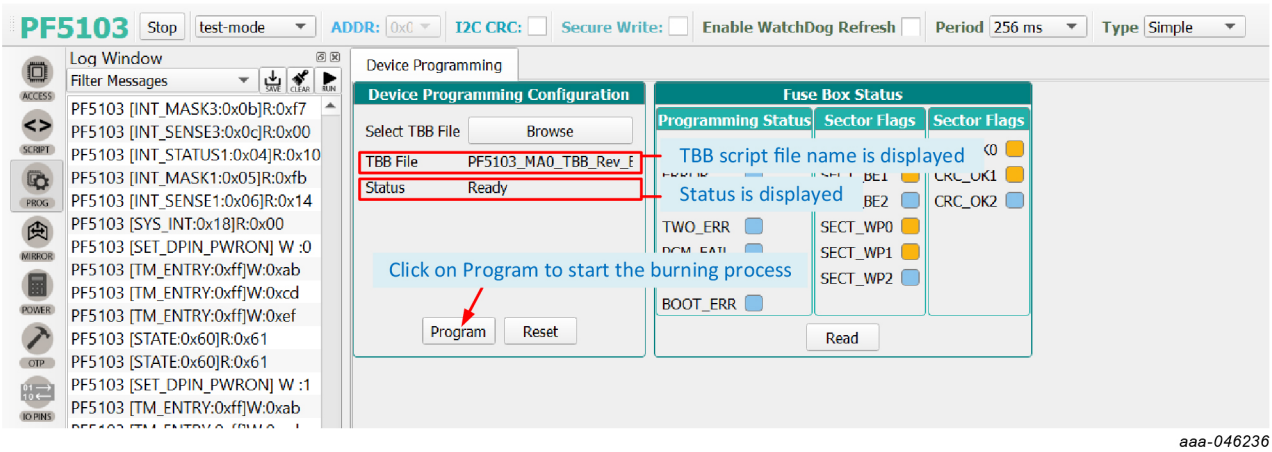


Figure 65. OTP programming

7. Click Program.
8. One pop-up window will appear asking confirmation for burning. Confirm to launch the burning process.

The device will start automatically at the end of OTP programming.

A good check is to use Measurement panel to see is all regulators are OK.

6.6 TBB script example

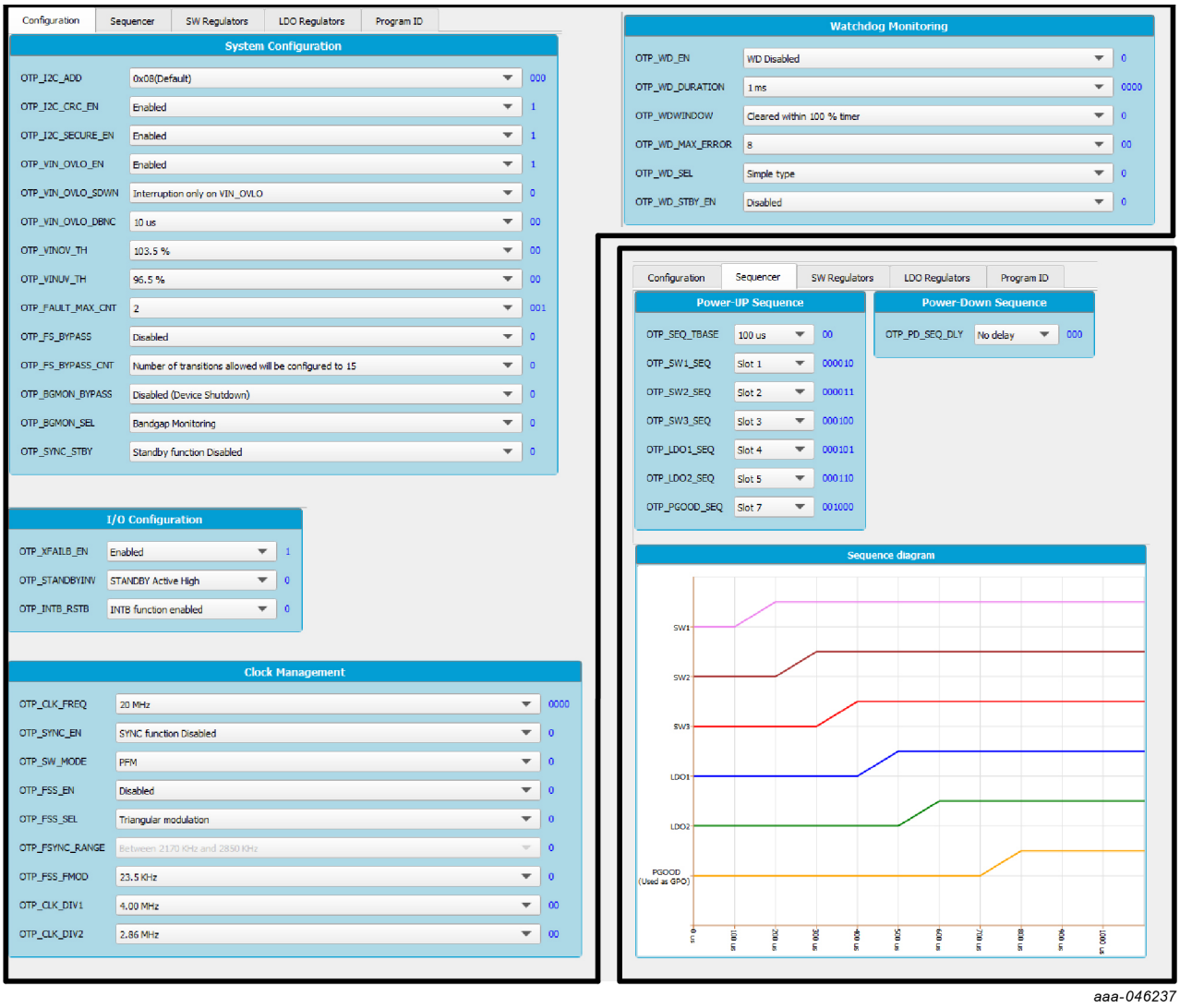
This section contains an example of a complete TBB script that can be loaded and executed for PF5103.

Note: *A TBB script file contains program information and Script Commands. Script Commands access registers via address and set register values, whereas a CFG file contains Customer Data, Program Information and OTP registers content in an hexadecimal format. There are no commands. This is simply informative.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.



aaa-046237

Figure 66. Configuration for PF5103

Table 14. Regulators settings

	BUCK1	BUCK2	BUCK3	LDO1	LDO2
Voltage	3.3 V	2 V	1 V	3.3 V	2 V
Switching frequency	CLK_DIV2	CLK_DIV2	CLK_DIV2	CLK_DIV2	CLK_DIV2
PGOOD enabled/ disabled	Enabled	Enabled	Enabled	Enabled	Enabled

Table 15. Example TBB script

//PF5103 - TBB file	SET_REG:PF5103:OTP_Controller:FMRDATA:0x04
//file generated on mar. mars 22 16:34:39 2022	SET_REG:PF5103:OTP_Controller:FMRADDR:0x49
//Device Type : PF5103-ASILB	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
//OTP ID : A0	SET_REG:PF5103:OTP_Controller:FMRADDR:0x4A

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Table 15. Example TBB script...*continued*

//OTP Revision : A	SET_REG:PF5103:OTP_Controller:FMRDATA:0x03
//Part Marking : PPF5103AMBA0ES	SET_REG:PF5103:OTP_Controller:FMRADDR:0x53
//Customer : NXP	SET_REG:PF5103:OTP_Controller:FMRDATA:0x1f
	SET_REG:PF5103:OTP_Controller:FMRADDR:0x54
//MAIN_OTP	SET_REG:PF5103:OTP_Controller:FMRDATA:0x05
SET_REG:PF5103:OTP_Controller:FMRADDR:0x35	SET_REG:PF5103:OTP_Controller:FMRADDR:0x55
SET_REG:PF5103:OTP_Controller:FMRDATA:0x18	SET_REG:PF5103:OTP_Controller:FMRDATA:0x04
SET_REG:PF5103:OTP_Controller:FMRADDR:0x36	SET_REG:PF5103:OTP_Controller:FMRADDR:0x56
SET_REG:PF5103:OTP_Controller:FMRDATA:0x01	SET_REG:PF5103:OTP_Controller:FMRDATA:0x12
SET_REG:PF5103:OTP_Controller:FMRADDR:0x37	SET_REG:PF5103:OTP_Controller:FMRADDR:0x57
SET_REG:PF5103:OTP_Controller:FMRDATA:0x04	SET_REG:PF5103:OTP_Controller:FMRDATA:0x06
SET_REG:PF5103:OTP_Controller:FMRADDR:0x38	SET_REG:PF5103:OTP_Controller:FMRADDR:0x58
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x04
SET_REG:PF5103:OTP_Controller:FMRADDR:0x39	SET_REG:PF5103:OTP_Controller:FMRADDR:0x59
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3A	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5A
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3B	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5B
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3C	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5C
SET_REG:PF5103:OTP_Controller:FMRDATA:0x10	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3D	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5D
SET_REG:PF5103:OTP_Controller:FMRDATA:0x20	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3E	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5E
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x24
SET_REG:PF5103:OTP_Controller:FMRADDR:0x3F	SET_REG:PF5103:OTP_Controller:FMRADDR:0x5F
SET_REG:PF5103:OTP_Controller:FMRDATA:0xd4	SET_REG:PF5103:OTP_Controller:FMRDATA:0x04
SET_REG:PF5103:OTP_Controller:FMRADDR:0x40	SET_REG:PF5103:OTP_Controller:FMRADDR:0x60
SET_REG:PF5103:OTP_Controller:FMRDATA:0x02	SET_REG:PF5103:OTP_Controller:FMRDATA:0xdd
SET_REG:PF5103:OTP_Controller:FMRADDR:0x41	SET_REG:PF5103:OTP_Controller:FMRADDR:0x61
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FMRDATA:0x0d
SET_REG:PF5103:OTP_Controller:FMRADDR:0x42	SET_REG:PF5103:OTP_Controller:FMRADDR:0x62
SET_REG:PF5103:OTP_Controller:FMRDATA:0x03	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x43	SET_REG:PF5103:OTP_Controller:FMRADDR:0x63
SET_REG:PF5103:OTP_Controller:FMRDATA:0x90	SET_REG:PF5103:OTP_Controller:FMRDATA:0x00
SET_REG:PF5103:OTP_Controller:FMRADDR:0x44	
SET_REG:PF5103:OTP_Controller:FMRDATA:0x03	//SET CRC VALUES
SET_REG:PF5103:OTP_Controller:FMRADDR:0x45	SET_REG:PF5103:OTP_Controller:FCMD:0xA5
SET_REG:PF5103:OTP_Controller:FMRDATA:0x00	SET_REG:PF5103:OTP_Controller:FCMD:0xA4
SET_REG:PF5103:OTP_Controller:FMRADDR:0x46	DELAY:100
SET_REG:PF5103:OTP_Controller:FMRDATA:0x03	//Rev,A
SET_REG:PF5103:OTP_Controller:FMRADDR:0x47	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Table 15. Example TBB script*...continued*

SET_REG:PF5103:OTP_Controller:FMRDATA:0x41
SET_REG:PF5103:OTP_Controller:FMRADDR:0x48

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

7 Using the Tools access bar

The Tools access bar appears in a vertical row along the left side of the Framework window. It provides access to tools that implement various GUI functions. The Tools access bar consists of seven items:

- **Access:** Provides access to I^2C registers
- **Script:** Create, open, save, and run scripts
- **Prog:** Manage OTP fuse-burning process
- **Mirror:** Provides access to Mirror registers
- **Power:** Not available in this release
- **OTP:** Create and save OTP configuration files
- **I/O PINS:** Read and set PF5103 I/O pins



Figure 67. Framework window tools bar

7.1 Access

The Access tool provides access to all I²C registers, either in a register map format or in a graphical and more readable view.

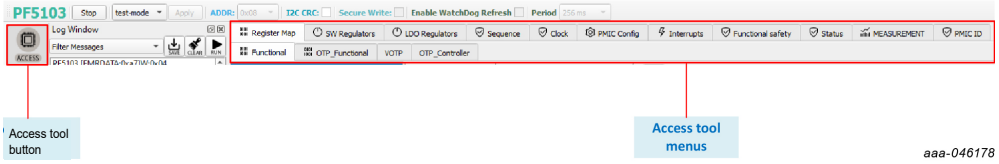


Figure 68. Access tool

7.1.1 Tab content

The Tab Content window in the Access tab provides access to GUI functions that configure, monitor, and control the PF510x device during the evaluation session.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Note: *For all graphical panels (except Register Map), register names that appear in blue with an OTP suffix are set by OTP and available later in the I²C register mapping. See Figure 69 for an example.*

VSWx_RUN (OTP) is part of OTP and the I²C functional mapping.

SWx_RUN_MODE is available only in the I²C functional mapping.

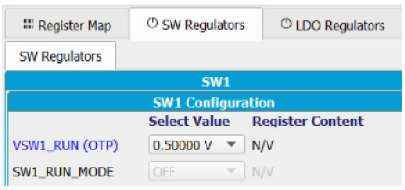


Figure 69. Framework window tools bar tab content

The Tab Content window contains eleven tabs:

- Register Map
- SW Regulators
- LDO Regulators
- Sequence
- Clock
- PMIC Config
- Functional Safety
- Interrupts
- Status
- MEASUREMENT
- PMIC ID

7.1.1.1 Register Map

The Register Map tab allows the user to read or write to the PF510x registers. There are three sub-menus:

- **Functional:** Functional registers access (I²C register map).
- **OTP Functional:** OTP functional registers access (OTP mirrors register map).
- **VOTP:** ASIL/QM level of the configuration.

In each sub-menu, registers are organized by categories in the panel on the left.

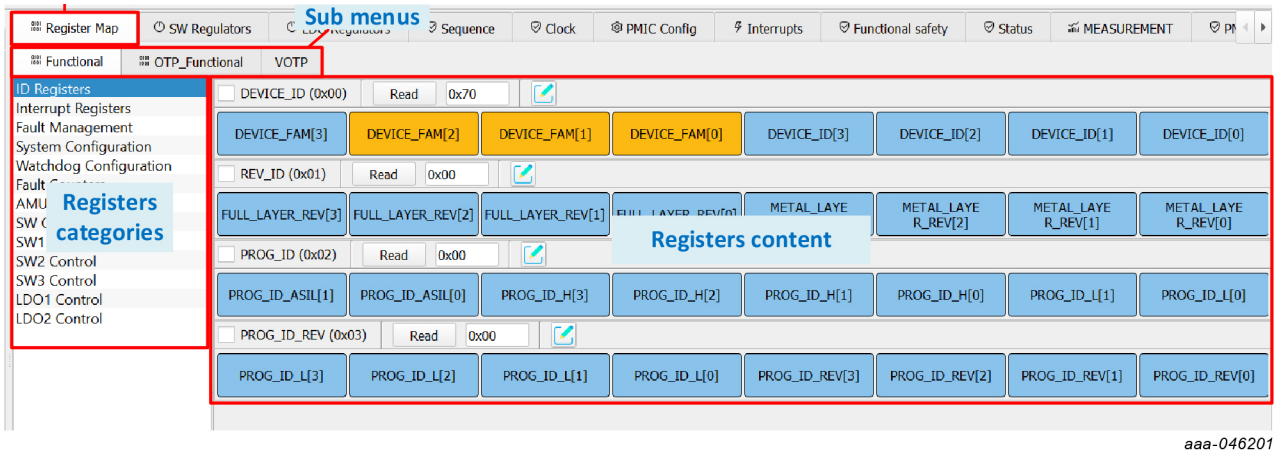


Figure 70. Register map menu

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

The PF5103 has two types of registers:

- Read Only registers, for example, ID registers, appear with a Read button only.

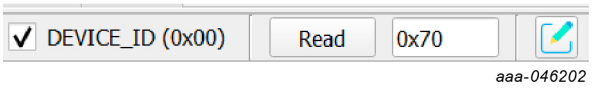


Figure 71. Register map menu Read Only registers

- Read/Write registers, such as Interrupt Registers, Fault Management, etc., appear with both a Read and a Write button.

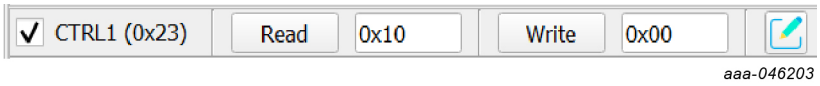


Figure 72. Register map menu Read and Write registers

To edit the registers content, either:

- Use dialog windows that include bits descriptions.
- Write hexadecimal value directly in one or multiple registers.

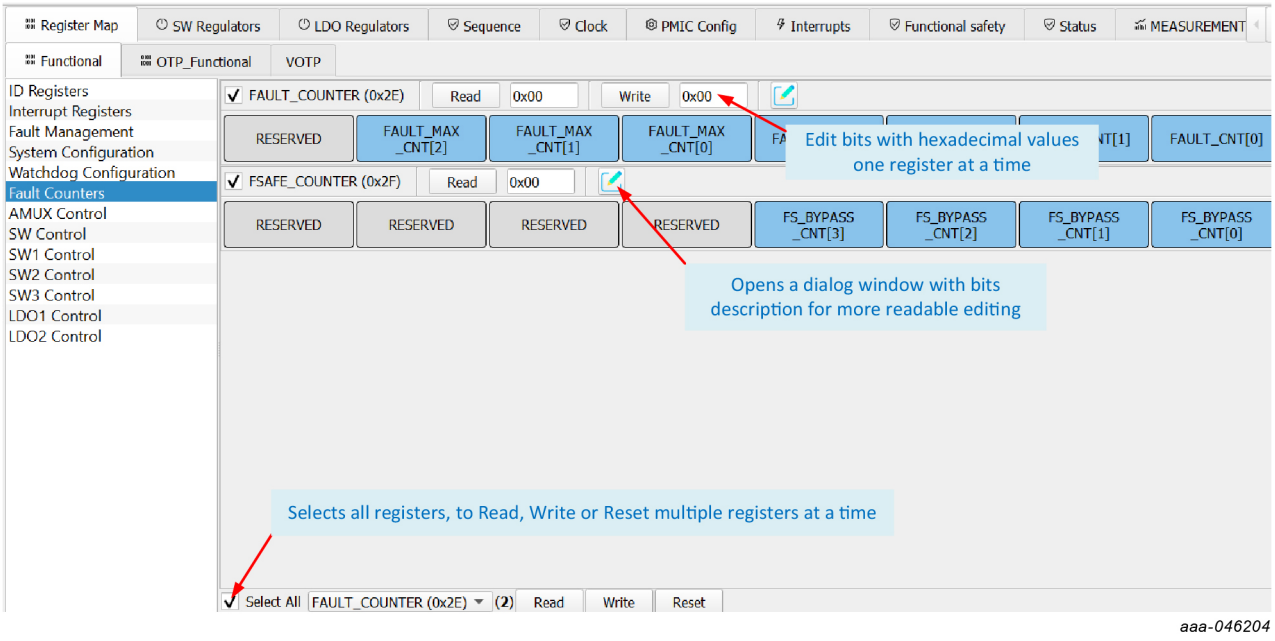


Figure 73. Register map menu Fault Counters

Using the dialog windows

To open a window that shows the name and description of all of the bitfields in a register, click on the green pen icon above the register. Figure 74 is an example of a dialog window for register CTRL1.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

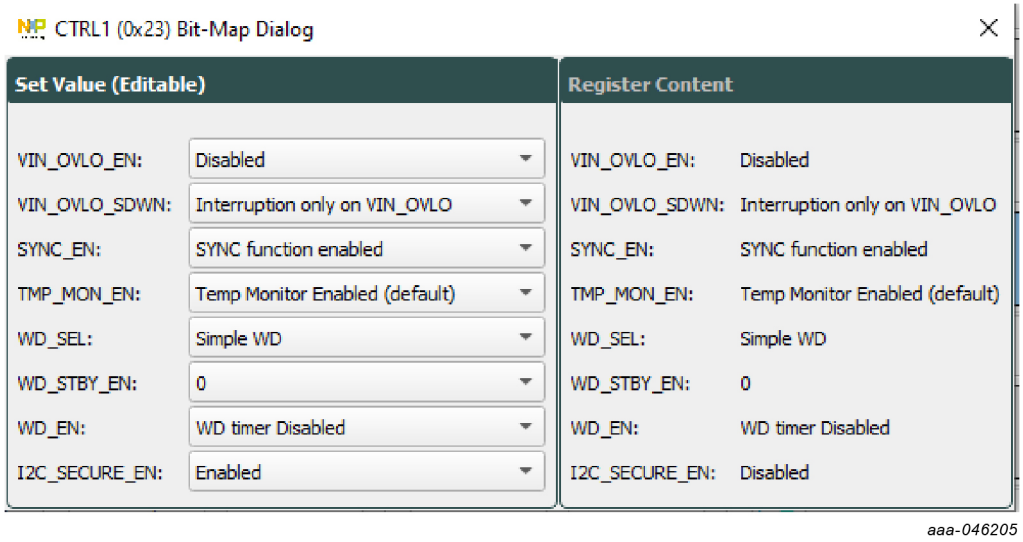


Figure 74. CTRL1 Bit-Map Dialog

Reading, writing, or resetting multiple registers at a time

Clicking in the Select All checkbox in the bottom left side of the register panel allows a user to simultaneously read or write to all of the registers in the window. Clicking on the Reset button switches all of the bits in the registers to 0.

7.1.1.2 SW Regulators

The SW Regulators tab allows the user to read and write the parameters related to the three bucks, giving access to the main settings of each buck, their monitoring configuration and fault event behaviors configuration.

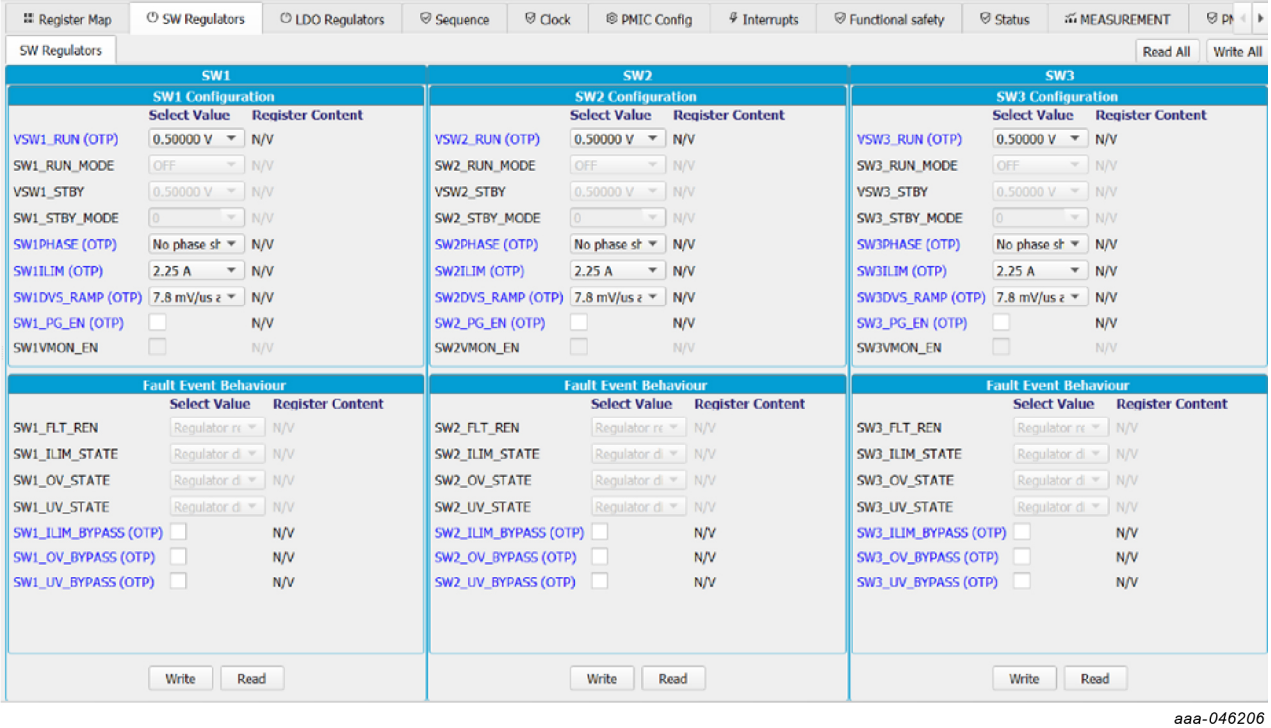


Figure 75. Register map menu SW Regulators

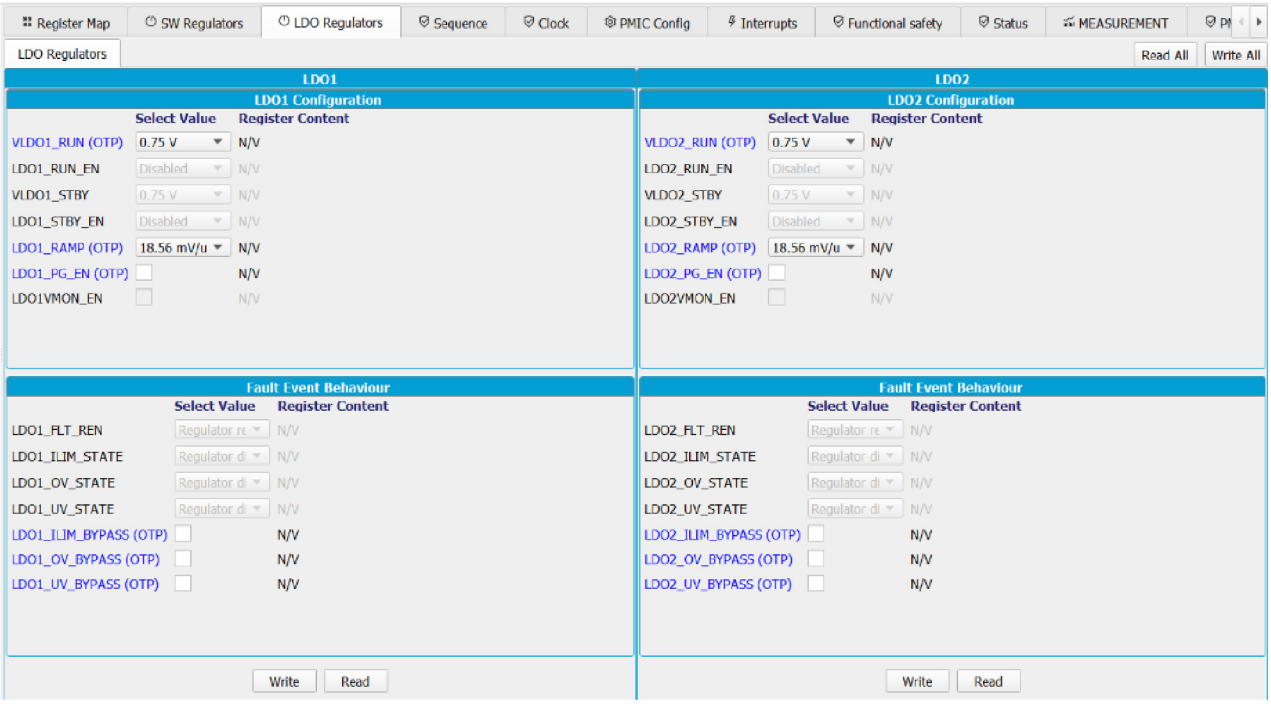
All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

7.1.1.3 LDO Regulators

The LDO Regulators tab allows the user to read and write the parameters related to the two LDOs, giving access to the main settings of each LDO, their monitoring configuration and fault event behaviors configuration.



aaa-046207

Figure 76. Register map menu LDO Regulators

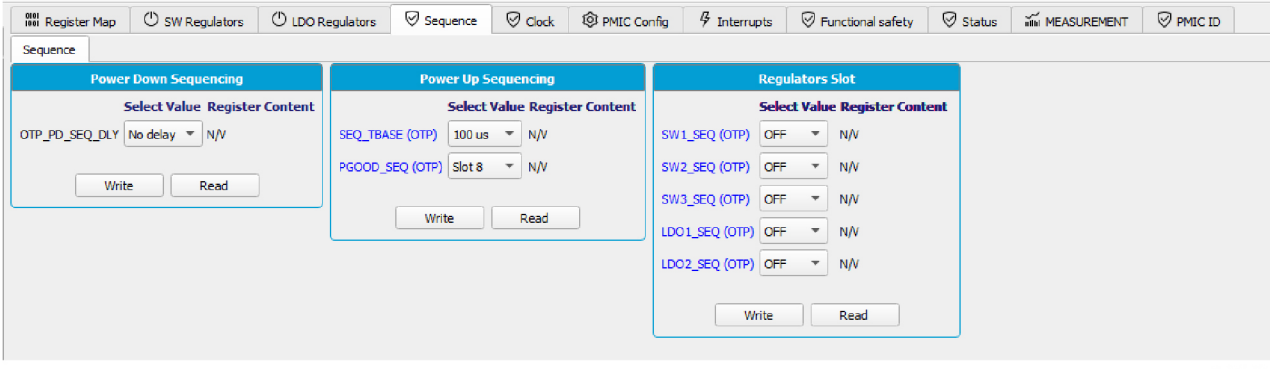
7.1.1.4 Sequence

The Sequence tab sets up the power-up/power-down sequence and the switcher slot assignments for the device. The tab has three sections:

Power Down Sequencing: Allows the user to read or write power-down sequencing parameters.

Power Up Sequencing: Allows the user to read or write power-up sequencing parameters

Switcher Slot: Allows the user to read or write the slots assigned to SW1, SW2 or SW3.



aaa-046208

Figure 77. Register map menu Sequence

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

7.1.1.5 Clock

The Clock tab manages the SYNC pin, switcher clock frequency, and spread spectrum.

The SYNC pin is used to either input the frequency synchronization or as a STANDBY input. When SYNC_EN is enabled (the SYNC pin is used as the synchronization pin), FSYNC_RANGE sets the frequency range of the SYNC signal expected. When SYNC_EN is disabled, FSYNC_RANGE is not used, and is not available and displayed in gray.

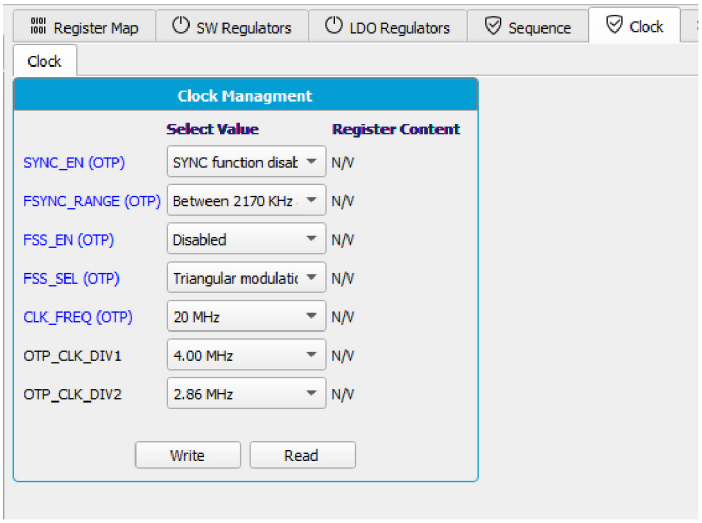


Figure 78. Register map menu Clock - Clock Management

7.1.1.6 PMIC Config

The PMIC Config tab allows the user to manage values related to various functions such as watchdog, thermal monitoring, etc. The PMIC Config tab contains the following windows:

- **AMUX:** Sets values for AMUX_SEL and AMUX_EN
- **Low Power Mode:** Selects the Low Power Mode
- **GPO (on PGOOD Pin):** Sets PGOOD low or high
- **Thermal Monitor:** Enables/disables the Thermal Monitor and selects whether the thermal monitor is always on, or whether it is turned on once every millisecond
- **VINOver_Voltage_Lockout:** Enables/disables VIN Over_Voltage lockout and selects whether an overvoltage triggers an interrupt or a shutdown
- **WD:** Sets up watchdog parameters
- **Debounce Monitoring:** Sets the debounce time for UV and OV monitoring

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

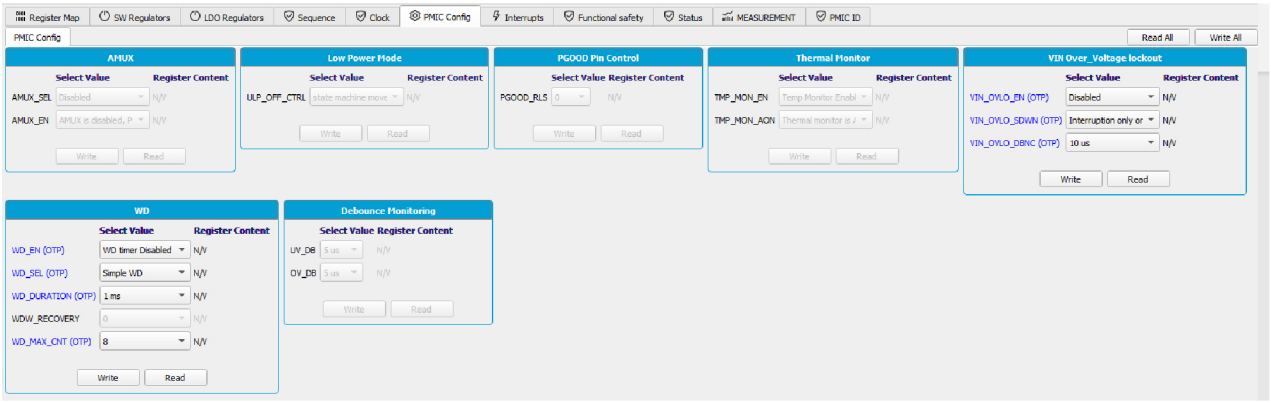


Figure 79. Register map menu PMIC Config

7.1.1.7 Interrupts

The Interrupts tag displays interruptions by category and allows the user to read or poll interrupt status, and clear or mask selected interrupts.

Interruption categories observable in this tab are:

- **SWx interrupts:** Gives information about BUCK1, BUCK2, and BUCK3
- **Thermal interrupts:** Gives thermal status of the board
- **System interrupts:** Gives information on system status
- **Watchdog interrupts:** Gives information on watchdog status
- **Miscellaneous interrupts:** Regroups interruptions from specific functions

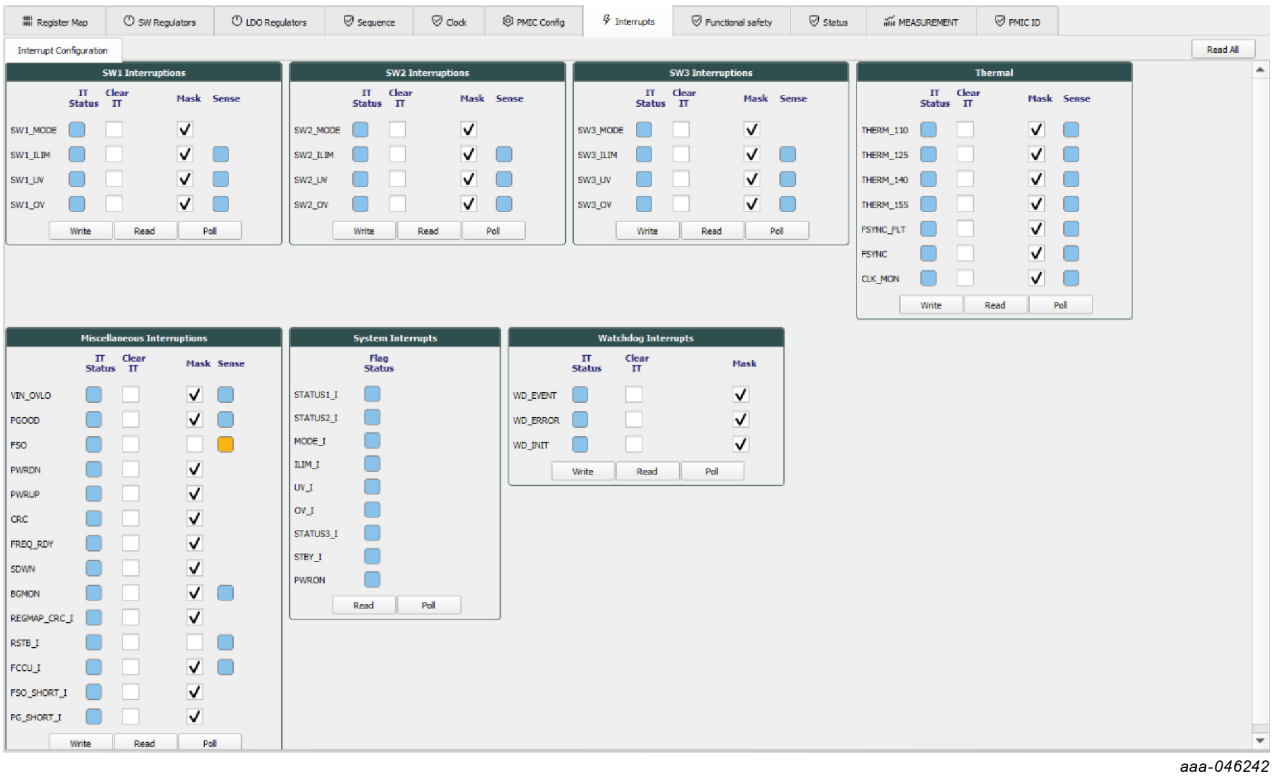


Figure 80. Register map menu Interrupts

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

7.1.1.8 Functional safety

For ASIL B, a list of bits is available only in the I^{2}C functional registers. The Functional safety tab manages the parameters for:

- **ABIST:** Allows the user to run ABIST and read or clear ABIST UV/OV status
- **Functional safety fault:** Displays fail-safe bypass counter value
- **Self-test status:** Displays the self-test result

Secure I^{2}C: Allows the user to enable and configure Secure I²C functionality

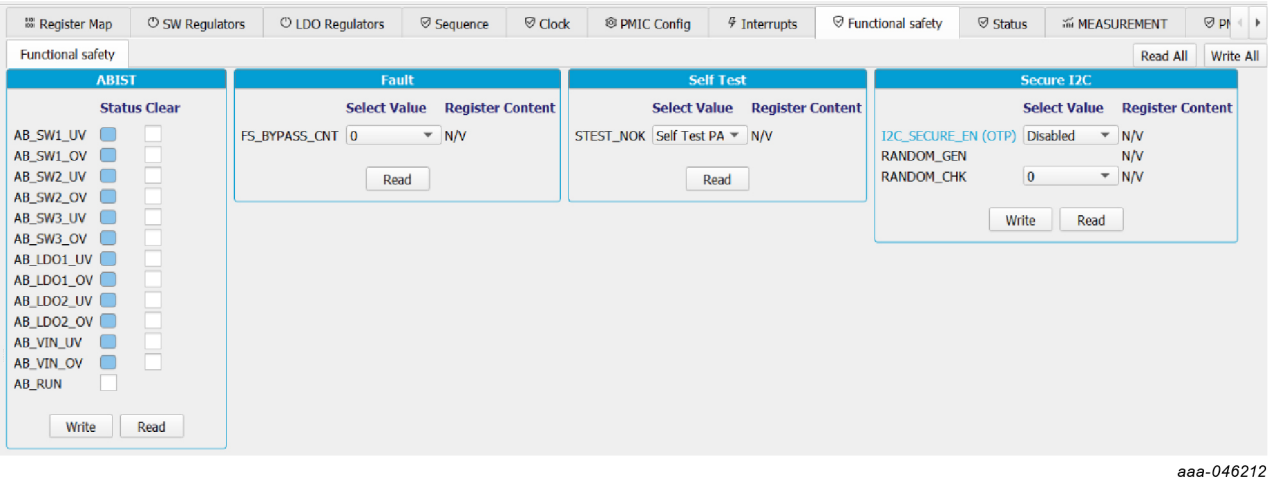


Figure 81. Register map menu Functional Safety

7.1.1.9 Status

The Status tab displays the status of selected functions and allows the user to modify the associated values of those functions. The tab provides status on the following:

- **Fail Safe Transition Event:** Allows the user to read or clear fail-safe hard-fault flags
- **OTP Mirror Check:** Allows a user to read and modify Mirror register test flags
- **WD:** Allows a user to read the Watchdog expiration counter
- **Fault:** Allows a user to read and modify the fault-counter bitfield and to enable/disable the max-fault counter

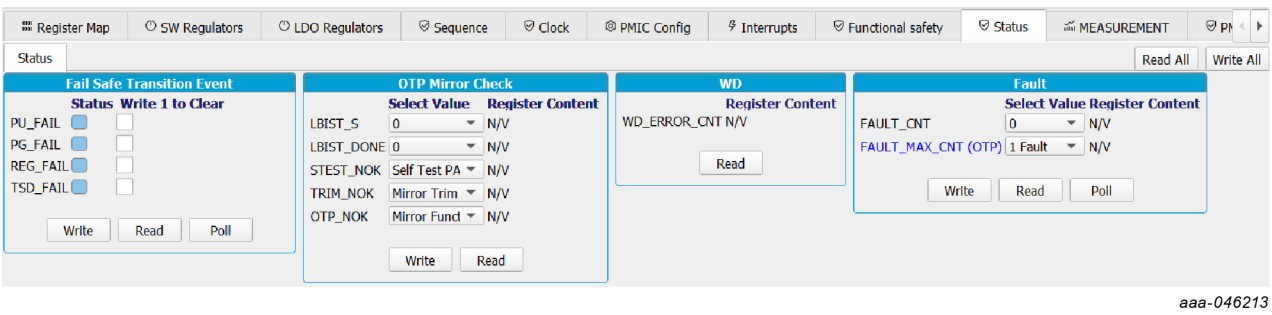


Figure 82. Register map menu Status

7.1.1.10 Measurement

The Measurement tab allows the user to get the values of:

- Analog voltage using the FRDM-KL25ZADC (BUCKs and LDO)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

- PGOOD/INTB_RSTB/XFAIL logical levels connected to the FRDM-KL25Z GPIO pins
- Junction temperature as measured by reading the analog voltage on the PGOOD pin configured as AMUX

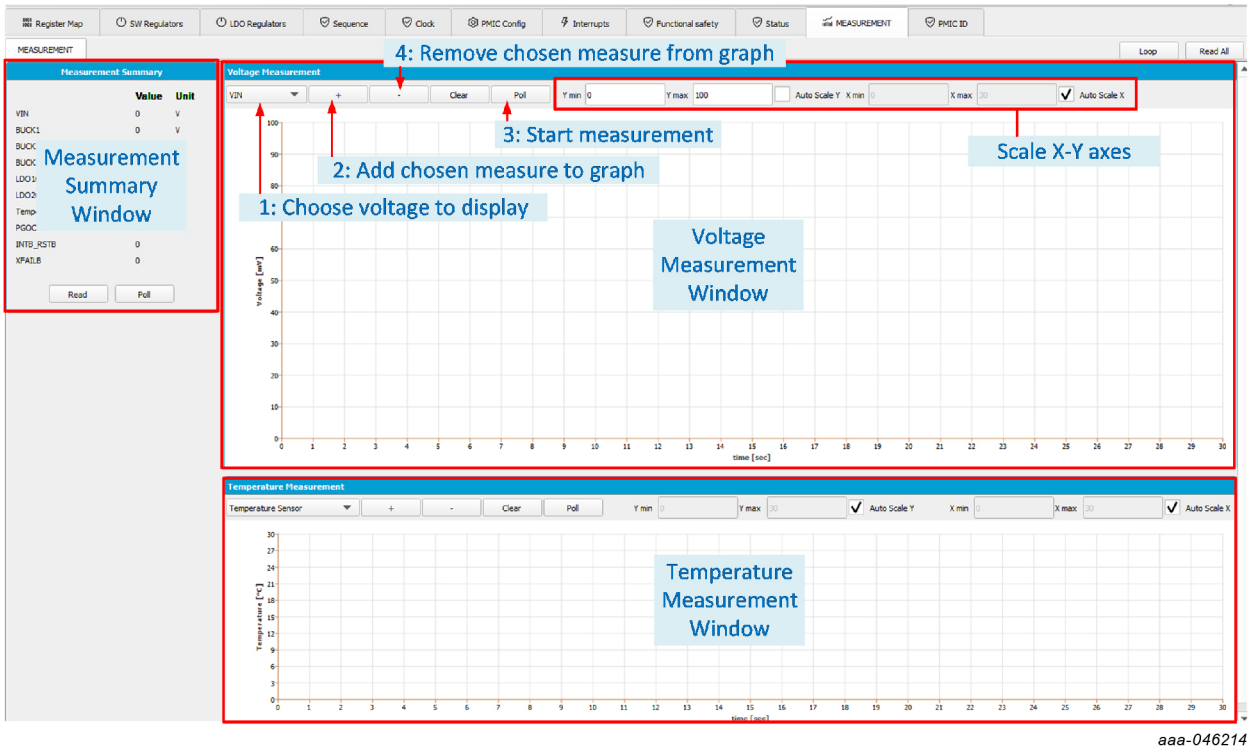


Figure 83. Register map menu Measurement

The Measurement tab panel contains three sections:

- **Measurement Summary:** Reads the current value of the functions being monitored
- **Voltage Measurement:** Displays voltage measurement values as a function of time for selected items
  - The menu bar at the top contains a drop-down menu that allows you to select which voltages are to be measured (BUCKs/LDOs)
  - Selecting from the drop-down menu and clicking the + sign causes the selected item to be added to the chart. The menu bar also allows a user to determine how to scale the x and y axes
- **Temperature Measurement:** Displays the temperature measurement as a function of time. The menu bar contains a drop-down menu that shows the sensor status.
  - The + sign adds the sensor to the graph. As with the Voltage Measurement graph, the menu bar also allows the user to determine how to scale the x and y axes.
  - Clicking on Poll starts the measurement.

PGOOD pin notes

Depending on the user settings, PGOOD pin can be used as:

- GPO (general purpose output)
- PGOOD signal
- Temperature junction analog voltage

Using the PGOOD pin as a GPO requires an external pull-up resistor. However, the junction temperature measurement requires the PGOOD pin not be pulled up. Therefore, using PGOOD as a GPO and using it as a temperature sensor are mutually exclusive.

To enable PGOOD as a GPO, place a jumper on PGOOD_SEL at position 2-3.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

To enable temperature sensor measurement, place a jumper on PGOOD_SEL at position 1-2.

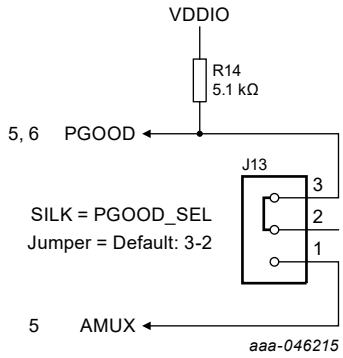


Figure 84. PGOOD pin user settings

7.1.1.11 PMIC ID

The PMIC tab provides basic information regarding the device. It contains three sections:

- **Device ID:** Shows the device family and indicates whether the part is trimmed ASIL B or QM
- **Silicon ID:** Shows the revision level of the silicon layers
- **OTP ID:** Shows the OTP version burned in the part

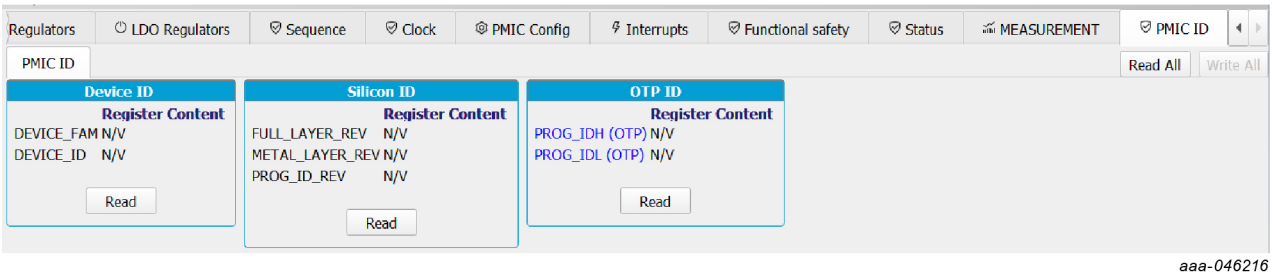


Figure 85. Register map menu PMIC ID

7.2 Script

The Script editor allows the user to create new script sequences or to send existing sequences to the device. The user can read/write individually to a register, to a digital pin, or to an analog pin. The user also can emulate an OTP configuration with this tool. The SCRIPT tool is accessible from Tools access bar.

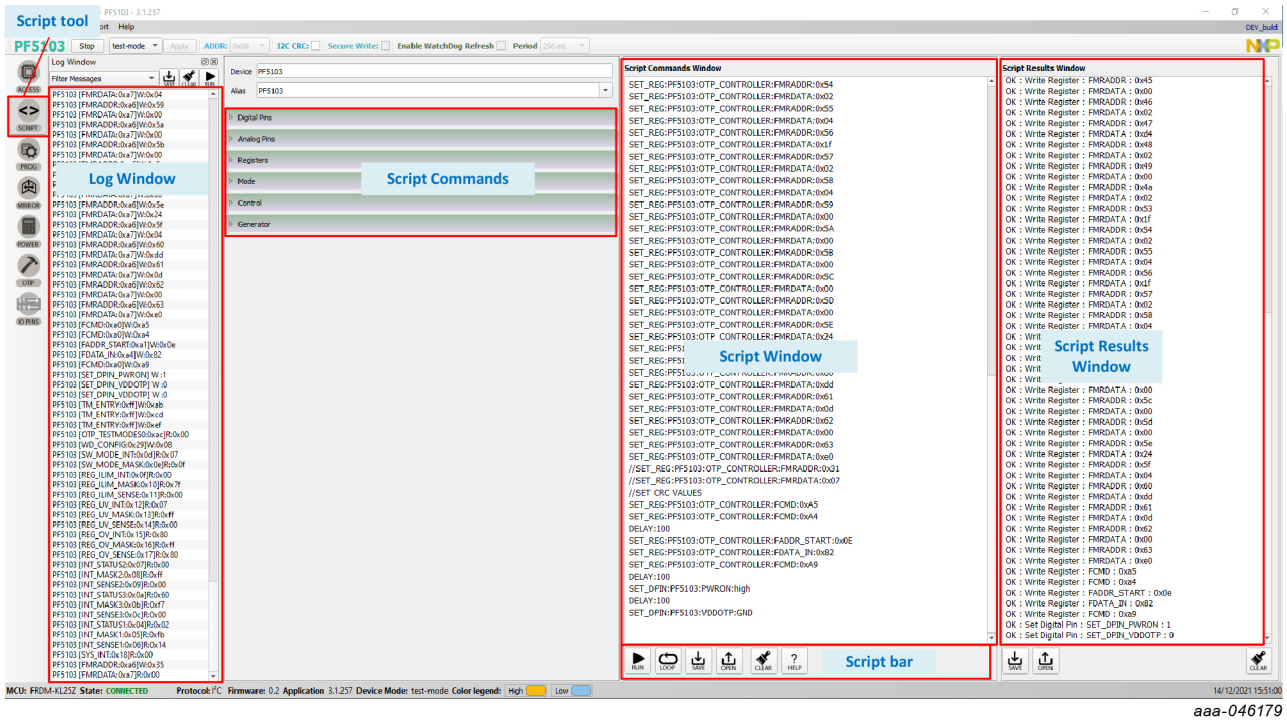
The Script editor window consists of four sections:

- Log Window
- Script Commands
- Script Window
- Script Results Window

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.



aaa-046179

Figure 86. Log Window

Log Window

The Log Window lists events as they occur in real time when the script is executing. The Filter Messages box allows the user to limit log messages to certain events (Register Read, Register Write, Pin Read, Pin Write). The Log Window menu bar also contains buttons for saving the log contents to a file, clearing the log, or running the script in the Script Command window.

Script Commands

The Commands window allows the user to enter commands into the Script Command window by clicking on the appropriate command. This facilitates command entry and ensures that there are no syntax errors in the command. The commands are organized into functional categories in the menu. Opening one of the menu tabs and selecting the desired pin causes the associated command to appear in the Script Command window.



aaa-046180

Figure 87. Commands window

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

- **Digital Pins:** Enters the Script Command to read the value of the selected digital pin
- **Analog Pins:** Enters the Script Command to read the value of the selected analog pin
- **Registers:**Enters the Script Command to read or write to functional and OTP functional registers
- **Mode:** Enters the Script Command to set the desired mode
- **Control:** Enters the Script Command to pause script execution or to delay script execution. By default, 300 ms is entered as the delay value, but this value can be edited in the Script Command window and changed to any ms value. If a Pause command is entered in the Script Command window, execution halts when the Pause command is encountered and a pop-up window appears prompting you to continue execution.
- **Generator:** Clears the content of the Script Command window and enters an OTP script sequence

Note: *Click on Help in the Script bar for further information.*

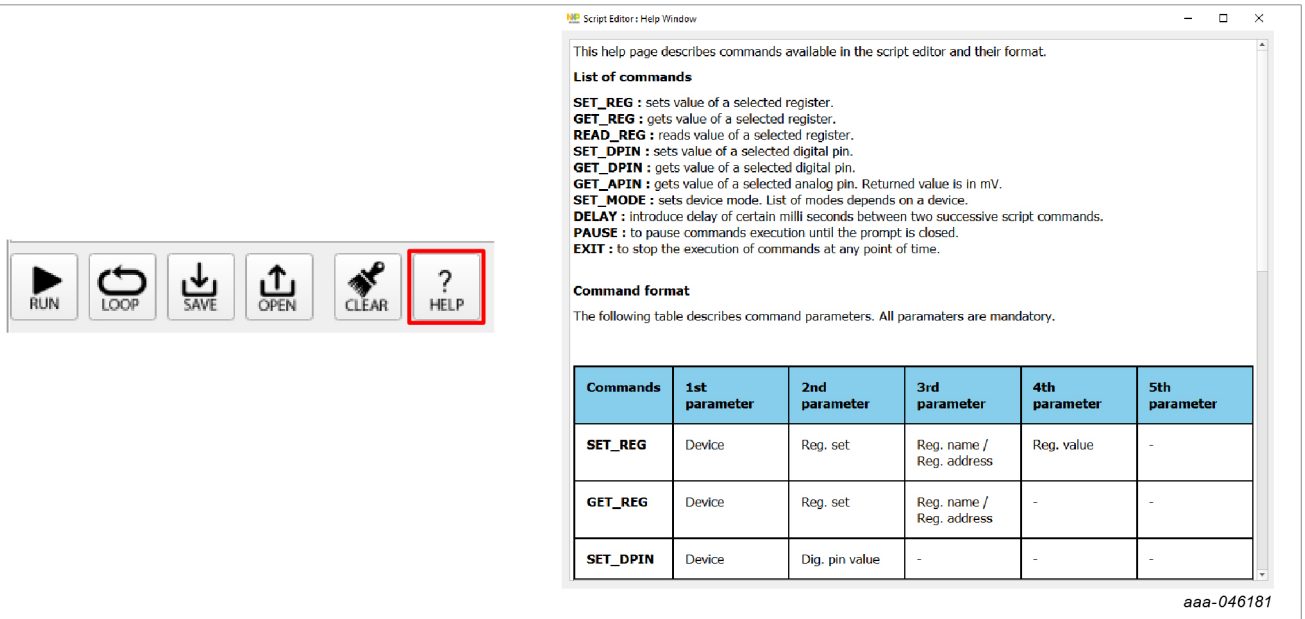


Figure 88. Script bar Help

All menu items work in a similar way. Figure 89 shows a typical process using the Registers menu tab.

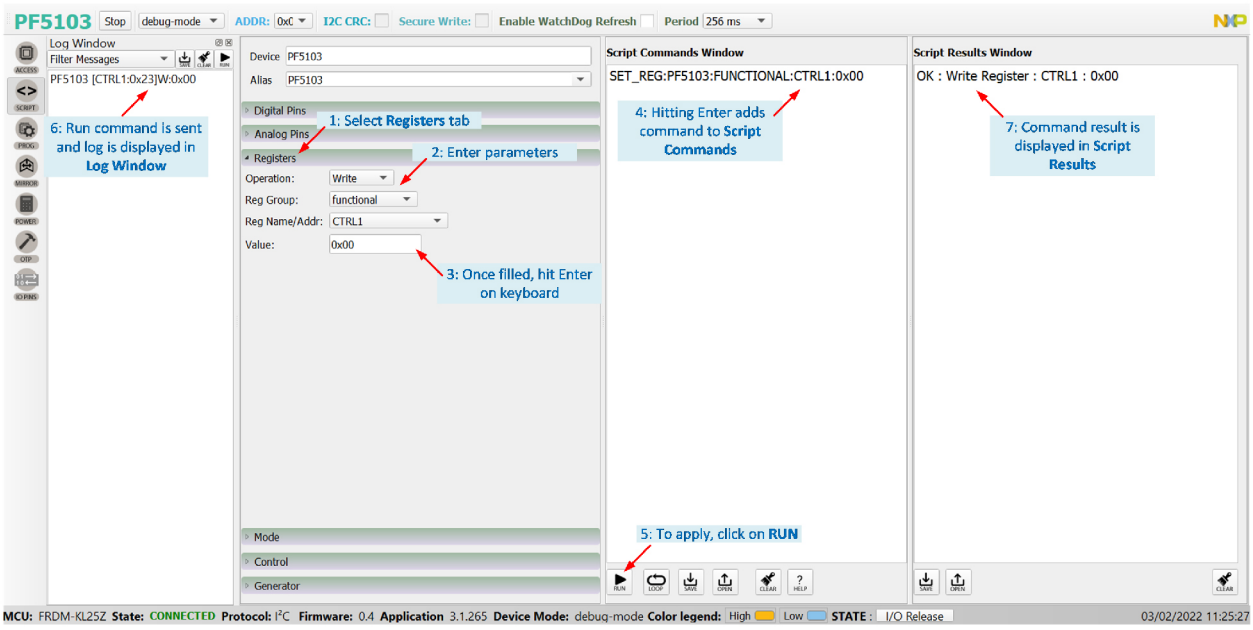
Clicking on the Register tab brings up the parameters panel shown in Figure 89. A Write operation to the CTRL1 register in the functional register group has been selected. The value 0x00 is selected as the value to be written to the register. Hitting Enter with the cursor in the value field enters the well-formed command in the Script Commands window.

To apply the commands on the Script Commands window, click RUN in the Script bar. The sent commands are displayed in the Log window and command results are displayed in the Script Results window.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.



aaa-046182

Figure 89. Using the Registers menu tab

Script Commands window

The Script Commands window is the area where existing script files can be loaded in test mode only and where script commands are entered, edited, and executed. The menu bar at the bottom of the window contains the following six buttons:

- **RUN:** Initiates execution of the script sequence in the Script Command window
- **LOOP:** Executes the script as a loop. Select LOOP, then click RUN
- **SAVE:** Saves the content of the Script Command window as a .txt file that can be subsequently reloaded
- **OPEN:**Clears the current content and loads a previously saved script into the Script Command window
  Note: *The loaded file has to be a TBB file with .txt extension.*
- **CLEAR:** Clears the current content of the Script Command window
- **HELP:** Shows a list of all script editor commands and their command formats



aaa-046183

Figure 90. Script Commands menu bar

Script Results window

The Script Results window displays the results of an executed script. The menu bar at the bottom of the window contains the following three buttons:

- **SAVE:** Saves the content of the Script Results window as .txt file that can be subsequently reloaded
- **OPEN:** Clears the current content and loads a previously saved results file into the Script Results window
- **CLEAR:** Clears the current content of the Script Results window

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.



Figure 91. Script Results menu bar

7.3 Prog

The Prog (programming) tool provides access to device programming configuration and programming tools.

Note: *A device can only be programmed once. Use this tab cautiously.*

The programming tool is available only in test mode.

The programming screen consists of two sections:

- Device Programming Configuration window
- Fuse Box Status window

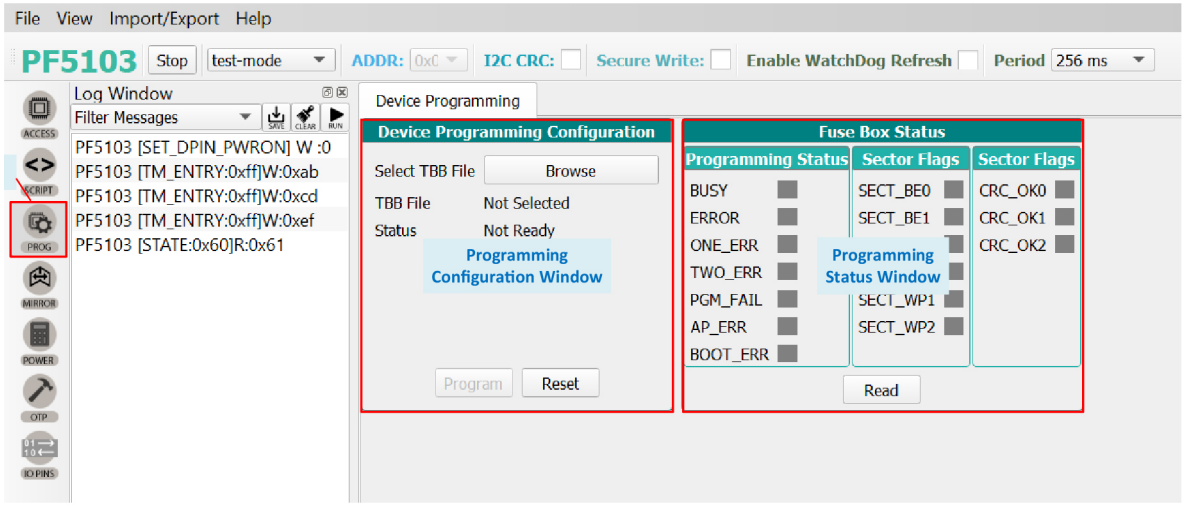


Figure 92. Prog tool

Device Programming Configuration window

This window allows the user to program an OTP operation from a saved TBB file.

To program the part and fuse OTP, see Programming an OTP operation.

7.3.1 Fuse Box Status window

The Fuse Box Status window gives advanced details about OTP fuse.

Some information about the sectors:

- SECT_BE0 / SECT_WP0 is NXP proprietary.
- SECT_BE1 / SECT_WP1 is ASIL/QM level configuration.
- SECT_BE2 / SECT_WP2 is customer OTP configuration as provided in TBB file.

In the indicator boxes, blue indicates low state, orange indicates high state.

Notice that an empty part has the following fuse box status, see Programming an OTP operation:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

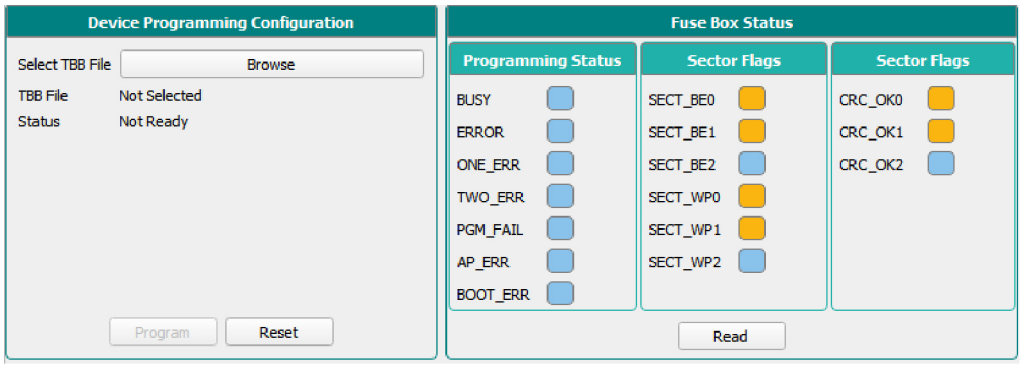


Figure 93. Fuse Box Status window

7.4 Mirror

The Mirror tool provides access to all mirror registers.

Note: *The Mirror tool display tabs are similar to the corresponding OTP tool tab. To avoid confusion, the tab header background colors are different. The Mirror tool tab header is purple. OTP tool tab headers are blue.*

The Mirror tool is available only in test mode. This mode loads required keys in order to have full access to mirror registers. This tool allows the user to:

- Read and write mirror registers values
- Load a TBB file into the Mirror registers and debug the configuration. For further details on TBB file preparation and parameters configuration, see Section 7.6.

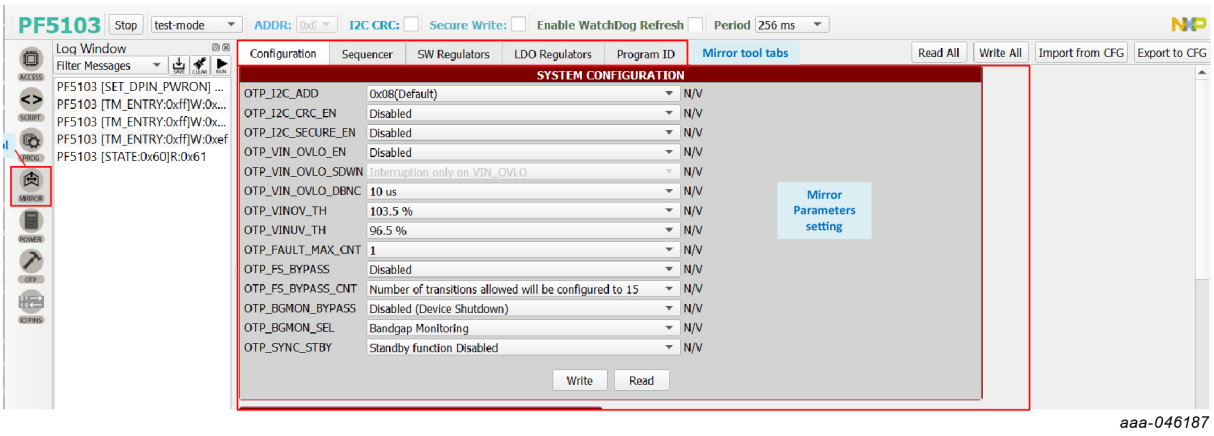


Figure 94. Mirror tool

7.5 Power

The Power tool is not available in this release.

7.6 OTP

The OTP tool allows the user to enter an OTP configuration and save it as a .cfg file. The .cfg file is used by the GUI to log all of the configuration information. A TBB file can be created with a .txt extension. The TBB file can be used either to load the mirror registers in debug mode or to burn OTP fuses using Section 7.3.

The main panel of the OTP tool main panel is divided into the two sections, as shown in :

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

- OTP Parameters setting section
- OTP details section

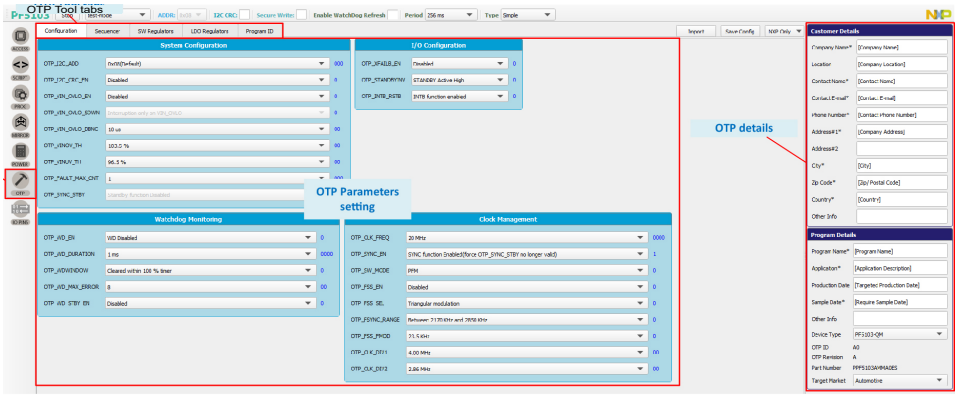


Figure 95. OTP tool

OTP Parameters setting section: This section is organized into five tabs.

Note: *In this section, Configuration tabs differ depending on safety level. Windows are the same for QM and ASIL B parts for all other tabs.*

- **Configuration tab:** Provides a means of setting miscellaneous PF5103 system configuration parameters

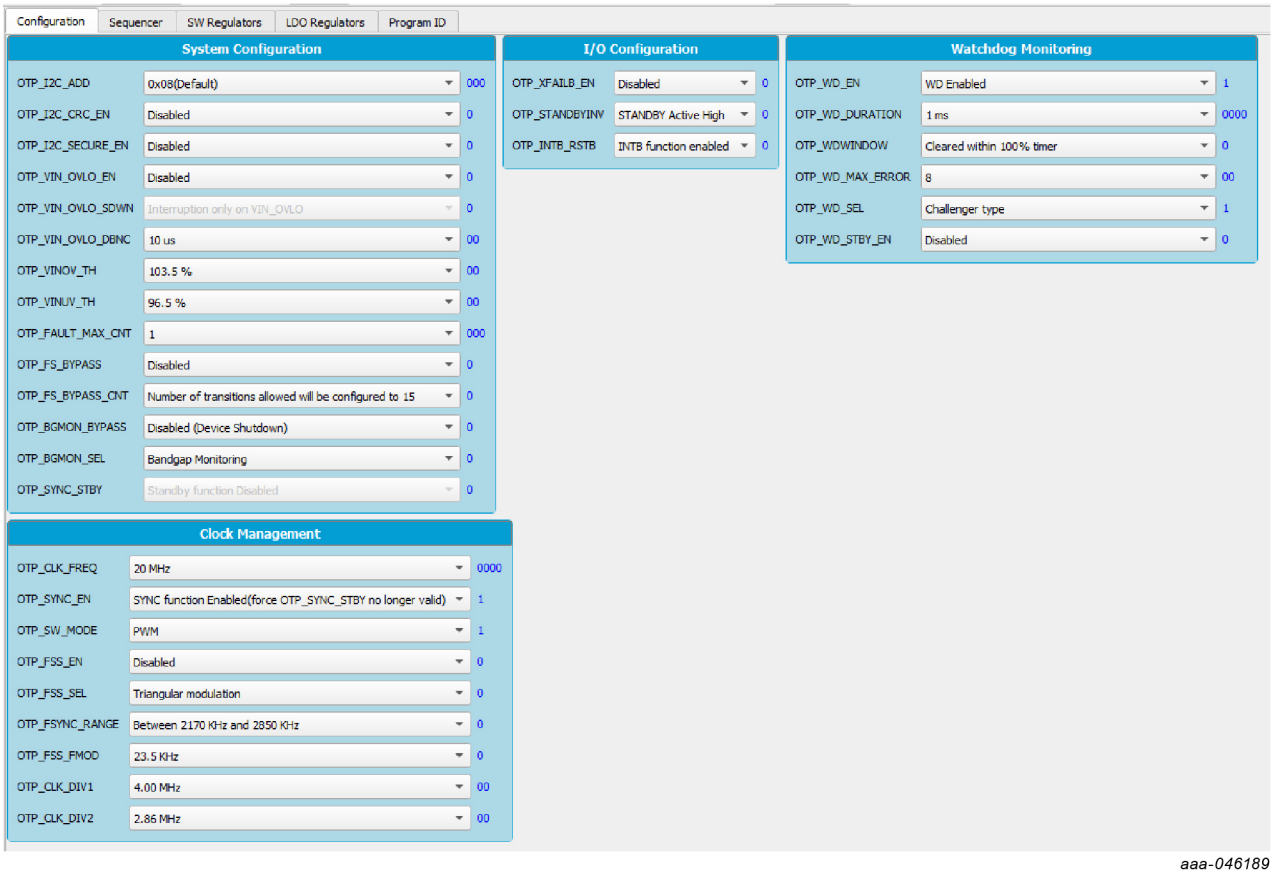


Figure 96. OTP Configuration tab

The system configuration tab displays a different window depending on the device's safety level (QM or ASIL B) selected in the Program Details panel. See Section 7.6.1.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

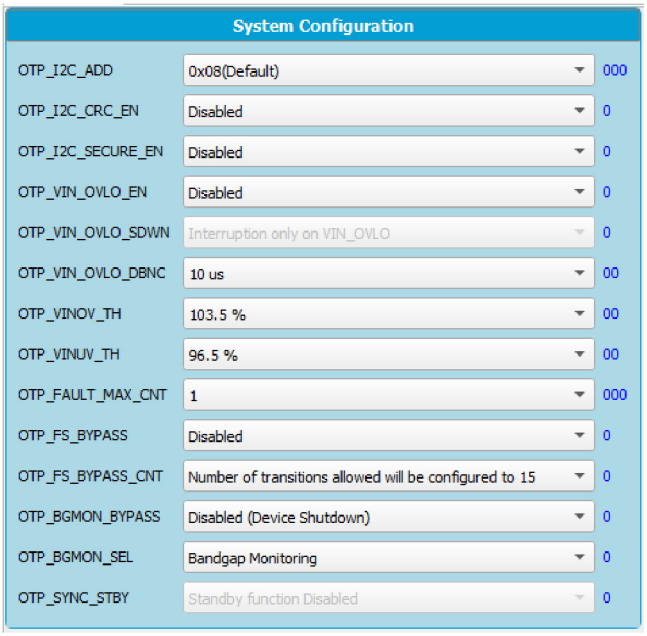


Figure 97. QM System Configuration

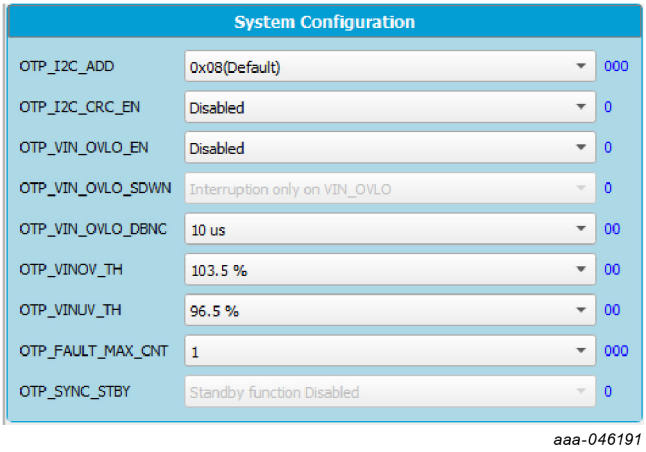


Figure 98. ASIL B System Configuration

- **Sequencer tab:** Allows the user to configure the sequence and slot for power rails and PGOOD pin when used as GPO.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

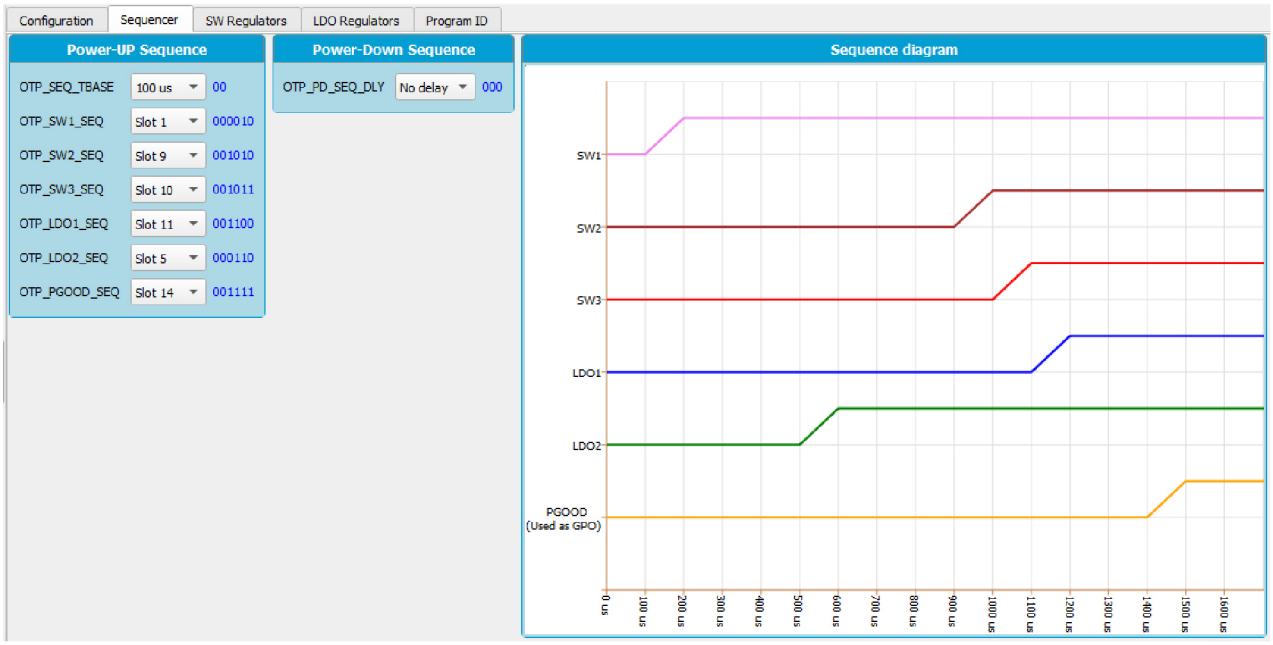


Figure 99. Sequence tab

The Sequence diagram graph displays the power-up sequence.

The x-axis of the Sequence Diagram can be set to:

– **Time mode:** Displays the sequence in increments of time

– **Slot mode:** Displays the sequence in terms of the assigned sequence slots

To change this setting, go to View/OTP sequence diagram mode and select the mode.

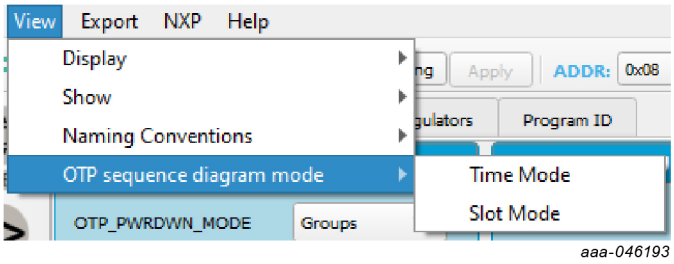


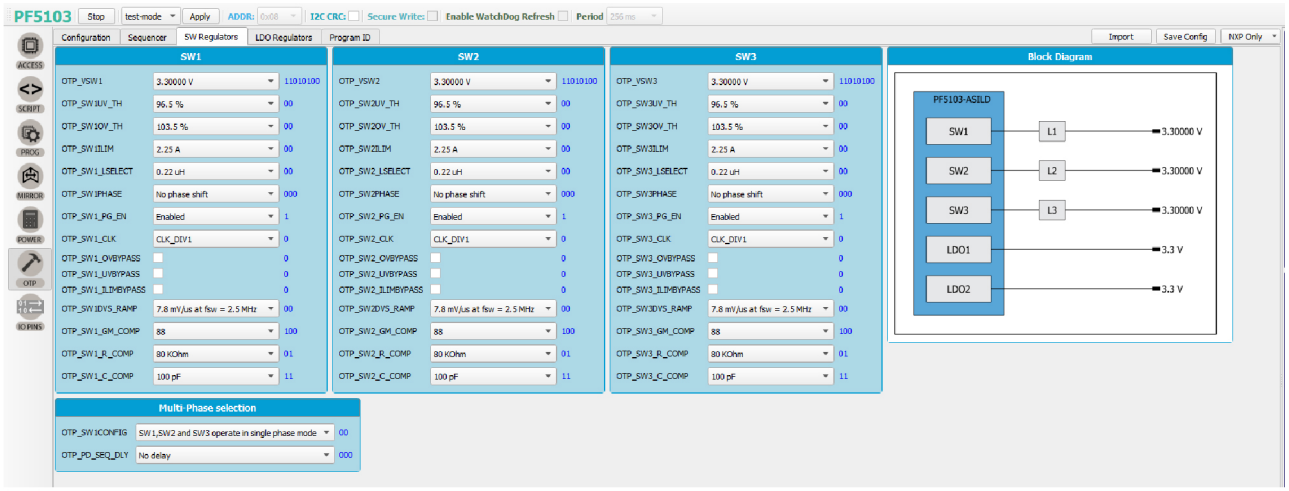
Figure 100. Time Mode/Slot Mode

- **SW Regulators tab:** Allows the user to set OTP parameters for BUCK1 (SW1), BUCK2 (SW2), and BUCK3 (SW3). The multiphase selection window allows SW1, SW2, and SW3 to be configured as single-phase, dual-phase, or triple-phase.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

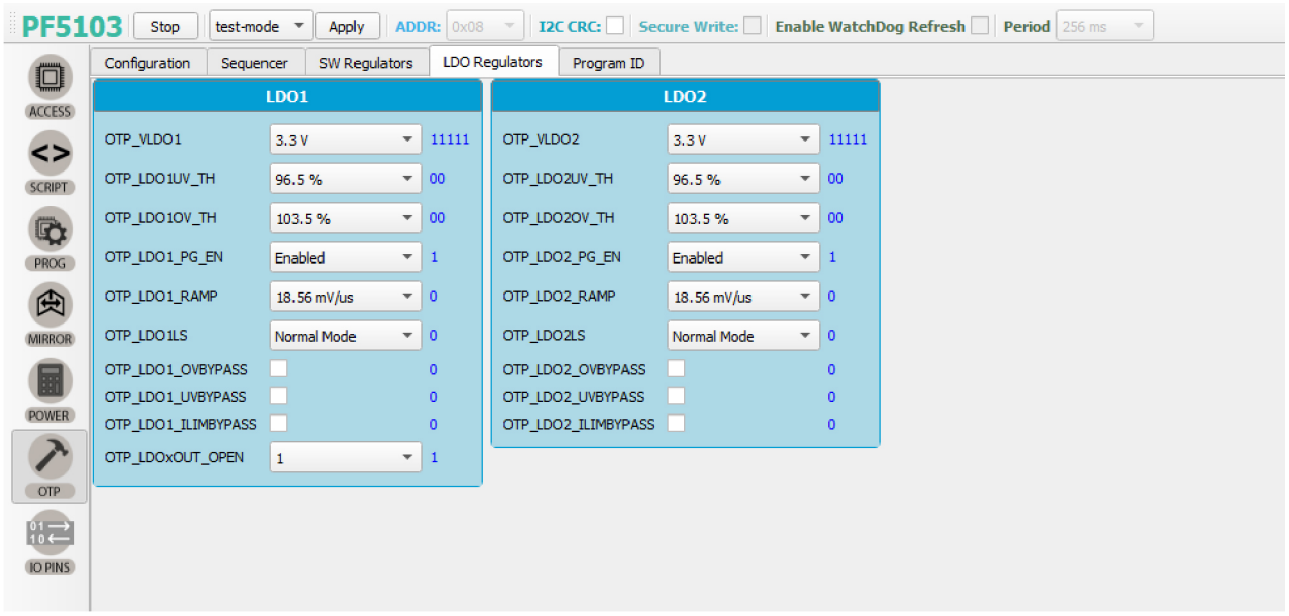
Downloaded from Arrow.com.



aaa-046194

Figure 101. SW Regulators tab

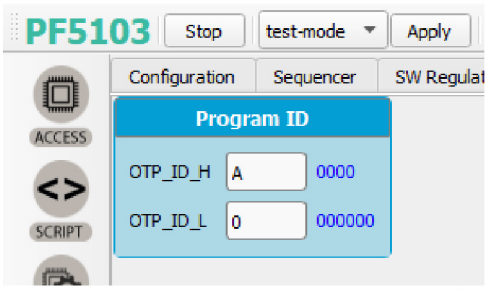
- **LDO Regulators tab:** Allows the user to set OTP parameters for LDO1 and LDO2.



aaa-046195

Figure 102. LDO Regulators tab

- **Program ID tab:** Displays the OTP ID. Only NXP users can create a new OTP ID.



aaa-046196

Figure 103. Program ID tab

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

7.6.1 OTP Details

The OTP Details section: Collects and stores information about the customer and OTP version. All the information entered in this section will be part of the CFG and TBB files.

This section has two windows:

- Customer Details window
- Program Details window

Customer Details window

This window collects and displays customer contact information.

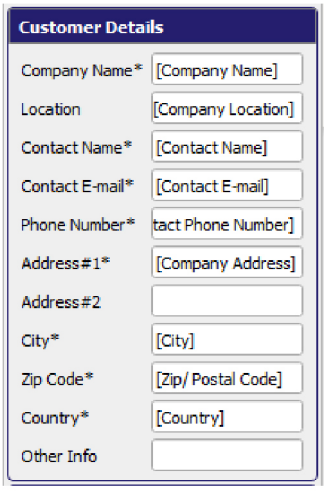


Figure 104. Customer Details

Program Details window

In addition to comments related to the application, this window allows a user to:

- Select device type. See Figure 96 for details.
- Display the OTP ID. (Set by NXP only).
- Display the build part number. (Set by NXP only).
- Select target market, either automotive or industrial.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

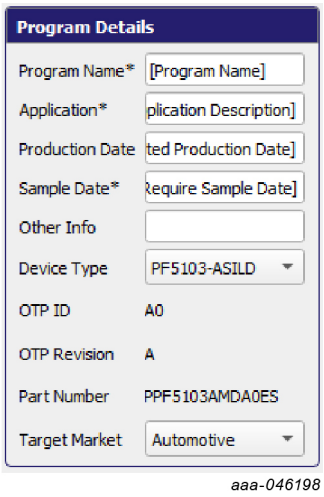


Figure 105. Program Details

7.7 I/O Pins

The I/O Pins tool provides a means of reading and setting the PF5103 I/O pins (PGOOD, INTB_RSTB, PWRON, SYNC)

The I/O Pins panel consists of three sections:

- **Log Window:** Maintains a running log of events initiated during the current session. A drop-down menu in the upper left allows the log to be filtered by register read, register write, pin read, and pin write. Buttons in the upper right allow the Log Window contents to be saved, cleared, or run.
- **Pins Polling Window:** Allows the listed pins to be read or polled during a selected time duration. In the indicator boxes, blue indicates low state, orange indicates high state.
  Note: *The displayed logical level is the last one sent to the device and not an actual sense of the pins.*
- **Pins Setting Window:** Allows the PWRON and VDDOTP pins to be set. In the indicator boxes, blue indicates low state, orange indicates high state. VDDOTP can be set either to GND, 5 V or 8 V.

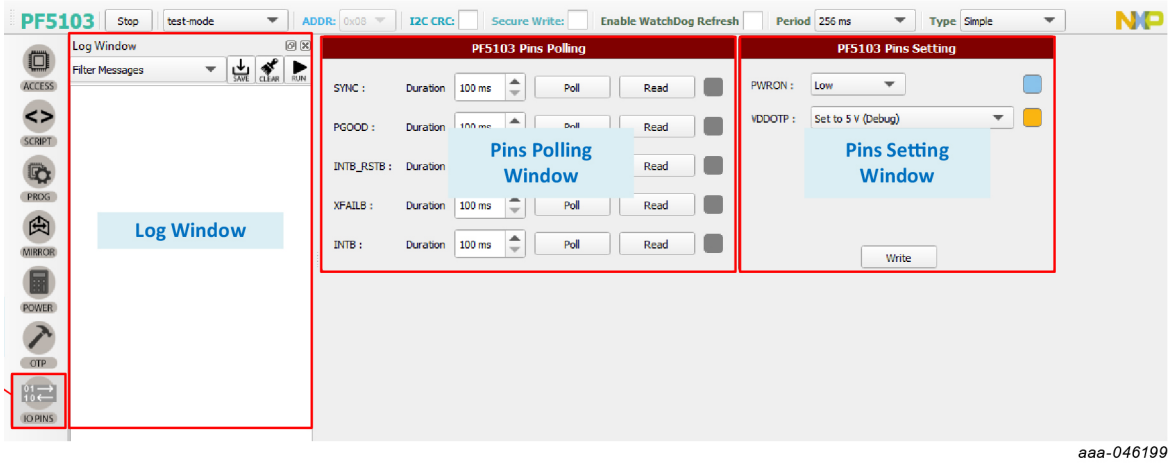


Figure 106. IO Pins tool

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

8 Abbreviations

Table 16. Abbreviations

Acronym	Description
ESD	Electrostatic discharge
GPO	General purpose output
GUI	Graphical user interface
I/O	Input/output
MCU	Microcontroller unit
OTP	One time programmable
PMIC	Power management integrated circuit
SMPS	Switch mode power supplies
SPI	Serial peripheral interface
TBB	Try before buy
USB	Universal serial bus

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

9 References

[1] **Data sheet**: PF5103 - Power management integrated circuit (PMIC) for high performance applications
http://www.nxp.com/KITPF5103FRDMEVM

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

10 Revision history

Table 17. Revision history

Document ID	Release date	Description
UM11792 v.2.1	06 March 2026	• Updated Figure 1 • Updated Figure 2 • Updated Figure 49
UM11792 v.2.0	06 February 2025	• Changed document status to "Public" from "Confidential" • Global editing for style, clarity, and grammar. • Added Section 2.1 • Updated incorrect reference and added missing figures in Section 6.3.4 • Updated incorrect references to Figure 1 in Section 6.3.4, Section 6.3.5.1, Section 6.3.5.2, and Section 6.3.6 • Updated title of Figure 100 and Figure 105. • Updated Figure 17, and **Note** below. • Section 10 was relocated from the front of this document to the end to conform with NXP's document content hierarchy. • Updated Legal information
UM11792 v. 1.1	4 November 2024	• Global: removed references to ASIL D • Updated Figure 29 • In Section 9, corrected title of PF5103 data sheet • Updated legal information
UM11792 v.1	23 May 2022	Initial version

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Hazardous voltage — Although basic supply voltages of the product may be much lower, circuit voltages up to 60 V may appear when operating this product, depending on settings and application. Customers incorporating or otherwise using these products in applications where such high voltages may appear during operation, assembly, test etc. of such application, do so at their own risk. Customers agree to fully indemnify NXP Semiconductors for any damages resulting from or in connection with such high voltages. Furthermore, customers are drawn to safety standards (IEC 950, EN 60 950, CENELEC, ISO, etc.) and other (legal) requirements applying to such high voltages.

AEC unqualified products — This product has not been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and should not be used in automotive applications, including but not limited to applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This evaluation product is intended solely for technically qualified professionals, specifically for use in research and development environments to facilitate evaluation purposes. It is not a finished product, nor is it intended to be a part of a finished product. Any software or software tools provided with an evaluation product are subject to the applicable license terms that accompany such software or software tools.

This evaluation product is provided on an "as is" and "with all faults" basis for evaluation purposes only and is not to be used for product qualification or production. If you choose to use these evaluation products, you do so at your risk and hereby agree to release, defend and indemnify NXP (and all of its affiliates) for any claims or damages resulting from your use. NXP, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this evaluation product remains with user.

In no event shall NXP, its affiliates or their suppliers be liable to user for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the evaluation product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that user might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP, its affiliates and their suppliers and user's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by user based on reasonable reliance up to the greater of the amount actually paid by user for the evaluation product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose and shall not apply in case of willful misconduct.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits.

The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

No (implied) license Car Connectivity Consortium IP — You are hereby informed that the sale, license and distribution of this NXP hardware and/or NXP software does not imply any licenses with respect to intellectual property rights of any third party, including, but not limited Essential Patents, in relation to the Car Connectivity Consortium ("CCC") and you need to obtain separate licenses in this respect. For the purpose of this section "Essential Patent" means a patent to the limited extent that infringement of such patent cannot be avoided in remaining compliant with the technology standards implicated by the usage of any of the NXP hardware and/or NXP software, including optional implementation of such standards, on technical but not commercial grounds, taking into account normal technical practice and the state of the art generally available at the time of standardization.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Tables

Tab. 1. Jumper or switches functions 6
Tab. 2. VIN connector (J4) 7
Tab. 3. BUCK1, BUCK2 and BUCK3 connectors 7
Tab. 4. LDO1 and LDO2 connectors 8
Tab. 5. PWRON_SEL Jumper (J2) 9
Tab. 6. USB_5V_TO_VIN jumper (J26) 10
Tab. 7. VDDIO_SEL jumper (J30) 10
Tab. 8. VDDIO_EN jumper (J29) 10
Tab. 9. PGOOD_SEL jumper (J13) 10
Tab. 10. VDDOTP_8V_CTL jumper (J27) 10
Tab. 11. VDDOTP_5V_CTL jumper (J28) 11
Tab. 12. XFAILB_FCCU_PU jumper (J32) 11
Tab. 13. PWRON_SEL switch (SW1) 11
Tab. 14. Regulators settings 38
Tab. 15. Example TBB script 38
Tab. 16. Abbreviations 62
Tab. 17. Revision history 64

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Figures

Fig. 1. Board image with callouts 6
Fig. 2. Test points 9
Fig. 3. Monitoring headers (J33 and J34) 12
Fig. 4. Bootloader – FRDM-KL25Z firmware – Windows 7 13
Fig. 5. Locate debug for FRDM-KL25Z 13
Fig. 6. Disabling storage services 14
Fig. 7. Bootloader – FRDM-KL25Z firmware – Windows 10 14
Fig. 8. Locate debug for FRDM-KL25Z 14
Fig. 9. Open NXP GUI package 15
Fig. 10. Launch NXP_GUI setup 15
Fig. 11. Initial application setup window 15
Fig. 12. License Agreement window 16
Fig. 13. Choose Components window 16
Fig. 14. Choose Install Location window 17
Fig. 15. Completing setup window 17
Fig. 16. NXPGUI app 18
Fig. 17. Kit selection window 18
Fig. 18. Framework window 19
Fig. 19. Framework bar 19
Fig. 20. Framework settings 20
Fig. 21. GUI Kit selection display settings 20
Fig. 22. GUI kit display 21
Fig. 23. GUI kit Show view 21
Fig. 24. GUI kit Show View Enabled and Disabled 21
Fig. 25. GUI kit View Naming conventions 22
Fig. 26. GUI kit View OTP sequence diagram mode 22
Fig. 27. GUI kit Import/Export 22
Fig. 28. GUI kit Import/Export HEX 23
Fig. 29. GUI kit Import/Export Default CFG 23
Fig. 30. GUI kit Help 23
Fig. 31. Set watchdog type 24
Fig. 32. GUI kit Device Manager bar 24
Fig. 33. PF5103 no start no user-mode 24
Fig. 34. Device connection State: Not detected 24
Fig. 35. Device connection Start 24
Fig. 36. Device connection State: Disconnected 24
Fig. 37. Device connection State: Connected 25
Fig. 38. I²C address selection 25
Fig. 39. I²C CRC enablement notification 25
Fig. 40. I²C test-mode 25
Fig. 41. Warning I2C_CRC is not enabled 26
Fig. 42. I²C Secure Write enabled by OTP 26
Fig. 43. I²C Secure Write enabled check Secure Write box 26
Fig. 44. I²C Secure Write not enabled warning 27
Fig. 45. Watchdog default configuration window 27
Fig. 46. Watchdog configuration bar 28
Fig. 47. Watchdog configuration bar WD Refresh 28
Fig. 48. Watchdog configuration bar WD Refresh Disabled 28
Fig. 49. KITPF5103FRDMEVM board setup 29
Fig. 50. State: Disconnected 30
Fig. 51. State: Not detected 30
Fig. 52. Connected 30
Fig. 53. GUI using Mode selection debug-mode 31
Fig. 54. GUI using I/O Pins debug-mode 31
Fig. 55. Open 32
Fig. 56. Run 32
Fig. 57. Test-mode mirror configuration 33
Fig. 58. GUI using Mode selection normal-mode 33
Fig. 59. GUI using I/O pins 34
Fig. 60. Generate TBB script 34
Fig. 61. Export OTP to TBB script window 35
Fig. 62. Export OTP to TBB script destination 35
Fig. 63. Programming an OTP operation Fuse Box Status 36
Fig. 64. Load TBB file 36
Fig. 65. OTP programming 37
Fig. 66. Configuration for PF5103 38
Fig. 67. Framework window tools bar 41
Fig. 68. Access tool 41
Fig. 69. Framework window tools bar tab content 42
Fig. 70. Register map menu 42
Fig. 71. Register map menu Read Only registers 43
Fig. 72. Register map menu Read and Write registers 43
Fig. 73. Register map menu Fault Counters 43
Fig. 74. CTRL1 Bit-Map Dialog 44
Fig. 75. Register map menu SW Regulators 44
Fig. 76. Register map menu LDO Regulators 45
Fig. 77. Register map menu Sequence 45
Fig. 78. Register map menu Clock - Clock Management 46
Fig. 79. Register map menu PMIC Config 47
Fig. 80. Register map menu Interrupts 47
Fig. 81. Register map menu Functional Safety 48
Fig. 82. Register map menu Status 48
Fig. 83. Register map menu Measurement 49
Fig. 84. PGOOD pin user settings 50
Fig. 85. Register map menu PMIC ID 50
Fig. 86. Log Window 51
Fig. 87. Commands window 51
Fig. 88. Script bar Help 52
Fig. 89. Using the Registers menu tab 53
Fig. 90. Script Commands menu bar 53
Fig. 91. Script Results menu bar 54
Fig. 92. Prog tool 54
Fig. 93. Fuse Box Status window 55
Fig. 94. Mirror tool 55
Fig. 95. OTP tool 56
Fig. 96. OTP Configuration tab 56
Fig. 97. QM System Configuration 57
Fig. 98. ASIL B System Configuration 57
Fig. 99. Sequence tab 58
Fig. 100. Time Mode/Slot Mode 58
Fig. 101. SW Regulators tab 59
Fig. 102. LDO Regulators tab 59
Fig. 103. Program ID tab 59
Fig. 104. Customer Details 60
Fig. 105. Program Details 61

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Fig. 106. IO Pins tool 61

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Downloaded from Arrow.com.

Contents

1 Introduction 2
2 Finding kit resources and information on the NXP web site 3
2.1 Collaborate with the NXP community 3
3 Getting ready 4
3.1 Kit contents 4
3.2 Additional hardware 4
3.3 Assumptions 4
3.4 Static handling requirements 4
3.5 Minimum system requirements 4
3.6 Software 4
4 Getting to know the hardware 5
4.1 Kit overview 5
4.2 Board features 5
4.3 Block diagram 5
4.4 Kit featured components 6
4.4.1 Connectors 7
4.4.1.1 VIN connectors 7
4.4.1.2 BUCK1, BUCK2, and BUCK3 connectors 7
4.4.1.3 LDO1 and LDO2 connectors 8
4.4.2 Test points 8
4.4.3 Jumpers 9
4.4.3.1 PWRON_SEL Jumper (J2) 9
4.4.3.2 USB_5V_TO_VIN Jumper (J26) 10
4.4.3.3 VDDIO_SEL Jumper (J30) 10
4.4.3.4 VDDIO_EN Jumper (J29) 10
4.4.3.5 PGOOD_SEL Jumper (J13) 10
4.4.3.6 VDDOTP_8V_CTL Jumper (J27) 10
4.4.3.7 VDDOTP_5V_CTL Jumper (J28) 11
4.4.3.8 XFAILB_FCCU_PU Jumper (J32) 11
4.4.4 LED 11
4.4.5 Switches 11
4.4.5.1 PWRON_SW (SW1) 11
4.4.6 Monitoring headers (J33 and J34) 11
4.5 Schematic, board layout and bill of materials 12
5 Installing and configuring software tools 13
5.1 Flashing the FRDM-KL25Z firmware – Windows 7 13
5.2 Flashing the FRDM-KL25Z firmware – Windows 10 13
5.3 Flashing or updating the GUI firmware 14
5.4 PF51 NXP GUI 15
5.4.1 Installing the GUI software package 15
5.4.2 Launching the PF51 NXP GUI 17
5.4.3 The Framework window 19
5.4.3.1 Framework settings 20
5.4.4 Device manager 23
5.4.4.1 Device connection 24
5.4.4.2 I2C address selection 25
5.4.4.3 I2C CRC enablement 25
5.4.4.4 Secure Write mode enablement 26
5.4.4.5 Watchdog management 27
6 Configuring the hardware 29
6.1 Setting up the KITPF5103FRDMEVM 29
6.2 Connecting the KITPF5103FRDMEVM to the GUI 29
6.3 Operation modes 30
6.3.1 Debug mode 30
6.3.2 Test mode 30
6.3.3 Normal mode 30
6.3.4 Debug-mode operation 31
6.3.5 Test-mode operation 32
6.3.5.1 Modify mirror registers with a TBB Script 32
6.3.5.2 Modify Mirror with the Mirror tool 32
6.3.6 Normal-mode operation 33
6.4 Generate a TBB script 34
6.5 Programming an OTP operation 35
6.6 TBB script example 37
7 Using the Tools access bar 41
7.1 Access 41
7.1.1 Tab content 41
7.1.1.1 Register Map 42
7.1.1.2 SW Regulators 44
7.1.1.3 LDO Regulators 45
7.1.1.4 Sequence 45
7.1.1.5 Clock 46
7.1.1.6 PMIC Config 46
7.1.1.7 Interrupts 47
7.1.1.8 Functional safety 48
7.1.1.9 Status 48
7.1.1.10 Measurement 48
7.1.1.11 PMIC ID 50
7.2 Script 50
7.3 Prog 54
7.3.1 Fuse Box Status window 54
7.4 Mirror 55
7.5 Power 55
7.6 OTP 55
7.6.1 OTP Details 60
7.7 I/O Pins 61
8 Abbreviations 62
9 References 63
10 Revision history 64
Legal information 65

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. **All rights reserved.**

Downloaded from Arrow.com.