3.3 V ECL 2:1 Multiplexer

Description

The MC100LVEL58 is a 2:1 multiplexer. The device is pin and functionally equivalent to the EL58 and works from a 3.3 V supply. With AC performance similar to the EL58 device, the LVEL58 is ideal for low voltage applications which require the ultimate in AC performance.

Features

- 440 ps Typical Propagation Delays
- ESD Protection: > 4 kV Human Body Model,
 > 200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level
 - ◆ Level 1 for SOIC-8 NB
 - ◆ Level 3 for TSSOP-8
 - For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 93 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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SOIC-8 NB D SUFFIX CASE 751



TSSOP-8 DT SUFFIX CASE 948R

MARKINGDIAGRAMS*



SOIC-8 NB



A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note <u>AND8002/D</u>.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVEL58DG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC100LVEL58DTG	TSSOP-8 (Pb-Free)	100 Units/Tube
MC100LVEL58DTR2G	TSSOP-8 (Pb-Free)	2500/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

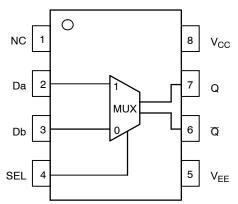


Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Da, Db	ECL Data Inputs
Q, Q	ECL Differential Data Outputs
SEL	ECL Select Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply
NC	No Connect

Table 2. TRUTH TABLE

SEL	Data
H	a
L	b

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	٧
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8 to 0	٧
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$\begin{array}{c} V_I \leq V_{CC} \\ V_I \geq V_{EE} \end{array}$	6 to 0 -6 to 0	V
l _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
$\theta_{\sf JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
θЈС	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44 ± 5%	°C/W
θJA	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8	185 140	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

			-40°C		25°C		85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		21	28		21	28		23	30	mA
V _{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V _{OL}	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V _{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary ± 0.3 V.
- 2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.

Table 5. LVNECL DC CHARACTERISTICS ($V_{CC} = 0.0 \text{ V}$; $V_{EE} = -3.3 \text{ V}$ (Note 1))

		-40°C		25°C		85°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		21	28		21	28		23	30	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with $V_{CC}.\ V_{EE}$ can vary $\pm 0.3\ V.$
- 2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.

Table 6. AC CHARACTERISTICS ($V_{CC} = 3.3 \text{ V}$; $V_{EE} = 0.0 \text{ V}$ or $V_{CC} = 0.0 \text{ V}$; $V_{EE} = -3.3 \text{ V}$ (Note 1))

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t _{PLH} t _{PHL}	Propagation D to Q Delay SEL to Q	340 350	435 455	560 570	350 360	440 460	570 580	370 380	450 470	590 600	ps
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	100		320	100		320	100		320	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{EE} can vary ±0.3 V.

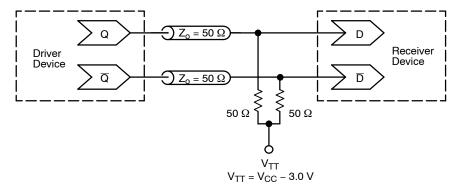


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AND8001/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

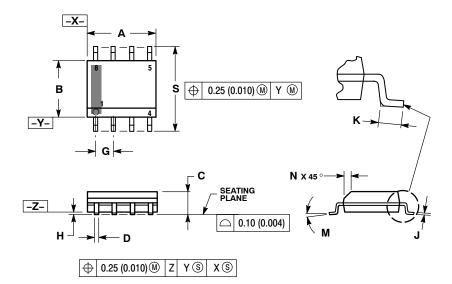
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 **ISSUE AK**

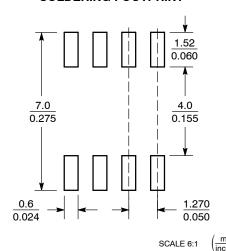


NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE
 MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
 PER SIDE.
- PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL
 IN EXCESS OF THE D DIMENSION AT
 MAXIMUM MATERIAL CONDITION.
 751-01 THRU 751-06 ARE OBSOLETE. NEW
 STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
M	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

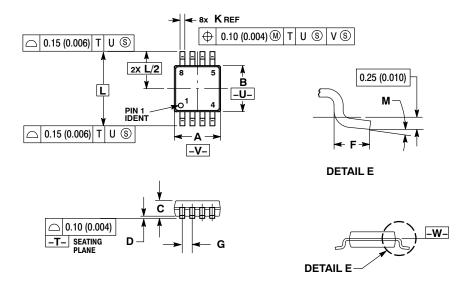
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, <u>SOLDERRM/D</u>.

PACKAGE DIMENSIONS

TSSOP-8 CASE948R-02 ISSUE A



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION B DOES NOT INCLUDE
- DÍMENSÍON B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.90	3.10	0.114	0.122	
В	2.90	3.10	0.114	0.122	
С	0.80	1.10	0.031	0.043	
D	0.05	0.15	0.002	0.006	
F	0.40	0.70	0.016	0.028	
G	0.65	BSC	0.026	BSC	
K	0.25	0.40	0.010	0.016	
L	4.90	4.90 BSC		BSC	
M	0 °	6 °	0 °	6°	

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