7-Stage Ripple Counter

MC14024B



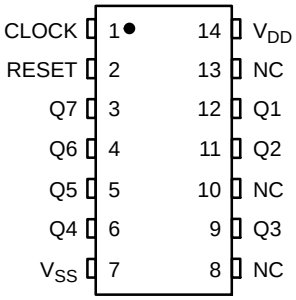
SOIC-14
D SUFFIX
CASE 751A

The MC14024B is a 7-stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

Features

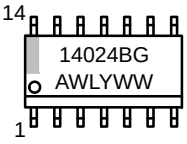
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

PIN ASSIGNMENT



V_{DD} = PIN 14
V_{SS} = PIN 7
NC = NO CONNECTION

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65 °C To 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

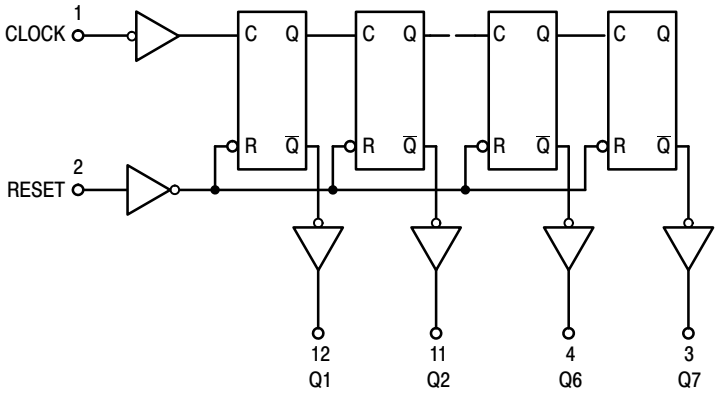
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TRUTH TABLE

Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⎍	0	No Change
⎍	1	All Outputs Low
⎎	0	Advance One Count
⎎	1	All Outputs Low

LOGIC DIAGRAM



Q3 = PIN 9
Q4 = PIN 6
Q5 = PIN 5

ORDERING INFORMATION

Device	Package	Shipping†
MC14024BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14024BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14024BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 2)

NLV14024BDG*	SOIC-14 (Pb-Free)	55 Units / Rail

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

2. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55 °C Min	−55 °C Max	25 °C Min	25 °C Typ (Note 3)	25 °C Max	125 °C Min	125 °C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD} “1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 4.5 Vdc) “1” Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	–	–0.51	–0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.6	–	−1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 4 & 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.31 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.60 μA/kHz) f + I_{DD}							
		15	I_T = (1.89 μA/kHz) f + I_{DD}							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25 °C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25 °C)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 7)	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 915 ns		5.0	–	1000	2000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	–	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	–	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	–	ns
		10	165	60	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	600	375	–	ns
		10	350	200	–	
		15	260	150	–	
Reset Removal Time	t_{rem}	5.0	625	250	–	ns
		10	190	75	–	
		15	145	50	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	1.0	s
		10	–	–	8.0	ms
		15	–	–	200	μs
Input Pulse Frequency	f_{cl}	5.0	–	2.5	1.0	MHz
		10	–	8.0	3.0	
		15	–	12	4.0	

6. The formulas given are for the typical characteristics only at 25 °C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

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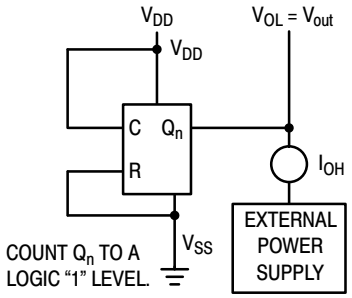


Figure 1. Typical Output Source Characteristics Test Circuit

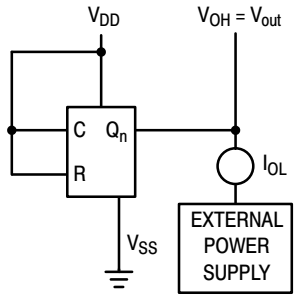


Figure 2. Typical Output Sink Characteristics Test Circuit

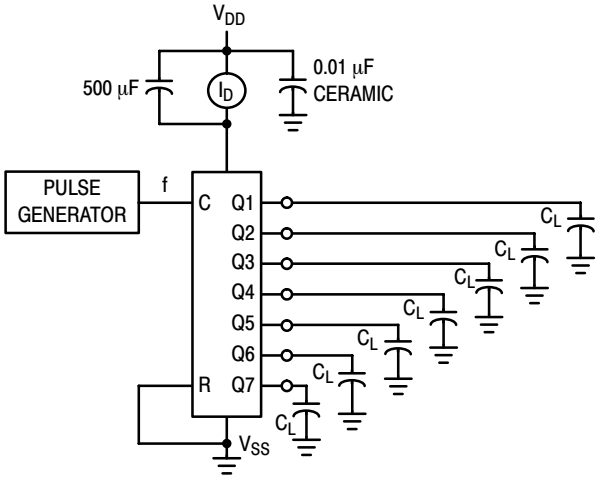


Figure 3. Power Dissipation Test Circuit

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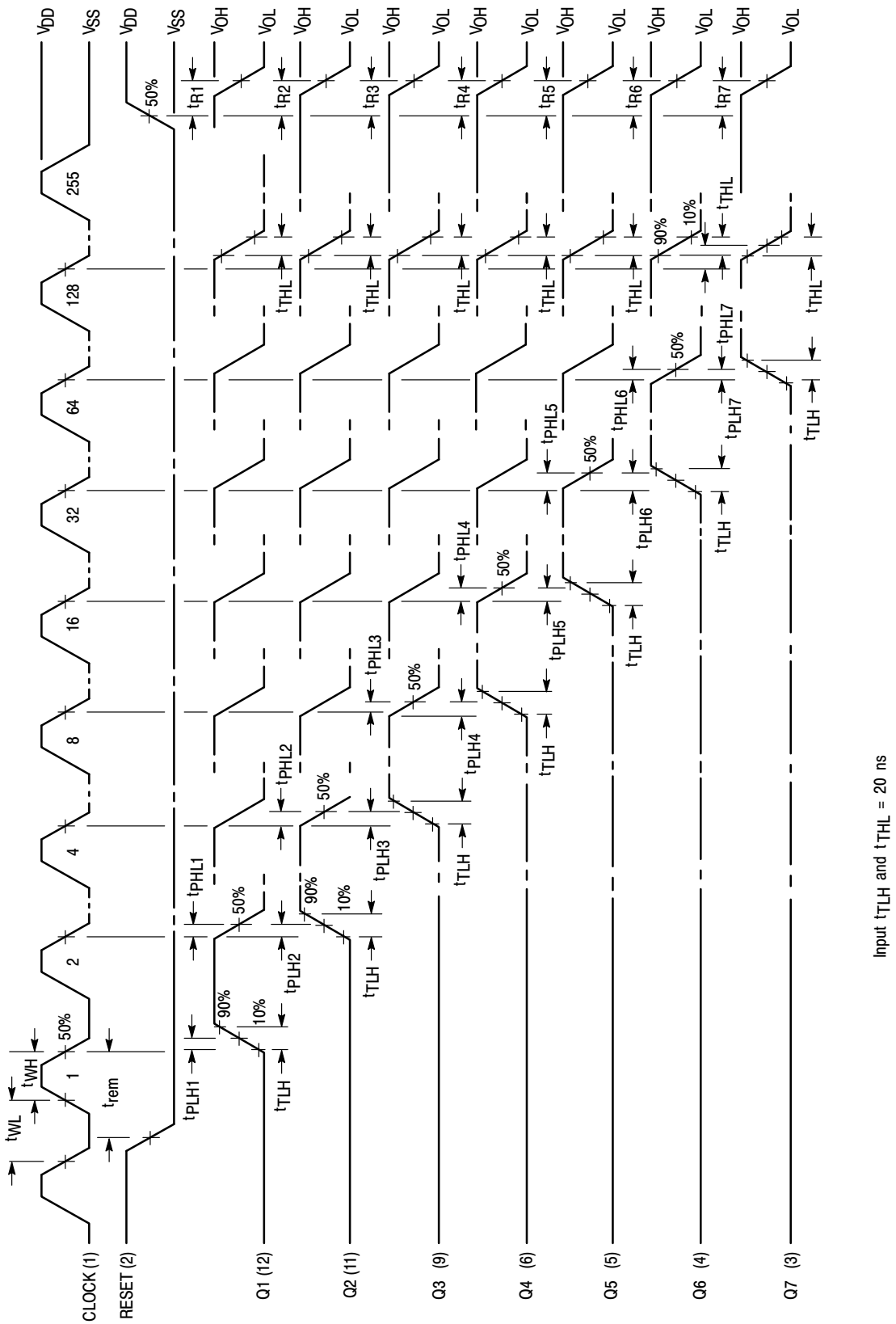


Figure 4. Functional Waveforms

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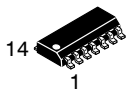
REVISION HISTORY

Revision	Description of Changes	Date
11	Rebranded the Data Sheet to onsemi format. NLV14024BDG OPN Marked as Discontinued.	8/25/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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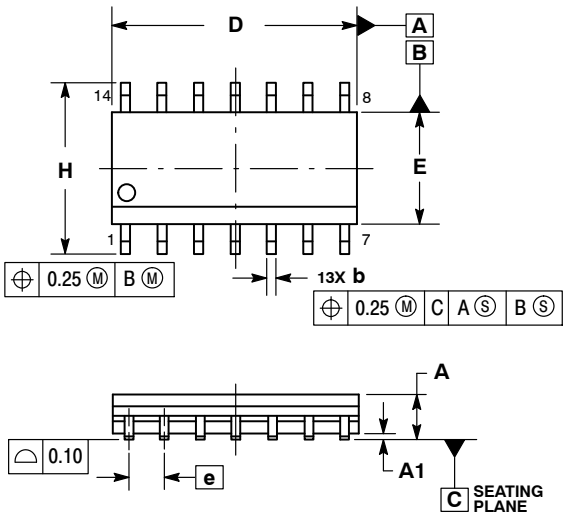
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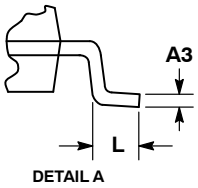


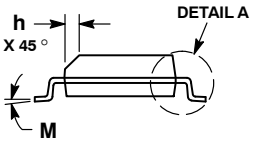
SCALE 1:1

SOIC−14 NB
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ISSUE L

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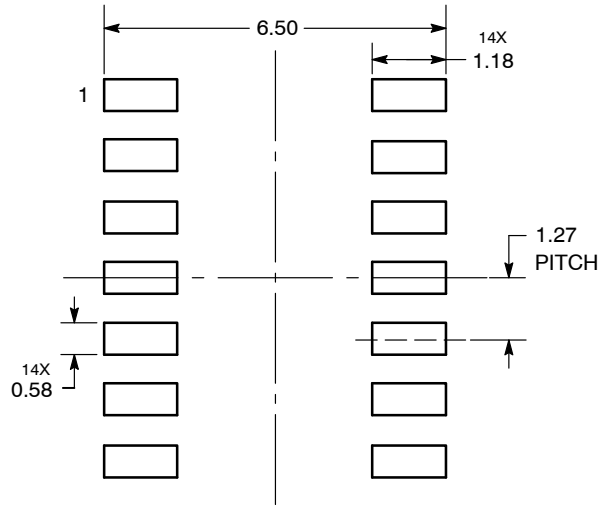




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

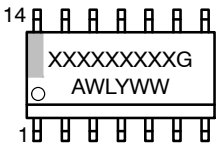
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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