

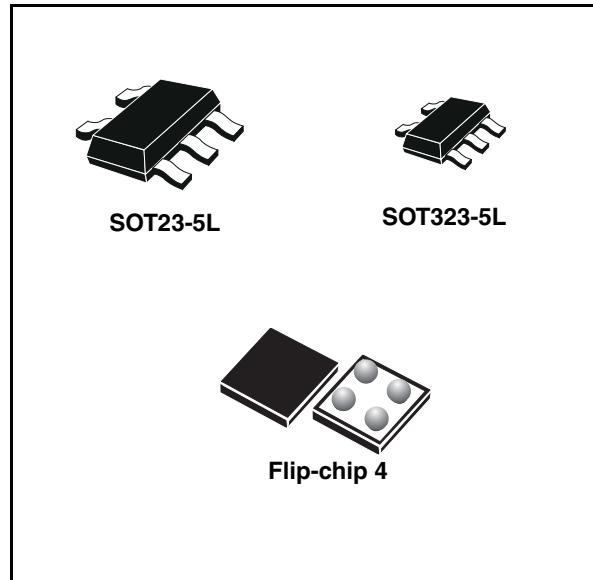
Single buffer/driver with open drain

Features

- 5 V tolerant inputs
- High speed: $t_{PD} = 4.2$ ns (max.) at $V_{CC} = 3.3$ V
- Low power dissipation:
 - $I_{CC} = 1$ μ A (max.) at $T_A = 25$ °C
- Power down protection on inputs and outputs
- Operating voltage range:
 - $V_{CC} (opr) = 1.65$ to 5.5 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance
 - 2000-V human body model (JESD 22 A114-A)
 - 200-V machine model (JESD 22 A115-A)
 - 1000-V charge device model (JESD 22 C101)

Applications

- Mobile phones



Description

The 74LX1G07 is a low voltage CMOS single buffer/driver (open drain) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The internal circuit composed of 2 stages including buffer output, provides high noise immunity and stable output.

Power down protection is provided on input and 0 to 7 V can be accepted on input with no regards to the supply voltage. This device can be used to interface 5 to 3 V.

Table 1. Device summary

Order code	Package	Packaging
74LX1G07STR	SOT23-5L	Tape and reel
74LX1G07CTR	SOT323-5L	Tape and reel
74LX1G07BJR	Flip-chip 4	Tape and reel

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1 Pin connection

Figure 1. Pin connection and IEC symbols

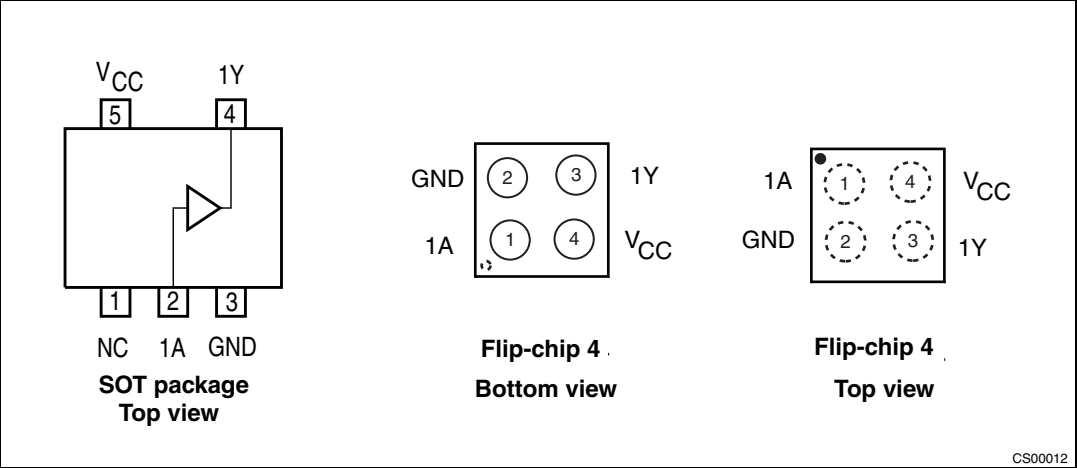


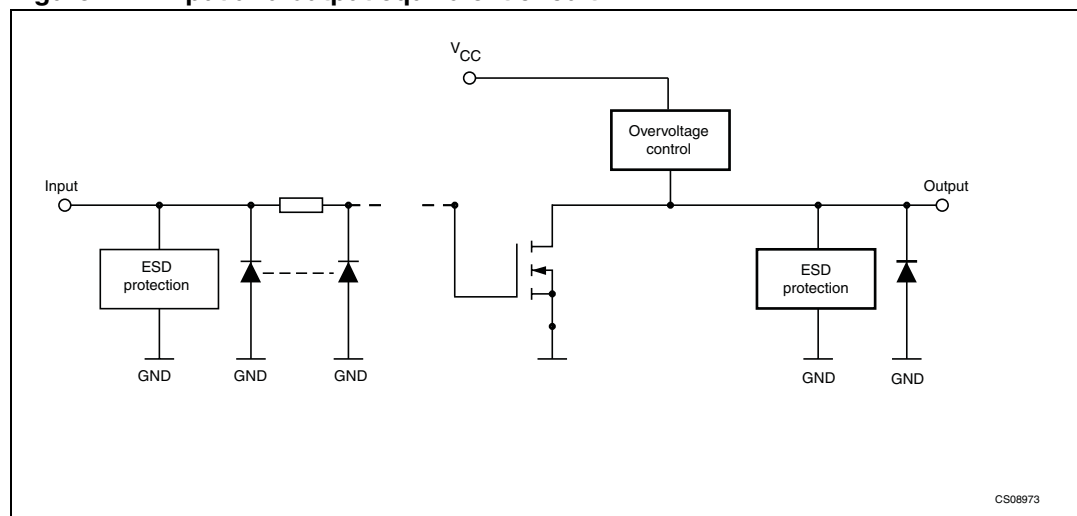
Table 2. Pin assignments

Pin number		Symbol	Name and function
Flip-chip 4	SOT		
—	1	NC	No connection
1	2	1A	Data input
3	4	1Y	Data output
2	3	GND	Ground (0V)
4	5	V _{CC}	Positive supply voltage

Table 3. Truth table

A	Y
L	L
H	Z

Z: High impedance

Figure 2. Input and output equivalent circuit

2 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to +7.0	V
V_O	DC output voltage ($V_{CC} = 0$ V)	-0.5 to +7.0	V
V_O	DC output voltage (high or low state)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	- 50	mA
I_{OK}	DC output diode current	- 50	mA
I_O	DC output current	± 50	mA
I_{CC}	DC supply current per supply pin	± 100	mA
I_{GND}	DC ground current per supply pin	± 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

2.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 5.5	V
V_I	Input voltage	0 to 5.5	V
V_O	Output voltage ($V_{CC} = 0$ V)	0 to 5.5	V
V_O	Output voltage (high or low state)	0 to V_{CC}	V
I_{OL}	High or low level output current ($V_{CC} = 4.5$ to 5.5 V)	+ 32	mA
I_{OL}	High or low level output current ($V_{CC} = 3.0$ to 3.6 V)	+24	mA
I_{OL}	High or low level output current ($V_{CC} = 2.7$ to 3.0 V)	+12	mA
I_{OL}	High or low level output current ($V_{CC} = 2.3$ to 2.7 V)	+8	mA
I_{OL}	High or low level output current ($V_{CC} = 1.65$ to 2.3 V)	+4	mA
T_{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time	0 to 10	ns/V

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		-40 to 85 °C		
				Min	Max	
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}		V
		2.3 – 2.7		0.7 V _{CC}		
		3.0 – 5.5		0.7 V _{CC}		
V _{IL}	Low level input voltage	1.65 – 1.95			0.35 V _{CC}	V
		2.3 – 2.7			0.3 V _{CC}	
		3.0 – 5.5			0.3 V _{CC}	
V _{OL}	Low level output voltage	1.65 – 4.5	I _O = 100 μA		0.1	V
		1.65	I _O = 4 mA		0.45	
		2.3	I _O = 8 mA		0.3	
		3.0	I _O = 16 mA		0.4	
			I _O = 24 mA		0.55	
		4.5	I _O = 32 mA		0.55	
I _{OZ}	High impedance output leakage current	3.6	V _I = 5.5 V		±10	μA
I _I	Input leakage current	1.65 – 5.5	V _I = 0 – 5.5 V		±5	μA
I _{off}	Power off leakage current	0	V _I or V _O = 5.5 V		10	μA
I _{CC}	Quiescent supply current	1.65 – 5.5	V _I = V _{CC} or GND		10	μA
		3.6	V _I or V _O = 3.6 to 5.5 V		±10	

Table 7. AC electrical characteristics

Symbol	Parameter	Test conditions				Value		Unit
		V _{CC} (V)	C _L (pF)	R ₁ (Ω)	t _s = t _r (ns)	-40 to 85 °C		
						Min	Max	
t _{PLZ}	Propagation delay time	1.65 – 1.95	30	1000	2.0	1.8	8.3	ns
		2.3 – 2.7	30	500	2.0	1.2	5.5	
		2.7	50	500	2.5	1	5	
		3.0 – 3.6	50	500	2.5	0.8	4.2	
		4.5 – 5.5	50	500	2.5	0.5	3.5	
t _{PZL}	Propagation delay time	1.65 – 1.95	30	1000	2.0	1.8	8.3	ns
		2.3 – 2.7	30	500	2.0	1.2	5.5	
		2.7	50	500	2.5	1	5	
		3.0 – 3.6	50	500	2.5	0.8	4.2	
		4.5 –5.5	50	500	2.5	0.5	3.5	

Table 8. Capacitive characteristics

Symbol	Parameter	Test conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min	Typ	Max	
C _{IN}	Input capacitance	3.3	V _{IN} = 0 or V _{CC}		2.5		pF
C _{OUT}	Output capacitance	3.3	V _{IN} = 0 or V _{CC}		4		pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	1.8	f _{IN} = 10 MHz		8		pF
		2.5			8		
		3.3			8		

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}

Figure 3. Test circuit

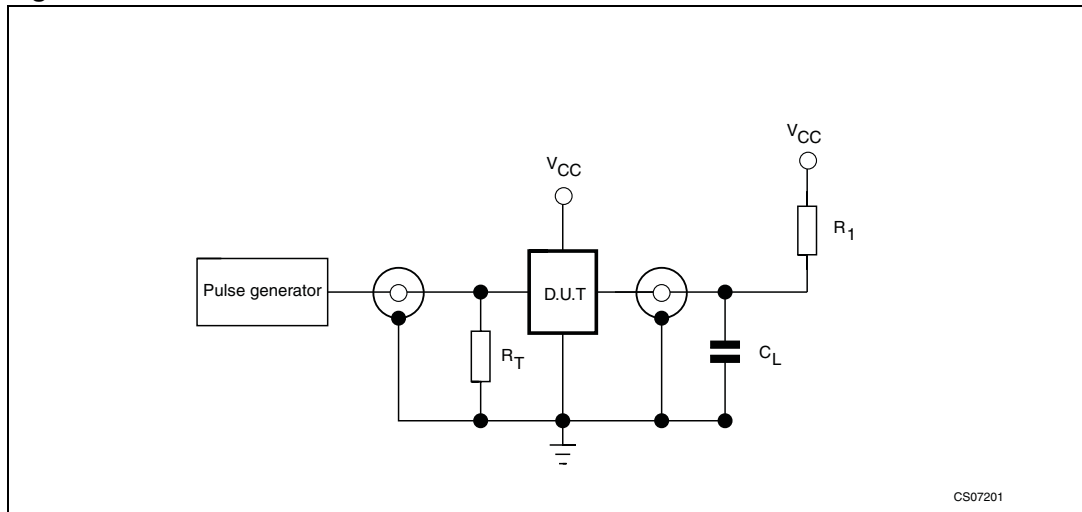
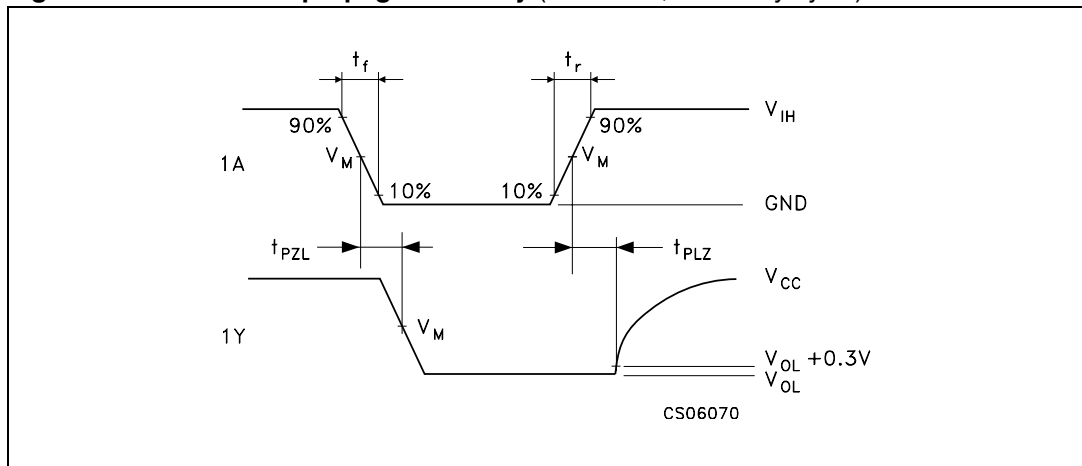


Table 9. Test circuit and waveform symbol value

Symbol	V _{CC}		
	1.65 – 1.95 V	2.3 – 2.7 V	2.7 – 5.5 V
C _L	30 pF	30 pF/ 50 pF	50 pF
R1	1000 Ω	500 Ω	500 Ω
V _{IH}	V _{CC}	V _{CC}	V _{CC}
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2
t _r = t _f	< 2.0 ns	< 2.0 ns	< 2.5 ns

Figure 4. Waveform: propagation delay ($f = 1$ MHz; 50% duty cycle)



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 5. SOT23-5L package outline

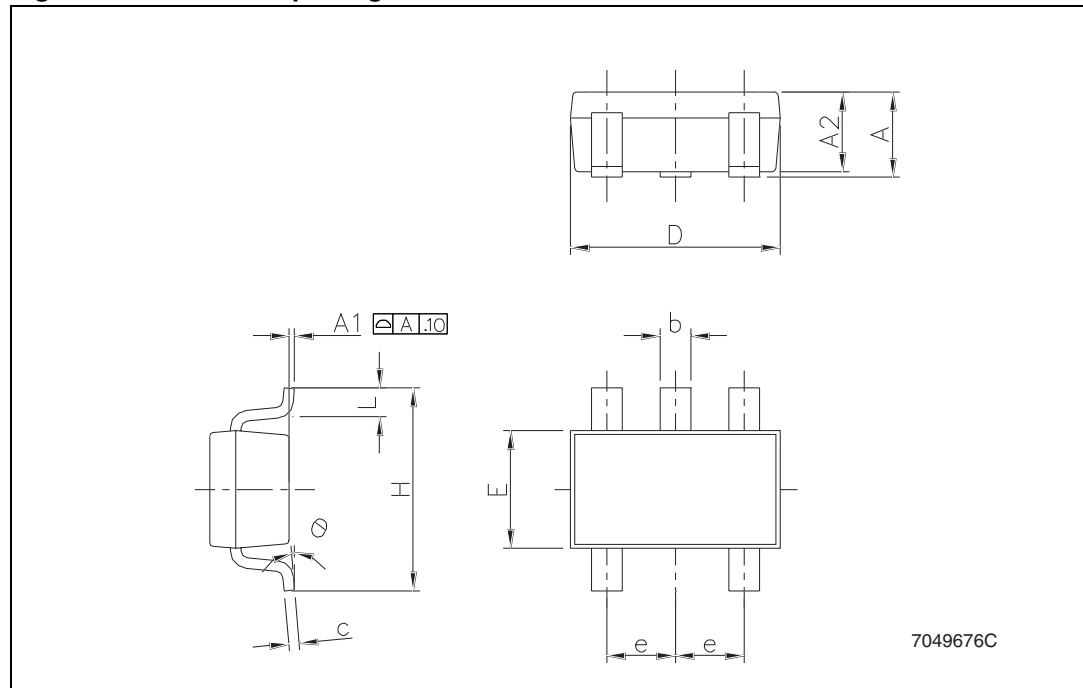


Table 10. SOT23-5L mechanical data

Symbol	millimeters			mils		
	Typ	Min	Max	Typ	Min	Max
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6

Figure 6. SOT323-5L package outline

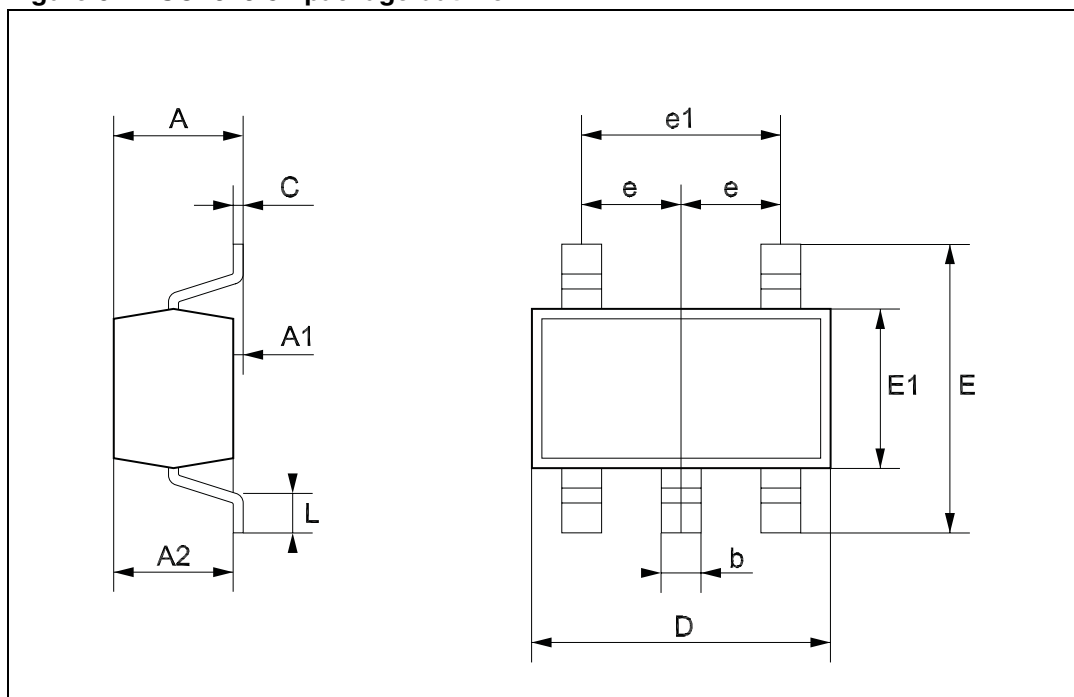


Table 11. SOT323-5L mechanical data

Symbol	millimeters			mils		
	Typ	Min	Max	Typ	Min	Max
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		39.4
b	0.15		0.30	5.9		11.8
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.20	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.65			25.6	
e1		1.3			51.2	
L	0.10		0.30	3.9		11.8

Figure 7. Flip-chip 4 package outline

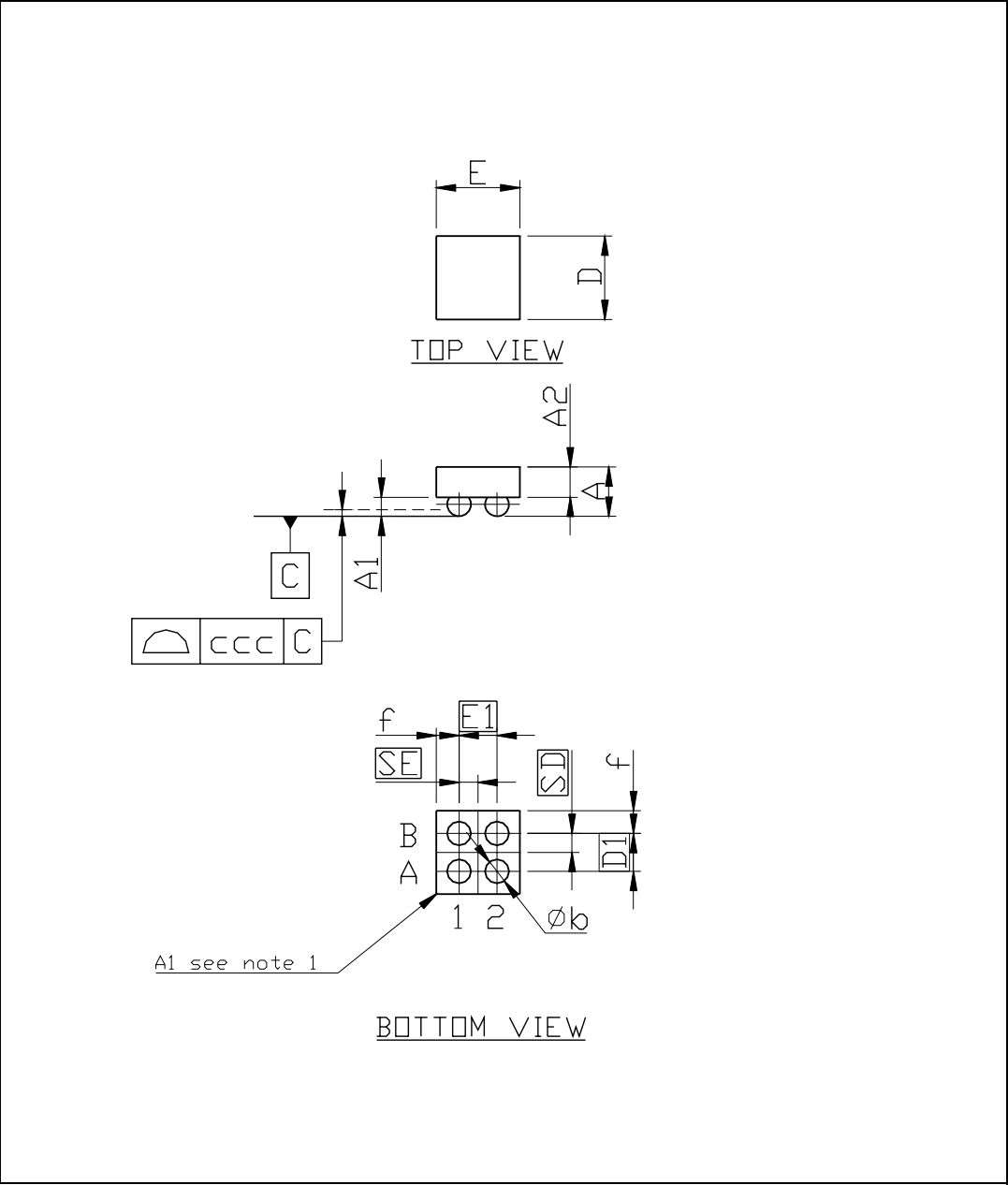


Table 12. Flip-chip 4 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.535	0.58	0.625
A1	0.18	0.205	0.23
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	0.84	0.87	0.9
D1		0.5	
E	0.84	0.87	0.9
E1		0.5	
SD		0.25	
SE		0.25	
f	0.175	0.185	0.195
ccc		0.080	

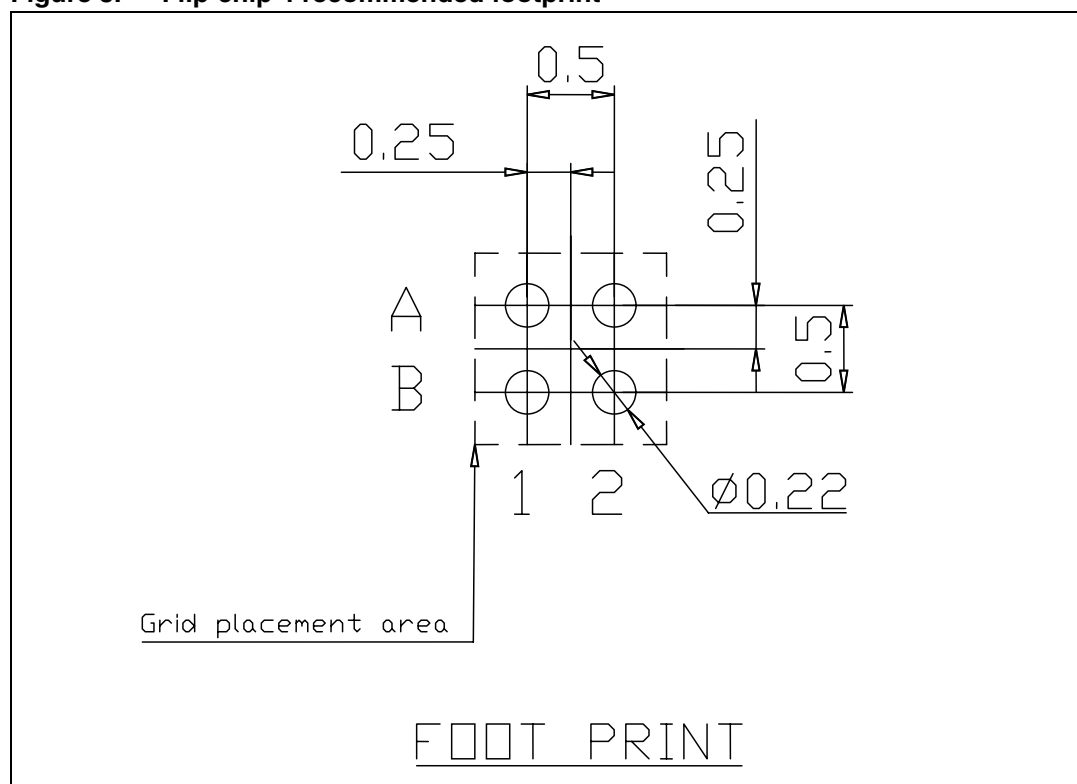
Figure 8. Flip-chip 4 recommended footprint

Figure 9. SOT23-xL tape and reel

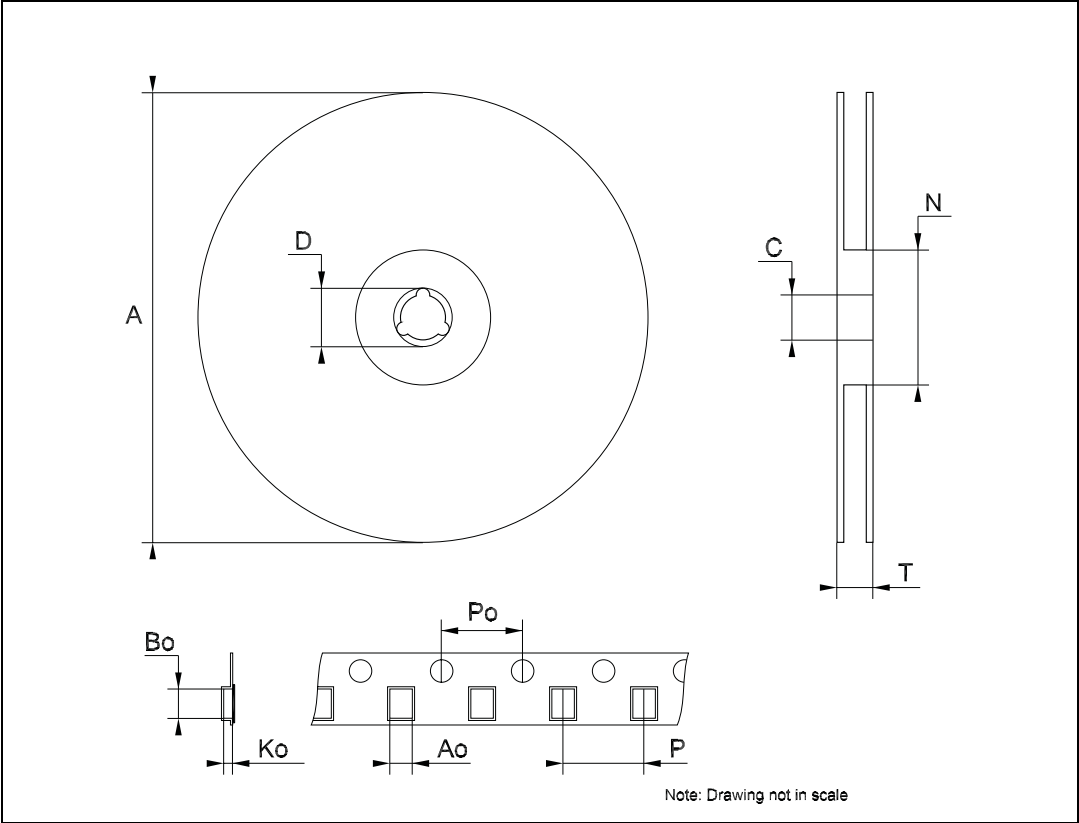
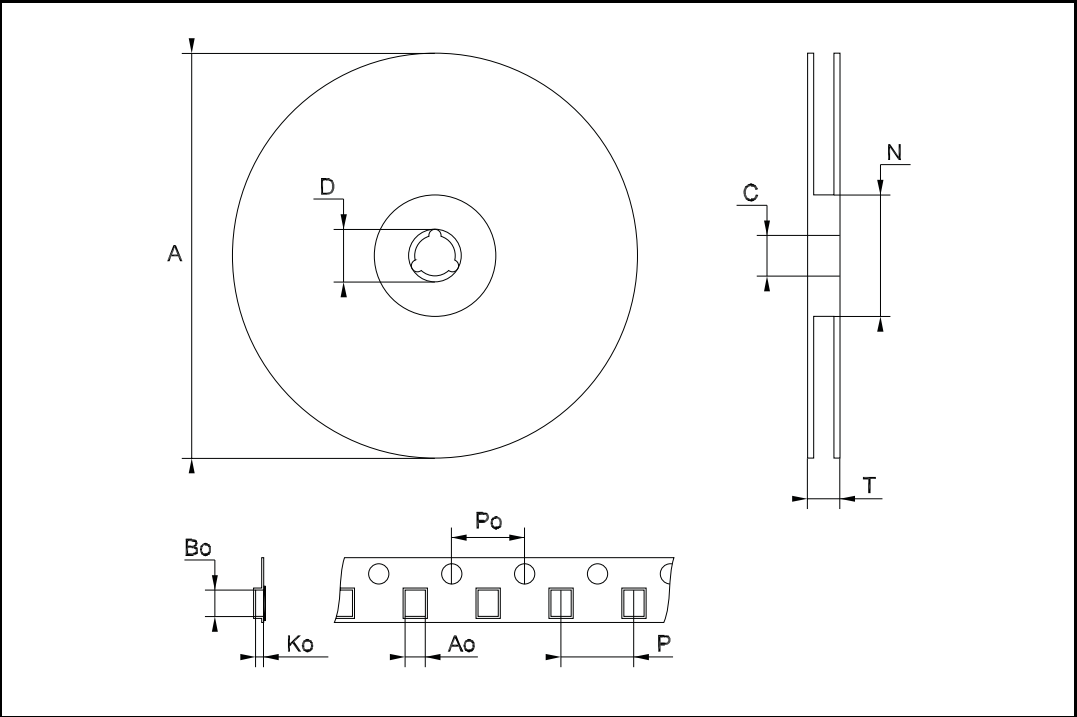


Table 13. SOT23-xL tape and reel mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161

Figure 10. SOT323-xL tape and reel



1. Drawing not to scale.

Table 14. SOT323-xL tape and reel mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	175	180	185	6.889	7.086	7.283
C	12.8	13	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	59.5	60	60.5		2.362	
T			14.4			0.567
Ao		2.25			0.088	
Bo		2.7			0.106	
Ko		1.2			0.047	
Po	3.9	4	4.1	0.153	0.157	0.161
P	3.8	4	4.2	0.149	0.157	0.165

Figure 11. Flip-chip 4 reel information - back side

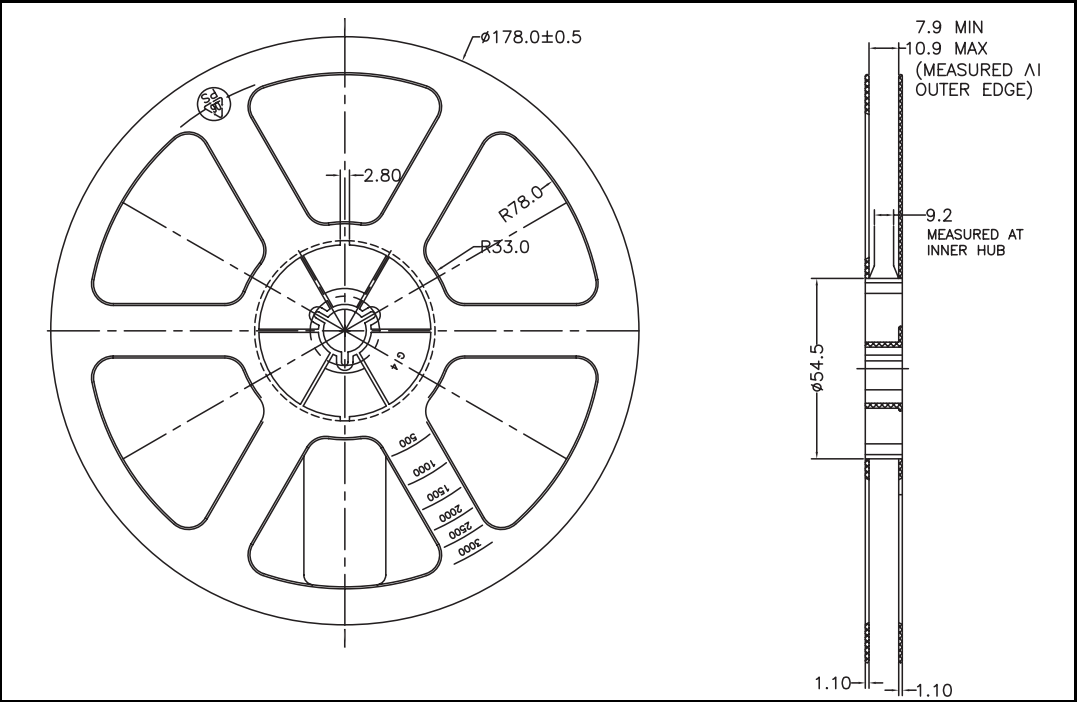
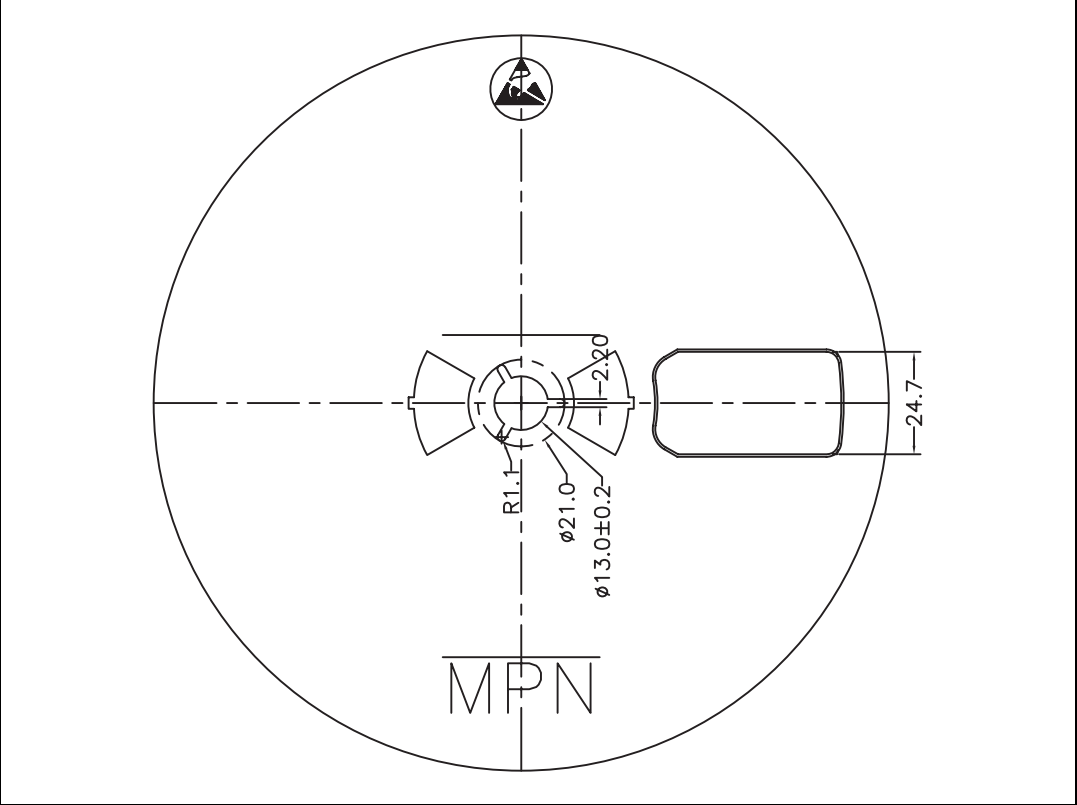


Figure 12. Flip-chip 4 reel information - front side



Technical drawing of a mechanical part with dimensions and cross-sections A-A and B-B.

Top View Dimensions:

- Overall width: 4.00 ± 0.10
- Overall height: $8.00 +0.30 -0.10$
- Distance from left edge to first hole center: 4.00 ± 0.10
- Distance between hole centers: 2.00 ± 0.05
- Hole diameter: $\varnothing 1.50 +0.10$
- Distance from right edge to last hole center: 1.75 ± 0.10
- Distance from hole center to bottom edge: 3.50 ± 0.05

Cross-section A-A:

- Top flange thickness: 0.20
- Bottom flange thickness: 0.96 ± 0.05
- Internal chamfer: 45° and 0°

Cross-section B-B:

- Top flange thickness: $.20 \pm 0.02$
- Bottom flange thickness: 0.69 ± 0.05
- Internal chamfer: 45° and 0°

Tape and reel

- Top view of package
- Balls underneath
- Pin A1 marked from target spec

5 Revision history

Table 15. Document revision history

Date	Revision	Changes
04-Sept-2004	4	Document change.
03-May-2006	5	Data reel updating.
17-Jan-2008	6	Document restructured and converted to new ST template. Added 74LX1G07BJR and related package information.
29-Jan-2008	7	Flip-Chip 4 replaced with Flip-chip 4 and updated Table 12 on page 13 .
21-Feb-2008	8	Replaced Flip-Chip 4 package name with Flip-chip 4, latch-up and ESD performance among the specifications in the cover page and updated Table 6 on page 7 , Table 8 on page 8 , and Table 12 on page 13 , replaced Figure 13 on page 18 and Figure 14 on page 18
23-Apr-2008	9	Modified: Table 12 on page 13 and Figure 13 on page 18 .

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