

MOSFET - Power, Single N-Channel STD Gate, SO8FL

80 V, 3 mΩ, 135 A

NVMFWS3D0N08X

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

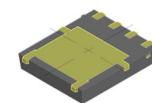
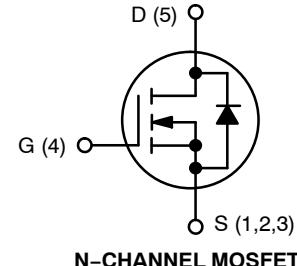
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	80	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (Note 1)	T _C = 25°C	I _D	A
	T _C = 100°C	96	
Power Dissipation (Note 1)	T _C = 25°C	P _D	119
Pulsed Drain Current	T _C = 25°C, t _p = 100 μs	I _{DM}	A
Pulsed Source Current (Body Diode)		I _{SM}	
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +175	°C
Source Current (Body Diode)	I _S	179	A
Single Pulse Avalanche Energy (I _{PK} = 47 A) (Note 2)	E _{AS}	110	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. E_{AS} of 110 mJ is based on started T_J = 25°C, I_{AS} = 47 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
80 V	3 mΩ @ 10 V	135 A



DFNW5 (SO-8FL)
CASE 507BA

3D0N8W
AYWZZ

3D0N8W = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

NVMFWS3D0N08X

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta,JC}$	1.26	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta,JA}$	39	

4. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.
 5. $R_{\theta,JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 1 \text{ mA}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	$I_D = 1 \text{ mA}$, Referenced to 25°C		31.6		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 80 \text{ V}, T_J = 25^{\circ}\text{C}$		1		μA
		$V_{\text{DS}} = 80 \text{ V}, T_J = 125^{\circ}\text{C}$		250		
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 20 \text{ V}, V_{\text{GS}} = 0 \text{ V}$		100		nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 31 \text{ A}$		2.6	3.0	$\text{m}\Omega$
Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 153 \mu\text{A}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{\text{GS}(\text{TH})}/\Delta T_J$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 153 \mu\text{A}$		-7.5		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 5 \text{ V}, I_D = 31 \text{ A}$		97		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 40 \text{ V}, f = 1 \text{ MHz}$		2680		pF
Output Capacitance	C_{OSS}			780		
Reverse Transfer Capacitance	C_{RSS}			12		
Output Charge	Q_{OSS}			56		nC
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 6 \text{ V}, V_{\text{DD}} = 40 \text{ V}, I_D = 31 \text{ A}$		23		
				38		
				7		
		$V_{\text{GS}} = 10 \text{ V}, V_{\text{DD}} = 40 \text{ V}, I_D = 31 \text{ A}$		13		
				6		
				4.7		
				0.7		
Gate Resistance	R_G	$f = 1 \text{ MHz}$				Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	Resistive Load, $V_{\text{GS}} = 0/10 \text{ V}, V_{\text{DD}} = 64 \text{ V},$ $I_D = 31 \text{ A}, R_G = 2.5 \Omega$		22		ns
Rise Time	t_r			8		
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$			33		
Fall Time	t_f			5		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}, I_S = 31 \text{ A}, T_J = 25^{\circ}\text{C}$		0.82	1.2	V
		$V_{\text{GS}} = 0 \text{ V}, I_S = 31 \text{ A}, T_J = 125^{\circ}\text{C}$		0.66		

NVMFWS3D0N08X

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = 0 \text{ V}$, $dI/dt = 1000 \text{ A}/\mu\text{s}$, $I_S = 31 \text{ A}$, $V_{DD} = 64 \text{ V}$		22		ns
Charge Time	t_a			13		
Discharge Time	t_b			9		
Reverse Recovery Charge	Q_{RR}			150		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFWS3D0N08XT1G	3D0N8W	DFNW5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

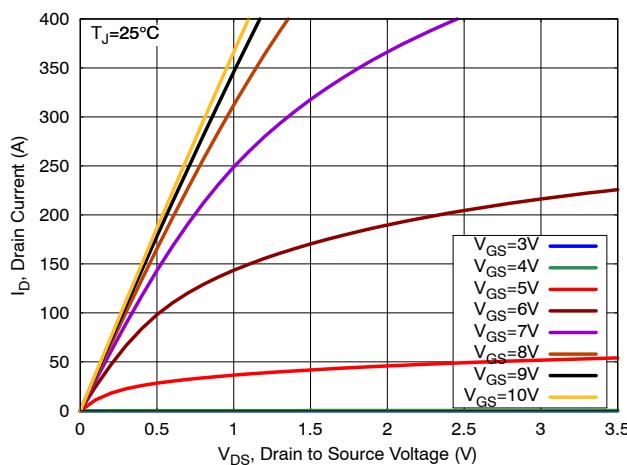


Figure 1. On-Region Characteristics

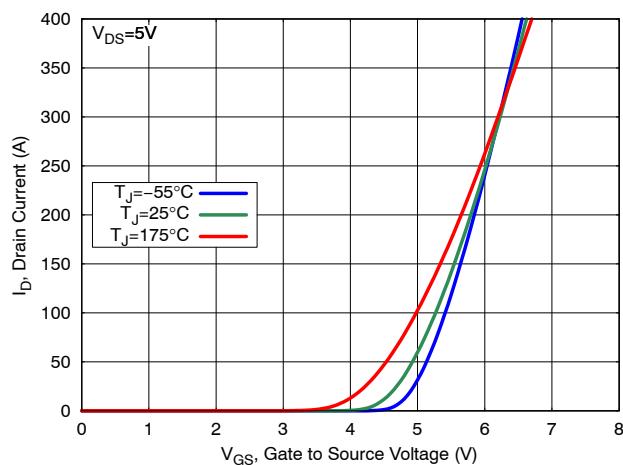


Figure 2. Transfer Characteristics

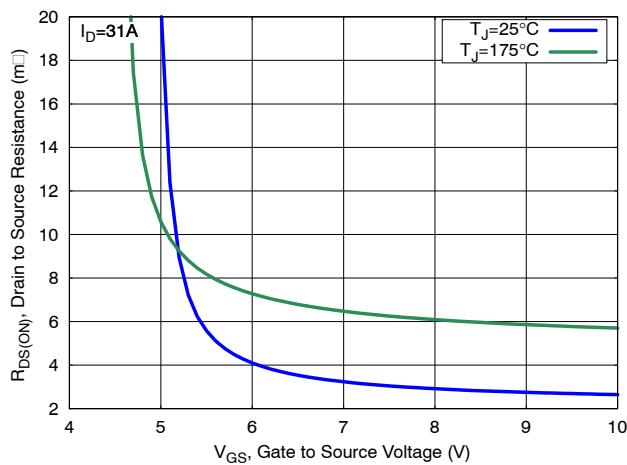


Figure 3. On-Resistance vs. Gate Voltage

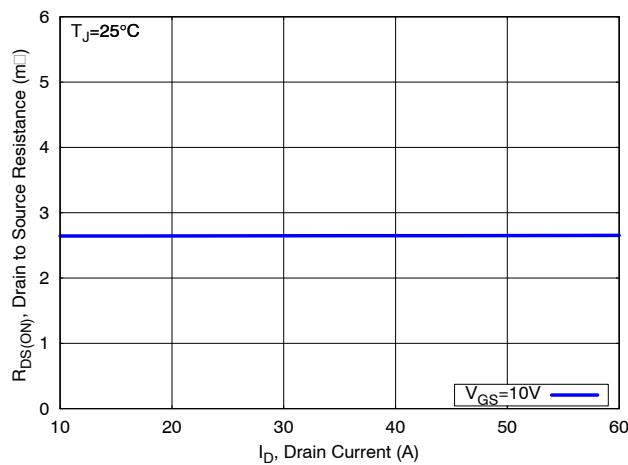


Figure 4. On-Resistance vs. Drain Current

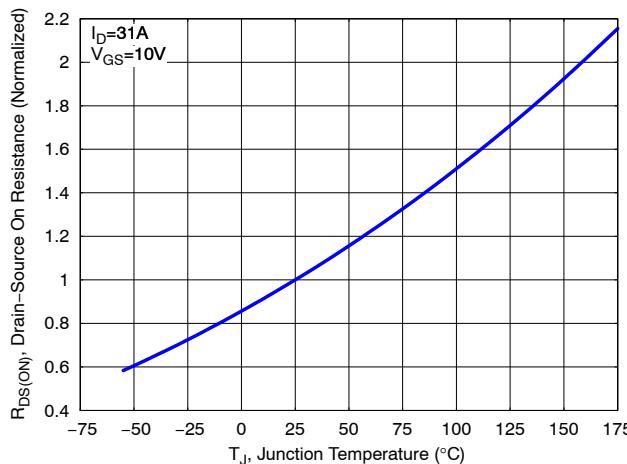


Figure 5. Normalized ON Resistance vs. Junction Temperature

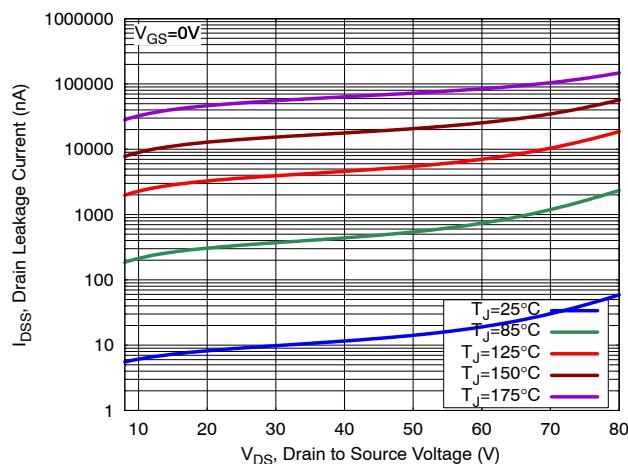
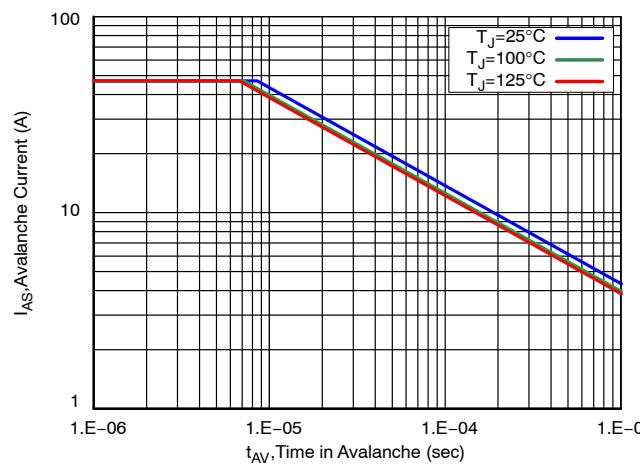
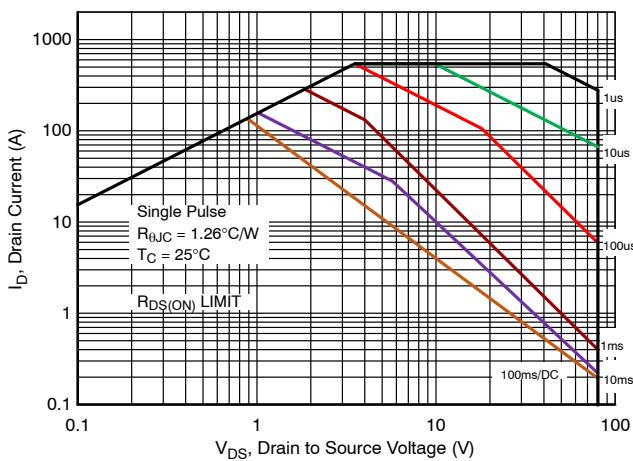
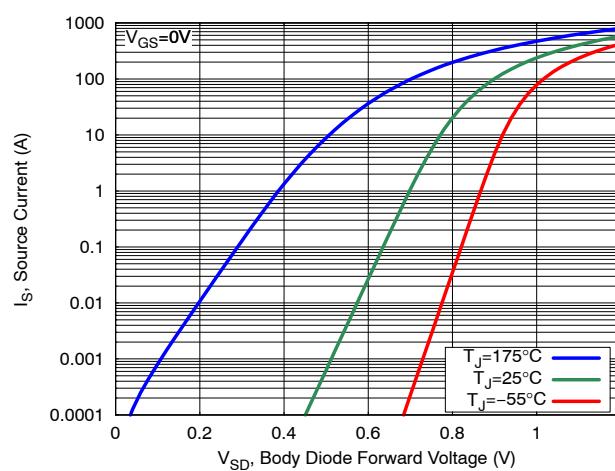
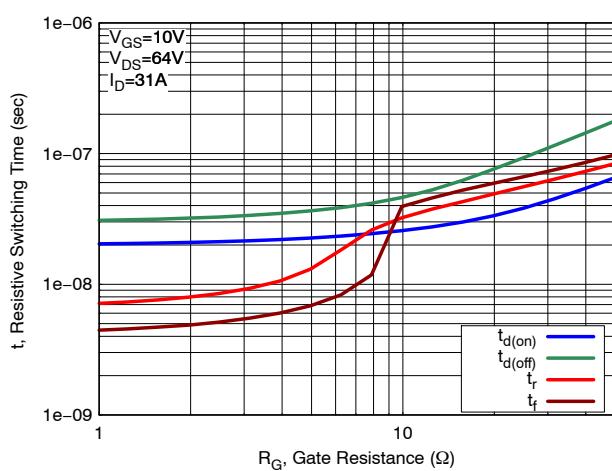
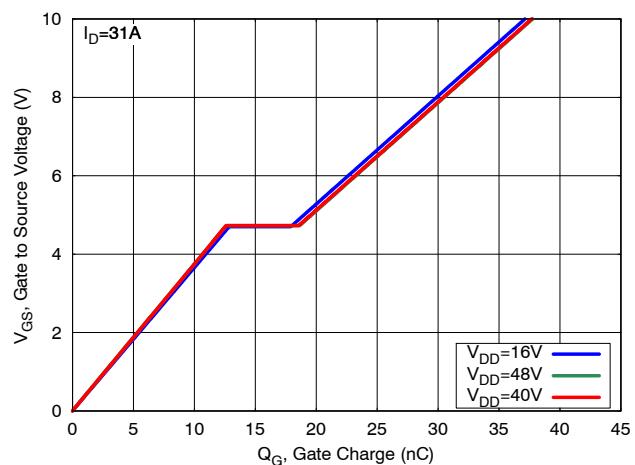
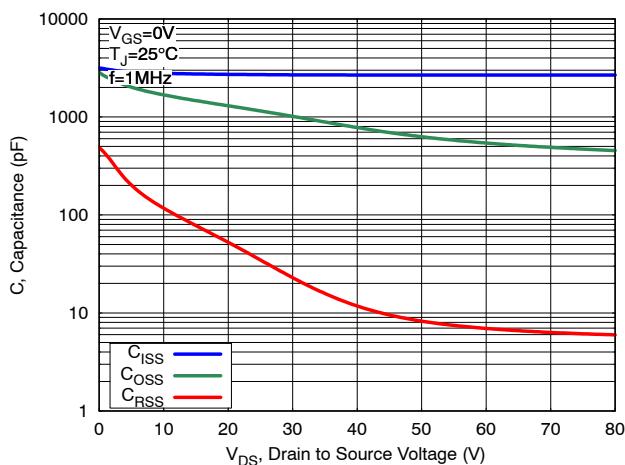


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

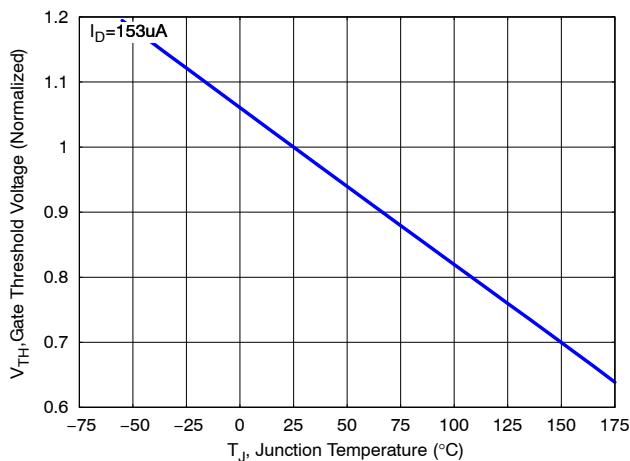


Figure 13. Gate Threshold Voltage vs Junction Temperature

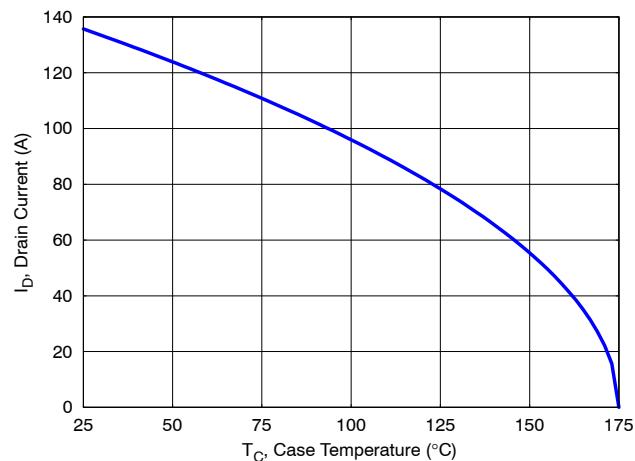


Figure 14. Maximum Current vs. Case Temperature

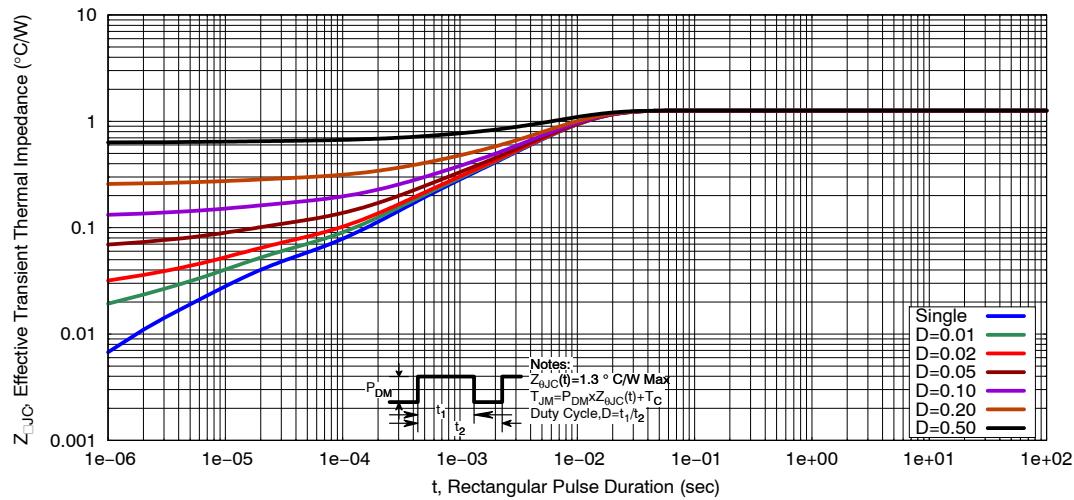
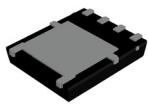
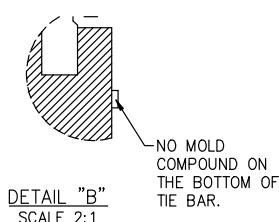
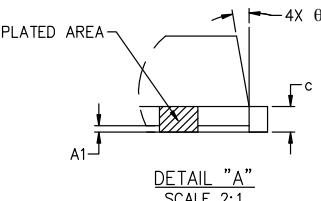
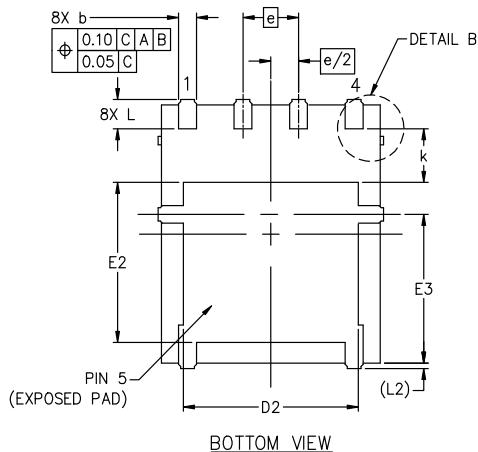
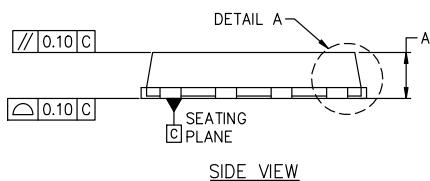
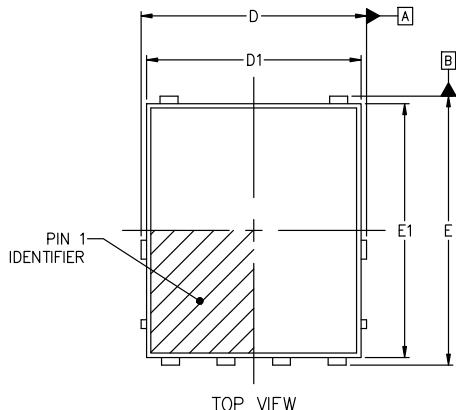


Figure 15. Transient Thermal Response



DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

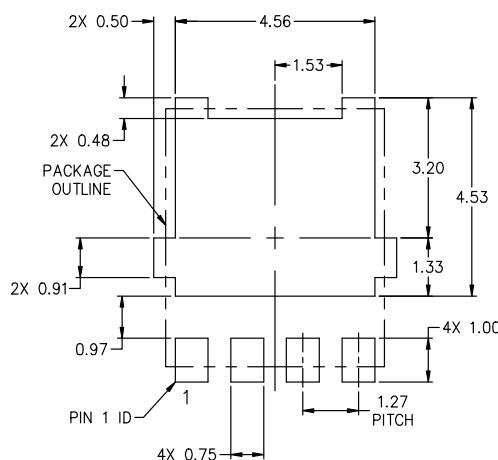
DATE 19 SEP 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

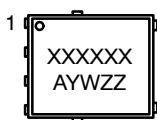
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e		1.27 BSC	
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2		0.15 REF.	
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.
 Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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