

N-CHANNEL ENHANCEMENT MODE MOSFET
Product Summary (Typ. @ $V_{GS} = 3.3V$, $T_A = +25^\circ C$)

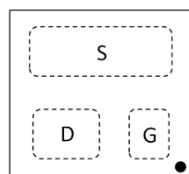
V_{DSS}	$R_{DS(ON)}$	Q_g	Q_{gd}	I_D
12V	14.1m Ω	10.5nC	4.1nC	7.5A

Description

This new generation MOSFET is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. Using Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{DS(ON)}$ per footprint area.

Applications

- DC-DC Converters
- Battery Management
- Load Switch

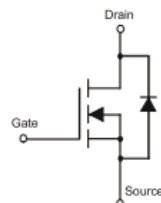

 Top-View
Pin Configuration

Features

- TR-MOS Technology with the Lowest $R_{DS(ON)}$:
 $R_{DS(ON)} = 14.1m\Omega$ to Minimize On-State Losses
- CSP with Footprint 1.0mm $\times$ 1.0mm
- Height = 0.29mm for Low Profile
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.**
<https://www.diodes.com/quality/product-definitions/>

Mechanical Data

- Case: X3-DSN1010-3
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish: Matte Tin Annealed Over Copper Pillar (63)
- Solder Cap Material: SnAg (Ag: 2.0+/-0.5%)
- Weight: 0.00062 grams (Approximate)



Equivalent Circuit

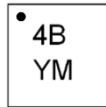
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN1017UCP3-7	X3-DSN1010-3	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information (Note 5)

Marking 1



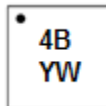
4B = Product Type Marking Code
YM = Date Code Marking
Y or Y = Year (ex: 1 = 2021)
M or M = Month (ex: 9 = September)

Date Code Key

Year	2017	...	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	E	...	I	J	K	L	M	N	O	P	R	S

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Marking 2



4B = Product Type Marking Code
YW = Date Code Marking
Y or Y = Year (ex: 1 = 2021)
W or W = Week (ex: a = Week 27; z Represents Week 52 and 53)

Date Code Key

Year	2017	...	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	7	...	1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	z

Note: 5. The marking code changed to Marking 2 from week 6, 2021.

Maximum Ratings

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	12	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current @ $V_{GS} = 3.3V$ (Note 6)	I_D	5.4 4.3	A
Continuous Drain Current @ $V_{GS} = 3.3V$ (Note 7)	I_D	7.5 6.1	A
Pulsed Drain Current (Pulse Duration 10 μ s, Duty Cycle $\leq 1\%$)	I_{DM}	15	A
Continuous Source-Drain Diode Current (Note 7)	I_S	1.47	A
Pulse Diode Forward Current (Note 7)	I_{SM}	15	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P_D	0.74	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	167	$^{\circ}C/W$
Total Power Dissipation (Note 7)	P_D	1.47	W
Thermal Resistance, Junction to Ambient (Note 7)	$R_{\theta JA}$	85	$^{\circ}C/W$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^{\circ}C$

Electrical Characteristics (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 9.6V, V_{GS} = 0V$
Gate-Body Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 8V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	0.7	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	14.1	17.0	m Ω	$V_{GS} = 3.3V, I_D = 5.0A$
		—	14.4	19.0		$V_{GS} = 3.0V, I_D = 5.0A$
		—	15.5	21.0		$V_{GS} = 2.5V, I_D = 5.0A$
		—	16.0	23.0		$V_{GS} = 2.3V, I_D = 5.0A$
		—	16.8	24.0		$V_{GS} = 2.1V, I_D = 5.0A$
		—	21.3	34.0		$V_{GS} = 2.1V, I_D = 5.0A, +125^{\circ}C$ (Note 9)
		—	20.0	30.0		$V_{GS} = 1.8V, I_D = 3.0A$
Forward Transfer Admittance	$ Y_{fs} $	—	6.6	—	S	$V_{DS} = 6V, I_S = 1.0A$
Body Diode Forward Voltage	V_{SD}	—	0.7	1	V	$V_{GS} = 0V, I_S = 1.0A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1002	1503	pF	$V_{DS} = 6V, V_{GS} = 0V, f = 1.0MHz$
Output Capacitance	C_{oss}	—	312	468	pF	
Reverse Transfer Capacitance	C_{rss}	—	259	389	pF	
Gate Resistance	R_g	—	2.2	4.4	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge	Q_g	—	10.5	16	nC	$V_{GS} = 3.3V, V_{DS} = 6V, I_D = 5.0A$
Gate-Source Charge	Q_{gs}	—	1.0	1.5	nC	
Gate-Drain Charge	Q_{gd}	—	4.1	6.2	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.7	10	ns	$V_{DD} = 6V, I_D = 5.0A, V_{GEN} = 4.5V, R_G = 1\Omega, R_L = 1.2\Omega$
Turn-On Rise Time	t_R	—	6.3	15	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	17.9	35	ns	
Turn-Off Fall Time	t_F	—	7.5	15	ns	$I_F = 5A, di/dt = 100A/\mu s$
Reverse Recovery Charge	Q_{RR}	—	2.7	5	nC	
Body Diode Reverse Recovery Time	t_{RR}	—	14.2	28	ns	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

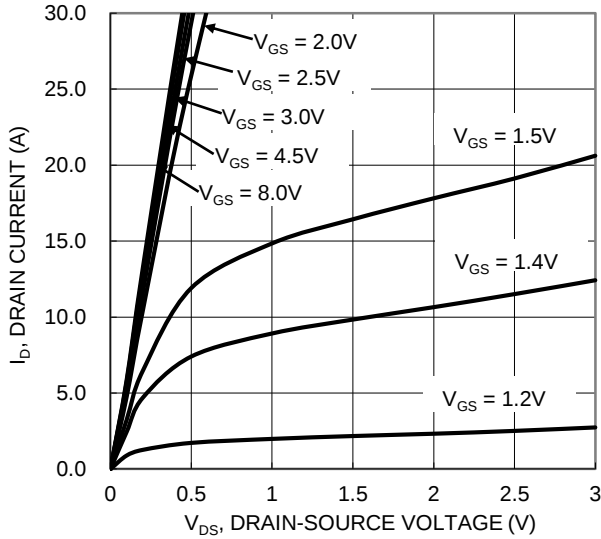


Figure 1. Typical Output Characteristic

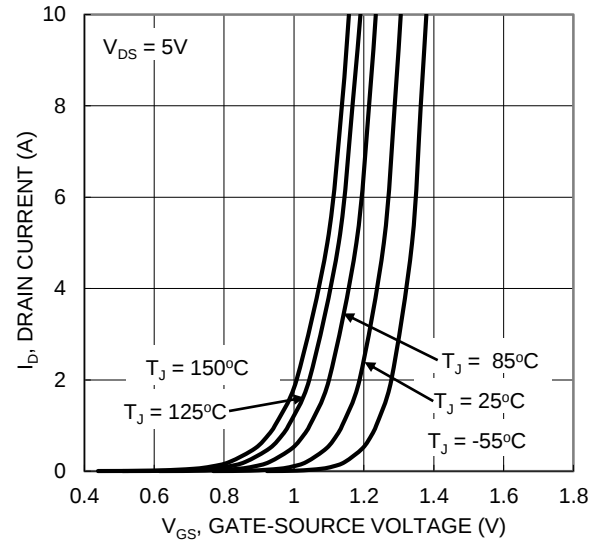


Figure 2. Typical Transfer Characteristic

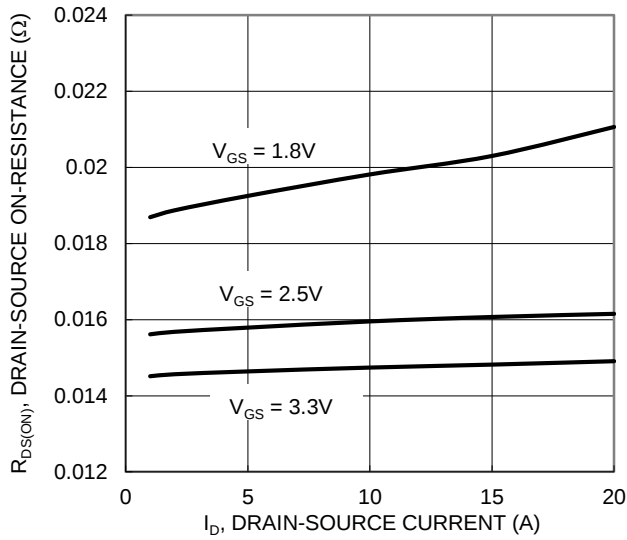


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

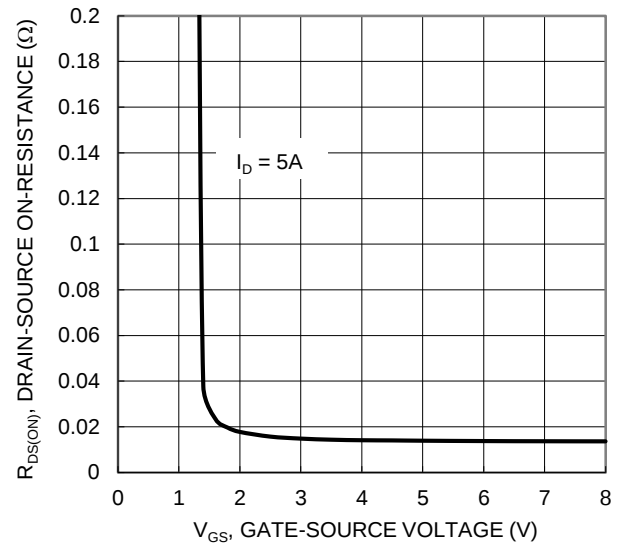


Figure 4. Typical Transfer Characteristic

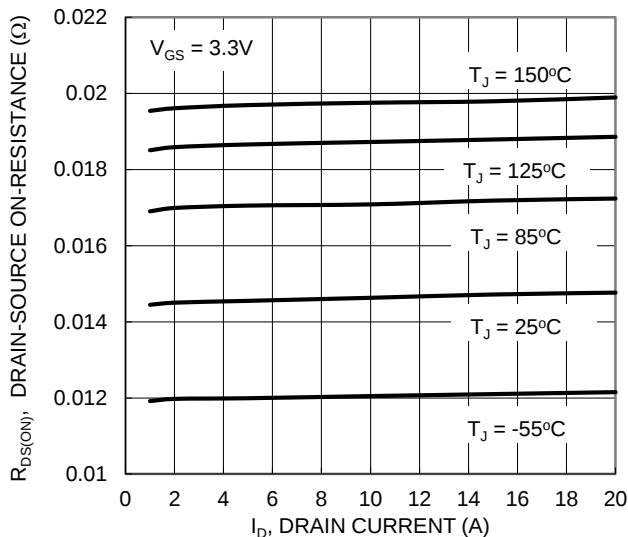


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

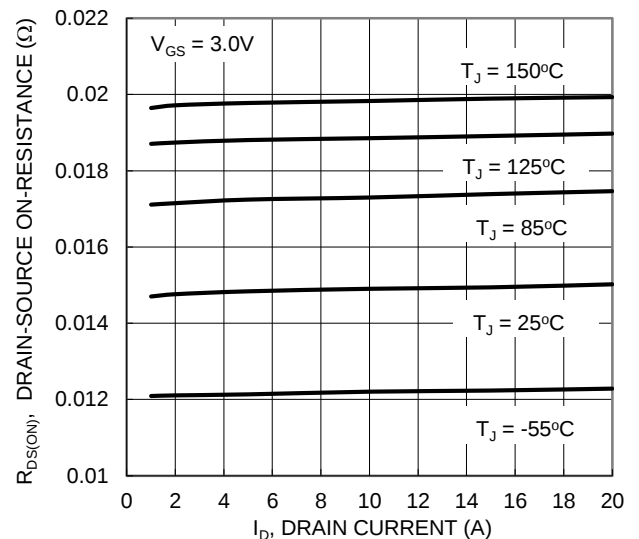


Figure 6. Typical On-Resistance vs. Drain Current and Junction Temperature

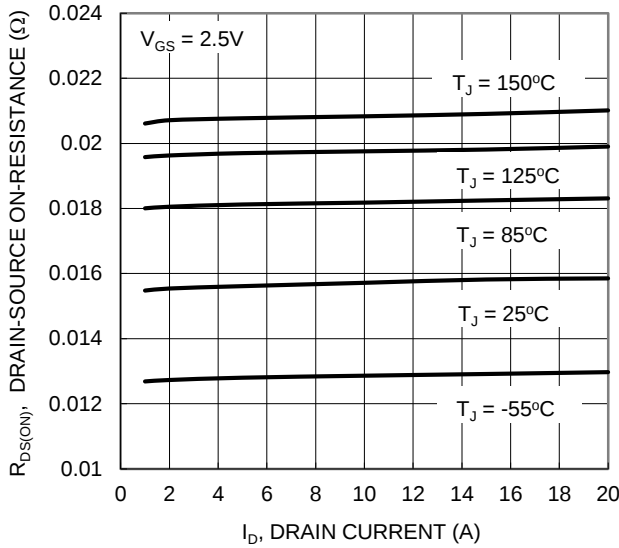


Figure 7. Typical On-Resistance vs. Drain Current and Junction Temperature

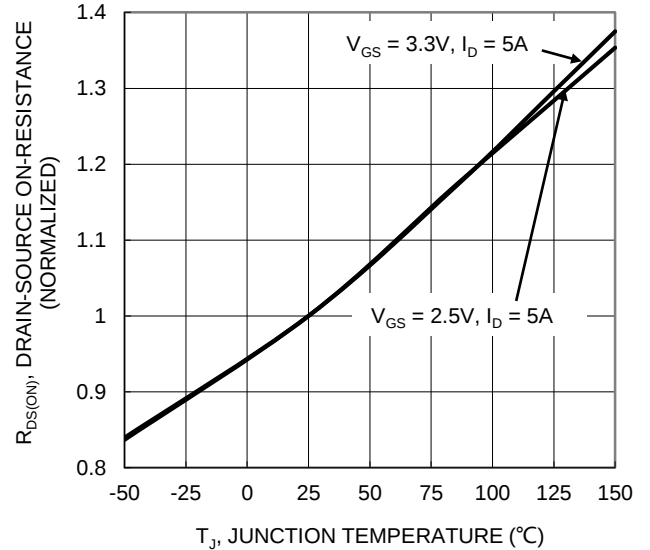


Figure 8. On-Resistance Variation with Junction Temperature

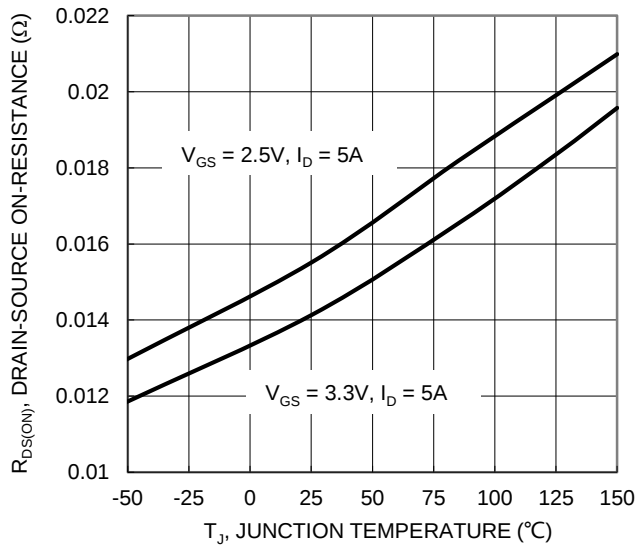


Figure 9. On-Resistance Variation with Junction Temperature

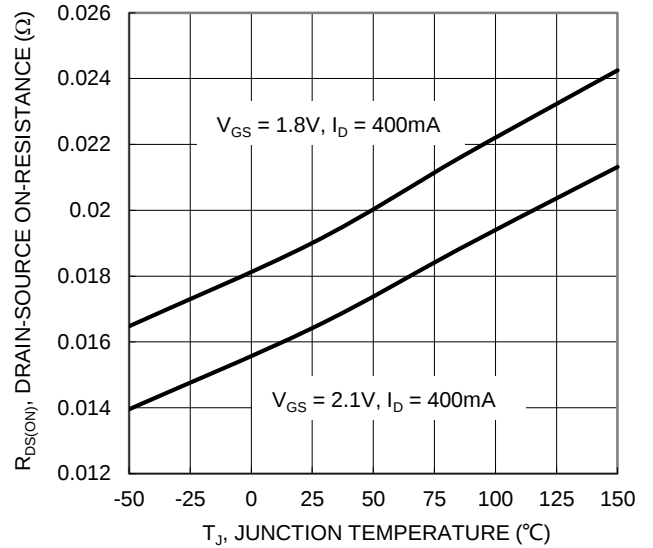


Figure 10. On-Resistance Variation with Junction Temperature

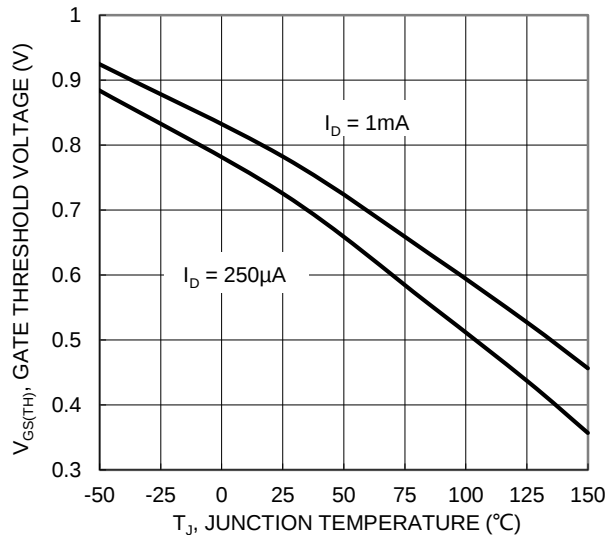


Figure 11. Gate Threshold Variation vs. Junction Temperature

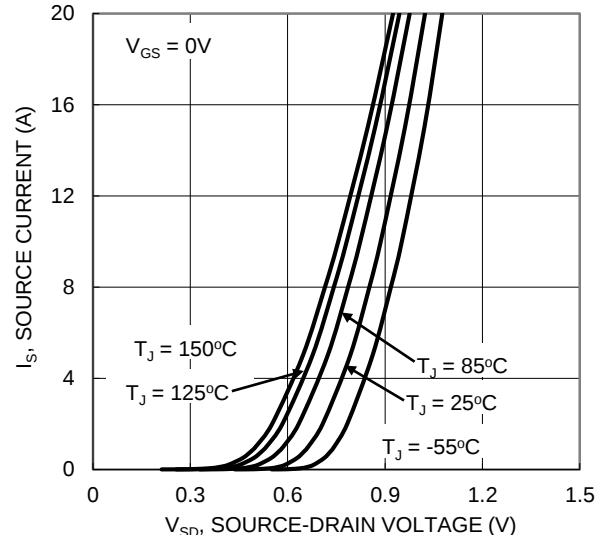
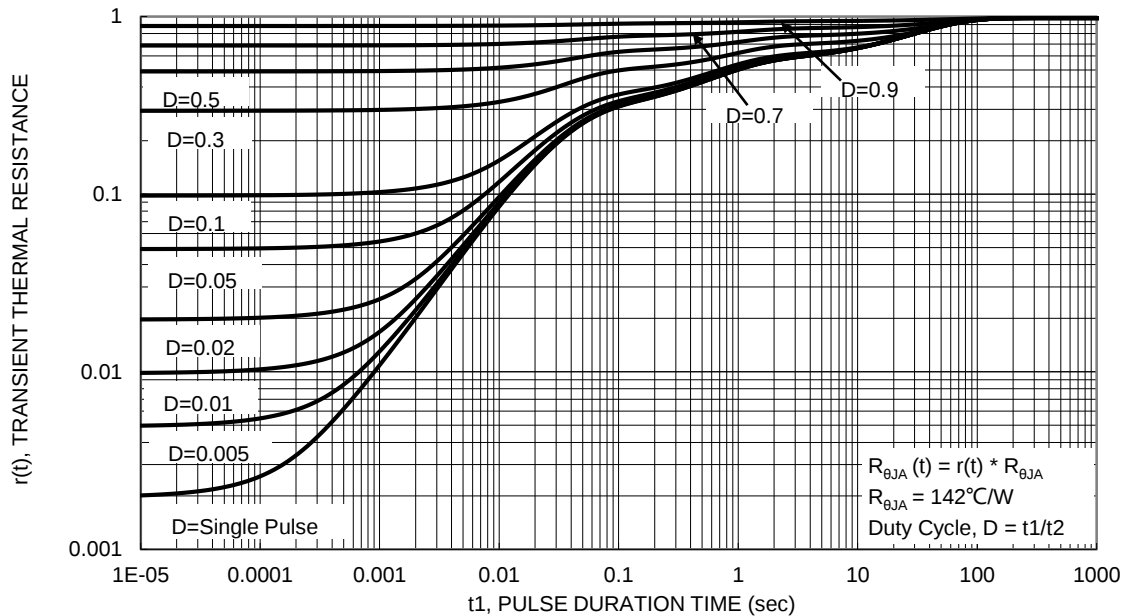
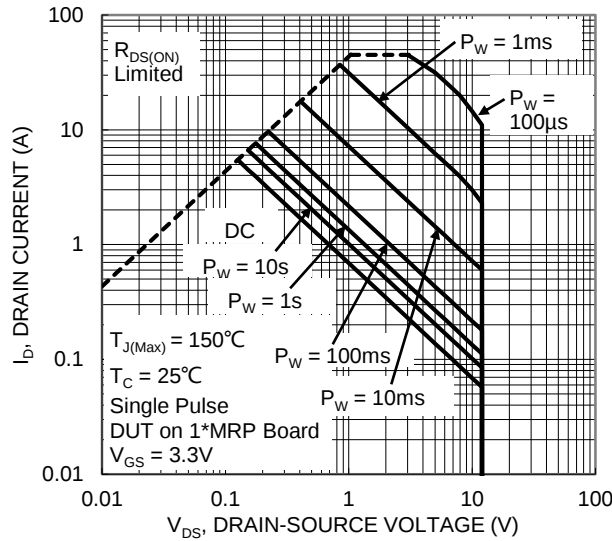
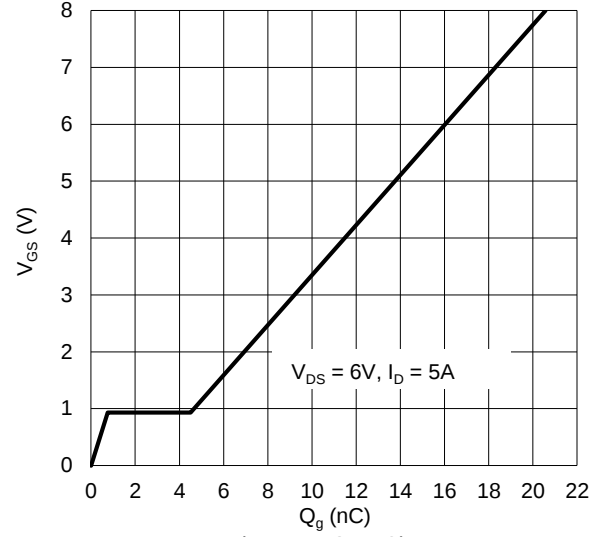
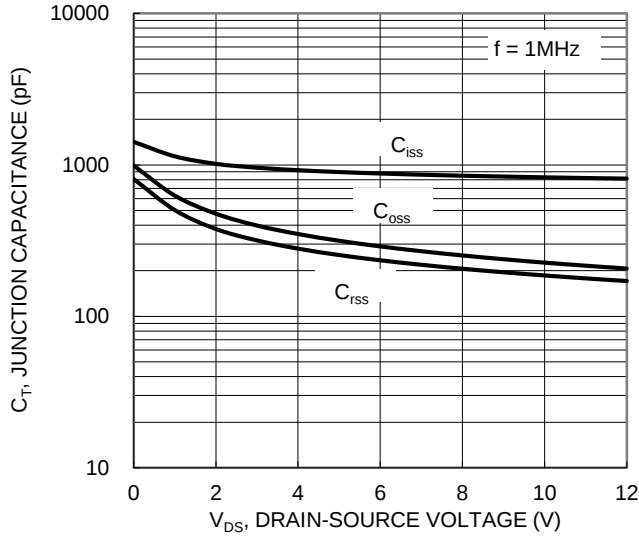


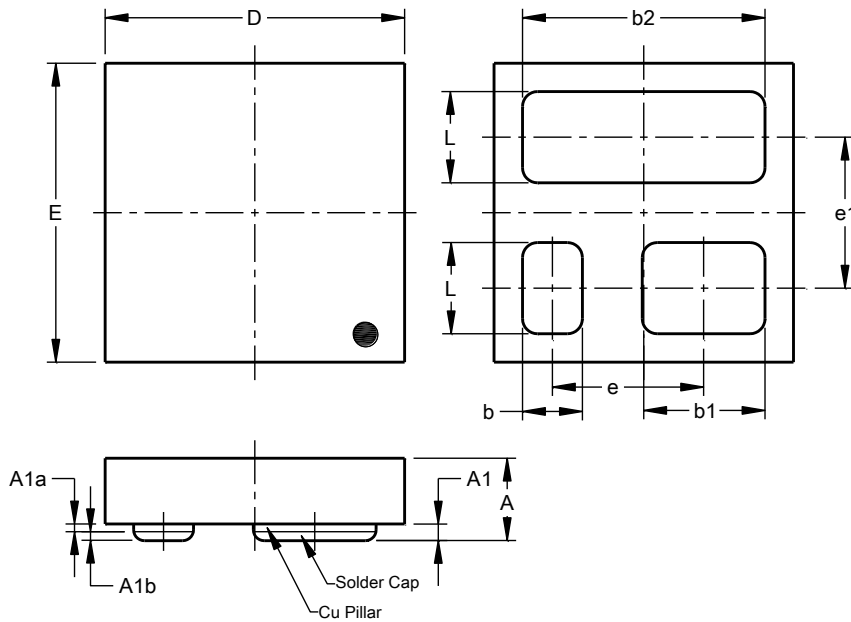
Figure 12. Diode Forward Voltage vs. Current



Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X3-DSN1010-3

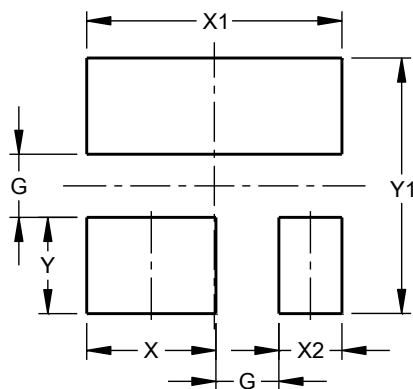


X3-DSN1010-3			
Dim	Min	Max	Typ
A	-	0.29	0.27
A1	0.034	0.046	0.04
A1a	0.015	0.025	0.02
A1b	0.017	0.023	0.02
b	0.18	0.22	0.20
b1	0.39	0.43	0.41
b2	0.79	0.83	0.81
D	0.92	1.00	0.96
E	0.92	1.00	0.96
e	-	-	0.505
e1	-	-	0.505
L	0.285	0.325	0.305
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X3-DSN1010-3



Dimensions	Value (in mm)
G	0.200
X	0.410
X1	0.810
X2	0.200
Y	0.305
Y1	0.810

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