RL78/G22

RENESAS MCU

R01DS0424EJ0120
Rev.1.20
Jun 30, 2026

True low-power platform, 37.5-µA/MHz operating current, 200-nA stop current, 32-/64-KB code flash memory and 4-KB RAM, up to 29 capacitive touch sensors, from 16 to 48 pins, 1.6 to 5.5 V

1. Outline

1.1 Features

Ultra-low power consumption technology
- Operation from a single power supply (V_{DD}) within the 1.6-V to 5.5-V range
- HALT mode
- STOP mode
  High-speed wakeup from the STOP mode is possible.
- SNOOZE mode

RL78 CPU core
- CISC architecture with 3-stage pipeline
- The minimum instruction execution time can be changed from high to ultra-low speed.
  - High speed: 0.03125 µs at 32-MHz operation with the high-speed on-chip oscillator clock
  - Ultra-low speed: 30.5 µs at 32.768-kHz operation with the subsystem clock
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers:
  (8-bit register × 8) × 4 banks
- On-chip RAM: 4 KB

Code flash memory
- Code flash memory: 32 or 64 KB
- Block size: 2 KB
- Security function: Prohibition of block erase and rewriting
- On-chip debugging
- Self-programming with boot swapping and flash shield window

Data flash memory
- Data flash memory: 2 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator
- Selectable from among 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0%
  (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Middle-speed on-chip oscillator
- Selectable from among 4 MHz, 2 MHz, and 1 MHz with adjustability

Low-speed on-chip oscillator
- 32.768 kHz (typ.) with adjustability

Operating ambient temperature
- T_A = -40 to +85°C (2D: Consumer applications)
- T_A = -40 to +105°C (3C: Industrial applications)

Power management and reset function
- Power-on-reset circuit (POR)
- Voltage detectors (LVD0 and LVD1)

Data transfer controller (DTC)
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

SNOOZE mode sequencer (SMS)
- Calculations and comparison of values by the commands for use in processing by the sequencer can realize intermittent operations where the RL78/G22 does not have to return to normal operation.
- Sequentially handling a total of 32 processes with the use of desired commands from among 21 different ones
- The SNOOZE mode sequencer offers operation with low power consumption without using the CPU, flash memory, and RAM.

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Event link controller (ELC)
- 20 event signals can be set up between specified peripheral functions.

Serial interface
- Simplified SPI (CSI[Note]): 1 to 5 channels
- UART/UART (LIN-bus supported)/UARTA: 1 to 4 channels
- I^2C/Simplified I^2C: 2 to 6 channels

Timers
- 16-bit timer: 8 channels
- 32-bit interval timer:
  1 channel in 32-bit counter mode
  2 channels in 16-bit counter mode
  4 channels in 8-bit counter mode
- Realtime clock: 1 channel (counting of one second to 99 years, alarm interrupt, and clock correction)
- Watchdog timer: 1 channel (operates with the low-speed on-chip oscillator clock)

A/D converter
- 8-/10-bit resolution
- Analog input: 3 to 10 channels
- Internal reference voltage (1.48 V (typ.)) and temperature sensor

Capacitive sensing unit
- Operating voltage: V_{DD} = 1.8 to 5.5 V
- Self-capacitance method: A single pin configures a single key, supporting up to 29 keys
- Mutual capacitance method: Pins for transmission and reception can be selected from among up to 29 pins to create a matrix configuration for the keys.

Input/output port pins
- Number of port pins: 12 to 44
  N-ch open-drain I/O pins (withstand voltage of 6 V): 0 to 4
  N-ch open-drain I/O pins (withstand voltage of V_{DD}): 4 to 13
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

Others
- Binary-coded decimal (BCD) correction circuit
- Key interrupt input
- Clock output/buzzer output controller

Note Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Remark The functions mounted depend on the product. For details, see **1.6 Outline of Functions**.

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O ROM, RAM capacities

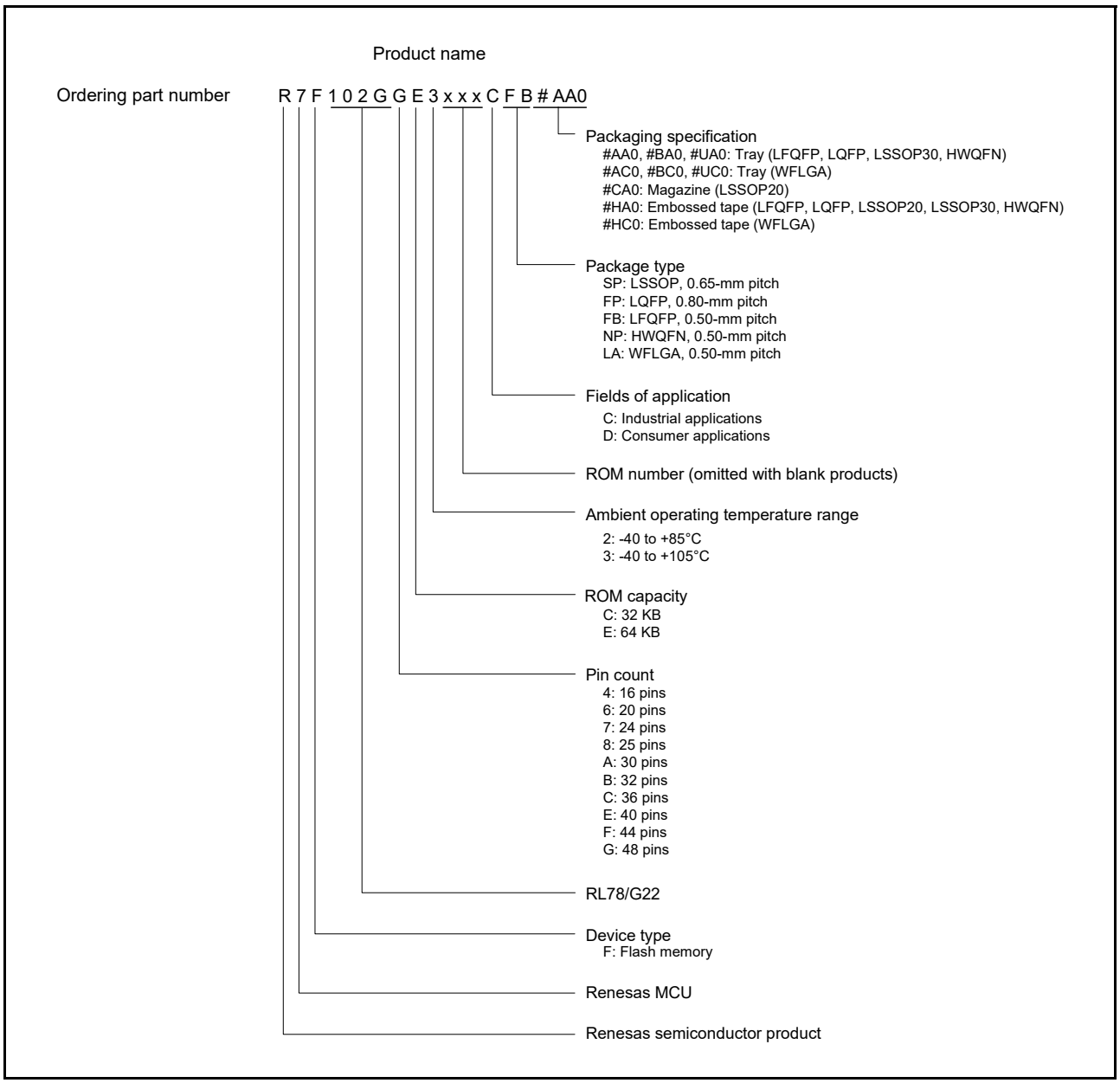
Code flash memory	Data flash memory	RAM	RL78/G22				
			16 pins	20 pins	24 pins	25 pins	30 pins
64 KB	2 KB	4 KB	R7F102G4E	R7F102G6E	R7F102G7E	R7F102G8E	R7F102GAE
32 KB	2 KB	4 KB	R7F102G4C	R7F102G6C	R7F102G7C	R7F102G8C	R7F102GAC

Code flash memory	Data flash memory	RAM	RL78/G22				
			32 pins	36 pins	40 pins	44 pins	48 pins
64 KB	2 KB	4 KB	R7F102GBE	R7F102GCE	R7F102GEE	R7F102GFE	R7F102GGE
32 KB	2 KB	4 KB	R7F102GBC	R7F102GCC	R7F102GEC	R7F102GFC	R7F102GGC

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1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22



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Table 1 - 1 List of Ordering Part Numbers

Pin Count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
16	16-pin plastic HWQFN (3 × 3 mm, 0.50-mm pitch)	C	R7F102G4C3CNP, R7F102G4E3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0016KD-A
		D	R7F102G4C2DNP, R7F102G4E2DNP		
20	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	C	R7F102G6C3CSP, R7F102G6E3CSP	#CA0, #HA0	PLSP0020JB-A
		D	R7F102G6C2DSP, R7F102G6E2DSP		
24	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	C	R7F102G7C3CNP, R7F102G7E3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0024KG-A
		D	R7F102G7C2DNP, R7F102G7E2DNP		
25	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	C	R7F102G8C3CLA, R7F102G8E3CLA	#AC0, #BC0, #UC0, #HC0	PWLG0025KB-A
		D	R7F102G8C2DLA, R7F102G8E2DLA		
30	30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)	C	R7F102GAC3CSP, R7F102GAE3CSP	#AA0, #BA0, #UA0, #HA0	PLSP0030JB-B
		D	R7F102GAC2DSP, R7F102GAE2DSP		
32	32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)	C	R7F102GBC3CNP, R7F102GBE3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0032KE-A
		D	R7F102GBC2DNP, R7F102GBE2DNP		
	32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)	C	R7F102GBC3CFP, R7F102GBE3CFP	#AA0, #BA0, #UA0, #HA0	PLQP0032GB-A, PLQP0032GE-A
		D	R7F102GBC2DFP, R7F102GBE2DFP		
36	36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)	C	R7F102GCC3CLA, R7F102GCE3CLA	#BC0, #AC0, #UC0, #HC0	PWLG0036KB-A
		D	R7F102GCC2DLA, R7F102GCE2DLA		
40	40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)	C	R7F102GEC3CNP, R7F102GEE3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0040KD-A
		D	R7F102GEC2DNP, R7F102GEE2DNP		
44	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	C	R7F102GFC3CFP, R7F102GFE3CFP	#AA0, #BA0, #UA0, #HA0	PLQP0044GC-A, PLQP0044GE-A
		D	R7F102GFC2DFP, R7F102GFE2DFP		
48	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	C	R7F102GGC3CFB, R7F102GGE3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0048KB-B, PLQP0048KL-A
		D	R7F102GGC2DFB, R7F102GGE2DFB		
	48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)	C	R7F102GGC3CNP, R7F102GGE3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0048KC-A
		D	R7F102GGC2DNP, R7F102GGE2DNP		

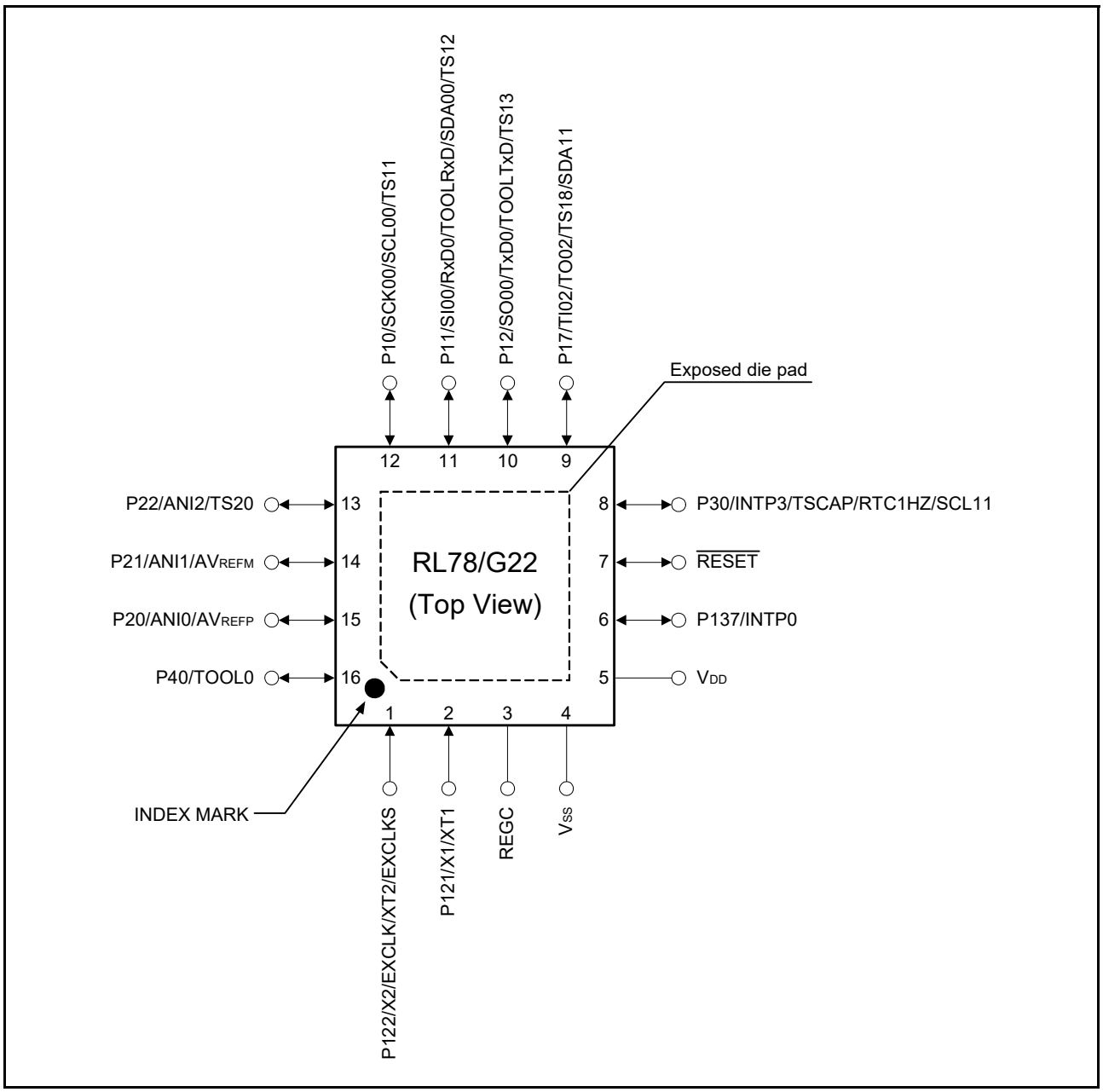
Note For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22**.

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1.3 Pin Configuration (Top View)

1.3.1 16-pin products

- 16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)



Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remark For pin identification, see **1.4 Pin Identification**.

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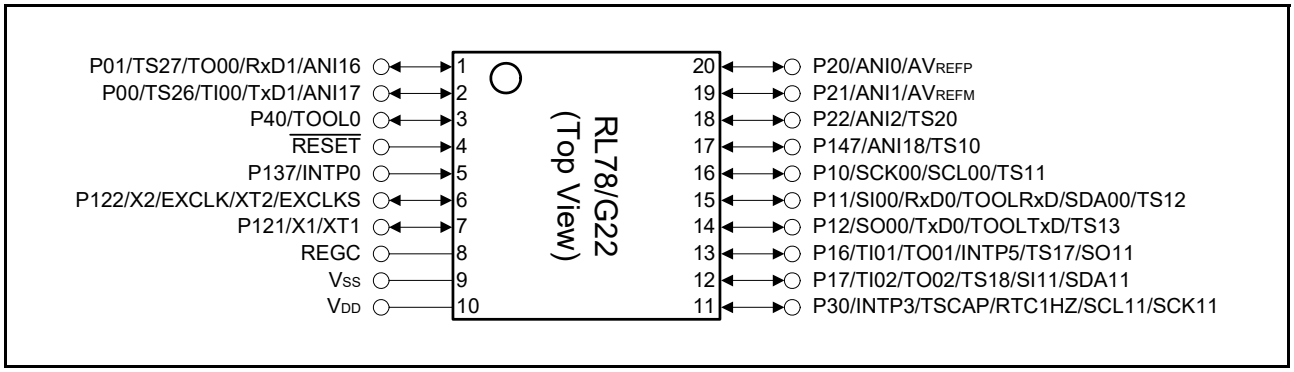
Table 1 - 2 Multiplexed Pin Functions of the 16-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
16HWQFN	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
2	P121	X1/XT1	—	—	—	—	—	—	—	—	—
3	—	REGC	—	—	—	—	—	—	—	—	—
4	—	VSS	—	—	—	—	—	—	—	—	—
5	—	VDD	—	—	—	—	—	—	—	—	—
6	P137	—	—	INTP0	—	—	—	—	—	—	—
7	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
8	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCL11	—	—
9	P17	—	—	—	—	TS18	TI02/TO02	—	SDA11	—	—
10	P12	TOOLTxD	—	—	—	TS13	—	—	SO00/ TxD0	—	—
11	P11	TOOLRxD	—	—	—	TS12	—	—	SI00/RxD0/ SDA00	—	—
12	P10	—	—	—	—	TS11	—	—	SCK00/ SCL00	—	—
13	P22	—	ANI2	—	—	TS20	—	—	—	—	—
14	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
15	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
16	P40	TOOL0	—	—	—	—	—	—	—	—	—

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1.3.2 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)



Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark For pin identification, see **1.4 Pin Identification**.

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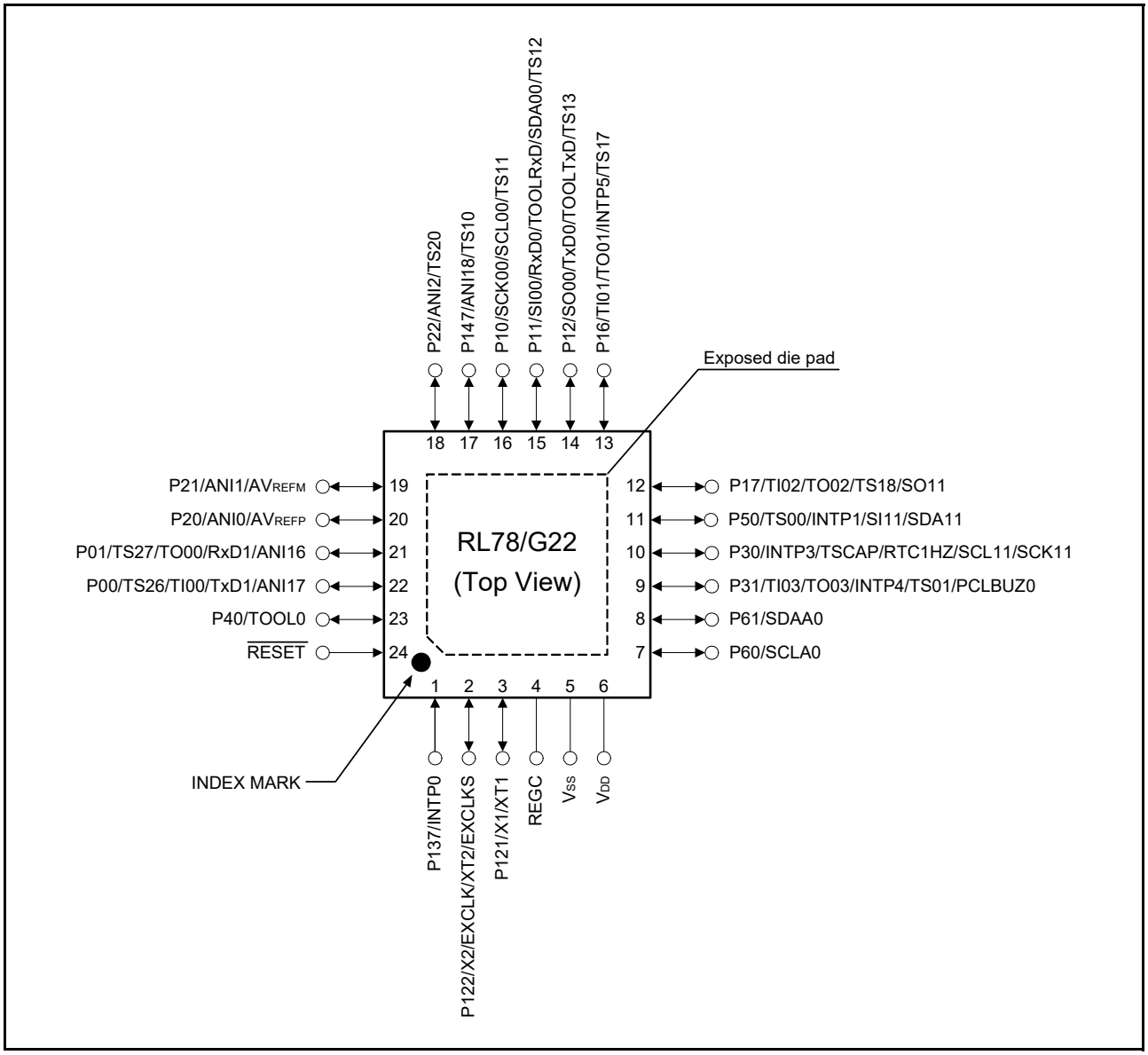
Table 1 - 3 Multiplexed Pin Functions of the 20-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
20LSSOP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P01	—	ANI16	—	—	TS27	TO00	—	RxD1	—	—
2	P00	—	ANI17	—	—	TS26	TI00	—	TxD1	—	—
3	P40	TOOL0	—	—	—	—	—	—	—	—	—
4	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
5	P137	—	—	INTP0	—	—	—	—	—	—	—
6	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
7	P121	X1/XT1	—	—	—	—	—	—	—	—	—
8	—	REGC	—	—	—	—	—	—	—	—	—
9	—	V_{SS}	—	—	—	—	—	—	—	—	—
10	—	V_{DD}	—	—	—	—	—	—	—	—	—
11	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
12	P17	—	—	—	—	TS18	TI02/TO02	—	SI11/ SDA11	—	—
13	P16	—	—	INTP5	—	TS17	TI01/TO01	—	SO11	—	—
14	P12	TOOLTxD	—	—	—	TS13	—	—	SO00/ TxD0	—	—
15	P11	TOOLRxD	—	—	—	TS12	—	—	SI00/RxD0/ SDA00	—	—
16	P10	—	—	—	—	TS11	—	—	SCK00/ SCL00	—	—
17	P147	—	ANI18	—	—	TS10	—	—	—	—	—
18	P22	—	ANI2	—	—	TS20	—	—	—	—	—
19	P21	—	ANI1/ AV_{REFM}	—	—	—	—	—	—	—	—
20	P20	—	ANI0/ AV_{REFP}	—	—	—	—	—	—	—	—

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1.3.3 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.50-mm pitch)



Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark For pin identification, see **1.4 Pin Identification**.

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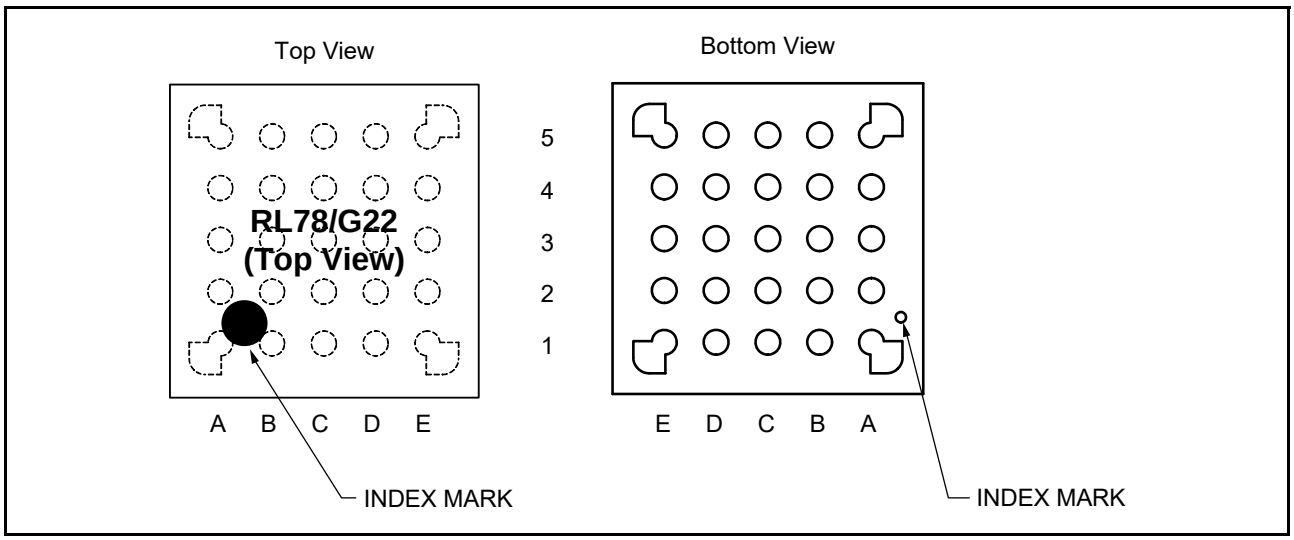
Table 1 - 4 Multiplexed Pin Functions of the 24-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
24HWQFN	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P137	—	—	INTP0	—	—	—	—	—	—	—
2	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
3	P121	X1/XT1	—	—	—	—	—	—	—	—	—
4	—	REGC	—	—	—	—	—	—	—	—	—
5	—	VSS	—	—	—	—	—	—	—	—	—
6	—	VDD	—	—	—	—	—	—	—	—	—
7	P60	—	—	—	—	—	—	—	—	SCLA0	—
8	P61	—	—	—	—	—	—	—	—	SDAA0	—
9	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
10	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
11	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
12	P17	—	—	—	—	TS18	TI02/TO02	—	SO11	—	—
13	P16	—	—	INTP5	—	TS17	TI01/TO01	—	—	—	—
14	P12	TOOLTxD	—	—	—	TS13	—	—	SO00/ TxD0	—	—
15	P11	TOOLRxD	—	—	—	TS12	—	—	SI00/RxD0/ SDA00	—	—
16	P10	—	—	—	—	TS11	—	—	SCK00/ SCL00	—	—
17	P147	—	ANI18	—	—	TS10	—	—	—	—	—
18	P22	—	ANI2	—	—	TS20	—	—	—	—	—
19	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
20	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
21	P01	—	ANI16	—	—	TS27	TO00	—	RxD1	—	—
22	P00	—	ANI17	—	—	TS26	TI00	—	TxD1	—	—
23	P40	TOOL0	—	—	—	—	—	—	—	—	—
24	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—

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1.3.4 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50-mm pitch)



	A	B	C	D	E	
5	P40/TOOL0	$\overline{\text{RESET}}$	P01/TS27/TO00/RxD1/ ANI16	P22/ANI2/TS20	P147/ANI18/TS10	5
4	P122/X2/EXCLK/XT2/ EXCLKS	P137/INTP0	P00/TS26/TI00/TxD1/ ANI17	P21/ANI1/AVREFM	P10/SCK00/SCL00/TS11	4
3	P121/X1/XT1	VDD	P20/ANI0/AVREFP	P12/SO00/TxD0/ TOOLTxD/TS13	P11/SI00/RxD0/ TOOLRxD/SDA00/TS12	3
2	REGC	VSS	P30/INTP3/TSCAP/ RTC1HZ/SCL11/SCK11	P17/TI02/TO02/TS18/ SO11	P50/TS00/INTP1/SI11/ SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/TO03/INTP4/ TS01/PCLBUZ0	P16/TI01/TO01/INTP5/ TS17	P130/TS19	1
	A	B	C	D	E	

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark For pin identification, see **1.4 Pin Identification**.

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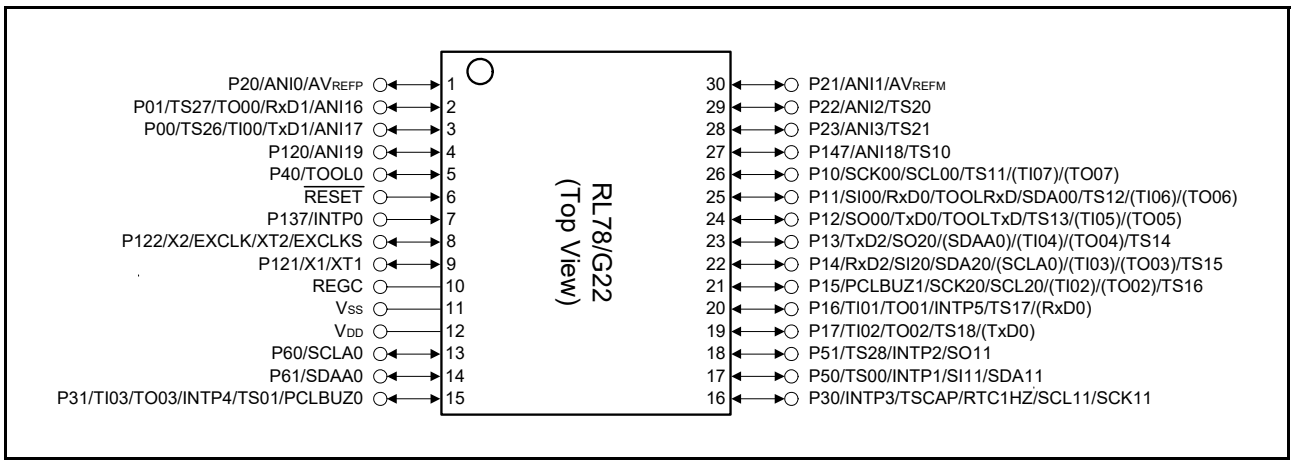
Table 1 - 5 Multiplexed Pin Functions of the 25-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
25WFLGA	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
A1	P60	—	—	—	—	—	—	—	—	SCLA0	—
A2	—	REGC	—	—	—	—	—	—	—	—	—
A3	P121	X1/XT1	—	—	—	—	—	—	—	—	—
A4	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
A5	P40	TOOL0	—	—	—	—	—	—	—	—	—
B1	P61	—	—	—	—	—	—	—	—	SDAA0	—
B2	—	VSS	—	—	—	—	—	—	—	—	—
B3	—	VDD	—	—	—	—	—	—	—	—	—
B4	P137	—	—	INTP0	—	—	—	—	—	—	—
B5	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
C1	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
C2	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
C3	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
C4	P00	—	ANI17	—	—	TS26	TI00	—	TxD1	—	—
C5	P01	—	ANI16	—	—	TS27	TO00	—	RxD1	—	—
D1	P16	—	—	INTP5	—	TS17	TI01/TO01	—	—	—	—
D2	P17	—	—	—	—	TS18	TI02/TO02	—	SO11	—	—
D3	P12	TOOLTxD	—	—	—	TS13	—	—	SO00/ TxD0	—	—
D4	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
D5	P22	—	ANI2	—	—	TS20	—	—	—	—	—
E1	P130	—	—	—	—	TS19	—	—	—	—	—
E2	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
E3	P11	TOOLRxD	—	—	—	TS12	—	—	SI00/RxD0/ SDA00	—	—
E4	P10	—	—	—	—	TS11	—	—	SCK00/ SCL00	—	—
E5	P147	—	ANI18	—	—	TS10	—	—	—	—	—

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1.3.5 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

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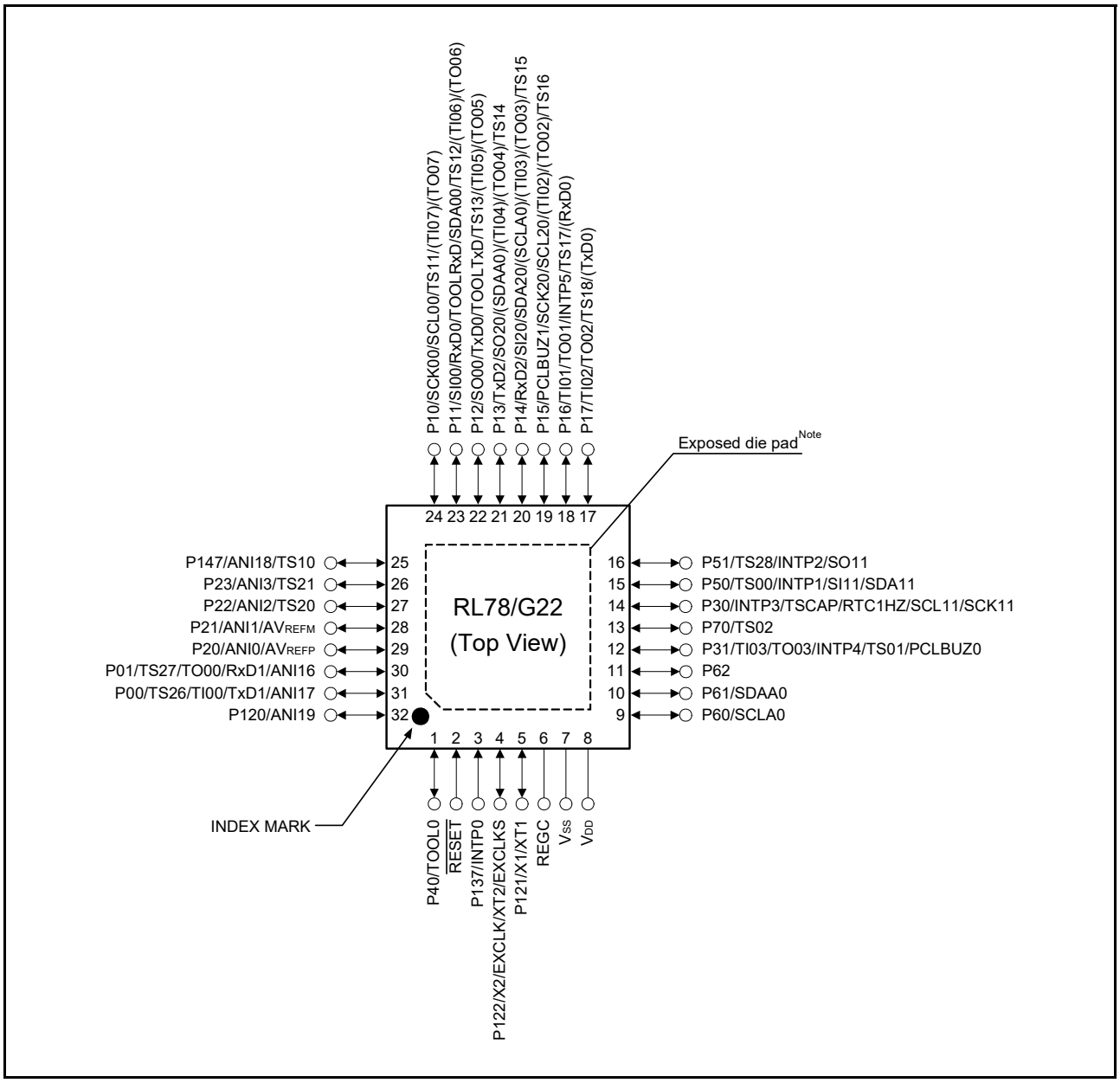
Table 1 - 6 Multiplexed Pin Functions of the 30-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
30LSSOP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
2	P01	—	ANI16	—	—	TS27	TO00	—	RxD1	—	—
3	P00	—	ANI17	—	—	TS26	TI00	—	TxD1	—	—
4	P120	—	ANI19	—	—	—	—	—	—	—	—
5	P40	TOOL0	—	—	—	—	—	—	—	—	—
6	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
7	P137	—	—	INTP0	—	—	—	—	—	—	—
8	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
9	P121	X1/XT1	—	—	—	—	—	—	—	—	
10	—	REGC	—	—	—	—	—	—	—	—	—
11	—	VSS	—	—	—	—	—	—	—	—	—
12	—	VDD	—	—	—	—	—	—	—	—	—
13	P60	—	—	—	—	—	—	—	—	SCLA0	—
14	P61	—	—	—	—	—	—	—	—	SDAA0	—
15	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03			—	—
16	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
17	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
18	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
19	P17	—	—		—	TS18	TI02/TO02	—	(TxD0)	—	—
20	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
21	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
22	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
23	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
24	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
25	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
26	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
27	P147	—	ANI18	—	—	TS10	—	—	—	—	—
28	P23	—	ANI3	—	—	TS21	—	—	—	—	—
29	P22	—	ANI2	—	—	TS20	—	—	—	—	—
30	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—

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1.3.6 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)
- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)



Note The 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch) products do not have an exposed die pad.

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to VSS.

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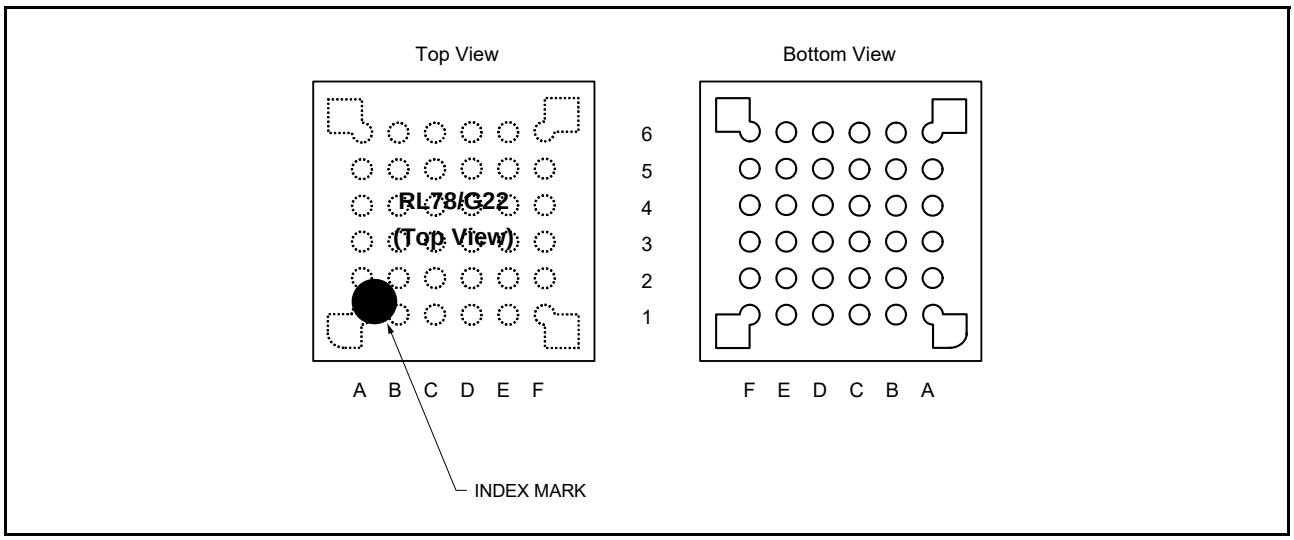
Table 1 - 7 Multiplexed Pin Functions of the 32-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
32HWQFN 32LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	TOOL0	—	—	—	—	—	—	—	—	—
2	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
3	P137	—	—	INTP0	—	—	—	—	—	—	—
4	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
5	P121	X1/XT1	—	—	—	—	—	—	—	—	—
6	—	REGC	—	—	—	—	—	—	—	—	—
7	—	VSS	—	—	—	—	—	—	—	—	—
8	—	VDD	—	—	—	—	—	—	—	—	—
9	P60	—	—	—	—	—	—	—	—	SCLA0	—
10	P61	—	—	—	—	—	—	—	—	SDAA0	—
11	P62	—	—	—	—	—	—	—	—	—	—
12	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
13	P70	—	—	—	—	TS02	—	—	—	—	—
14	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
15	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
16	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
17	P17	—	—		—	TS18	TI02/TO02	—	(TxD0)	—	—
18	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
19	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
20	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
21	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
22	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
23	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
24	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
25	P147	—	ANI18	—	—	TS10	—	—	—	—	—
26	P23	—	ANI3	—	—	TS21	—	—	—	—	—
27	P22	—	ANI2	—	—	TS20	—	—	—	—	—
28	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
29	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
30	P01	—	ANI16	—	—	TS27	TO00	—	RxD1	—	—
31	P00	—	ANI17	—	—	TS26	TI00	—	TxD1	—	—
32	P120	—	ANI19	—	—	—	—	—	—	—	—

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1.3.7 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)



	A	B	C	D	E	F
6	P60/SCLA0	VDD	P121/X1/XT1	P122/X2/EXCLK/ XT2/EXCLKS	P137/INTP0	P40/TOOL0
5	P62	P61/SDAA0	VSS	REGC	$\overline{\text{RESET}}$	P120/ANI19
4	P72/TS04/SO21/ TxDA0	P71/TS03/SI21/ SDA21/RxDA0	P14/RxD2/SI20/ SDA20/(SCLA0)/ (TI03)/(TO03)/TS15	P31/TI03/TO03/ INTP4/TS01/ PCLBUZ0	P00/TS26/TI00/ TxD1	P01/TS27/TO00/ RxD1
3	P50/TS00/INTP1/ SI11/SDA11	P70/TS02/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)/TS16	P22/ANI2/TS20	P20/ANI0/AVREFP	P21/ANI1/AVREFM
2	P30/INTP3/TSCAP/ RTC1HZ/SCL11/ SCK11	P16/TI01/TO01/ INTP5/TS17/(RxD0)	P12/SO00/TxD0/ TOOLTxD/TS13/ (TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/SDA00/ TS12/(TI06)/(TO06)	P24/ANI4/TS22	P23/ANI3/TS21
1	P51/TS28/INTP2/ SO11	P17/TI02/TO02/ TS18/(TxD0)	P13/TxD2/SO20/ (SDAA0)/(TI04)/ (TO04)/TS14	P10/SCK00/SCL00/ TS11/(TI07)/(TO07)	P147/ANI18/TS10	P25/ANI5/TS23

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

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Table 1 - 8 Multiplexed Pin Functions of the 36-pin Products (1/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
36WFLGA	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
A1	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
A2	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
A3	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
A4	P72	—	—	—	—	TS04	—	—	SO21	—	TxDA0
A5	P62	—	—	—	—	—	—	—	—	—	—
A6	P60	—	—	—	—	—	—	—	—	SCLA0	—
B1	P17	—	—	—	—	TS18	TI02/TO02	—	(TxD0)	—	—
B2	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
B3	P70	—	—	—	—	TS02	—	—	SCK21/ SCL21	—	—
B4	P71	—	—	—	—	TS03	—	—	SI21/ SDA21	—	RxDA0
B5	P61	—	—	—	—	—	—	—	—	SDAA0	—
B6	—	V_{DD}	—	—	—	—	—	—	—	—	—
C1	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
C2	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
C3	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
C4	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
C5	—	V_{SS}	—	—	—	—	—	—	—	—	—
C6	P121	X1/XT1	—	—	—	—	—	—	—	—	—
D1	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
D2	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
D3	P22	—	ANI2	—	—	TS20	—	—	—	—	—
D4	P31	PCLBUZ0	—	INTP4		TS01	TI03/TO03	—	—	—	—
D5	—	REGC	—	—	—	—	—	—	—	—	—
D6	P122	X2/XT2/EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—
E1	P147	—	ANI18	—	—	TS10	—	—	—	—	—
E2	P24	—	ANI4	—	—	TS22	—	—	—	—	—
E3	P20	—	ANI0/ AV_{REFP}	—	—	—	—	—	—	—	—
E4	P00	—	—	—	—	TS26	TI00	—	TxD1	—	—
E5	—	$\overline{RESET}$	—	—	—	—	—	—	—	—	—
E6	P137	—	—	INTP0		—	—	—	—	—	—
F1	P25	—	ANI5	—	—	TS23	—	—	—	—	—

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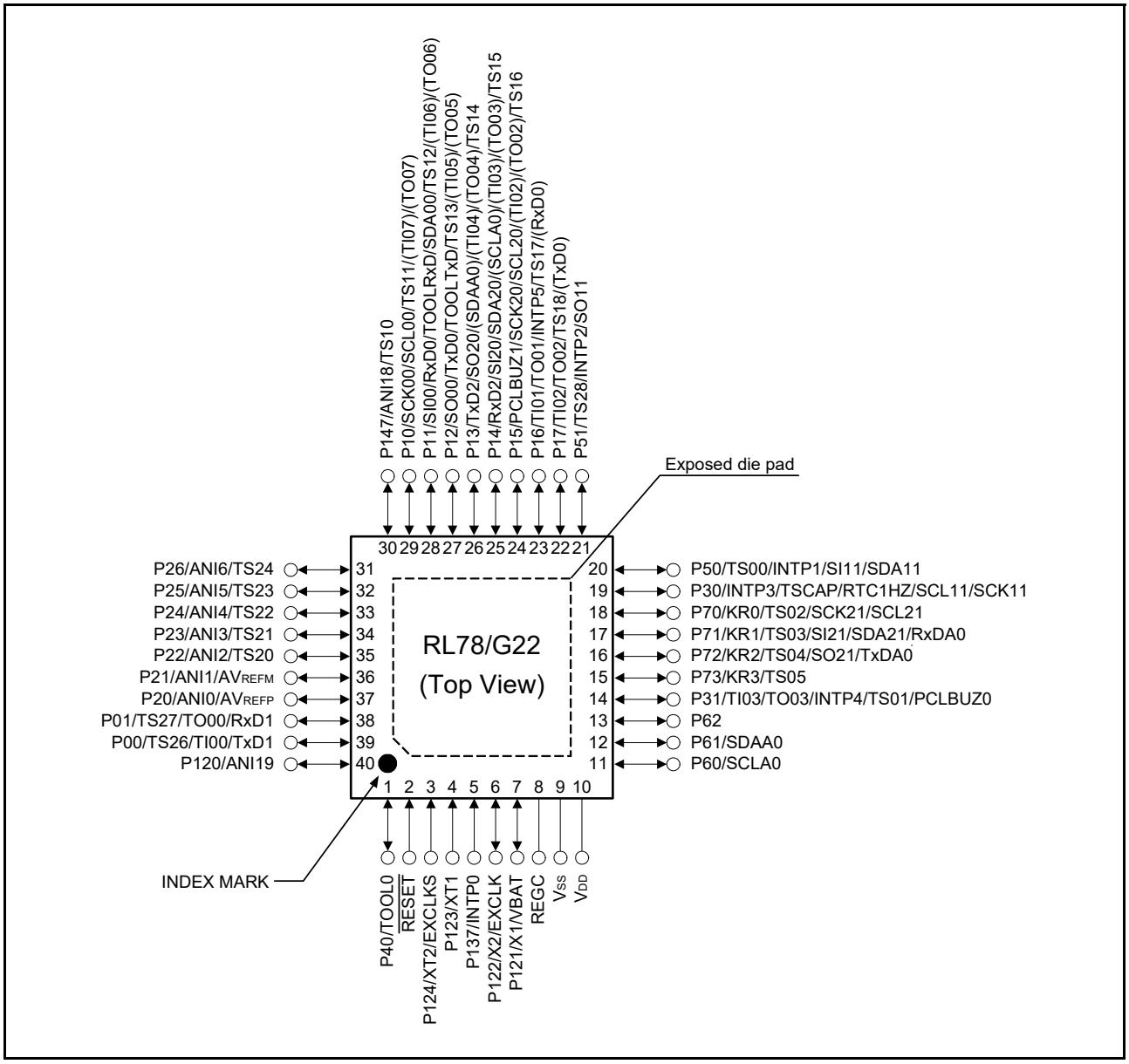
Table 1 - 8 Multiplexed Pin Functions of the 36-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
36WFLGA	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
F2	P23	—	ANI3	—	—	TS21	—	—	—	—	—
F3	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
F4	P01	—	—	—	—	TS27	TO00		RxD1	—	—
F5	P120	—	ANI19	—	—	—	—	—	—	—	—
F6	P40	TOOL0	—	—	—	—	—	—	—	—	—

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1.3.8 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to Vss.

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Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
40HWQFN	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	TOOL0	—	—	—	—	—	—	—	—	—
2	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
3	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
4	P123	XT1	—	—	—	—	—	—	—	—	—
5	P137	—	—	INTP0	—	—	—	—	—	—	—
6	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
7	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
8	—	REGC	—	—	—	—	—	—	—	—	—
9	—	VSS	—	—	—	—	—	—	—	—	—
10	—	VDD	—	—	—	—	—	—	—	—	—
11	P60	—	—	—	—	—	—	—	—	SCLA0	—
12	P61	—	—	—	—	—	—	—	—	SDAA0	—
13	P62	—	—	—	—	—	—	—	—	—	—
14	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
15	P73	—	—	—	KR3	TS05	—	—	—	—	—
<R> 16	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0
17	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0
18	P70	—	—	—	KR0	TS02	—	—	SCK21/ SCL21	—	—
19	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
20	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
21	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
22	P17	—	—	—	—	TS18	TI02/TO02	—	(TxD0)	—	—
23	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
24	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
25	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
26	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
27	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
28	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
29	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
30	P147	—	ANI18	—	—	TS10	—	—	—	—	—
31	P26	—	ANI6	—	—	TS24	—	—	—	—	—
32	P25	—	ANI5	—	—	TS23	—	—	—	—	—
33	P24	—	ANI4	—	—	TS22	—	—	—	—	—

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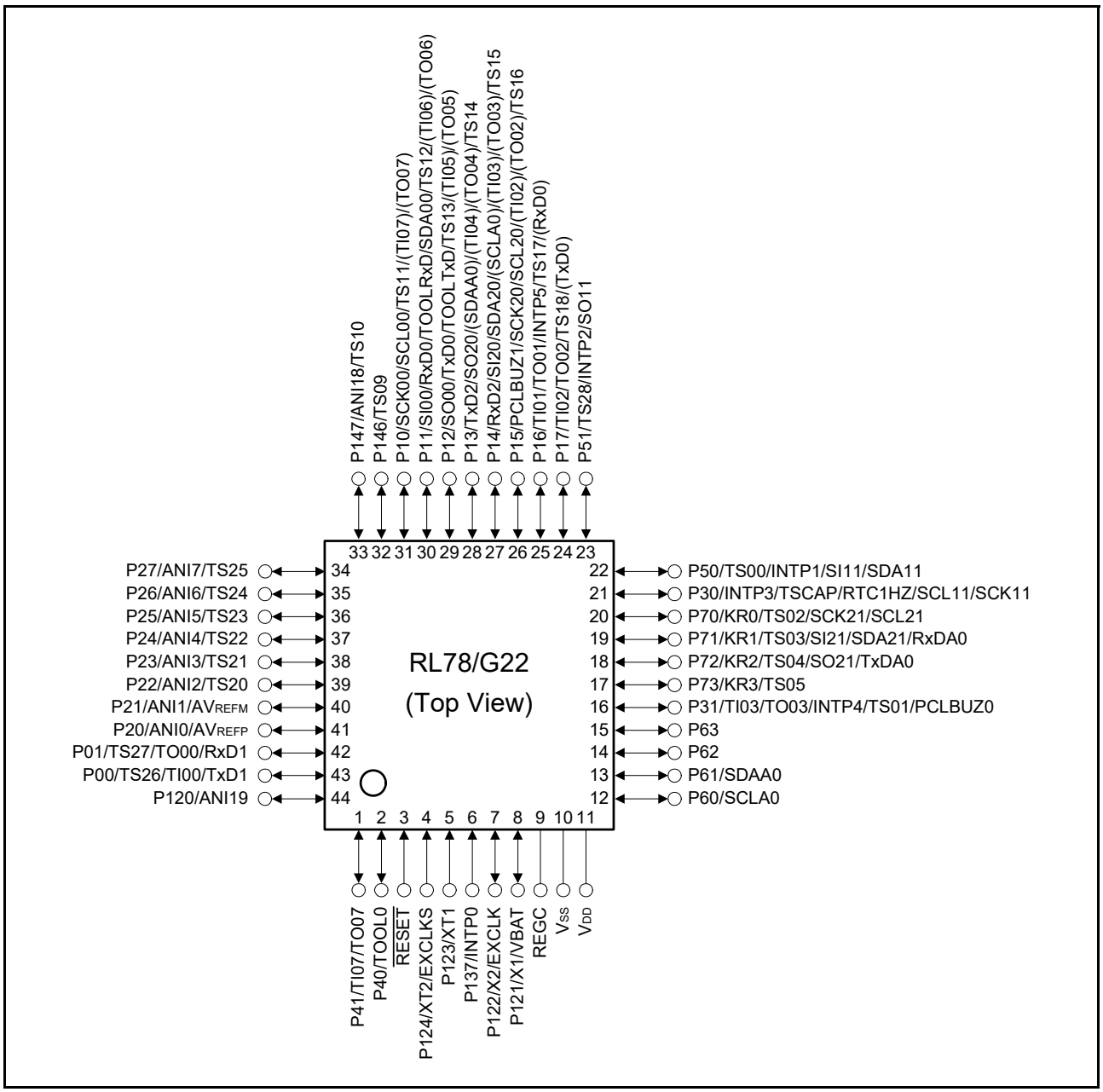
Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
40HWQFN	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
34	P23	—	ANI3	—	—	TS21	—	—	—	—	—
35	P22	—	ANI2	—	—	TS20	—	—	—	—	—
36	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
37	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
38	P01	—	—	—	—	TS27	TO00	—	RxD1	—	—
39	P00	—	—	—	—	TS26	TI00	—	TxD1	—	—
40	P120	—	ANI19	—	—	—	—	—	—	—	—

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1.3.9 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

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Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (1/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P41	—	—	—	—	—	TI07/TO07	—	—	—	—
2	P40	TOOL0	—	—	—	—	—	—	—	—	—
3	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
4	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
5	P123	XT1	—	—	—	—	—	—	—	—	—
6	P137	—	—	INTP0	—	—	—	—	—	—	—
7	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
8	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
9	—	REGC	—	—	—	—	—	—	—	—	—
10	—	V_{SS}	—	—	—	—	—	—	—	—	—
11	—	V_{DD}	—	—	—	—	—	—	—	—	—
12	P60	—	—	—	—	—	—	—	—	SCLA0	—
13	P61	—	—	—	—	—	—	—	—	SDAA0	—
14	P62	—	—	—	—	—	—	—	—	—	—
15	P63	—	—	—	—	—	—	—	—	—	—
16	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
17	P73	—	—	—	KR3	TS05	—	—	—	—	—
<R> 18	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0
19	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0
20	P70	—	—	—	KR0	TS02	—	—	SCK21/ SCL21	—	—
21	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
22	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
23	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
24	P17	—	—	—	—	TS18	TI02/TO02	—	(TxD0)	—	—
25	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
26	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
27	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
28	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
29	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
30	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
31	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
32	P146	—	—	—	—	TS09	—	—	—	—	—
33	P147	—	ANI18	—	—	TS10	—	—	—	—	—

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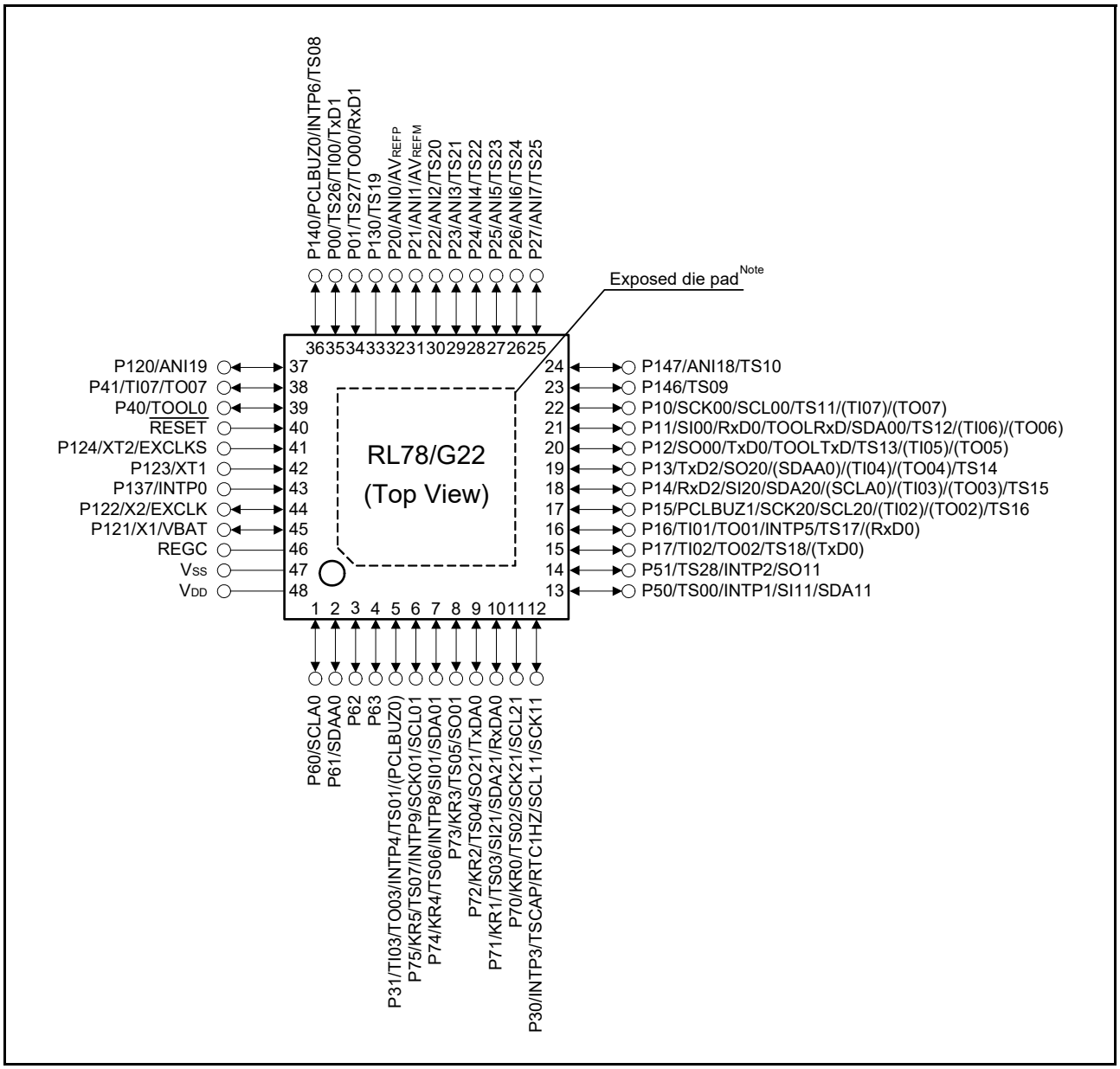
Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
34	P27	—	ANI7	—	—	TS25	—	—	—	—	—
35	P26	—	ANI6	—	—	TS24	—	—	—	—	—
36	P25	—	ANI5	—	—	TS23	—	—	—	—	—
37	P24	—	ANI4	—	—	TS22	—	—	—	—	—
38	P23	—	ANI3	—	—	TS21	—	—	—	—	—
39	P22	—	ANI2	—	—	TS20	—	—	—	—	—
40	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—
41	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
42	P01	—	—	—	—	TS27	TO00	—	RxD1	—	—
43	P00	—	—	—	—	TS26	TI00	—	TxD1	—	—
44	P120	—	ANI19	—	—	—	—	—	—	—	—

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1.3.10 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)



Note The 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **4.3.9 Peripheral I/O redirection register (PIOR)** in the RL78/G22 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to Vss.

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Table 1 - 11 Multiplexed Pin Functions of the 48-pin Products (1/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
48HWQFN 48LFQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P60	—	—	—	—	—	—	—	—	SCLA0	—
2	P61	—	—	—	—	—	—	—	—	SDAA0	—
3	P62	—	—	—	—	—	—	—	—	—	—
4	P63	—	—	—	—	—	—	—	—	—	—
5	P31	(PCLBUZ0)	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
6	P75	—	—	INTP9	KR5	TS07	—	—	SCK01/ SCL01	—	—
7	P74	—	—	INTP8	KR4	TS06	—	—	SI01/ SDA01	—	—
8	P73	—	—	—	KR3	TS05	—	—	SO01	—	—
9	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0
10	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0
11	P70	—	—	—	KR0	TS02	—	—	SCK21/ SCL21	—	—
12	P30	—	—	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—
13	P50	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—
14	P51	—	—	INTP2	—	TS28	—	—	SO11	—	—
15	P17	—	—	—	—	TS18	TI02/TO02	—	(TxD0)	—	—
16	P16	—	—	INTP5	—	TS17	TI01/TO01	—	(RxD0)	—	—
17	P15	PCLBUZ1	—	—	—	TS16	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—
18	P14	—	—	—	—	TS15	(TI03)/ (TO03)	—	SI20/RxD2/ SDA20	(SCLA0)	—
19	P13	—	—	—	—	TS14	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—
20	P12	TOOLTxD	—	—	—	TS13	(TI05)/ (TO05)	—	SO00/ TxD0	—	—
21	P11	TOOLRxD	—	—	—	TS12	(TI06)/ (TO06)	—	SI00/RxD0/ SDA00	—	—
22	P10	—	—	—	—	TS11	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—
23	P146	—	—	—	—	TS09	—	—	—	—	—
24	P147	—	ANI18	—	—	TS10	—	—	—	—	—
25	P27	—	ANI7	—	—	TS25	—	—	—	—	—
26	P26	—	ANI6	—	—	TS24	—	—	—	—	—
27	P25	—	ANI5	—	—	TS23	—	—	—	—	—
28	P24	—	ANI4	—	—	TS22	—	—	—	—	—
29	P23	—	ANI3	—	—	TS21	—	—	—	—	—
30	P22	—	ANI2	—	—	TS20	—	—	—	—	—
31	P21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—

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Table 1 - 11 Multiplexed Pin Functions of the 48-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
48HWQFN 48LFQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
32	P20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—
33	P130	—	—	—	—	TS19	—	—	—	—	—
34	P01	—	—	—	—	TS27	TO00	—	RxD1	—	—
35	P00	—	—	—	—	TS26	TI00	—	TxD1	—	—
36	P140	PCLBUZ0	—	INTP6	—	TS08	—	—	—	—	—
37	P120	—	ANI19	—	—	—	—	—	—	—	—
38	P41	—	—	—	—	—	TI07/TO07	—	—	—	—
39	P40	TOOL0	—	—	—	—	—	—	—	—	—
40	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
41	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
42	P123	XT1	—	—	—	—	—	—	—	—	—
43	P137	—	—	INTP0	—	—	—	—	—	—	—
44	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
45	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
46	—	REGC	—	—	—	—	—	—	—	—	—
47	—	VSS	—	—	—	—	—	—	—	—	—
48	—	VDD	—	—	—	—	—	—	—	—	—

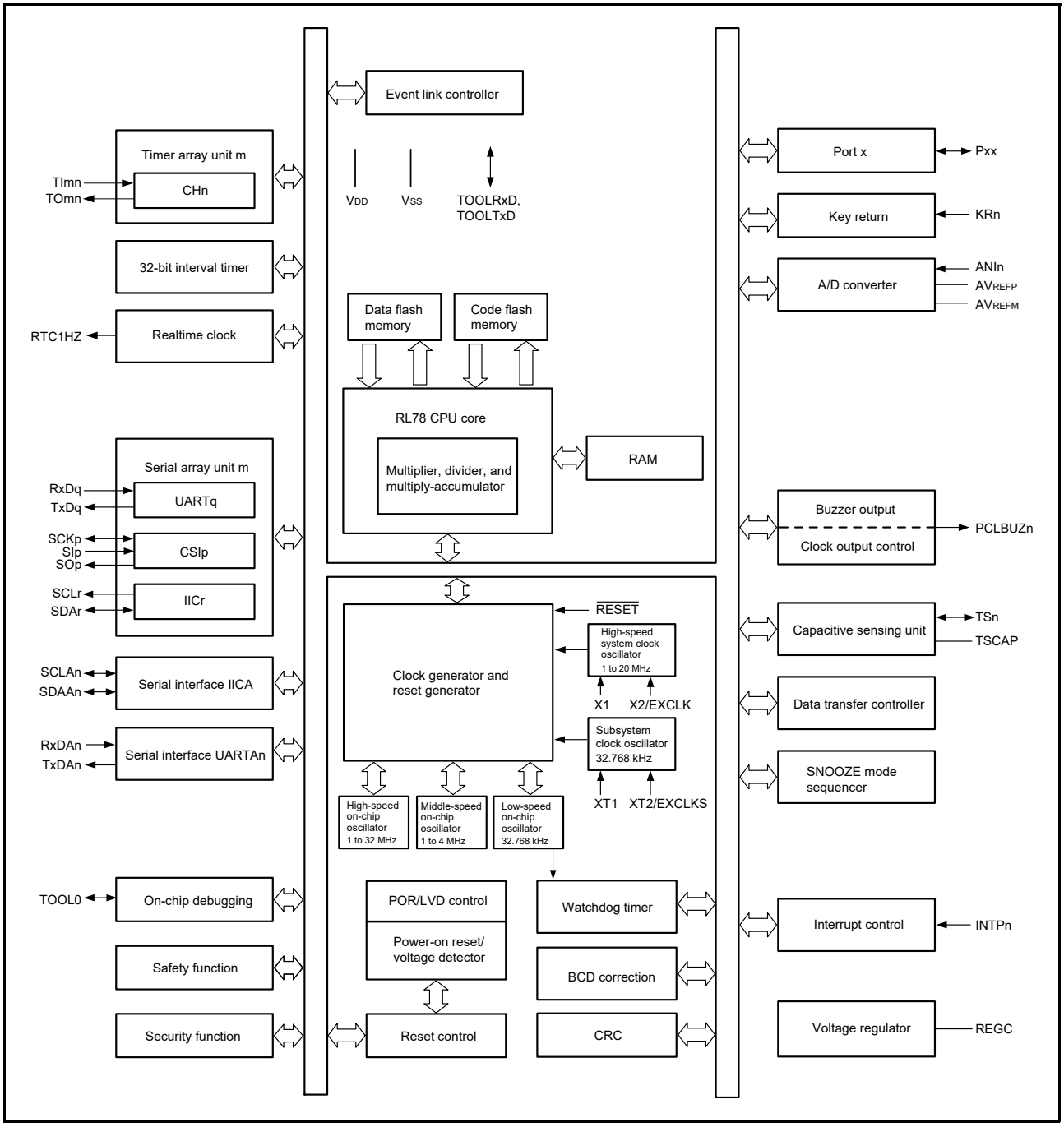
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1.4 Pin Identification

ANI0 to ANI7,		RxD0 to RxD2,	
ANI16 to ANI19	: Analog input	RxDA0	: Receive data
AV_{REFM}	: Analog reference voltage minus	SCLA0,	
AV_{REFP}	: Analog reference voltage plus	SCK00, SCK01,	
EXCLK	: External clock input	SCK11, SCK20, SCK21	: Serial clock input/output
	(main system clock)	SCL00, SCL01,	
EXCLKS	: External clock input	SCL11, SCL20,	
	(subsystem clock)	SCL21	: Serial clock output
INTP0 to INTP6, INTP8,		SDAA0, SDA00,	
INTP9	: Interrupt request from peripheral	SDA01, SDA11,	
KR0 to KR5	: Key return input	SDA20, SDA21	: Serial data input/output
P00, P01	: Port 0	SI00, SI01, SI11,	
P10 to P17	: Port 1	SI20, SI21	: Serial data input
P20 to P27	: Port 2	SO00, SO01	
P30, P31	: Port 3	SO11, SO20, SO21	: Serial data output
P40, P41	: Port 4	TSCAP	: Touch sensor capacitance
P50, P51	: Port 5	TI00 to TI07	: Timer input
P60 to P63	: Port 6	TO00 to TO07	: Timer output
P70 to P75	: Port 7	TOOL0	: Data input/output for tool
P120 to P124	: Port 12	TOOLRxD, TOOLTxD	: Data input/output for external device
P130, P137	: Port 13	TS00 to TS28	: Capacitive touch sensor
P140, P146, P147	: Port 14	TxD0 to TxD2	
PCLBUZ0, PCLBUZ1	: Programmable clock output/buzzer	TxDA0	: Transmit data
	output	VBAT	: Battery backup power supply
REGC	: Regulator capacitance	V_{DD}	: Power supply
$\overline{\text{RESET}}$	: Reset	V_{SS}	: Ground
RTC1HZ	: Realtime clock correction clock (1 Hz)	X1, X2	: Crystal oscillator (main system clock)
	output	XT1, XT2	: Crystal oscillator (subsystem clock)

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1.5 Block Diagram



Caution 1. The serial interface IICA is only incorporated in the 24- to 48-pin products.

Caution 2. The serial interface UARTAn is only incorporated in the 36- to 48-pin products.

Caution 3. The key return function is only incorporated in the 40- to 48-pin products.

Remark m: Unit number, n: Channel number, p: Simplified SPI (CSI) number, q: UART number, r: Simplified I^2C number, xx: Port number

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1.6 Outline of Functions

Caution This outline describes the functions at the time when the peripheral I/O redirection register (PIOR) is set to 00H.

(1/4)

Item		16-pin R7F102G4x	20-pin R7F102G6x	24-pin R7F102G7x	25-pin R7F102G8x	30-pin R7F102GAx	32-pin R7F102GBx	36-pin R7F102GCx	40-pin R7F102GEx	44-pin R7F102GFx	48-pin R7F102GGx
Code flash memory		32 or 64 KB									
Data flash memory		2 KB									
RAM		4 KB									
Address space		1 Mbyte									
CPU/ peripheral hardware clock frequency (f_{CLK})	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz[Note 1] (V_{DD} = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (V_{DD} = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz[Note 1] (V_{DD} = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz[Note 1] (V_{DD} = 1.6 to 5.5 V)									
	Subsystem clock	SUB mode: 32.768 kHz (V_{DD} = 1.6 to 5.5 V)									
Main system clock	High-speed system clock (f_{MX})	1 to 20 MHz									
	High-speed on-chip oscillator clock (f_{IH})	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz									
	Middle-speed on-chip oscillator clock (f_{IM})	1 MHz, 2 MHz, 4 MHz									
Subsystem clock	Subsystem clock X (f_{SX})	32.768 kHz (V_{DD} = 2.4 to 5.5 V)							32.768 kHz (V_{DD} = 1.6 to 5.5 V)		
	Low-speed on-chip oscillator clock (f_{IL})	32.768 kHz (typ.)									
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)									
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (f_{IH}))									
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.									

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(2/4)

Item		16-pin	20-pin	24-pin	25-pin	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F102G4x	R7F102G6x	R7F102G7x	R7F102G8x	R7F102GAx	R7F102GBx	R7F102GCx	R7F102GEx	R7F102GFx	R7F102GGx
I/O port	Total number of pins	12	16	20	21	26	28	32	36	40	44
	CMOS I/O	11 (N-ch open-drain I/O [withstand voltage of VDD]: 4)	15 (N-ch open-drain I/O [withstand voltage of VDD]: 5)	17 (N-ch open-drain I/O [withstand voltage of VDD]: 6)		23 (N-ch open-drain I/O [withstand voltage of VDD]: 10)	24 (N-ch open-drain I/O [withstand voltage of VDD]: 10)	28 (N-ch open-drain I/O [withstand voltage of VDD]: 12)	30 (N-ch open-drain I/O [withstand voltage of VDD]: 12)	33 (N-ch open-drain I/O [withstand voltage of VDD]: 12)	36 (N-ch open-drain I/O [withstand voltage of VDD]: 13)
	CMOS input	1							3		
	CMOS output	—			1	—		1			
	N-ch open-drain I/O (withstand voltage of 6 V)	—		2			3			4	
Timers	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Realtime clock (RTC)	1 channel									
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode									
	Timer output	1 channel (PWM output: 1)	3 channels (PWM outputs: 2Note 2)	4 channels (PWM outputs: 3Note 2)		4 channels (PWM outputs: 3Note 2), 8 channels (PWM outputs: 7Note 2)Note 3					
	RTC output	1 channel									
Clock output/buzzer output		2									
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fSXP))									
8-/10-bit resolution A/D converter		3 channels	6 channels			8 channels			9 channels	10 channels	

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(3/4)

Item		16-pin	20-pin	24-pin	25-pin	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F102G4x	R7F102G6x	R7F102G7x	R7F102G8x	R7F102GAx	R7F102GBx	R7F102GCx	R7F102GEx	R7F102GFx	R7F102GGx
Serial interfaces		[16-pin products] • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified I²C: 1 channel									
		[20- to 25-pin products] • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel									
		[30- and 32-pin products] • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART (UART supporting LIN-bus): 1 channel									
		[36- to 44-pin products] • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 2 channels, simplified I²C: 2 channels, UART (UART supporting LIN-bus): 1 channel									
		[48-pin products] • Simplified SPI (CSI): 2 channels, simplified I²C: 2 channels, UART: 1 channel • Simplified SPI (CSI): 1 channel, simplified I²C: 1 channel, UART: 1 channel • Simplified SPI (CSI): 2 channels, simplified I²C: 2 channels, UART (UART supporting LIN-bus): 1 channel									
	UARTA	—						1 channel			
	I²C bus	—		1 channel							
Data transfer controller (DTC)		21 sources	23 sources	25 sources		28 sources		30 sources	31 sources		32 sources
Event link controller (ELC)	Event inputs	11	12	14		15		17	18		19
	Event trigger outputs	7									
SNOOZE mode sequencer (SMS)		1									
Capacitive sensing unit		5	9	11	12	16	17	21	23	25	29
Vectored interrupt sources	Internal	23	25	26		29		32			
	External	2	3	5		6			7		10
Key interrupt		—							4		6
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution**Note 4** • Internal reset by RAM parity error • Internal reset by illegal-memory access									
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)									
Voltage detector	LVD0	Detection voltage • Rising edge: 1.67 to 4.00 V (6 stages) • Falling edge: 1.63 to 3.92 V (6 stages)									
	LVD1	Detection voltage • Rising edge: 1.67 to 4.16 V (18 stages) • Falling edge: 1.63 to 4.08 V (18 stages)									
On-chip debugging		Available									
Power supply voltage		V_{DD} = 1.6 to 5.5 V									

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(4/4)

Item	16-pin	20-pin	24-pin	25-pin	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
	R7F102G4x	R7F102G6x	R7F102G7x	R7F102G8x	R7F102GAx	R7F102GBx	R7F102GCx	R7F102GEx	R7F102GFx	R7F102GGx
Operating ambient temperature	T_A = –40 to +85°C (2D: Consumer applications), T_A = –40 to +105°C (3C: Industrial applications)									

Note 1. Ensure that the operating voltage is at least 1.8 V during overwriting of the flash memory.

Note 2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G22 User's Manual.

Note 3. This applies when the corresponding bit in the peripheral I/O redirection register (PIOR) is set to 1.

Note 4. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

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2. Electrical Characteristics

This section describes the electrical characteristics of the following products.

- 2D: Consumer applications, T_A = -40 to +85°C
  R7F102Gxx2Dxx
- 3C: Industrial applications, T_A = -40 to +105°C
  R7F102Gxx3Cxx

Caution 1. This MCU has on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

Caution 2. For the consumer application products, the ambient operating temperature of T_A = -40 to +85°C applies. Note that the characteristics of the A/D converter for each of the ranges of ambient operating temperature are described in the following sections.
2.6.1 Characteristics of the A/D converter for T_A = -40 to +85°C
2.6.2 Characteristics of the A/D converter for T_A = -40 to +105°C

Caution 3. The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product in the RL78/G22 User's Manual.

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2.1 Absolute Maximum Ratings

(1/2)

Item	Symbols	Conditions		Ratings	Unit
Supply voltage	V_{DD}			-0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC		-0.3 to +2.1 and -0.3 to V_{DD} + 0.3 **Note 1**	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147		-0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{I2}	P60 to P63 (N-ch open-drain)		-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		-0.3 to V_{DD} + 0.3 **Note 2**	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P130, P140, P146, P147		-0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{O2}	P20 to P27, P121, P122		-0.3 to V_{DD} + 0.3 **Note 2**	V
Analog input voltage	V_{AI1}	ANI16 to ANI19		-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 **Notes 2, 3**	V
	V_{AI2}	ANI0 to ANI7		-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 **Notes 2, 3**	V
High-level output current	I_{OH1}	Per pin	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147	-40	mA
		Total of all pins -170 mA	P00, P01, P40, P41, P120, P130, P140	-70	mA
			P10 to P17, P30, P31, P50, P51, P70 to P75, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121, P122	-5	mA
		Total of all pins		-20	mA
Low-level output current	I_{OL1}	Per pin	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147	40	mA
		Total of all pins 170 mA	P00, P01, P40, P41, P120, P130, P140	70	mA
			P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121, P122	10	mA
		Total of all pins		20	mA

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AV_{REFP} + 0.3.

(Caution and Remarks are listed on the next page.)

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(2/2)

Item	Symbols	Conditions		Ratings	Unit
Ambient operating temperature	T_A	In normal operation mode	3C: Industrial applications	-40 to +105	°C
			2D: Consumer applications	-40 to +85	
		In flash memory programming mode	3C: Industrial applications	-40 to +105	
			2D: Consumer applications	-40 to +85	
Storage temperature	T_{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. AV_{REFP} refers to the positive reference voltage of the A/D converter.

Remark 3. The reference voltage is V_{SS}.

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2.2 Characteristics of the Oscillators

2.2.1 Characteristics of the X1 oscillator

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time[Note]	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See **2.4 AC Characteristics** for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.**

2.2.2 Characteristics of the XT1 oscillator

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V (16- to 36-pin products), 1.6 V ≤ V_{DD} ≤ 5.5 V (40- to 48-pin products), V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (f_{XT})[Note]	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See **2.4 AC Characteristics** for instruction execution time.

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2.2.3 Characteristics of the on-chip oscillators

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}				1		32	MHz
High-speed on-chip oscillator clock frequency accuracy **Note 1**		HIPREC = 1	+85 to +105°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.5		+5.5	%
		HIPREC = 0 **Note 2**			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%
Middle-speed on-chip oscillator clock frequency **Note 3**	f_{IM}				1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy **Note 1**					-12		+12	%
Middle-speed on-chip oscillator clock correction resolution						0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient							±0.17 **Note 4**	%/°C
Low-speed on-chip oscillator clock frequency **Note 3**	f_{IL}					32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy **Note 1**					-15		+15	%
Low-speed on-chip oscillator clock correction resolution						0.3		%
Low-speed on-chip oscillator frequency temperature coefficient							±0.21 **Note 4**	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. This condition applies when the setting of the FRQSEL3 bit of the user option byte is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. See **2.4 AC Characteristics** for instruction execution time.

Note 4. These values are the results of characteristic evaluation and are not checked for shipment.

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2.3 DC Characteristics

2.3.1 Characteristics of pins

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/5)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current[Note 1]	I_{OH1}	Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147	1.6 V ≤ V_{DD} ≤ 5.5 V			-10.0[Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			-55.0[Note 4]	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-2.5	mA
		Total of P10 to P17, P30, P31, P50, P51, P70 to P75, P146, P147 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			-80.0[Note 5]	mA
			2.7 V ≤ V_{DD} < 4.0 V			-19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-10.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70%[Note 3])	1.6 V ≤ V_{DD} ≤ 5.5 V			-135.0[Note 6]	mA
	I_{OH2}	Per pin for P20 to P27, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0[Note 2]	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0[Note 2]	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5[Note 2]	mA
		Total of all pins (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the V_{DD} pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)

  Example when n = 80% and I_{OH} = -10.0 mA

  Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -30 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

Note 5. The maximum value is -50 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

Note 6. The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of -40 to +85°C and of +85 to +105°C.

Caution **The following pins are not capable of the output of high-level signals in the N-ch open-drain output mode.**
P00, P10 to P15, P17, P50, P71, P72, P74, and P120

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/5)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current[Note 1]	I_{OL1}	Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0[Note 4]	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75, P146, P147 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0[Note 4]	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70%[Note 3])				150.0[Note 5]	mA
	I_{OL2}	Per pin for P20 to P27, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5[Note 2]	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6[Note 2]	mA
			1.6 V ≤ V_{DD} < 1.8 V			0.4[Note 2]	mA
		Total of all pins (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			20	mA
			2.7 V ≤ V_{DD} < 4.0 V			20	mA
			1.8 V ≤ V_{DD} < 2.7 V			15	mA
			1.6 V ≤ V_{DD} < 1.8 V			10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the V_{SS} pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is 40 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

Note 5. The maximum value is 80 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/5)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P01, P10, P11, P13 to P17, P41, P71	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P27		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P01, P10, P11, P13 to P17, P41, P71	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution **The maximum value of V_{IH} of pins P00, P10 to P15, P17, P50, P71, P72, P74, and P120 is V_{DD}, even in the N-ch open-drain output mode.**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (4/5)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -2.0 mA	V_{DD} - 0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -1.5 mA	V_{DD} - 0.5			V
			1.6 V ≤ V_{DD} < 5.5 V, I_{OH1} = -1.0 mA	V_{DD} - 0.5			V
	V_{OH2}	P20 to P27, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OH2} = -0.5 mA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA			0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution **P00, P10 to P15, P17, P50, P71, P72, P74, and P120 do not output high-level signals in the N-ch open-drain output mode.**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (5/5)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147	$V_I = V_{DD}$			0.5	μA
	I_{LIH2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$			0.5	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$			0.5	μA
Input leakage current, low	I_{LIL1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147	$V_I = V_{SS}$			-0.5	μA
	I_{LIL2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$			-0.5	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$			-0.5	μA
On-chip pull-up resistance	R_U	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P122, P140, P146, P147	$V_I = V_{SS}$, In input port	10	20	100	kΩ

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

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2.3.2 Characteristics of the supply current

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 2**	Basic operation	V_{DD} = 5.0 V		1.2		mA
						V_{DD} = 1.8 V		1.2		
					Normal operation	V_{DD} = 5.0 V		2.7	4.6	mA
						V_{DD} = 1.8 V		2.7	4.6	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		2.0	3.5	mA
						V_{DD} = 1.8 V		2.0	3.5	
				f_{IH} = 16 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		1.5	2.5	mA
						V_{DD} = 1.8 V		1.5	2.5	
				f_{IM} = 4 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		0.4	0.7	mA
						V_{DD} = 1.6 V		0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		179	300	µA
						V_{DD} = 1.6 V		179	300	
				f_{IM} = 1 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		100	163	µA
						V_{DD} = 1.6 V		100	163	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.7	2.9	mA
						V_{DD} = 1.8 V		1.6	2.8	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.5	2.7	mA
						V_{DD} = 1.8 V		1.5	2.7	
				f_{MX} = 20 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.7	3.0	mA
						V_{DD} = 1.8 V		1.7	3.0	
				f_{MX} = 10 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.5	mA
						V_{DD} = 1.8 V		0.8	1.4	
				f_{MX} = 10 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.6	mA
						V_{DD} = 1.8 V		0.9	1.6	
				f_{MX} = 8 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.7	1.2	mA
						V_{DD} = 1.8 V		0.7	1.2	
				f_{MX} = 8 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.8	1.3	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

<R> - The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, <R> and subsystem clock X are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and <R> subsystem clock X are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip <R> oscillator, and subsystem clock X are stopped.

(Remarks are listed on the next page.)

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Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency
Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz **Note 2**, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		2.9	4.7	µA
						T_A = +25°C		3.1	4.9	
						T_A = +50°C		3.3	6.3	
						T_A = +70°C		3.6	9.6	
						T_A = +85°C		4.1	15.2	
						T_A = +105°C		5.4	32.2	
				f_{SUB} = 32.768 kHz **Note 3**, Square wave input	Normal operation	T_A = -40°C		2.9	4.9	µA
						T_A = +25°C		3.0	5.0	
						T_A = +50°C		3.2	6.4	
						T_A = +70°C		3.5	9.7	
						T_A = +85°C		4.0	15.3	
						T_A = +105°C		5.4	32.4	
				f_{SUB} = 32.768 kHz **Note 3**, Resonator connection	Normal operation	T_A = -40°C		2.9	4.9	µA
						T_A = +25°C		3.1	5.3	
						T_A = +50°C		3.3	6.7	
						T_A = +70°C		3.6	10.2	
						T_A = +85°C		4.1	15.8	
						T_A = +105°C		5.5	33.3	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. In the subsystem clock operation, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock X are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.49	1.87	mA
					V_{DD} = 1.8 V		0.49	1.87	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V		0.41	1.46	mA
					V_{DD} = 1.8 V		0.40	1.45	
				f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V		0.42	1.15	mA
					V_{DD} = 1.8 V		0.41	1.14	
				f_{IM} = 4 MHz Note 4	V_{DD} = 5.0 V		0.08	0.26	mA
					V_{DD} = 1.6 V		0.07	0.25	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 4	V_{DD} = 5.0 V		29	115	μA
					V_{DD} = 1.6 V		29	115	
				f_{IM} = 1 MHz Note 4	V_{DD} = 5.0 V		25	71	μA
					V_{DD} = 1.6 V		25	71	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.19	1.03	mA
					V_{DD} = 1.8 V		0.16	0.99	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.19	1.03	mA
					V_{DD} = 1.8 V		0.16	0.99	
				f_{MX} = 20 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.38	1.26	mA
					V_{DD} = 1.8 V		0.37	1.25	
				f_{MX} = 10 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.12	0.54	mA
					V_{DD} = 1.8 V		0.10	0.52	
				f_{MX} = 10 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.22	0.67	mA
					V_{DD} = 1.8 V		0.22	0.66	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.10	0.45	mA
					V_{DD} = 1.8 V		0.09	0.43	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.20	0.57	mA
					V_{DD} = 1.8 V		0.20	0.56	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.

<R> - The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, <R> and subsystem clock X are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and <R> subsystem clock X are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip <R> oscillator, and subsystem clock X are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz **Note 3**, Low-speed on-chip oscillator operation	T_A = -40°C		0.48	1.84	μA
					T_A = +25°C		0.57	1.89	
					T_A = +50°C		0.67	3.19	
					T_A = +70°C		0.91	6.33	
					T_A = +85°C		1.69	12.66	
					T_A = +105°C		3.04	29.93	
				f_{SUB} = 32.768 kHz, Square wave input **Note 4**	T_A = -40°C		0.20	1.72	μA
					T_A = +25°C		0.29	1.75	
					T_A = +50°C		0.49	3.75	
					T_A = +70°C		0.90	8.16	
					T_A = +85°C		1.41	14.55	
					T_A = +105°C		2.79	32.65	
				f_{SUB} = 32.768 kHz, Resonator connection **Note 5**	T_A = -40°C		0.21	1.79	μA
					T_A = +25°C		0.33	2.03	
					T_A = +50°C		0.44	3.40	
					T_A = +70°C		0.97	8.65	
					T_A = +85°C		1.48	15.04	
					T_A = +105°C		2.92	33.56	
	I_{DD3}	STOP mode **Note 6**	T_A = -40°C				0.15	1.10	μA
			T_A = +25°C				0.20	1.10	
			T_A = +50°C				0.40	2.40	
			T_A = +70°C				0.80	5.50	
			T_A = +85°C				1.30	11.00	
			T_A = +105°C				2.70	28.00	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock X are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B). They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 6. The listed currents apply when all clocks are stopped. For the currents when operating the low-speed on-chip oscillator or subsystem clock X in the STOP mode, refer to the currents when operating the subsystem clock in the HALT mode.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency

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Peripheral Functions

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1				380		μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20		μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005		μA
		f_{RTCCLK} = 128 Hz			0.002		μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter internal reference voltage current	I_{ADREF} Note 1				100		μA
Temperature sensor operating current	I_{TMPS} Note 1				110		μA
<R> Serial interface UARTA operating current	I_{UARTA} Notes 1, 2, 7	f_{SXP} = 32.768 kHz	1 channel: Reception at 2400 bps		0.14		μA
LVD operating current	I_{LVD0} Notes 1, 8				0.02		μA
	I_{LVD1} Notes 1, 8				0.02		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.5	12.2	mA
Data flash memory rewrite operating current	I_{BGO} Notes 1, 10				2.5	12.2	mA
SNOOZE mode sequencer operating current	I_{SMS} Notes 1, 11	f_{IH} = 32 MHz			0.93		mA
		f_{IL} = 32.768 kHz			0.97		μA
SNOOZE operating current	I_{SNOZ} Note 1	f_{IH} = 32 MHz	ADC to be in use: The ADC is shifting from the STOP mode to the SNOOZE mode. Note 12		0.5	0.7	mA
			The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		0.9	1.4	
			Simplified SPI (CSI)/UART to be in use		0.6	0.79	mA
			SMS Note 13		1.4		mA
Low-speed peripheral clock supply current	I_{SXP} Notes 1, 14	RTCLPC = 0			0.22		μA

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(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating current of the true random number generator	I_{TRNG} **Note 1**				1.1		mA

Note 1. This current flows into V_{DD}.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of this MCU is the sum of either I_{DD1} or I_{DD2}, and I_{RTC}, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current. I_{DD2} in the subsystem clock operation mode includes the operating current of the realtime clock.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of this MCU is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 5. This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of this MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is operating.

Note 6. This current only flows to the A/D converter. The supply current of this MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating or in the HALT mode.

<R> **Note 7.** This current only flows to the serial interface UARTA. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of this MCU is the sum of I_{DD1} or I_{DD2} and I_{UARTA} when the serial interface UARTA is operating or in the HALT mode. Note that when the serial interface UARTA is in the HALT mode with the subsystem clock X (f_{SX}) selected as the CPU/peripheral hardware clock (f_{CLK}), the low-speed peripheral clock supply current (I_{SXP}) is also added to the supply current.

Note 8. This current only flows to the LVD. The supply current of this MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD is in operation.

Note 9. This current only flows during self-programming.

Note 10. This current only flows while the data flash memory is being rewritten.

Note 11. This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of this MCU is the sum of either I_{DD1} or I_{DD2}, and I_{SMS}, when the SNOOZE mode sequencer is operating or in the HALT mode.

Note 12. For shift time to the SNOOZE mode, see **20.3.3 SNOOZE mode** in the RL78/G22 User's Manual.

Note 13. The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to I_{DD1}. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.

Note 14. This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the subsystem clock X (f_{SX}) selected as the CPU clock, while the subsystem clock X (fsx) is oscillating.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SX}: Subsystem clock X frequency

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

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2.4 AC Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

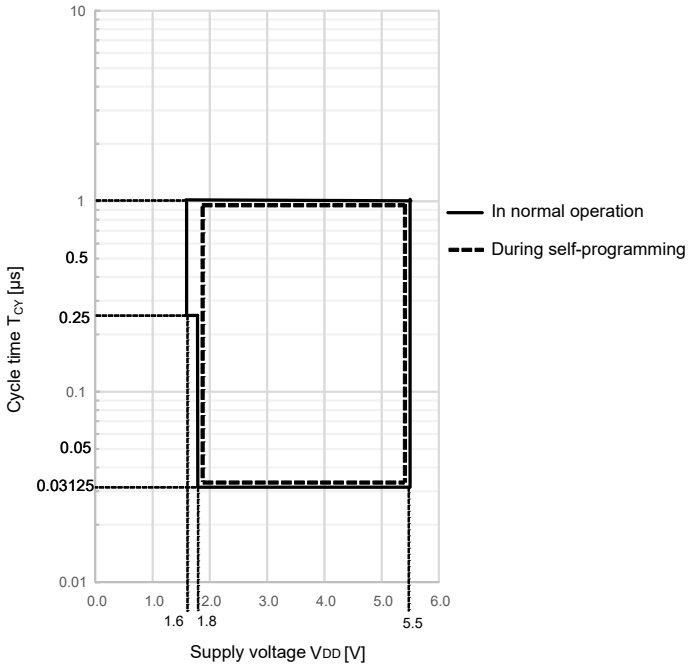
Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	µs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	µs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	µs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	µs
		Subsystem clock (f_{SUB}) operation		1.6 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	µs
		In the self-programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	µs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
External system clock frequency	f_{EX}	1.8 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	1.8 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			µs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode LS (low-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				1.8 V ≤ V_{DD} < 2.7 V			4	MHz
				1.6 V ≤ V_{DD} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ V_{DD} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode LS (low-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				1.8 V ≤ V_{DD} < 2.7 V			4	MHz
				1.6 V ≤ V_{DD} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ V_{DD} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP6, INTP8, INTP9		1.6 V ≤ V_{DD} ≤ 5.5 V	1			µs
Key interrupt input high-level width, low-level width	t_{KRH}, t_{KRL}	KR0 to KR5		1.8 V ≤ V_{DD} ≤ 5.5 V	250			ns
				1.6 V ≤ V_{DD} < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			µs

Remark f_{MCK}: Timer array unit operating clock frequency
To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn).
m: Unit number (m = 0), n: Channel number (n = 0 to 3)

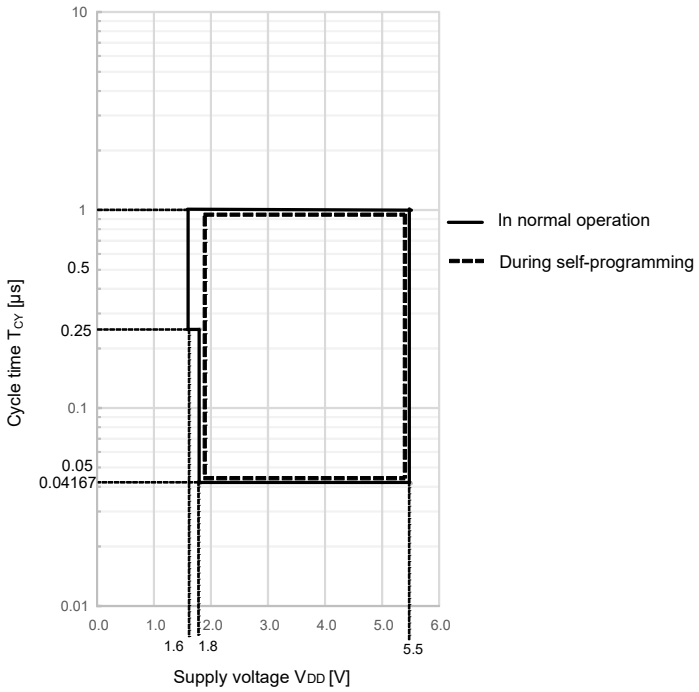
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Minimum Instruction Execution Time during Main System Clock Operation

TCY vs VDD in HS (high-speed main) mode

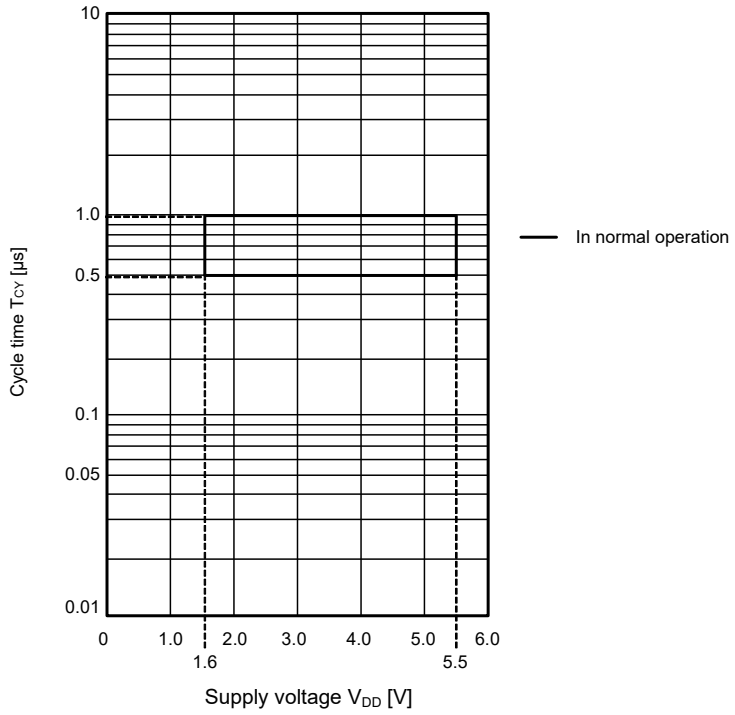


TCY vs VDD in LS (low-speed main) mode

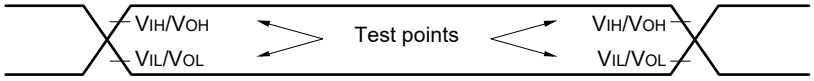


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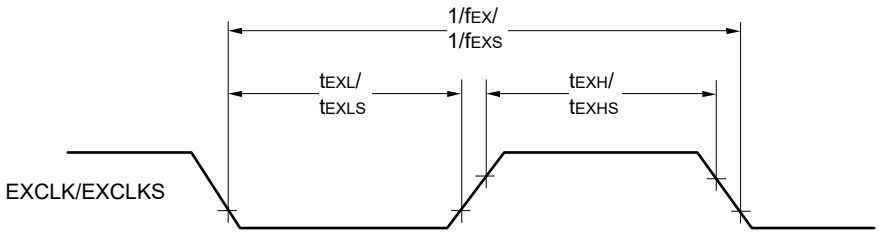
TCY vs VDD in LP (low-power main) mode



AC Timing Test Points

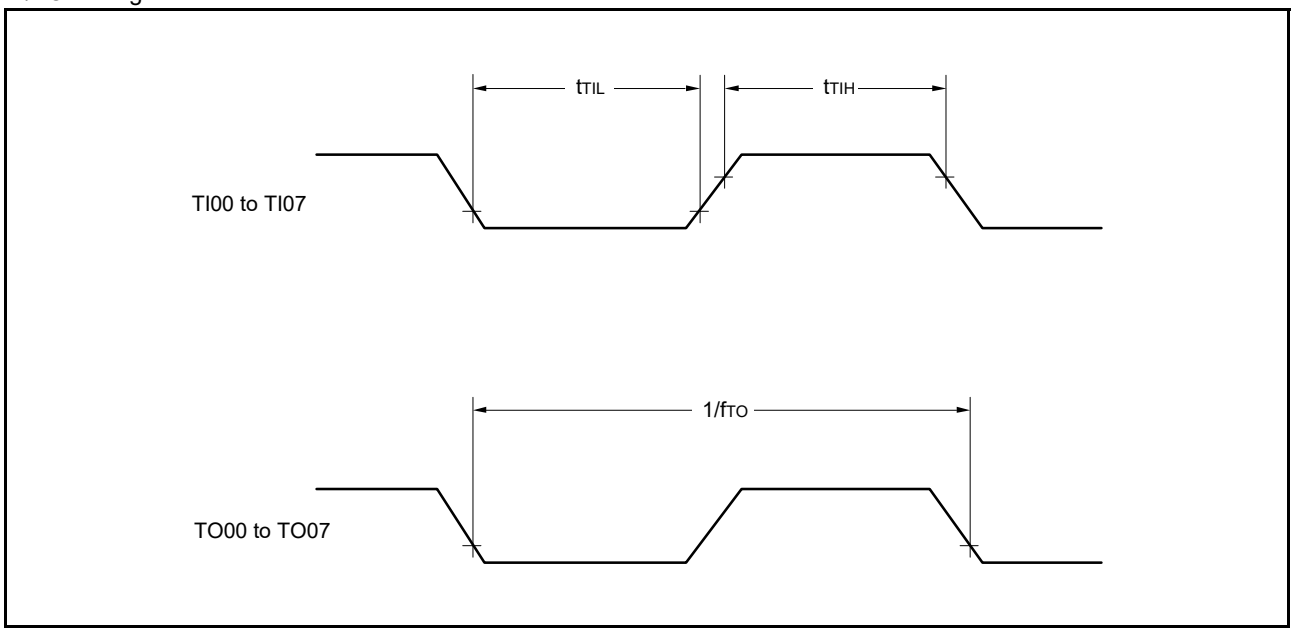


External System Clock Timing

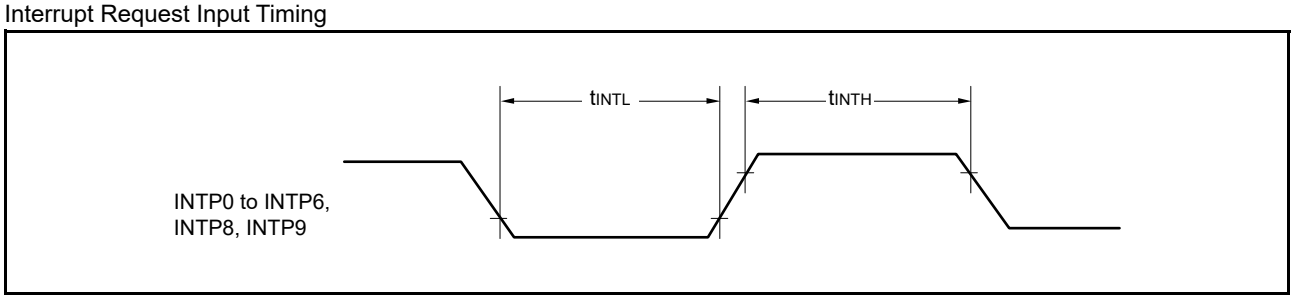


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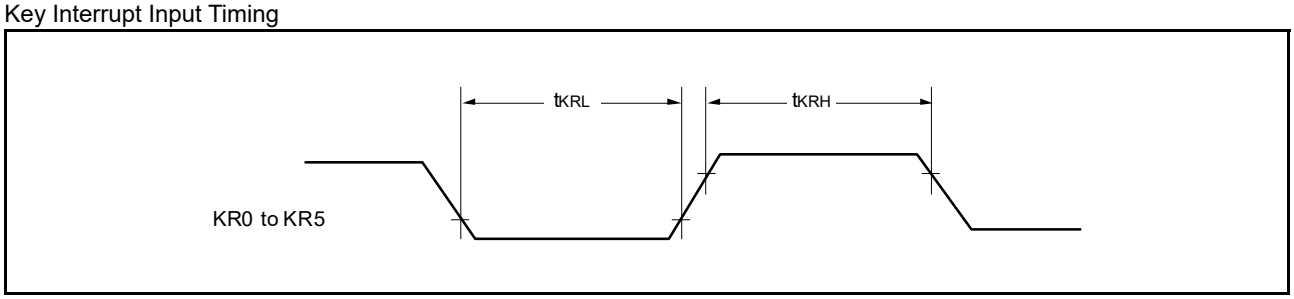
TI/TO Timing



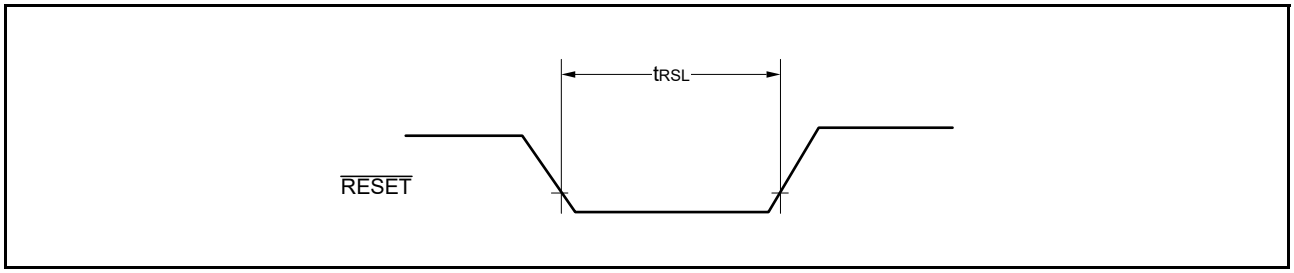
Interrupt Request Input Timing



Key Interrupt Input Timing



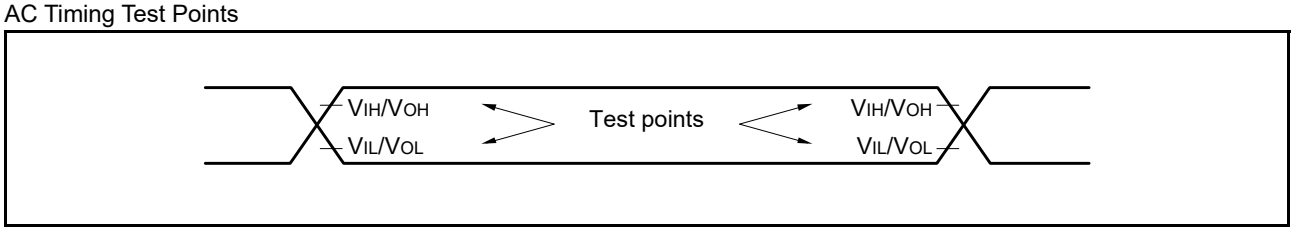
$\overline{\text{RESET}}$ Input Timing



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2.5 Characteristics of the Peripheral Functions

AC Timing Test Points



2.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate **Note 1**		1.6 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		4		0.33	Mbps

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

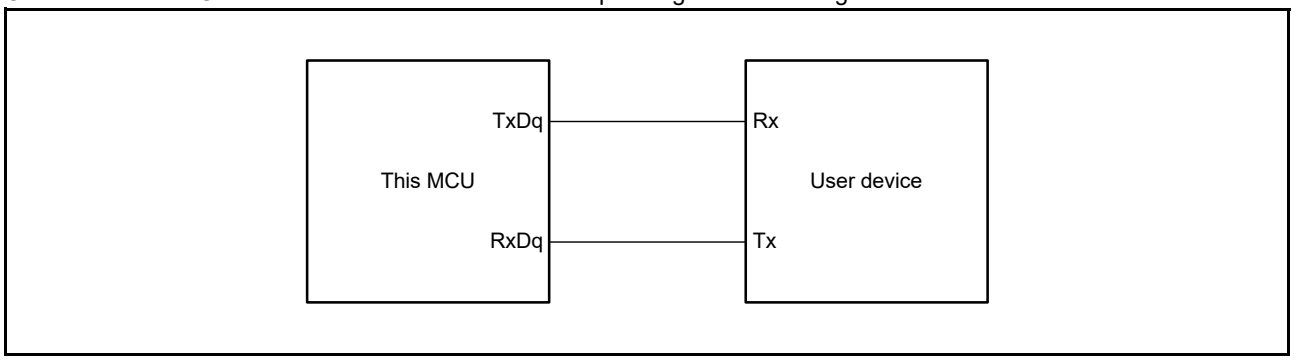
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are as follows.

HS (high-speed main) mode: 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

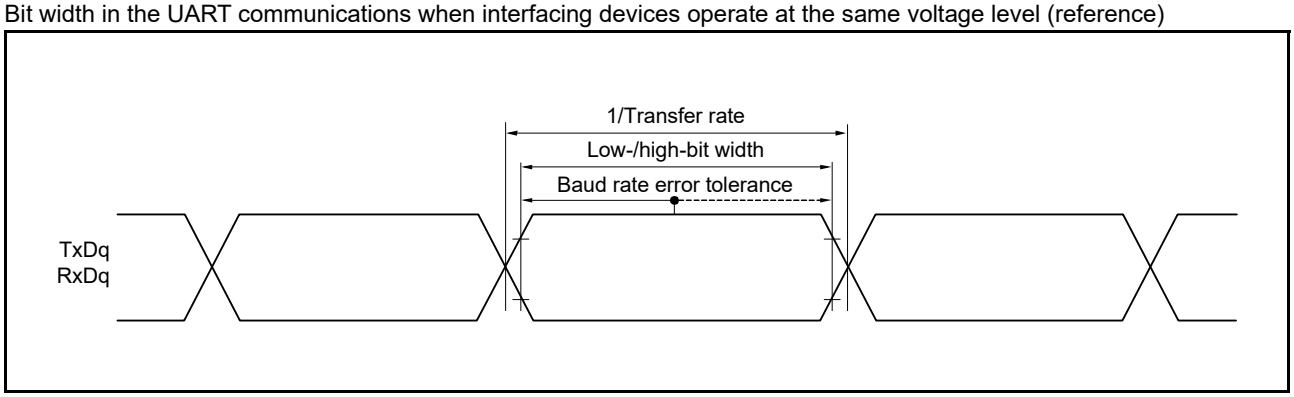
Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register (PIMg) and port output mode register (POMg).

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Connection in the UART communications with devices operating at same voltage levels



Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, set the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

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2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	62.5		83.3		1000		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	83.3		125		1000		ns
SCKp high-/high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 7		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 10		t_{KCY1}/2 - 15		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑)**Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		23		33		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		33		50		110		ns
SIp hold time (from SCKp↑) **Note 1**	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output**Note 2**	t_{KSO1}	C = 20 pF**Note 3**			10		10		10	ns

Note 1. The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes “to SCKp↓” and that for the SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register (PIMg) and the port output mode register (POMg).

Remark 1. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

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3. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	125		166		2000		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		250		2000		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	500		500		2000		ns
			1.6 V ≤ V_{DD} ≤ 5.5 V	1000		1000		2000		ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		t_{KCY1}/2 - 21		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18		t_{KCY1}/2 - 25		t_{KCY1}/2 - 50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38		t_{KCY1}/2 - 38		t_{KCY1}/2 - 50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		ns
SIp setup time (to SCKp↑)**Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		54		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		54		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		75		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		110		110		110		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		220		220		220		ns
SIp hold time (from SCKp↑) **Note 1**	t_{KSI1}	1.6 V ≤ V_{DD} ≤ 5.5 V		19		19		19		ns
Delay time from SCKp↓ to SOp output**Note 2**	t_{KSO1}	1.6 V ≤ V_{DD} ≤ 5.5 V C = 30 pF**Note 3**			25		25		25	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes “to SCKp↓” and that for the SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register (PIMg) and the port output mode register (POMg).

Remark 1. p: CSI number (p = 00, 01, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 11)

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4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the external SCKp clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time **Note 4**	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/ high-level width, low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		ns

(Notes, Caution, and Remarks are listed on the next page.)

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4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the external SCKp clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↑)**Note 1**	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		1/f_{MCK} + 40		1/f_{MCK} + 40		ns
SIp hold time (from SCKp↑)**Note 1**	t_{KSI2}	1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 250		1/f_{MCK} + 250		1/f_{MCK} + 250		ns
Delay time from SCKp↓ to SOp output **Note 2**	t_{KSO2}	C = 30 pF **Note 3**	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 110		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.6 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 220		2/f_{MCK} + 220		2/f_{MCK} + 220	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes “to SCKp↓” and that for the SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output line.

Note 4. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

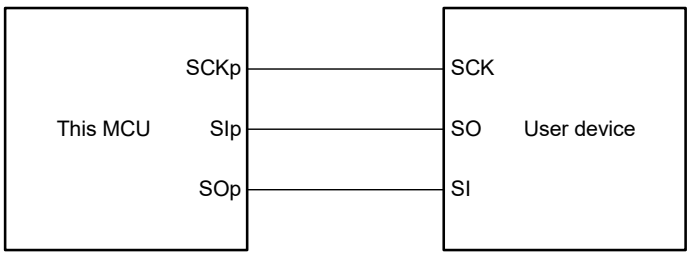
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the port input mode register (PIMg) and the port output mode register (POMg).

Remark 1. p: CSI number (p = 00, 01, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

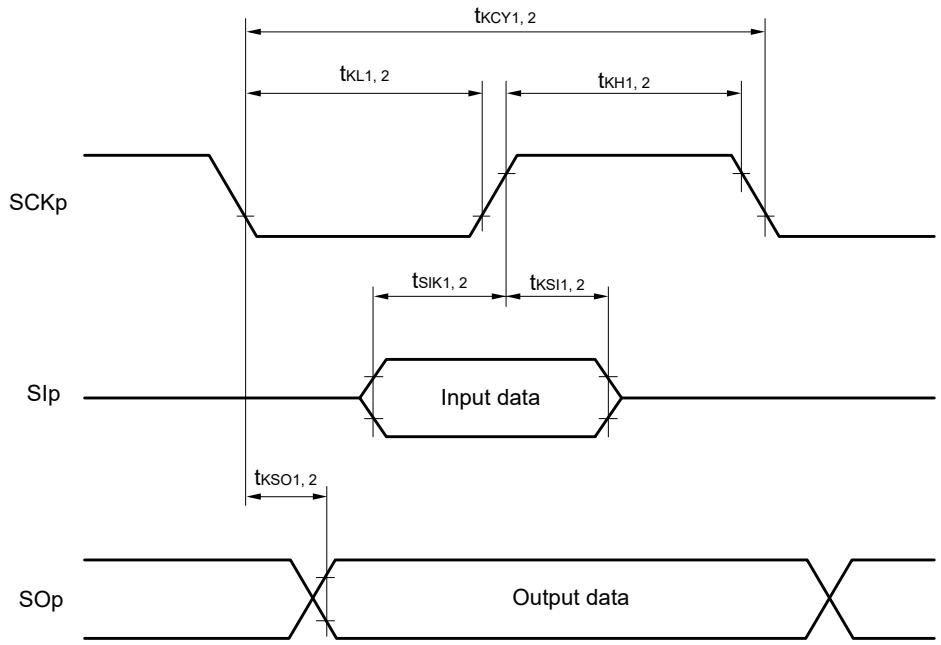
Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

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Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels

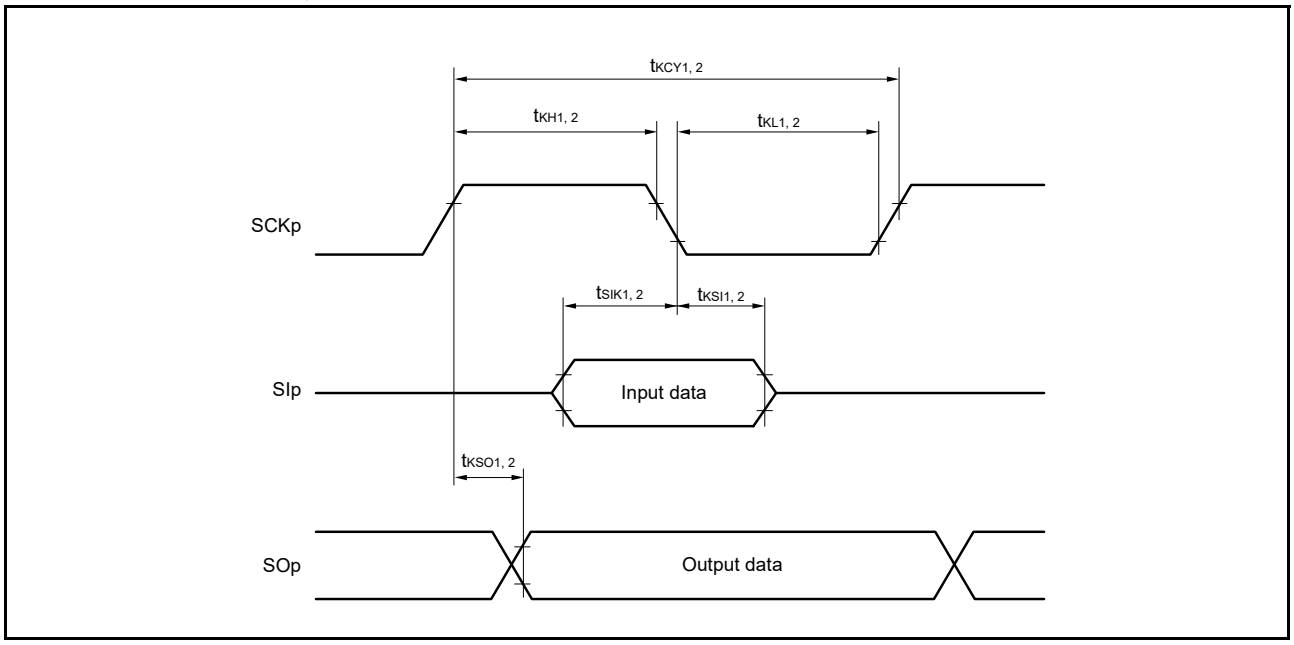


Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



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Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 11, 20, 21)

Remark 2. m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

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5. In simplified I²C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
Hold time when SCLr is low	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

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5. In simplified I²C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 **Note 2**		1/f_{MCK} + 85 **Note 2**		1/f_{MCK} + 145 **Note 2**		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 **Note 2**		1/f_{MCK} + 145 **Note 2**		1/f_{MCK} + 145 **Note 2**		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 **Note 2**		1/f_{MCK} + 230 **Note 2**		1/f_{MCK} + 230 **Note 2**		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 **Note 2**		1/f_{MCK} + 290 **Note 2**		1/f_{MCK} + 290 **Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.

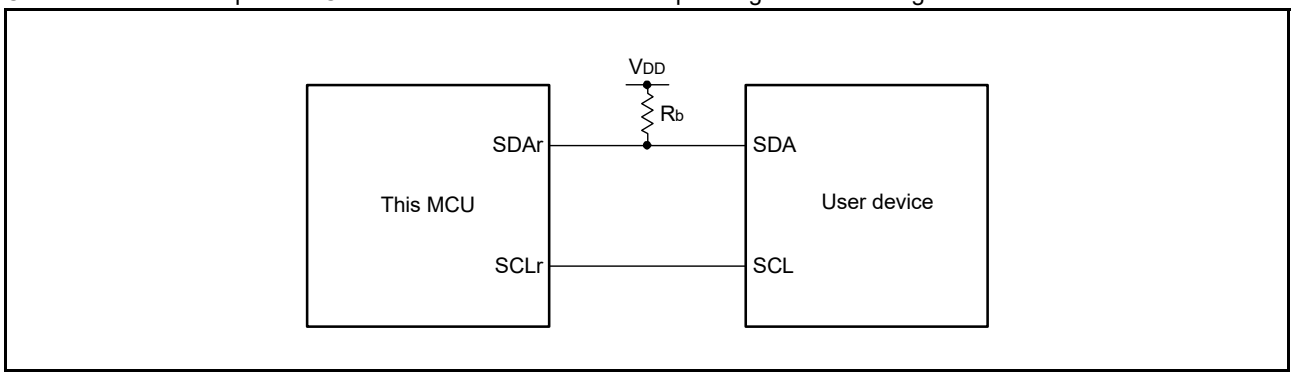
Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

Caution Select the normal input buffer and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register (PIMg) and port output mode register (POMh).

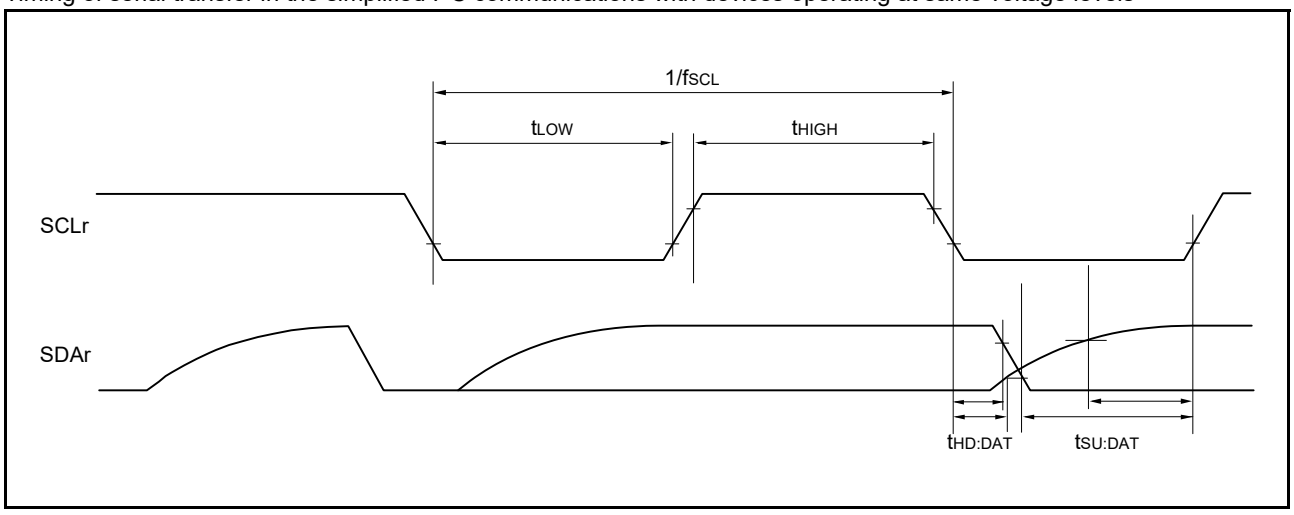
(Remarks are listed on the next page.)

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Connection in the simplified I2C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I2C communications with devices operating at same voltage levels



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 7), h: POM number (g = 1, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

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6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 3**		5.3		4		0.33	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 3**		5.3		4		0.33	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 **Notes 1, 2**		f_{MCK}/6 **Notes 1, 2**		f_{MCK}/6 **Notes 1, 2**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 3**		5.3		4		0.33	Mbps

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. Use this rate with $V_{DD} \geq V_b$.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the TxDq pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of the PIOR1 bit of the peripheral I/O redirection register (PIOR) is 1.

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6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 **Note 2**		2.8 **Note 2**		2.8 **Note 2**	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 **Note 4**		1.2 **Note 4**		1.2 **Note 4**	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 7**		0.43 **Note 7**		0.43 **Note 7**	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes and Caution are listed on the next page.)

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Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with $V_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

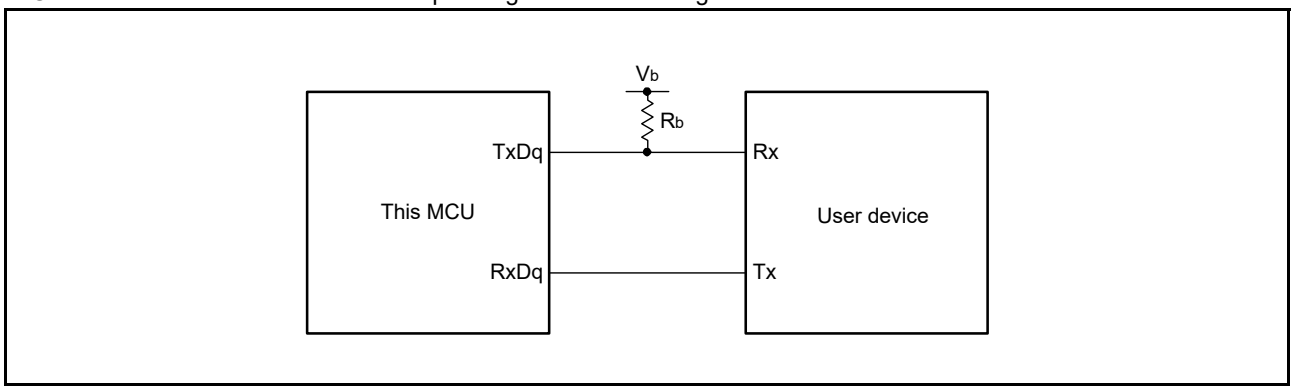
This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

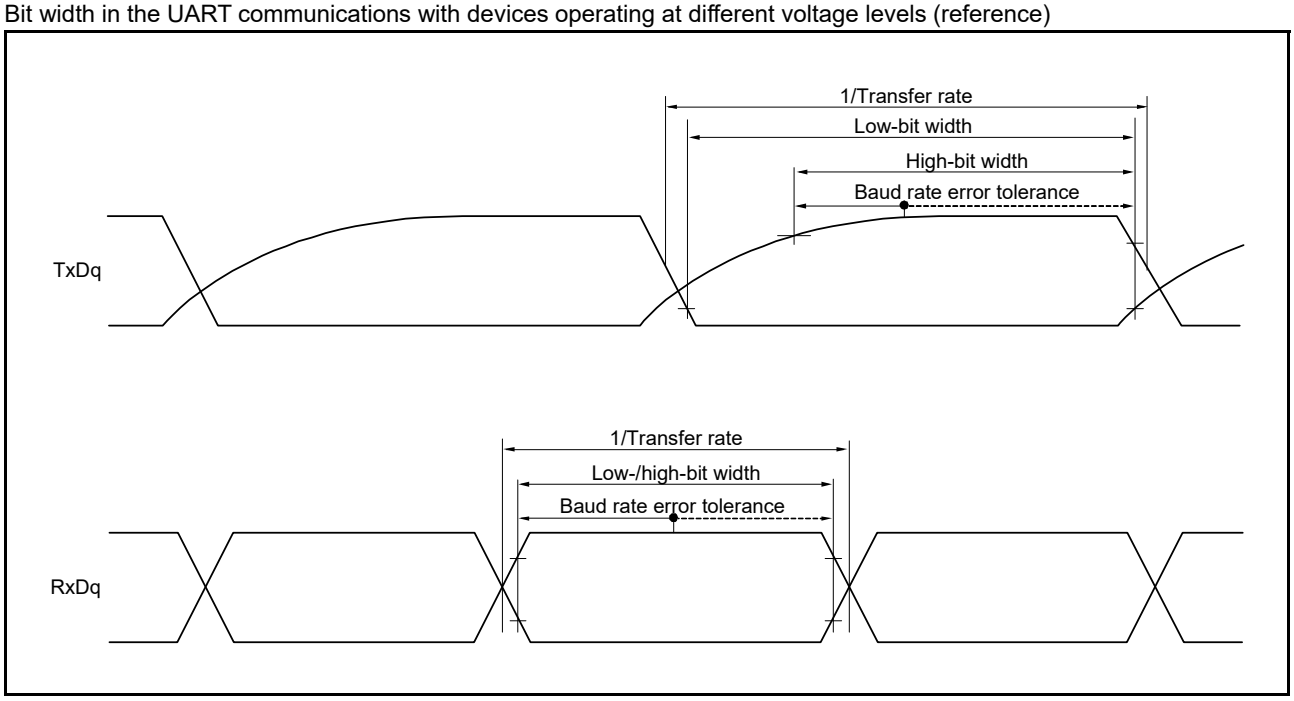
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the TxDq pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

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In UART communications with devices operating at different voltage levels



Bit width in the UART communications with devices operating at different voltage levels (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of the PIOR1 bit of the peripheral I/O redirection register (PIOR) is 1.

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7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		200		2300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		300		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 120		t_{KCY1}/2 - 120		t_{KCY1}/2 - 120		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 7		t_{KCY1}/2 - 7		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 10		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		58		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		121		479		ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output[Note 1]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

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7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↓)Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	23		23		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33		33		110		ns
SIp hold time (from SCKp↓)Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp outputNote 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SOp pin and SCKp pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn= 00)

Remark 4. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

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8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/3)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		300		2300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		500		2300		ns
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns

Note Use this setting with $V_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SOp pin and SCKp pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

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8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		81		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		177		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp outputNote 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use this setting with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SOp pin and SCKp pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

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8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↓)Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		44		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		44		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓)Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp outputNote 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 VNote 2, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

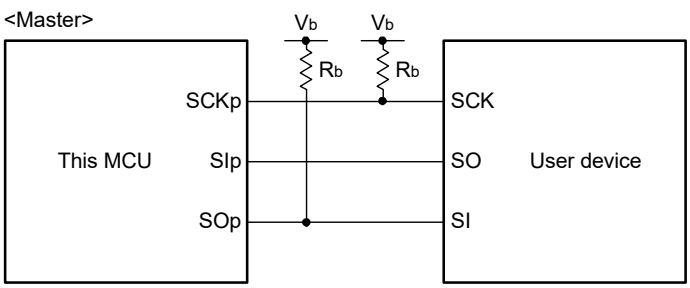
Note 2. Use this setting with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SOp pin and SCKp pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

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Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



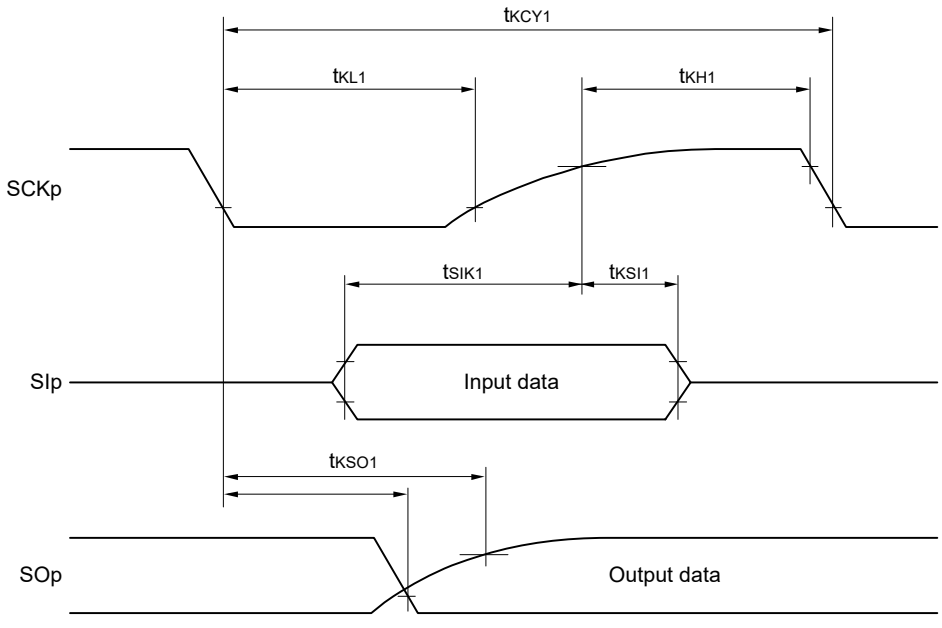
Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

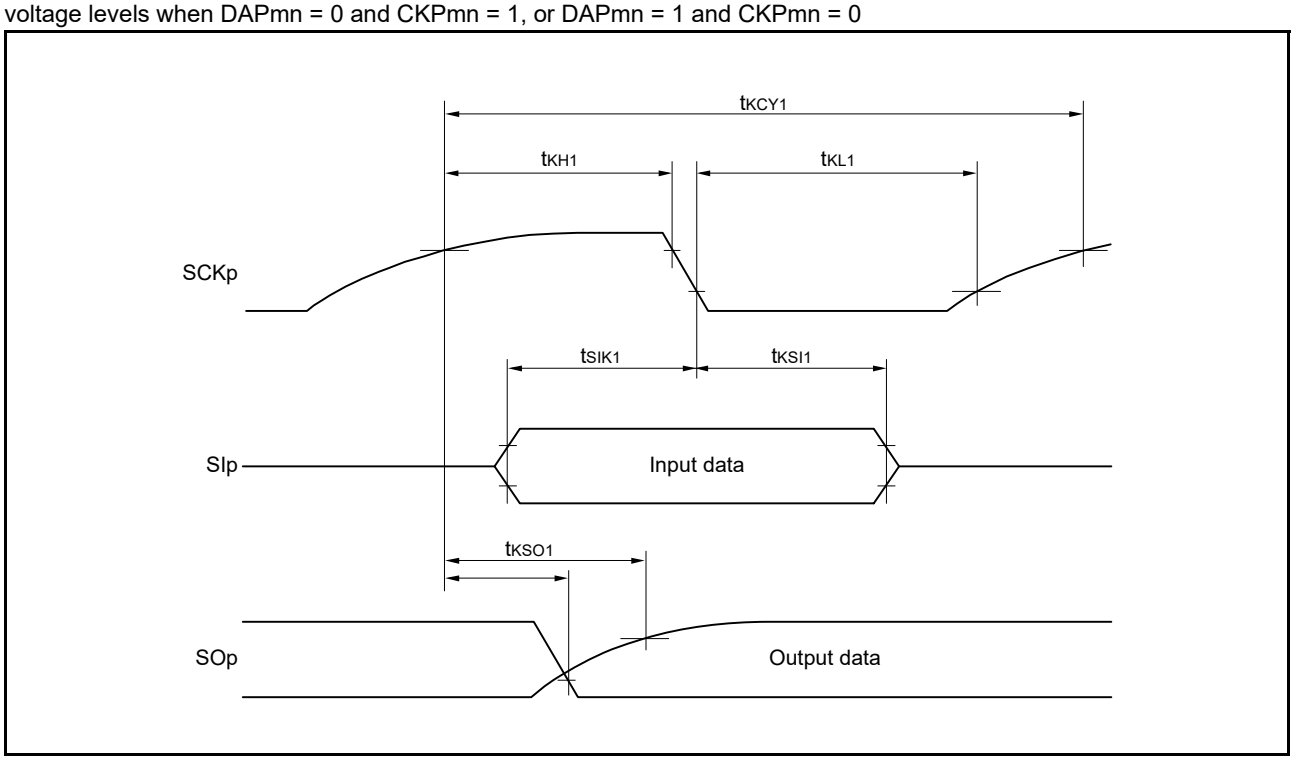
Remark 4. Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



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Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

Remark 2. Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

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9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time **Note 1**	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		10/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V,	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

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9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	t_{KCY2}/2 - 12		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**	t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑)**Note 3**	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑)**Note 3**	t_{KSI2}		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output**Note 4**	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} + 120		2/f_{MCK} + 120		2/f_{MCK} + 573	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note 2. Use this setting with V_{DD} ≥ V_b.

Note 3. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" and SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

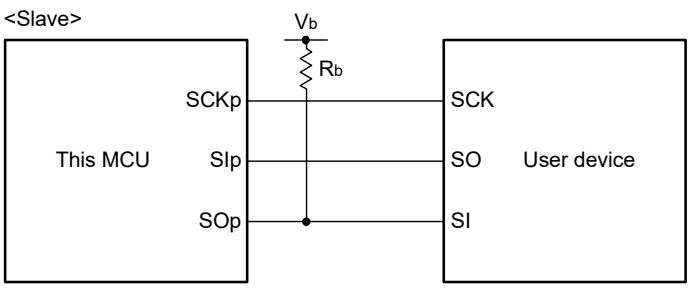
Note 4. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SOp pin and SCKp pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

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Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



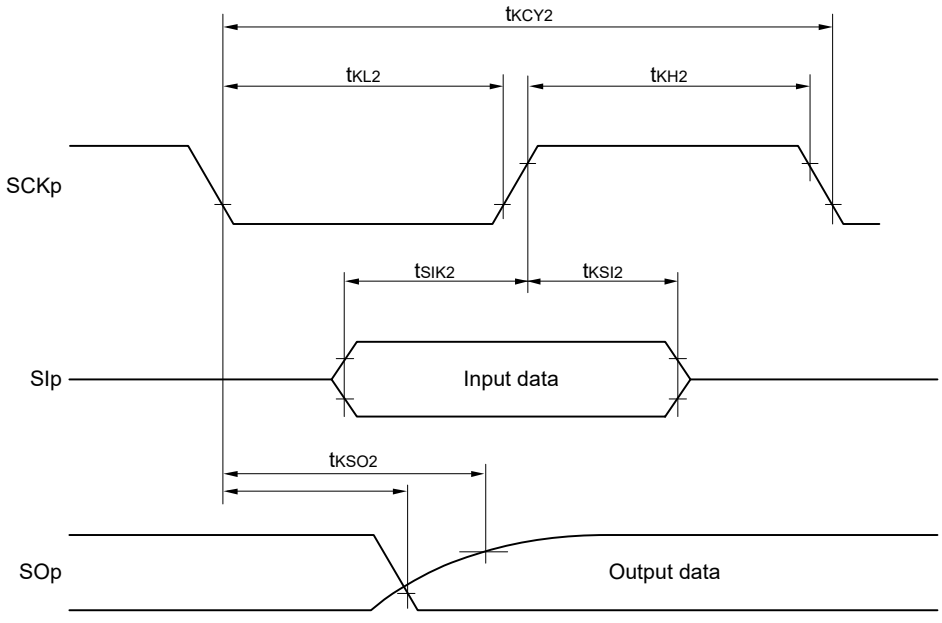
Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

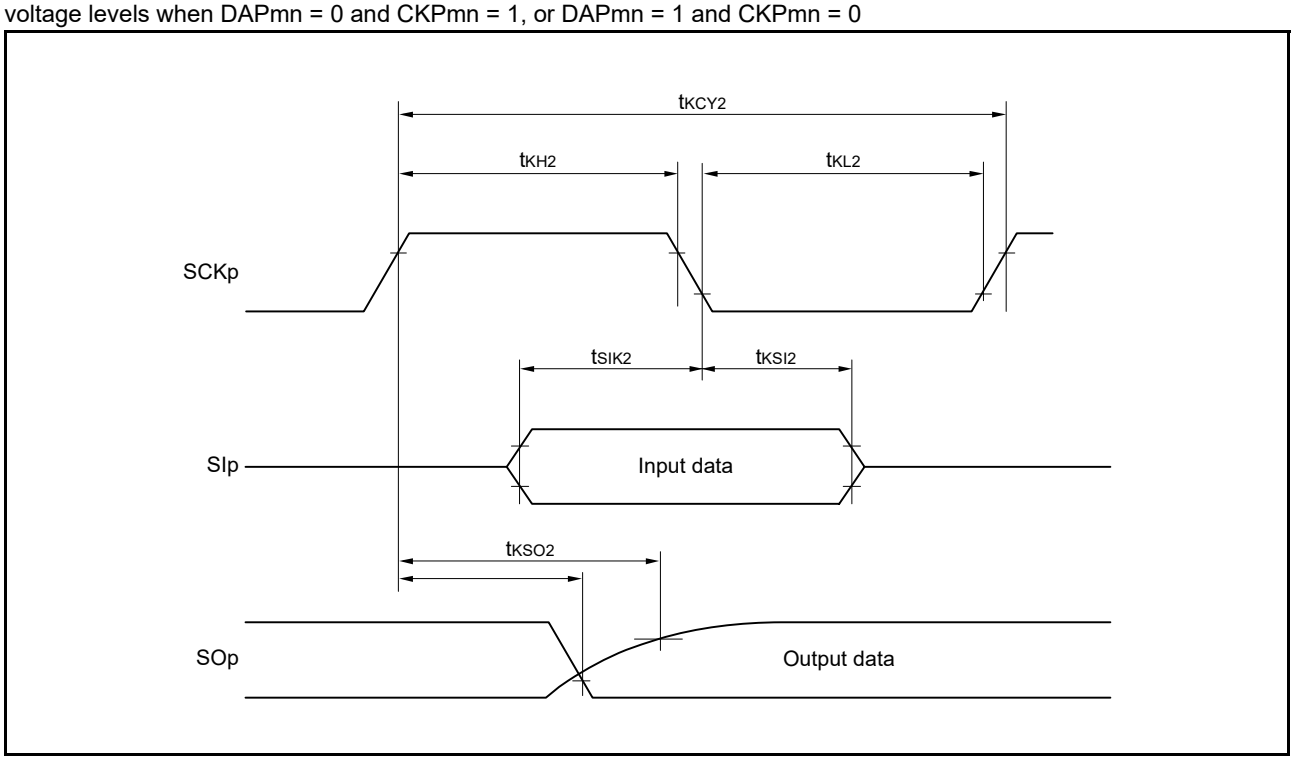
Remark 4. Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



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Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

Remark 2. Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

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10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr is low	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		ns

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10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 **Note 3**		1/f_{MCK} + 135 **Note 3**		1/f_{MCK} + 190 **Note 3**		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 **Note 3**		1/f_{MCK} + 135 **Note 3**		1/f_{MCK} + 190 **Note 3**		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		1/f_{MCK} + 190 **Note 3**		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.

Note 2. Use this setting with V_{DD} ≥ V_b.

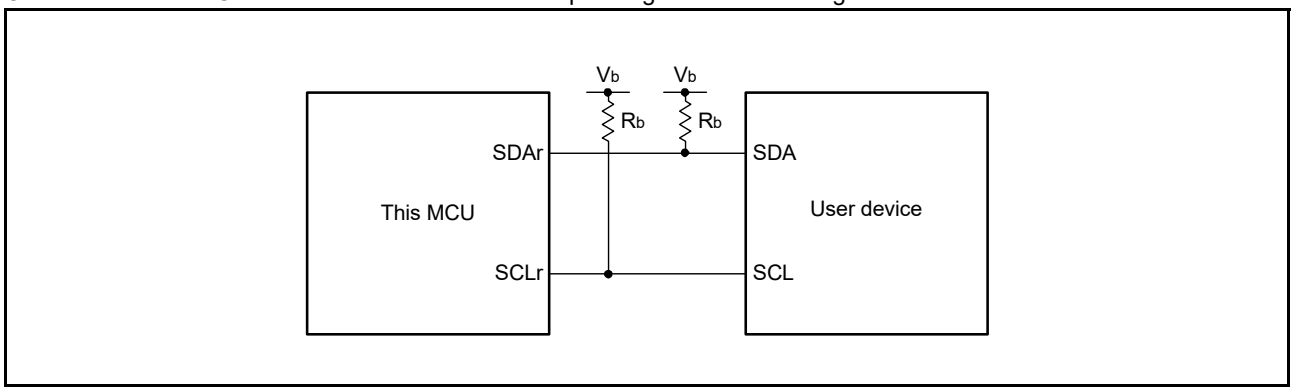
Note 3. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

Caution Select the TTL input buffer and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SDAr pin and the N-ch open drain output (withstand voltage of V_{DD}) mode for the SCLr pin by using port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

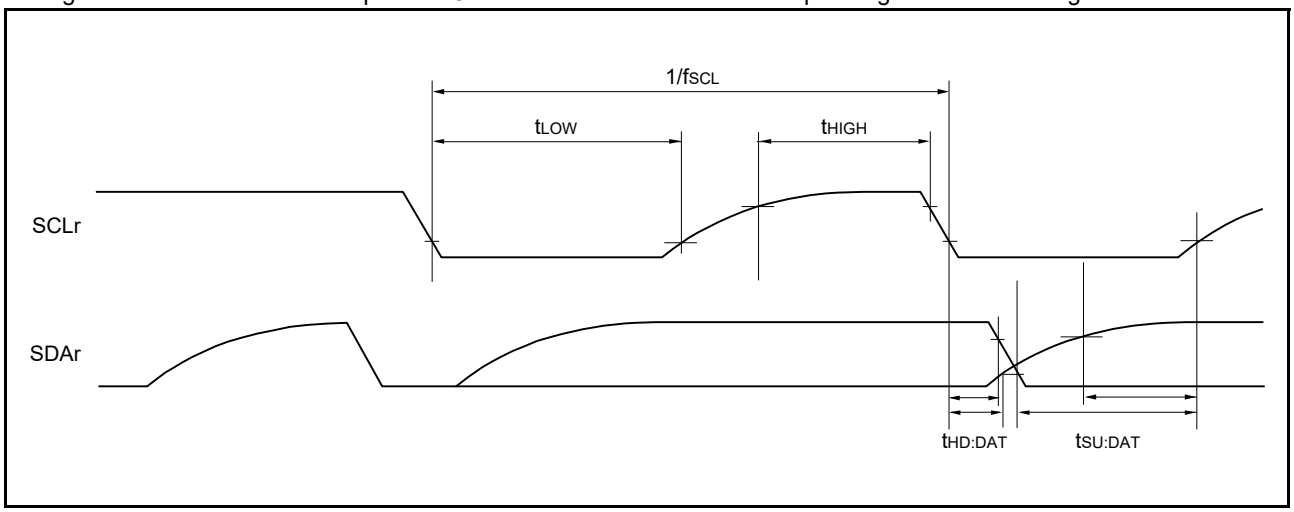
(Remarks are listed on the next page.)

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Connection in the I²C communications with devices operating at different voltage levels



Timing of serial transfer in the simplified I²C communications with devices operating at different voltage levels



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 11, 20, 21), g: PIM and POM number (g = 0, 1, 3, 7), POM number (h = 1, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 03, 10,11)

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2.5.2 Serial interface UARTA

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDAn pin and the normal output mode for the TxDAn pin by using port input mode register (PIMg) and port output mode register (POMg).

Remark 1. g: PIM or POM number (g = 7)
Remark 2. n: Unit number (n = 0)

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2.5.3 Serial interface IICA

1. I^2C standard mode

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0		100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7			µs
Hold time[Note 1]	$t_{HD:STA}$		4.0			µs
Hold time when SCLA0 is low	t_{LOW}		4.7			µs
Hold time when SCLA0 is high	t_{HIGH}		4.0			µs
Data setup time (reception)	$t_{SU:DAT}$		250			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0		3.45	µs
Setup time of stop condition	$t_{SU:STO}$		4.0			µs
Bus-free time	t_{BUF}		4.7			µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution **The listed frequency and times apply even when the PIOR2 bit in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 400 pF, R_b = 2.7 kΩ

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2. I^2C fast mode

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz 1.8 V ≤ V_{DD} ≤ 5.5 V	0		400	kHz
Setup time of restart condition	$t_{SU:STA}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			μs
Hold time[Note 1]	$t_{HD:STA}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			μs
Hold time when SCLA0 is low	t_{LOW}	1.8 V ≤ V_{DD} ≤ 5.5 V	1.3			μs
Hold time when SCLA0 is high	t_{HIGH}	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			μs
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V	100			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0		0.9	μs
Setup time of stop condition	$t_{SU:STO}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			μs
Bus-free time	t_{BUF}	1.8 V ≤ V_{DD} ≤ 5.5 V	1.3			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution **The values in the above table apply even when the PIOR2 bit in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 320 pF, R_b = 1.1 kΩ

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3. I^2C fast mode plus

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz 2.7 V ≤ V_{DD} ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Hold time when SCLA0 is low	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.5			µs
Hold time when SCLA0 is high	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	50			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.45	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.5			µs

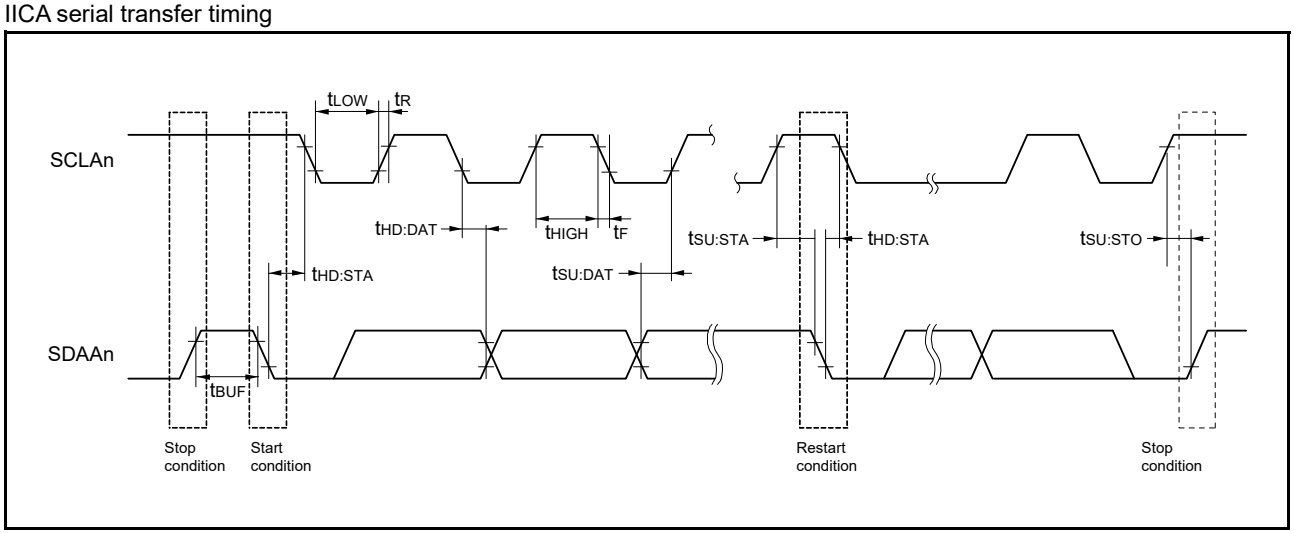
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when the PIOR2 bit in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0

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2.6 Characteristics of the Analog Circuits

2.6.1 Characteristics of the A/D converter for T_A = -40 to +85°C

Reference for the characteristics of the A/D converter

Reference Voltage Input Channel	Reference Voltage (+) = AV_{REFP} Reference Voltage (–) = AV_{REFM}	Reference Voltage (+) = V_{DD} Reference Voltage (–) = V_{SS}	Reference Voltage (+) = V_{BGR} Reference Voltage (–) = AV_{REFM}
ANI0 to ANI7	See **1** in **2.6.1**.	See **3** in **2.6.1**.	See **4** in **2.6.1**.
ANI16 to ANI19	See **2** in **2.6.1**.		
Internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU	See **1** in **2.6.1**.		—

1. Reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error**Note 1**	AINL	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V**Note 3**		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution conversion target: ANI2 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	µs
		10-bit resolution conversion target: Internal reference temperature sensor output voltage, and TSCAP voltage of the CTSU	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error**Notes 1, 4**	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V**Note 3**			±0.50	%FSR
Full-scale error**Notes 1, 4**	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V**Note 3**			±0.50	%FSR
Integral linearity error**Note 1**	ILE	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V**Note 3**			±5.0	LSB
Differential linearity error**Note 1**	DLE	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V**Note 3**			±2.0	LSB

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(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V) (2/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog input voltage	V_{AIN}	ANI2 to ANI7	0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TMPS25} Note 5			V
		TSCAP voltage of the CTSU (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TSCAP}			V

Note 1. This value does not include the quantization error (±1/2 LSB).

<R> **Note 2.** When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value when V_{DD} = AV_{REFP}.
Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when V_{DD} = AV_{REFP}.
Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when V_{DD} = AV_{REFP}.

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

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2. Reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI19

(TA = -40 to +85°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = AVREFP, reference voltage (–) = AVREFM = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 2	1.8 V ≤ AVREFP ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 3		1.2	±5.0	
Conversion time	tCONV	10-bit resolution conversion target: ANI16 to ANI19	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	μs
			1.6 V ≤ VDD ≤ 5.5 V	57		95	
Zero-scale error Notes 1, 4	EZS	10-bit resolution AVREFP = VDD Note 2	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 3			±0.60	
Full-scale error Notes 1, 4	EFS	10-bit resolution AVREFP = VDD Note 2	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 3			±0.60	
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 2	1.8 V ≤ AVREFP ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 3			±6.0	
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 2	1.8 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 3			±2.5	
Analog input voltage	VAIN	ANI16 to ANI19		0		AVREFP	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When AVREFP < VDD, the maximum values are as follows.
Overall error: Add ±4.0 LSB to the maximum value when VDD = AVREFP.
Zero-scale/full-scale error: Add ±0.20%FSR to the maximum value when VDD = AVREFP.
Integral linearity error/differential linearity error: Add ±2.0 LSB to the maximum value when VDD = AVREFP.

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs.

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

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3. Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage[Note 1], temperature sensor output voltage[Note 1], TSCAP voltage of the CTSU

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error[Note 2]	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V[Note 3]		1.2	±10.5	LSB
Conversion time	t_{CONV}	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	µs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error[Notes 2, 4]	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V[Note 3]			±0.85	%FSR
Full-scale error[Notes 2, 4]	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V[Note 3]			±0.85	%FSR
Integral linearity error[Note 2]	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V[Note 3]			±6.0	LSB
Differential linearity error[Note 2]	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V[Note 3]			±2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI7, ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR}[Note 5]			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25}[Note 5]			V
		TSCAP voltage of the CTSU (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TSCAP}			V

Note 1. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, V_{DD} must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

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4. Reference voltage (+) = V_{DD} (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{BGR}**Note 1**, reference voltage (–) = AV_{REFM}**Note 2** = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			Bit
Conversion time	t_{CONV}		17		39	µs
Zero-scale error**Notes 3, 4**	E_{ZS}				±0.60	%FSR
Integral linearity error**Note 3**	ILE				±2.0	LSB
Differential linearity error**Note 3**	DLE				±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR}**Note 1**	V

Note 1. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

Note 2. When reference voltage (–) = V_{SS}, the maximum values are as follows.
Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (–) = AV_{REFM}.

Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

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2.6.2 Characteristics of the A/D converter for T_A = -40 to +105°C

Reference for the characteristics of the A/D converter

Reference Voltage Input Channel	Reference Voltage (+) = AV_{REFP} Reference Voltage (–) = AV_{REFM}	Reference Voltage (+) = V_{DD} Reference Voltage (–) = V_{SS}	Reference Voltage (+) = V_{BGR} Reference Voltage (–) = AV_{REFM}
ANI0 to ANI7	See **1** in **2.6.2**.	See **3** in **2.6.2**.	See **4** in **2.6.2**.
ANI16 to ANI19	See **2** in **2.6.2**.		
Internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU	See **1** in **2.6.2**.		—

1. Reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error**Note 1**	AINL	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution conversion target: ANI2 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error**Notes 1, 3**	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Full-scale error**Notes 1, 3**	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Integral linearity error**Note 1**	ILE	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
Differential linearity error**Note 1**	DLE	10-bit resolution AV_{REFP} = V_{DD}**Note 2**	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI7		0		AV_{REFP}	V
		Internal reference voltage		V_{BGR}**Note 4**			V
		Temperature sensor output voltage		V_{TMPS25}**Note 4**			V
		TSCAP voltage of the CTSU		V_{TSCAP}			V

Note 1. This value does not include the quantization error (±1/2 LSB).

<R> **Note 2.** When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value when V_{DD} = AV_{REFP}.
Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when V_{DD} = AV_{REFP}.
Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when V_{DD} = AV_{REFP}.

Note 3. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 4. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

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2. Reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI19

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = AVREFP, reference voltage (–) = AVREFM = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 2	2.4 V ≤ AVREFP ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI16 to ANI19	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 3	EZS	10-bit resolution AVREFP = VDD Note 2	2.4 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 3	EFS	10-bit resolution AVREFP = VDD Note 2	2.4 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 2	2.4 V ≤ AVREFP ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 2	2.4 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI19		0		AVREFP	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When AVREFP < VDD, the maximum values are as follows.
Overall error: Add ±4.0 LSB to the maximum value when VDD = AVREFP.
Zero-scale/full-scale error: Add ±0.20%FSR to the maximum value when VDD = AVREFP.
Integral linearity error/differential linearity error: Add ±2.0 LSB to the maximum value when VDD = AVREFP.

Note 3. This value is indicated as a ratio (%FSR) to the full-scale value.

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3. Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error**Note 1**	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage, and and TSCAP voltage of the CTSU	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error**Notes 1, 2**	E_{ZS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error**Notes 1, 2**	E_{FS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error**Note 1**	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error**Note 1**	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI7, ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage		V_{BGR}**Note 3**			V
		Temperature sensor output voltage		V_{TMPS25}**Note 3**			V
		TSCAP voltage of the CTSU		V_{TSCAP}			V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

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4. Reference voltage (+) = V_{DD} (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{BGR} **Note 1**, reference voltage (–) = AV_{REFM} **Note 2** = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			Bit
Conversion time	t_{CONV}		17		39	µs
Zero-scale error **Notes 3, 4**	E_{ZS}				±0.60	%FSR
Integral linearity error **Note 3**	ILE				±2.0	LSB
Differential linearity error **Note 3**	DLE				±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} **Note 1**	V

Note 1. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

Note 2. When reference voltage (–) = V_{SS}, the maximum values are as follows.
Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (–) = AV_{REFM}.

Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

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2.6.3 Characteristics of the temperature sensor and internal reference voltage

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	F_{VTMPS}	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

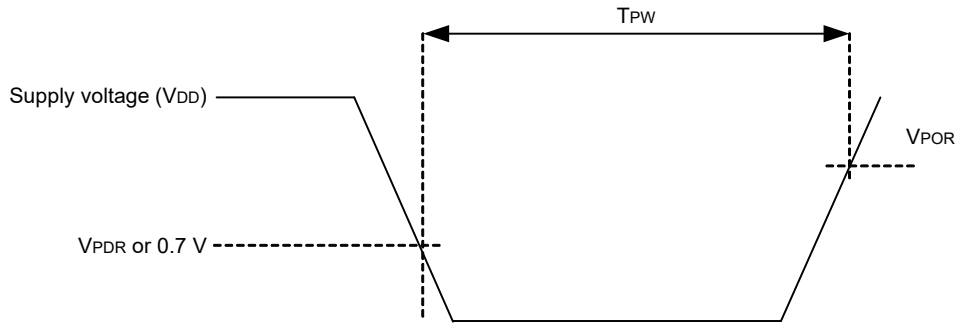
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2.6.4 Characteristics of the POR circuit

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V_{POR}, V_{PDR}		1.43	1.50	1.57	V
Minimum pulse width**Note**	T_{PW}		300			μs

Note This width is the minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This width is also the minimum time required for a POR reset from when V_{DD} falls below 0.7 V to when V_{DD} exceeds V_{POR} in the STOP mode or while the main system clock is stopped through setting the HIOSTOP and MSTOP bits in the clock operation status control register (CSC).



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2.6.5 Characteristics of the LVD circuit

1. LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		V_{LVD01}	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
		V_{LVD02}	The power supply voltage is rising.	2.59	2.67	2.75	V
			The power supply voltage is falling.	2.54	2.62	2.70	V
		V_{LVD03}	The power supply voltage is rising.	2.31	2.38	2.45	V
			The power supply voltage is falling.	2.26	2.33	2.40	V
		V_{LVD04}	The power supply voltage is rising.	1.84	1.90	1.95	V
			The power supply voltage is falling.	1.80	1.86	1.91	V
		V_{LVD05}	The power supply voltage is rising.	1.64	1.69	1.74	V
			The power supply voltage is falling.	1.60	1.65	1.70	V
Minimum pulse width		t_{LW}		500			μs
Detection delay time						500	μs

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2. LVD1 Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		V_{LVD11}	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		V_{LVD12}	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		V_{LVD13}	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		V_{LVD14}	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		V_{LVD15}	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		V_{LVD16}	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		V_{LVD17}	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		V_{LVD18}	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		V_{LVD19}	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		V_{LVD110}	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		V_{LVD111}	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		V_{LVD112}	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		V_{LVD113}	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		V_{LVD114}	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		V_{LVD115} **Note**	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		V_{LVD116} **Note**	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
		V_{LVD117} **Note**	The power supply voltage is rising.	1.64	1.67	1.70	V
			The power supply voltage is falling.	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		500			μs
Detection delay time						500	μs

Note This setting can only be used when LVD0 is disabled.

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2.6.6 Characteristics of the rising slope of the power supply voltage

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by LVD0 or an external reset until V_{DD} reaches the operating voltage range shown in AC characteristics.

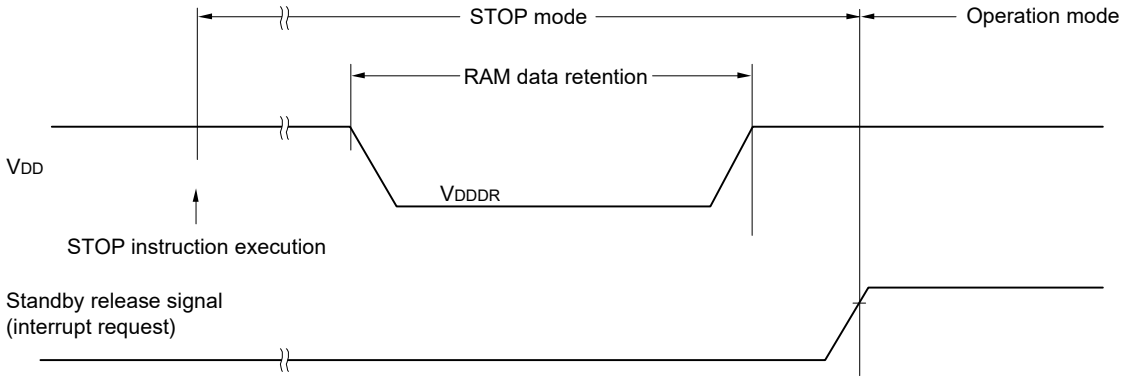
Downloaded from Arrow.com.

2.7 Characteristics of Retention of RAM Data

(T_A = -40 to +105°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		1.43[Note]		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.8 Characteristics of Flash Memory Programming

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}		1		32	MHz
Number of code flash memory rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = +85°C	1,000			Times
Number of data flash memory rewrites[Notes 1, 2, 3]		Retained for 1 year T_A = +25°C		1,000,000		
		Retained for 5 years T_A = +85°C	100,000			
		Retained for 20 years T_A = +85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using flash memory programmer and Renesas Electronics self-programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

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1. Code flash memory

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Security setting time		t_{AWSSAS}	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Data flash memory

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting of DFLCTL.DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

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2.9 Dedicated Flash Memory Programmer Communication (UART)

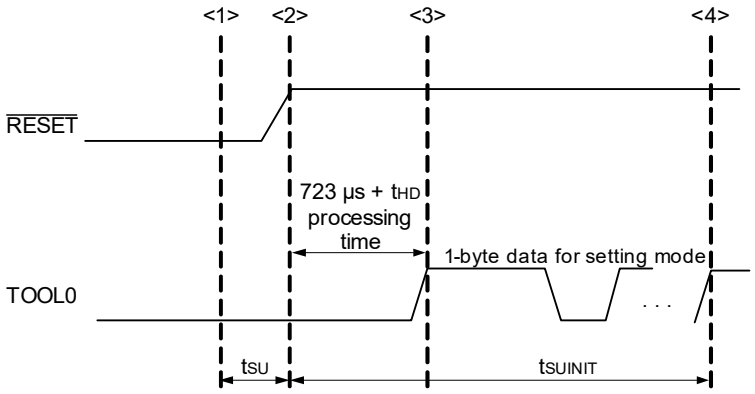
(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

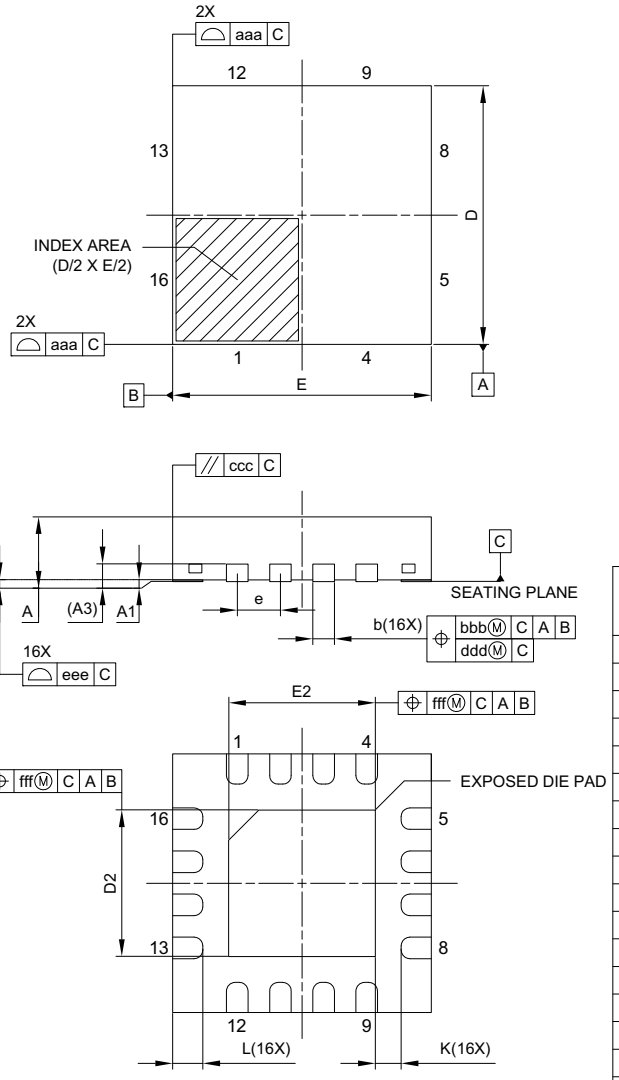
Remark t_{SUINIT}: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

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3. Package Drawings

3.1 16-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN016-3x3-0.50	PWQN0016KD-A	0.02

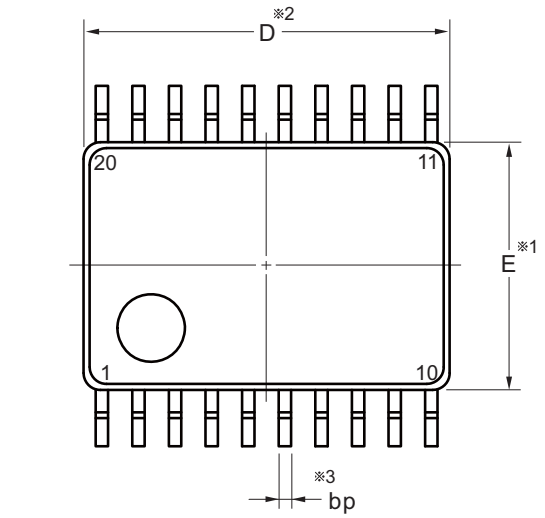


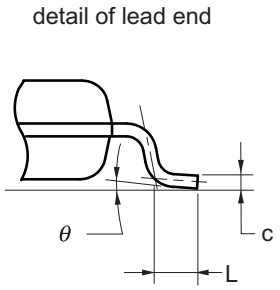
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
L	0.30	0.35	0.40
K	0.20	—	—
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

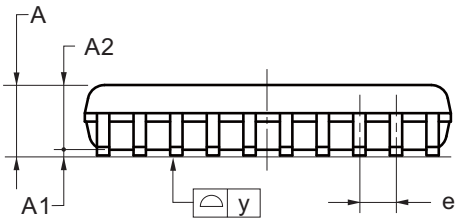
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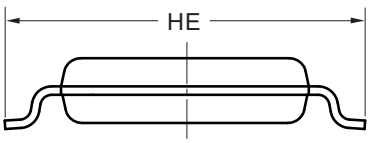
3.2 20-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1









(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

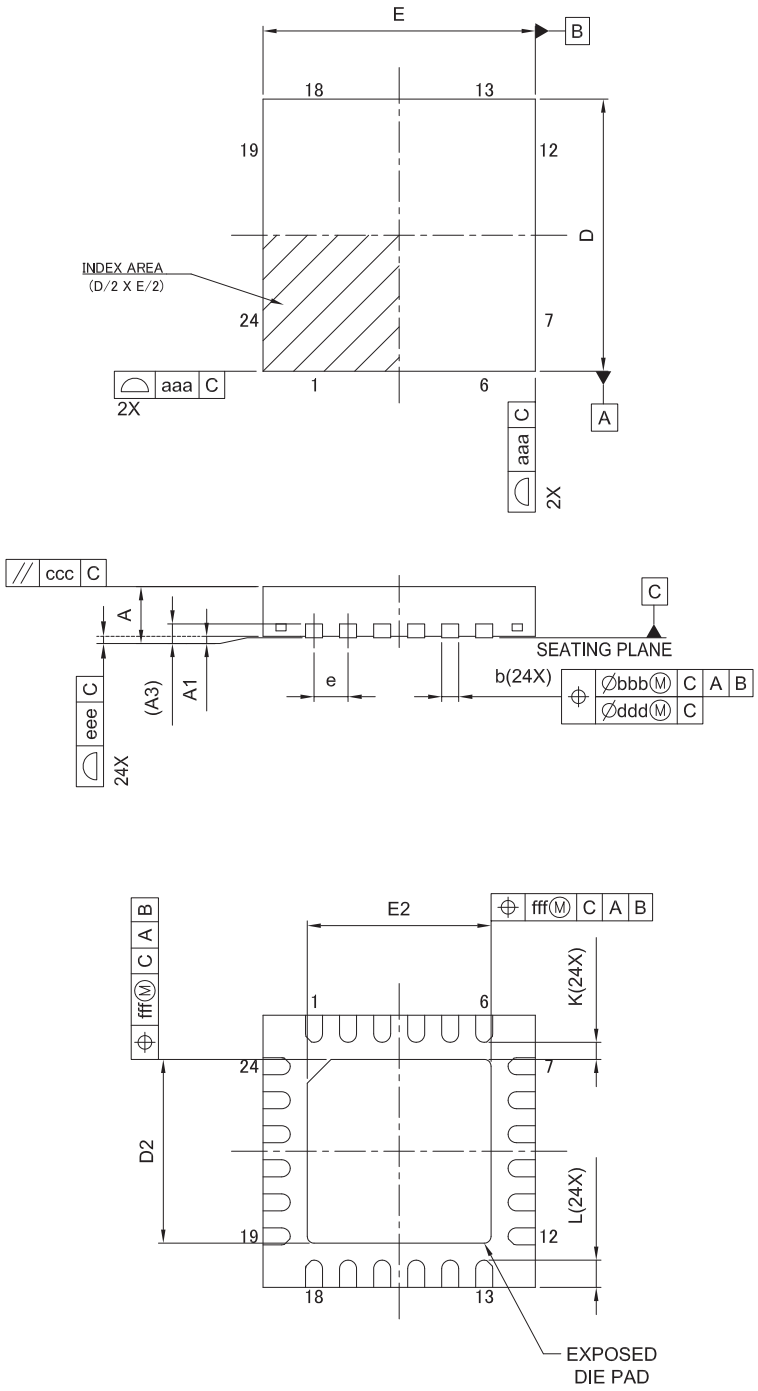
2.Dimension “※3” does not include trim offset.

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3.3 24-pin Products

JEITA Package Code	RENESAS Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KG-A	0.04

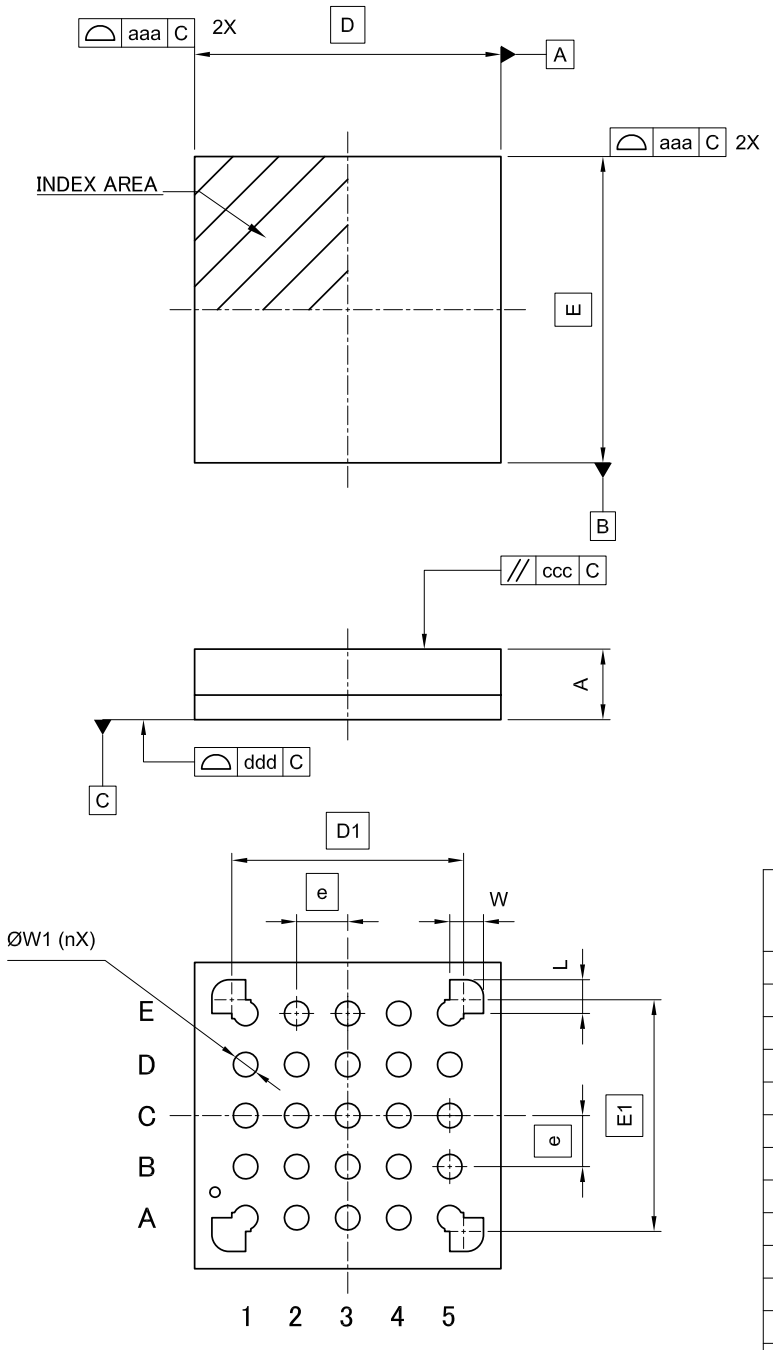


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

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3.4 25-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-WLGA25-3x3-0.50	PWLG0025KB-A	0.01

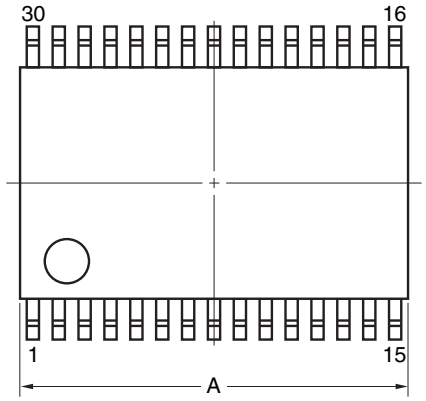


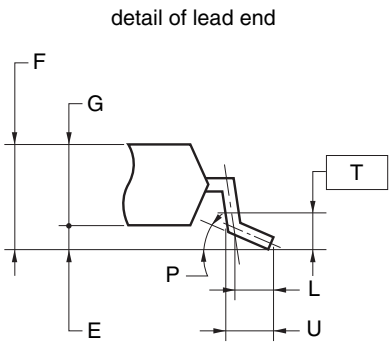
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	3.00	—
E	—	3.00	—
D1		2.27	
E1		2.27	
A	—	—	0.76
W1	0.19	0.24	0.29
W	—	0.330	—
L	—	0.330	—
e		0.50	
aaa	—	—	0.10
ccc	—	—	0.20
ddd	—	—	0.08
n	—	25	—

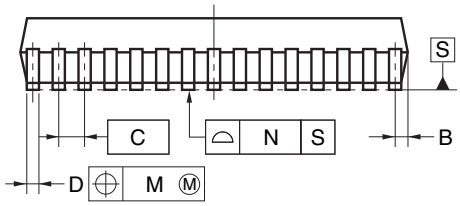
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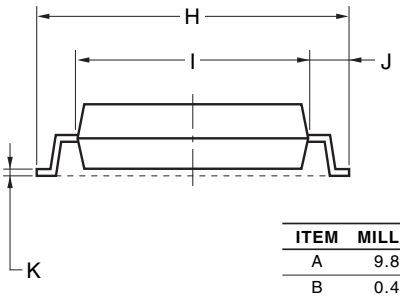
3.5 30-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18









NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

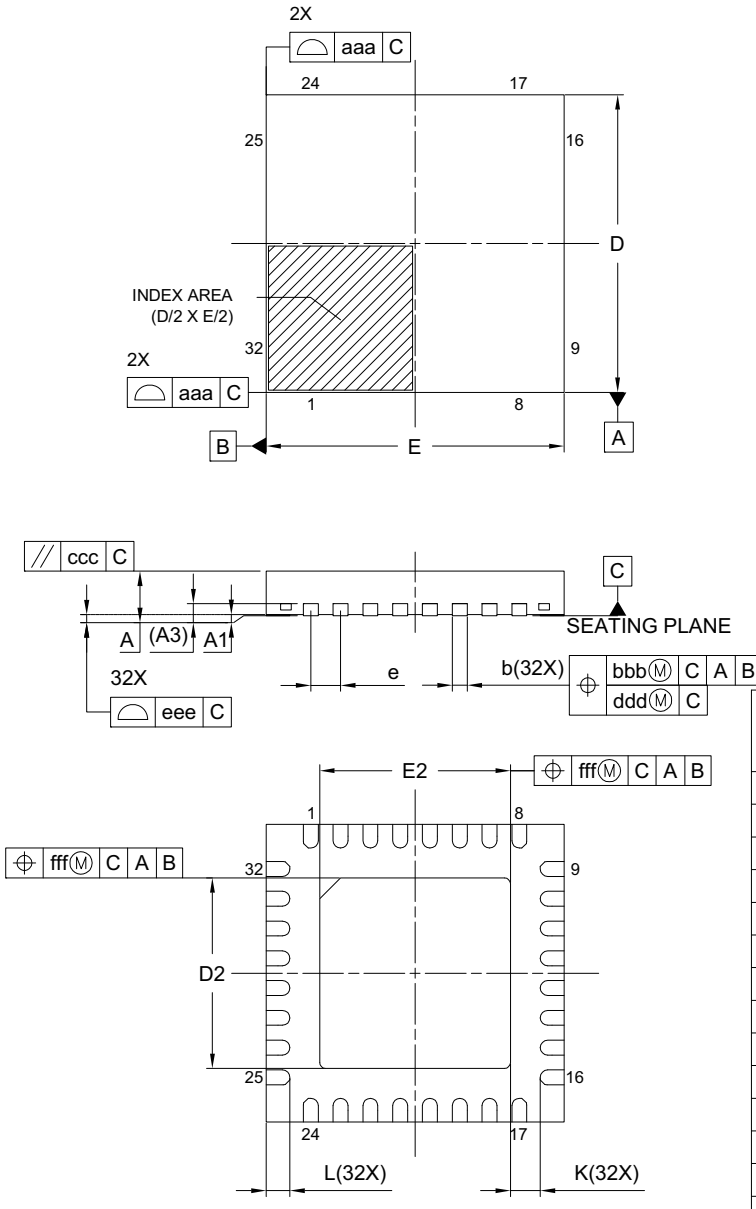
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

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3.6 32-pin Products

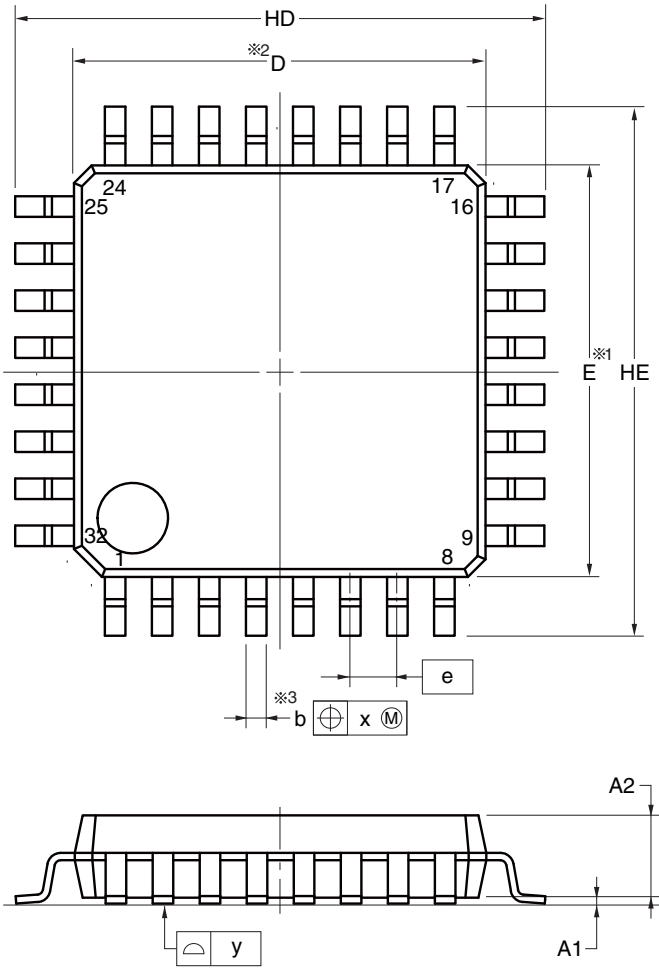
JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



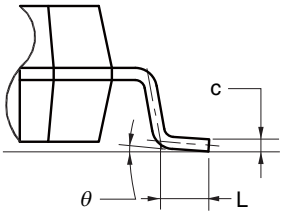
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

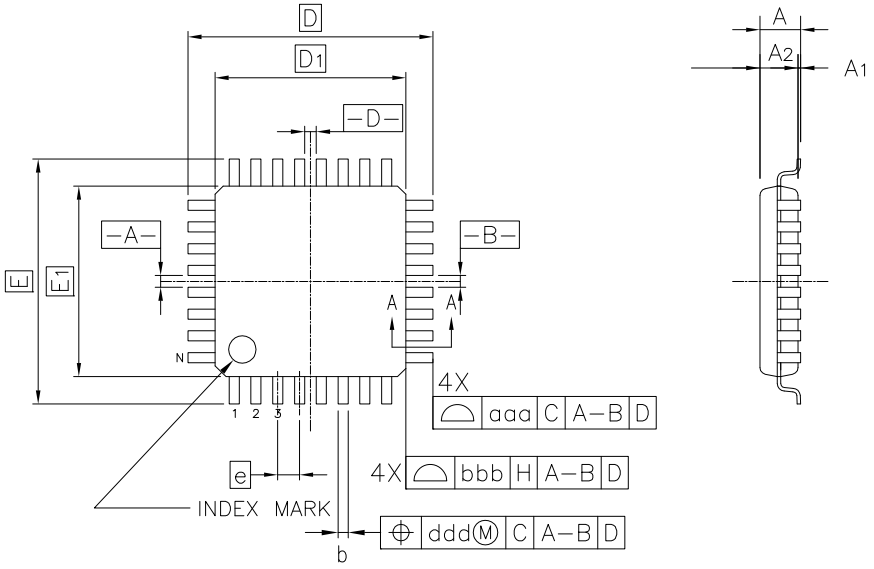
1.Dimensions "※1" and "※2" do not include mold flash.

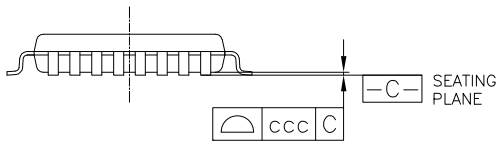
2.Dimension "※3" does not include trim offset.

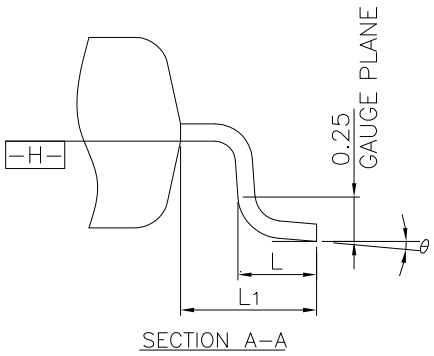
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JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP32-7x7-0.80	PLQP0032GE-A	0.18





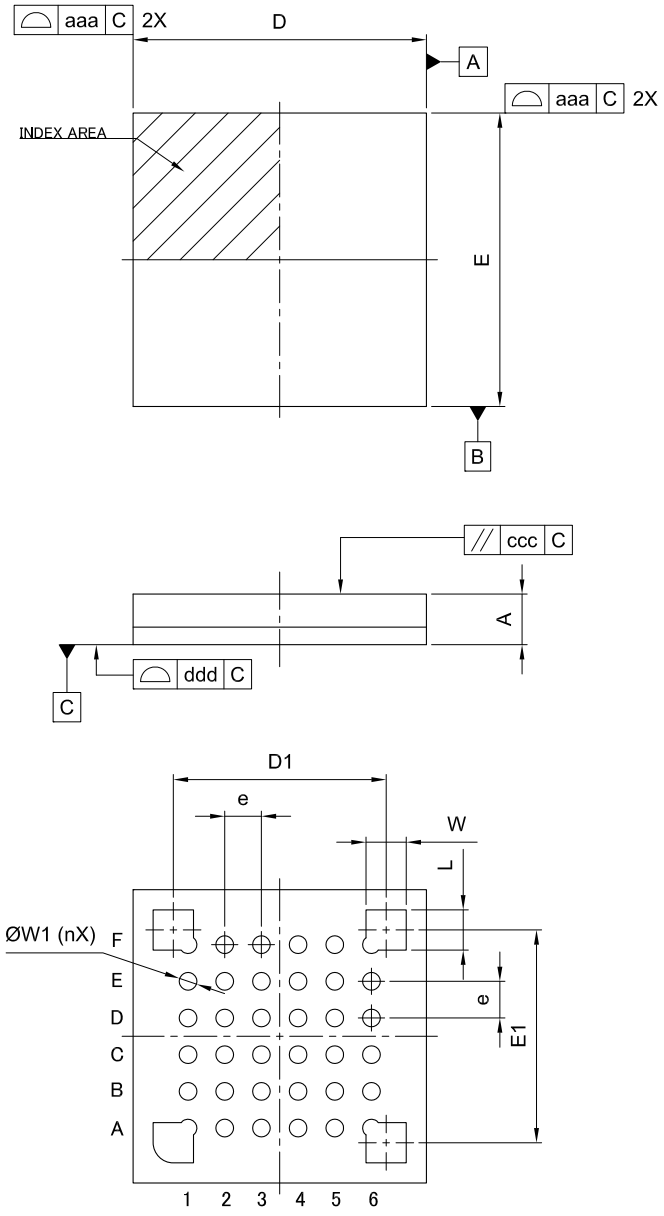


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	9.00	–
D_1	–	7.00	–
E	–	9.00	–
E_1	–	7.00	–
N	–	32	–
e	–	0.80	–
b	0.30	0.37	0.45
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.10
ddd	–	–	0.20

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3.7 36-pin Products

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-WFLGA36-4×4-0.50	PWLG0036KB-A	0.02

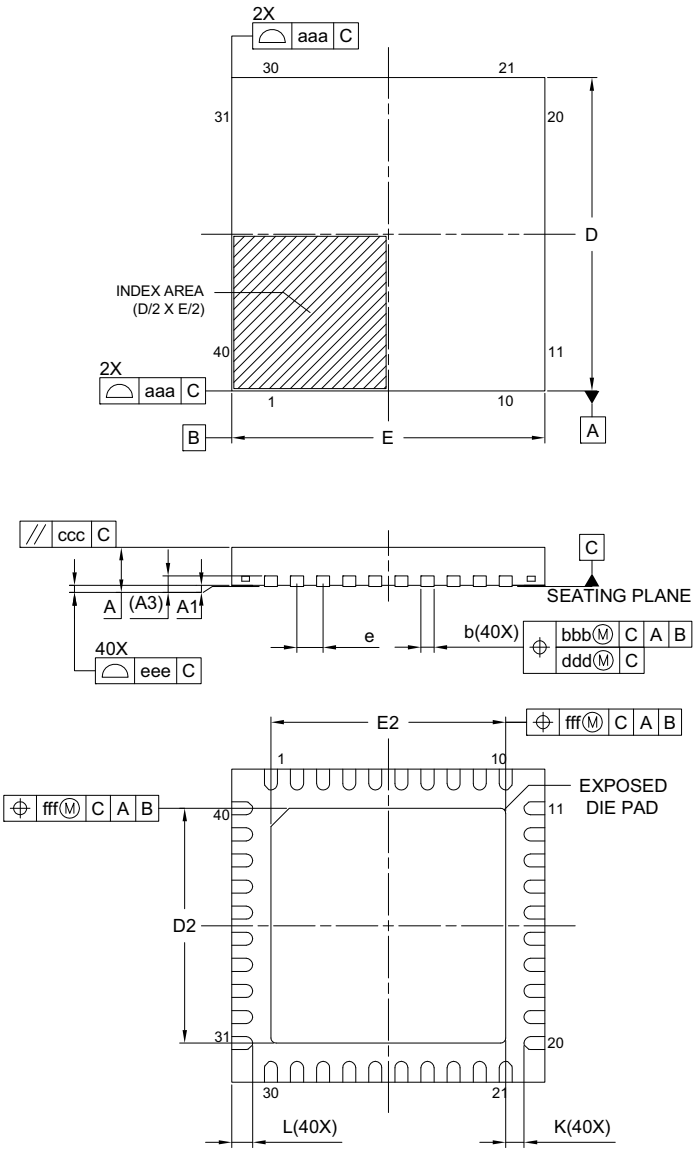


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	4.00	—
E	—	4.00	—
D1	2.90 BSC		
E1	2.90 BSC		
A	—	—	0.76
W1	0.19	0.24	0.29
W	—	0.55	—
L	—	0.55	—
e	0.50 BSC		
aaa	0.10		
ccc	0.20		
ddd	0.08		
n	—	36	—

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3.8 40-pin Products

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08

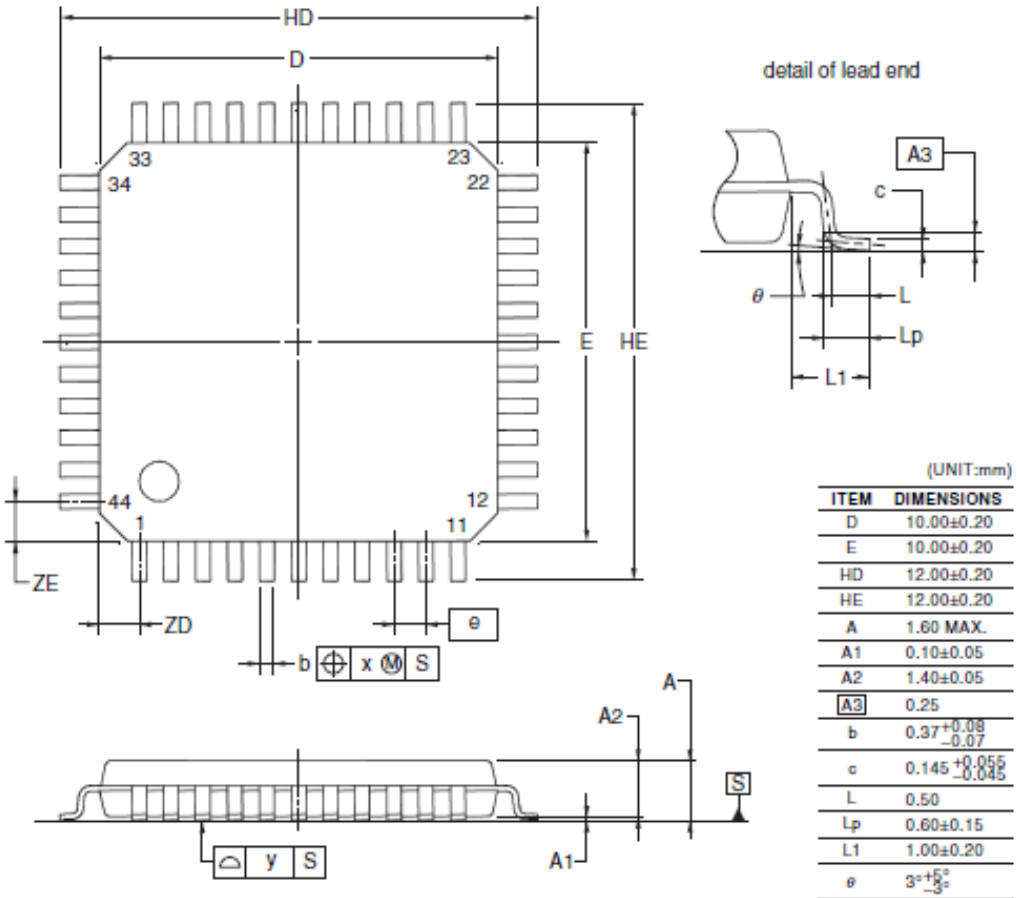


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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3.9 44-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



(UNIT:mm)

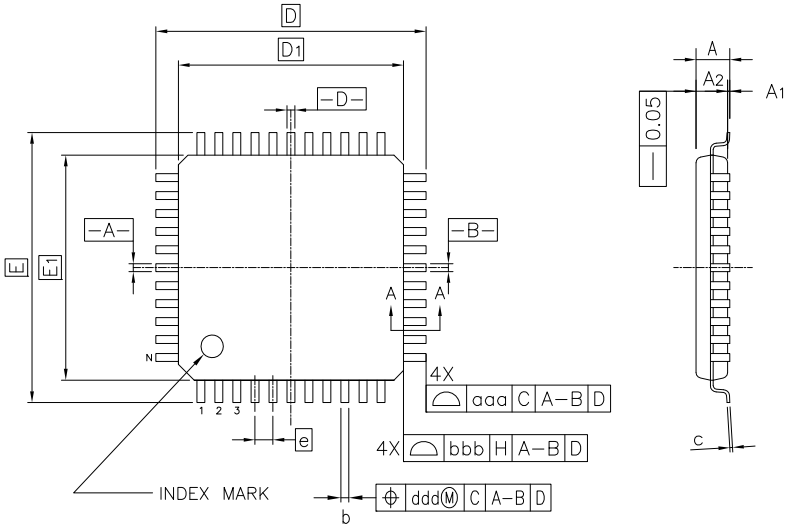
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

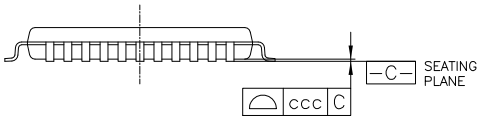
NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

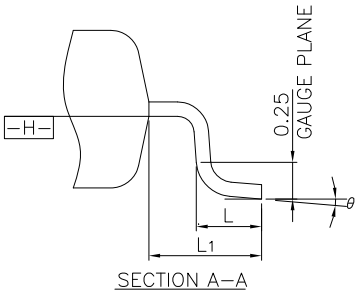
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JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP044-10x10-0.80	PLQP0044GE-A	0.34





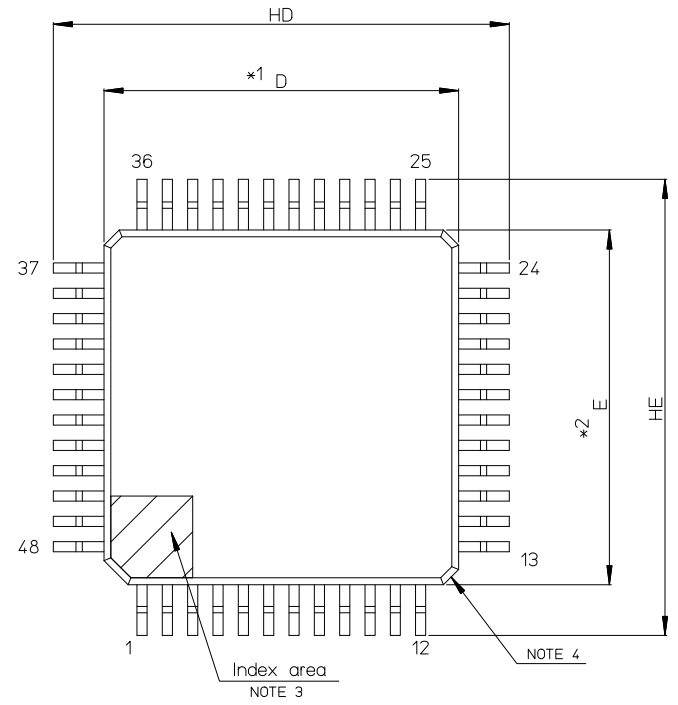


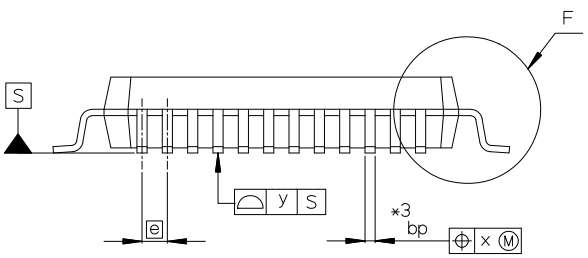
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	12.00	–
D_1	–	10.00	–
E	–	12.00	–
E_1	–	10.00	–
N	–	44	–
e	–	0.80	–
b	0.30	0.37	0.45
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.10
ddd	–	–	0.20

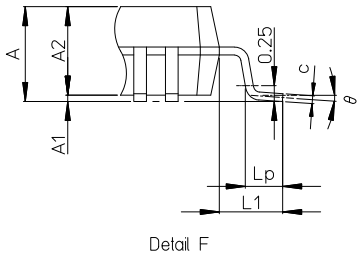
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3.10 48-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







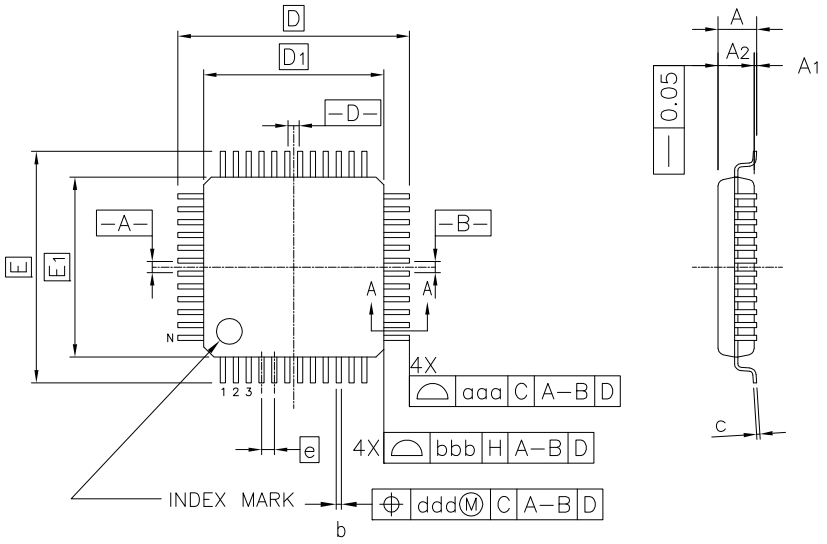
Detail F

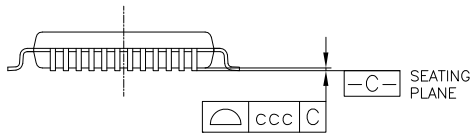
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

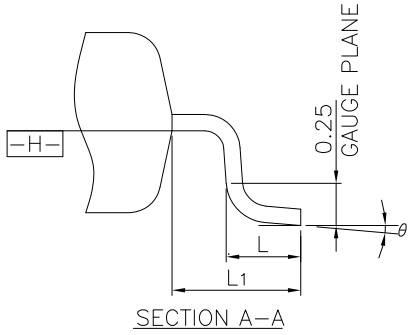
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

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JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP48-7x7-0.50	PLQP0048KL-A	0.18



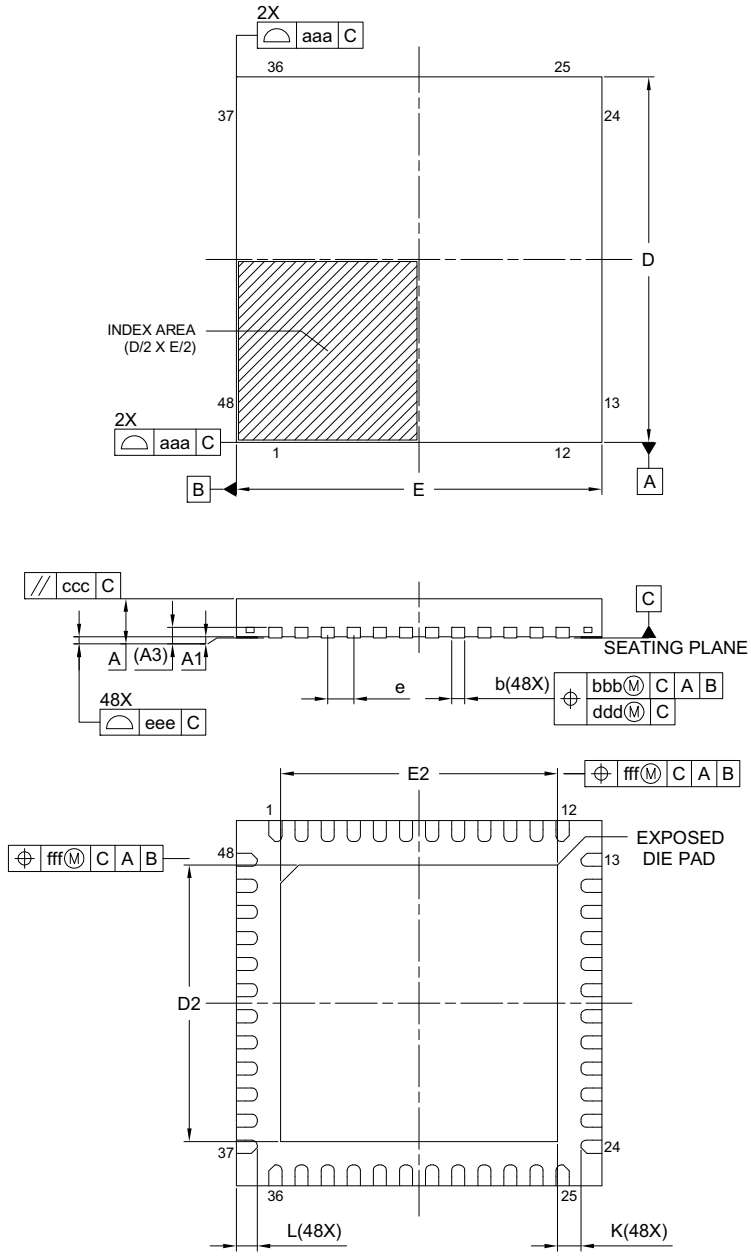




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	9.00	–
D_1	–	7.00	–
E	–	9.00	–
E_1	–	7.00	–
N	–	48	–
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

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JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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Revision History	RL78/G22 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 28, 2022	—	First edition issued
1.10	Jun 12, 2024	p.4	Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22 was modified.
		p.5	Table 1 - 1 List of Ordering Part Numbers was modified.
		p.54	2.4 AC Characteristics was modified.
		p.114	3.6 32-pin Products: The figure was added.
		p.118	3.9 44-pin Products: The figure was added.
		p.120	3.10 48-pin Products: The figure was added.
1.20	Jun 30, 2026	p.22	Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2) was modified.
		p.25	Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (1/2) was modified.
		p.46	2.3.2 Characteristics of the supply current: Notes 1 to 4 were modified.
		p.48	2.3.2 Characteristics of the supply current: Note 2 and Remark 2 were modified.
		p.49	2.3.2 Characteristics of the supply current: Notes 1 and 3 to 5 were modified.
		p.50	2.3.2 Characteristics of the supply current: Notes 3 and 6, and Remark 2 were modified.
		p.51, p.52	2.3.2 Characteristics of the supply current was modified, and Note 7 was added.
		p.91	2.6.1 Characteristics of the A/D converter for TA = -40 to +85°C: Note 2 was modified.
		p.95	2.6.2 Characteristics of the A/D converter for TA = -40 to +105°C: Note 2 was modified.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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