Datasheet

Serial EEPROM Series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24G256xxx-5 Series

General Description

BR24G256xxx-5 Series is a 256Kbit serial EEPROM of I²C BUS Interface.

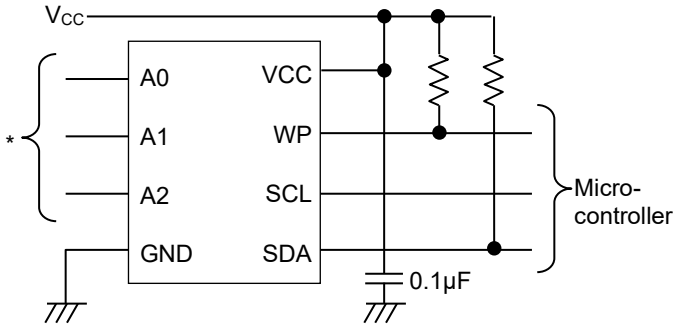
Features

- All Controls Available by 2 Ports of Serial Clock (SCL) and Serial Data (SDA)
- 1.6V to 5.5V Wide Limit of Operating Voltage, Possible 1MHz Operation
- Page Write Mode 64Byte
- Bit Format 32K x 8bit
- Low Current Consumption
- Prevention of Miswriting
  - ➢ WP (Write Protect) Function Added
  - ➢ Prevention of Miswriting at Low Voltage
- Noise Filter Built-in SCL / SDA Pin
- Initial Delivery State FFh

Applications

Ordinary Electronic Equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.).

Typical Application Circuit



* Connect A0, A1, A2 to VCC or GND.
These pins have pull-down elements inside the IC.
If pins are open, they are the same as when they are connected to GND.

Figure 1. Typical Application Circuit

Key Specifications

- Write Cycles: 4 Million Times (Ta=25°C)
- Data Retention: 200 Years (Ta=55°C)
- Write Cycle Time: 5ms (Max)
- Supply Voltage: 1.6V to 5.5V
- Ambient Operating Temperature: -40°C to +85°C

Packages

	W(Typ) x D(Typ) x H(Max)
SOP8*1	5.00mm x 6.20mm x 1.71mm
SOP-J8	4.90mm x 6.00mm x 1.65mm
TSSOP-B8	3.00mm x 6.40mm x 1.20mm
MSOP8	2.90mm x 4.00mm x 0.90mm
VSON008X2030*1	2.00mm x 3.00mm x 0.60mm
VSN08AX2030A	2.00mm x 3.00mm x 0.60mm

*1 Last Time Buy.

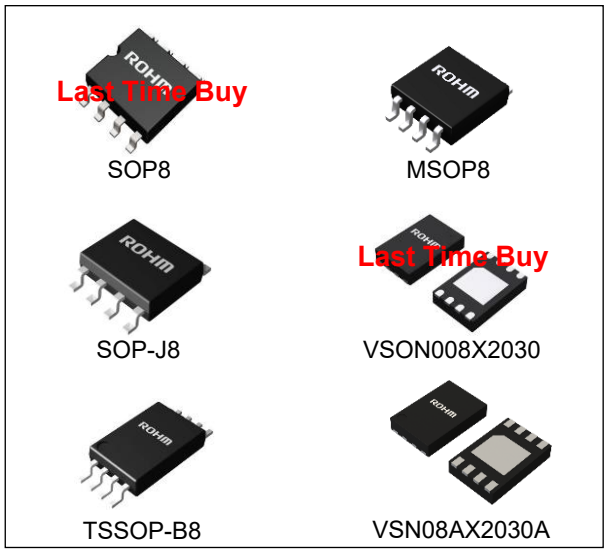


Figure 2

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Pin Configuration

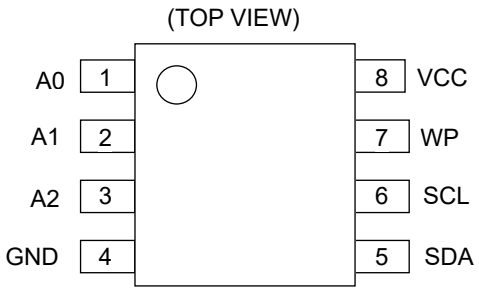


Figure 3-(a). Pin Configuration
(SOP8*1, SOP-J8, TSSOP-B8, MSOP8)
*1 Last Time Buy.

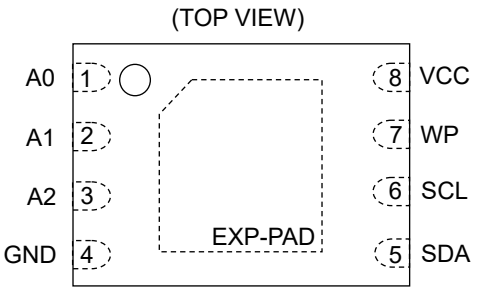


Figure 3-(b). Pin Configuration
(VSON008X2030*1, VSN08AX2030A)
*1 Last Time Buy.

Pin Description

Pin No.	Pin Name	Input / Output	Descriptions
1	A0	Input	Slave address setting*(Note 1)*
2	A1	Input	Slave address setting*(Note 1)*
3	A2	Input	Slave address setting*(Note 1)*
4	GND	-	Reference voltage of all input / output, 0V
5	SDA	Input / Output	Serial data input / serial data output*(Note 2)*
6	SCL	Input	Serial clock input
7	WP	Input	Write protect pin*(Note 3)*
8	VCC	-	Connect the power source
-	EXP-PAD	-	Leave as OPEN or connect to GND

(Note 1) Connect to VCC or GND. There are pull-down elements inside the IC. If pins are open, they are the same as when they are connected to GND.
(Note 2) SDA is NMOS open drain, so it requires a pull-up resistor.
(Note 3) Connect to VCC or GND, or control to 'HIGH' level or 'LOW' level. There are pull-down elements inside the IC. If this pin is open, this input is recognized as 'LOW'.

Block Diagram

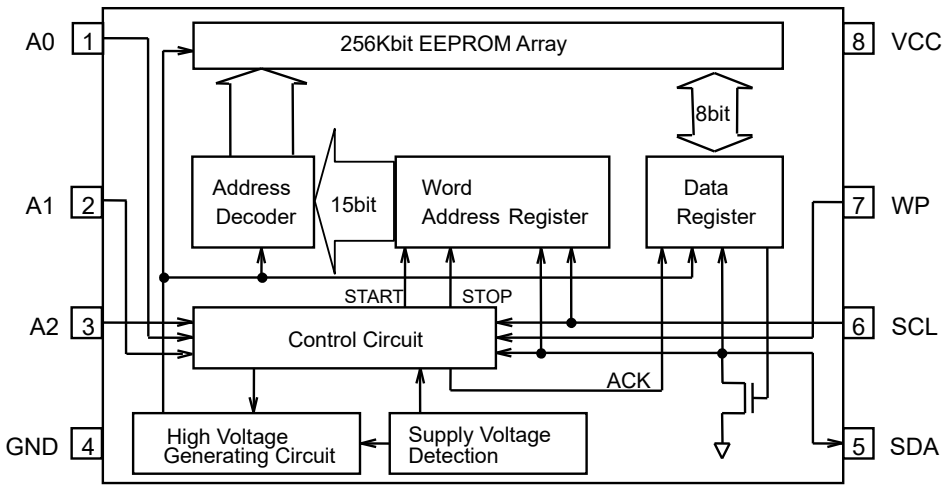


Figure 4. Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	Ta=25°C
Input Voltage / Output Voltage	-	-0.3 to V_{CC}+1.0	V	Ta=25°C.The maximum value of input voltage/ output voltage is not over than 6.5V. When the pulse width is 50ns or less, the minimum value of input voltage/output voltage is -1.0V.
Electro Static Discharge (Human Body Model)	V_{ESD}	-3000 to +3000	V	Ta=25°C
Maximum Output Low Current (SDA)	I_{OLMAX}	10	mA	Ta=25°C
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-65 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
SOP8*1				
Junction to Ambient	θ_{JA}	197.4	109.8	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	21	19	°C/W
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	18	11	°C/W
TSSOP-B8				
Junction to Ambient	θ_{JA}	251.9	152.1	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	31	20	°C/W
MSOP8				
Junction to Ambient	θ_{JA}	284.1	135.4	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	21	11	°C/W

*1 Last Time Buy.

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Thermal Resistance(Note 8) - continued

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 10)	2s2p(Note 11)	
VSON008X2030*1				
Junction to Ambient	θ_{JA}	308.3	69.6	°C/W
Junction to Top Characterization Parameter(Note 9)	Ψ_{JT}	43	10	°C/W
VSN08AX2030A				
Junction to Ambient	θ_{JA}	299.5	77.8	°C/W
Junction to Top Characterization Parameter(Note 9)	Ψ_{JT}	42	18	°C/W

*1 Last Time Buy.
(Note 8) Based on JESD51-2A(Still-Air)
(Note 9) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 10) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 11) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 12)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 12) This thermal via connects with the copper pattern of all layers.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	1.6	-	5.5	V
Ambient Operating Temperature	Ta	-40	-	+85	°C
Bypass capacitor(Note 13)	C	0.1	-	-	µF

(Note 13) Connect a bypass capacitor between the IC's VCC and GND pin.

Input / Output Capacitance (Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input / Output Capacitance (SDA)(Note 14)	$C_{I/O}$	-	-	8	pF	$V_{I/O}$=GND
Input Capacitance (SCL, A0, A1, A2, WP)(Note 14)	C_{IN}	-	-	8	pF	V_{IN}=GND

(Note 14) Not 100% TESTED.

Input Impedance (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC}=1.6V to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Impedance 1	Z_{IH}	500	-	-	kΩ	$0.7V_{CC} \leq V_{IN}$ (A0, A1, A2, WP)
Input Impedance 2	Z_{IL}	30	-	-	kΩ	$V_{IN} \leq 0.3V_{CC}$ (A0, A1, A2, WP)

Memory Cell Characteristics (V_{CC}=1.6V to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Write Cycles(Note 15,16)	-	4,000,000	-	-	Times	Ta=25°C
Data Retention(Note 15)	-	200	-	-	Years	Ta=55°C

(Note 15) Not 100% TESTED.
(Note 16) The Write Cycles is defined for unit of 4 data bytes with the same address bits of WA14 to WA2.

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Electrical Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC}=1.6V to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input High Voltage 1	V_{IH1}	0.7V_{CC}	-	V_{CC}+1.0	V	1.7V≤V_{CC}≤5.5V
Input Low Voltage 1	V_{IL1}	-0.3*(Note 17)*	-	+0.3V_{CC}	V	1.7V≤V_{CC}≤5.5V
Input High Voltage 2	V_{IH2}	0.8V_{CC}	-	V_{CC}+1.0	V	1.6V≤V_{CC}<1.7V
Input Low Voltage 2	V_{IL2}	-0.3*(Note 17)*	-	+0.2V_{CC}	V	1.6V≤V_{CC}<1.7V
Output Low Voltage 1	V_{OL1}	-	-	0.4	V	I_{OL}=3.2mA, 2.5V≤V_{CC}≤5.5V (SDA)
Output Low Voltage 2	V_{OL2}	-	-	0.2	V	I_{OL}=1.0mA, 1.6V≤V_{CC}<2.5V (SDA)
Input Leakage Current 1	I_{LI1}	-1	-	+1	μA	V_{IN}=0 or V_{CC} (A0, A1, A2, WP) Standby Mode
Input Leakage Current 2	I_{LI2}	-1	-	+1	μA	V_{IN}=0 to V_{CC} (SCL)
Output Leakage Current	I_{LO}	-1	-	+1	μA	V_{OUT}=0 to V_{CC} (SDA)
Supply Current (Write) *(Note 18)*	I_{CC1}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCL}=1MHz, t_{WR}=5ms, Byte Write, Page Write
Supply Current (Read) *(Note 18)*	I_{CC2}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCL}=1MHz Random Read, Current Read, Sequential Read
Standby Current	I_{SB}	-	-	2.5	μA	V_{CC}=5.5V, SDA, SCL=V_{CC} A0, A1, A2, WP=GND

(Note 17) When the pulse width is 50ns or less, it is -1.0V.
(Note 18) The average value during operation.

AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC}=1.6V to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{SCL}	-	-	1	MHz
Data Clock High Period	t_{HIGH}	260	-	-	ns
Data Clock Low Period	t_{LOW}	500	-	-	ns
SDA, SCL (input) Rise Time*(Note 19)*	t_R	-	-	1000	ns
SDA, SCL (input) Fall Time*(Note 19)*	t_{F1}	-	-	1000	ns
SDA (output) Fall Time*(Note 19)*	t_{F2}	-	-	120	ns
Start Condition Hold Time	$t_{HD:STA}$	250	-	-	ns
Start Condition Setup Time	$t_{SU:STA}$	200	-	-	ns
Input Data Hold Time	$t_{HD:DAT}$	0	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	50	-	-	ns
Output Data Delay Time	t_{PD}	50	-	450	ns
Output Data Hold Time	t_{DH}	50	-	-	ns
Stop Condition Setup Time	$t_{SU:STO}$	250	-	-	ns
Bus Free Time	t_{BUF}	500	-	-	ns
Write Cycle Time	t_{WR}	-	-	5	ms
Noise Suppression Time (SCL, SDA)	t_I	-	-	50	ns
WP Hold Time	$t_{HD:WP}$	1.0	-	-	μs
WP Setup Time	$t_{SU:WP}$	0.1	-	-	μs
WP High Period	$t_{HIGH:WP}$	1.0	-	-	μs

(Note 19) Not 100% TESTED.

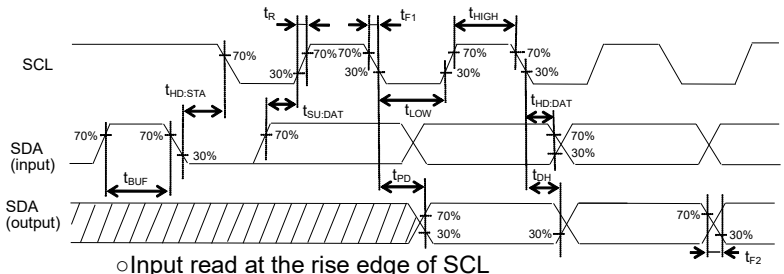
AC Characteristics Condition

Parameter	Symbol	Conditions	Unit
Load Capacitance	C_L	100	pF
Input Rise Time	t_R	20	ns
Input Fall Time	t_{F1}	20	ns
Input Voltage	V_{IL}/V_{IH}	0.2V_{CC}/0.8V_{CC}	V
Input / Output Data Timing Reference Level	-	0.3V_{CC}/0.7V_{CC}	V

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Input / Output Timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Figure 5-(a). Input / Output Timing

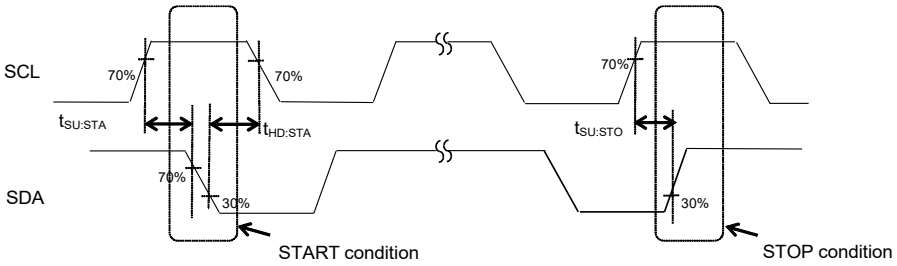


Figure 5-(b). Start-Stop Condition Timing

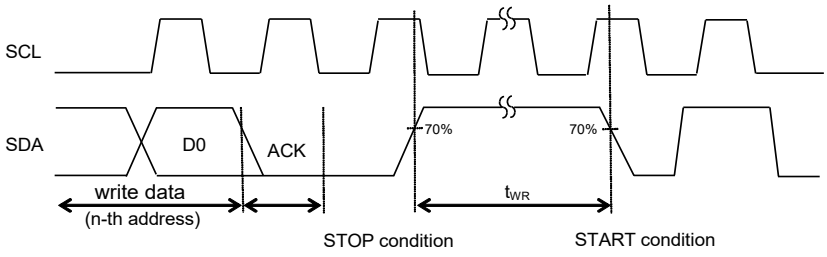


Figure 5-(c). Write Cycle Timing

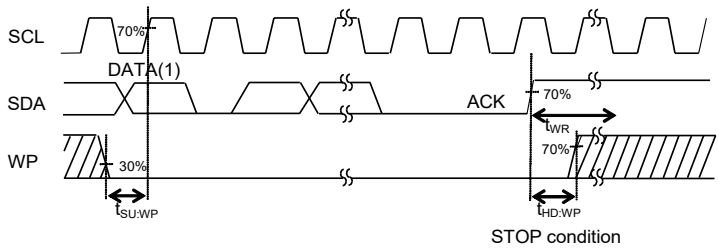


Figure 5-(d). WP Timing at Write Execution

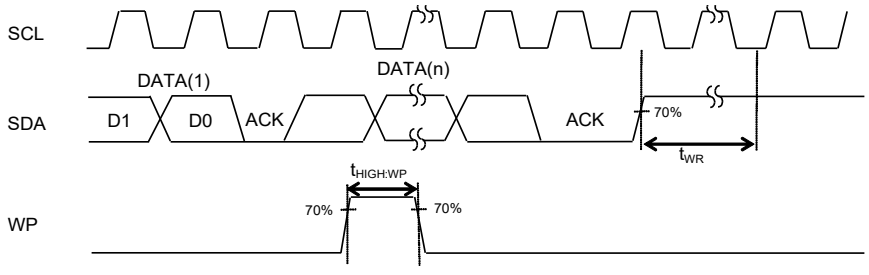


Figure 5-(e). WP Timing at Write Cancel

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Typical Performance Curves

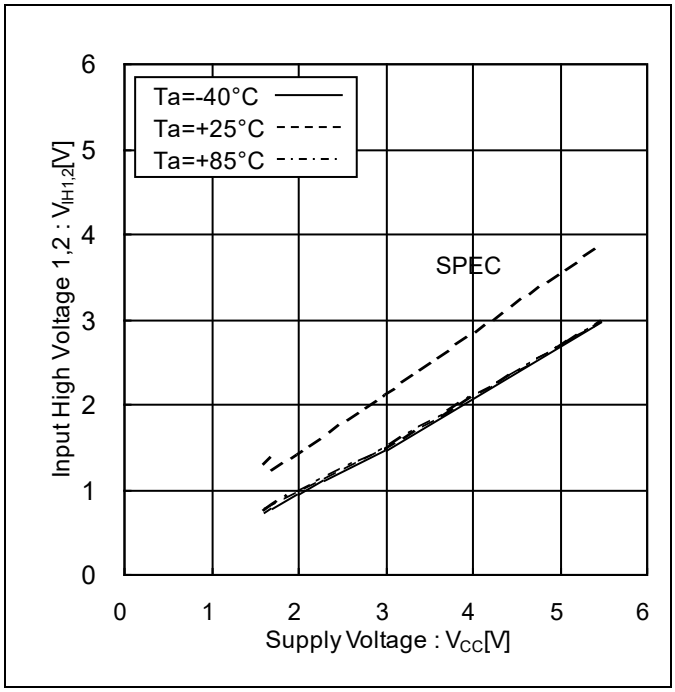


Figure 6. Input High Voltage 1,2 vs Supply Voltage

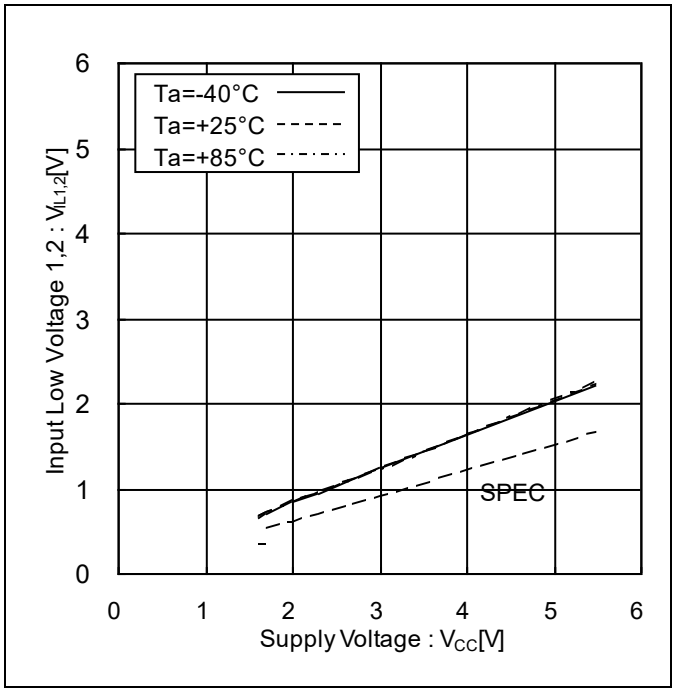


Figure 7. Input Low Voltage 1,2 vs Supply Voltage

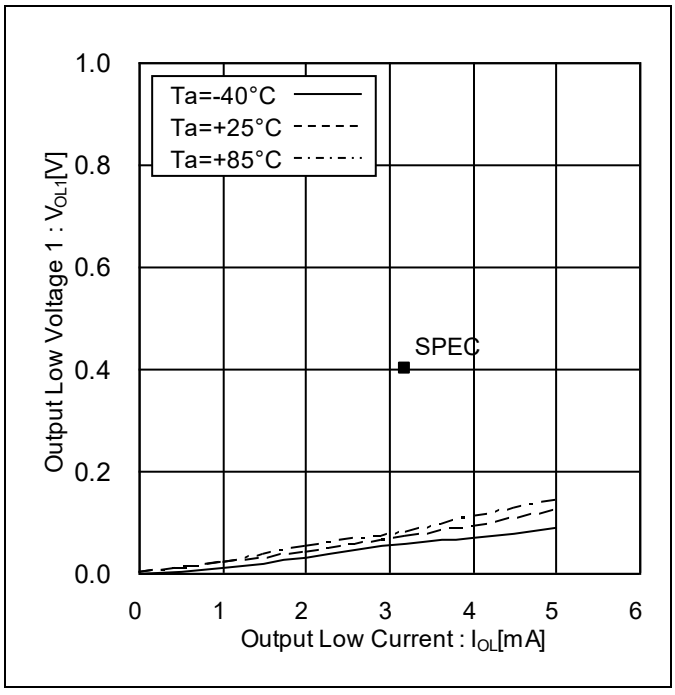


Figure 8. Output Low Voltage 1 vs Output Low Current (V_{CC}=2.5V)

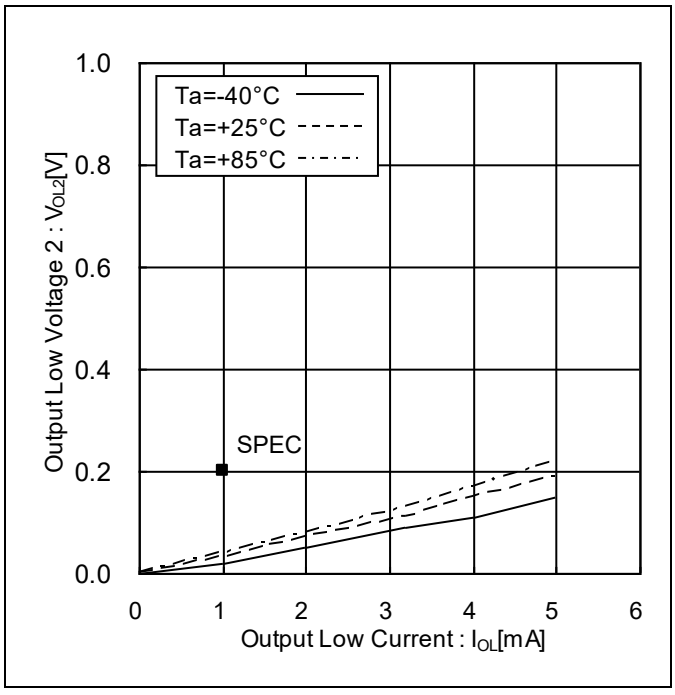


Figure 9. Output Low Voltage 2 vs Output Low Current (V_{CC}=1.6V)

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Typical Performance Curves - continued

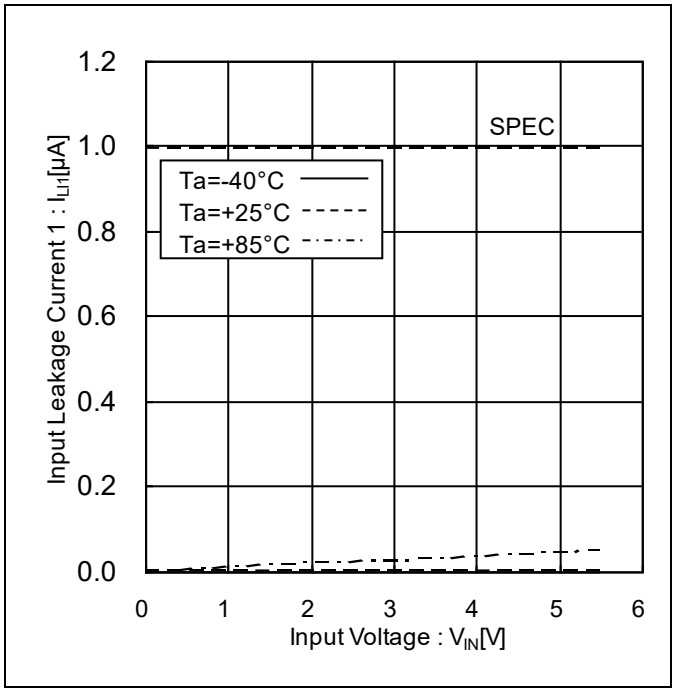


Figure 10. Input Leakage Current 1 vs Input Voltage (Standby Mode)

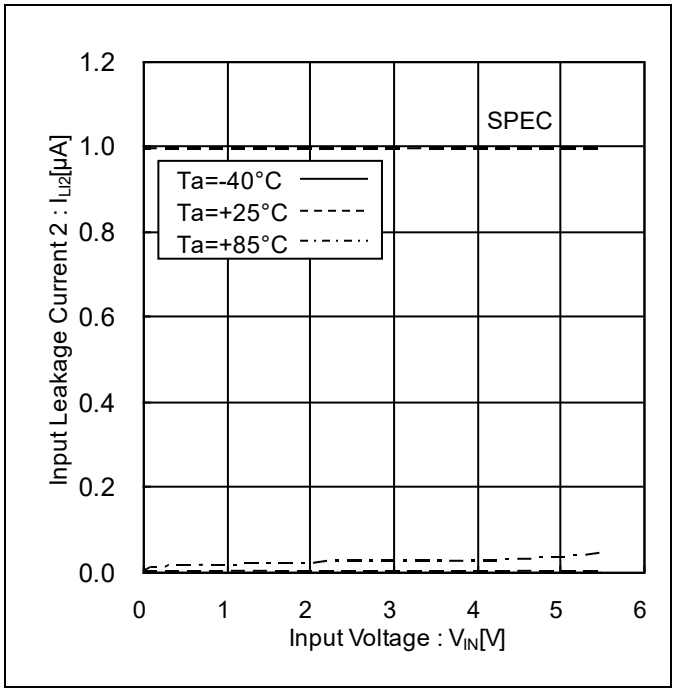


Figure 11. Input Leakage Current 2 vs Input Voltage

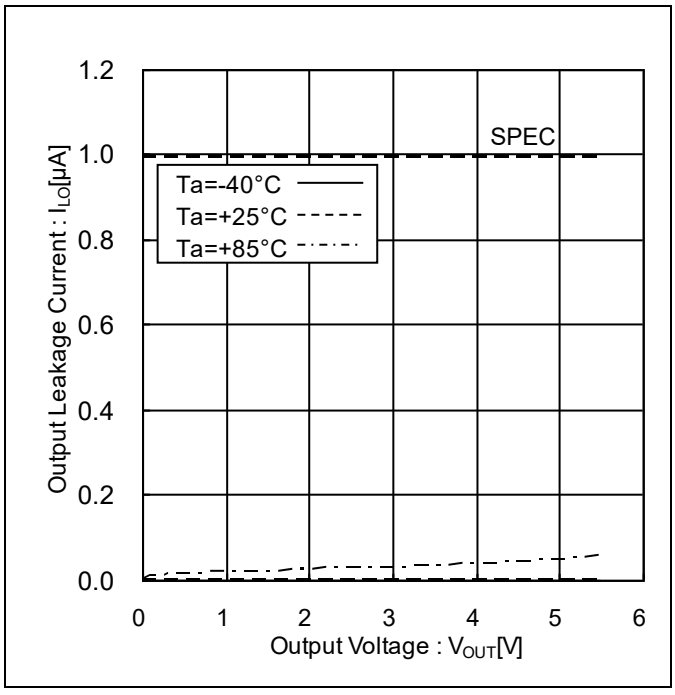


Figure 12. Output Leakage Current vs Output Voltage

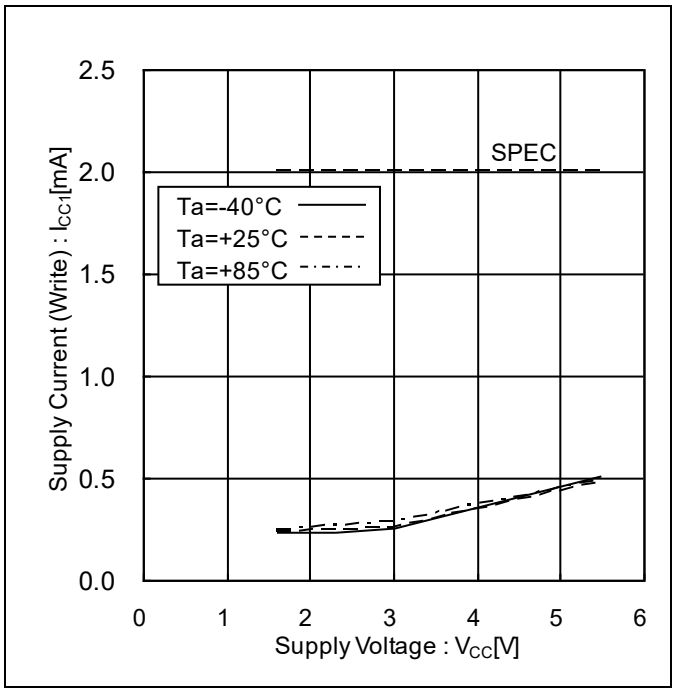


Figure 13. Supply Current (Write) vs Supply Voltage

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Typical Performance Curves - continued

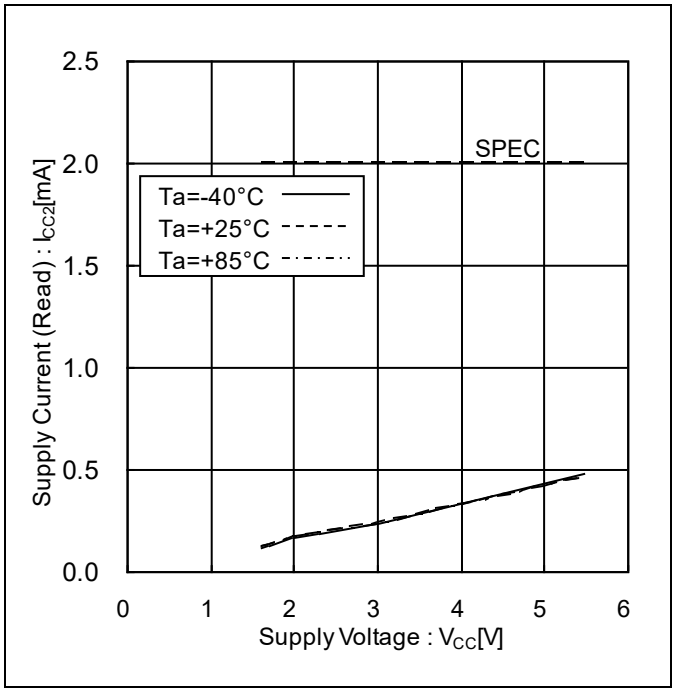


Figure 14. Supply Current (Read) vs Supply Voltage (f_{SCL}=1MHz)

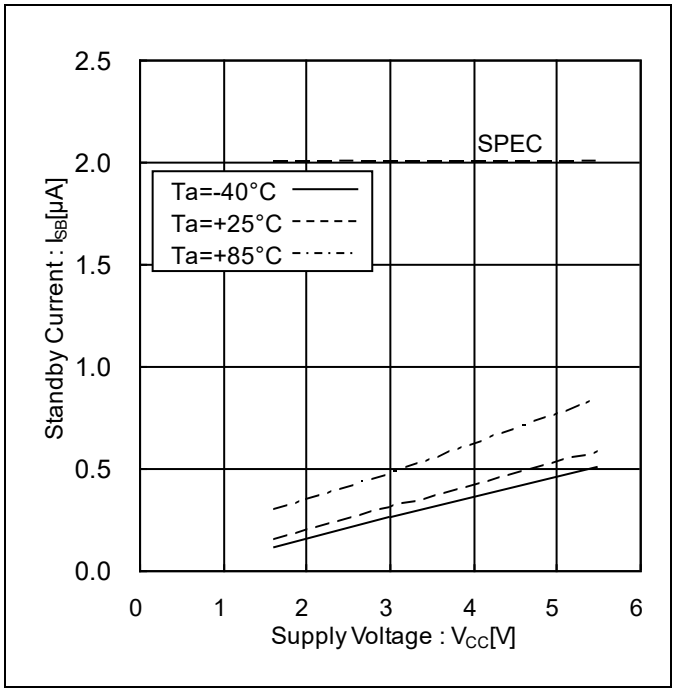


Figure 15. Standby Current vs Supply Voltage

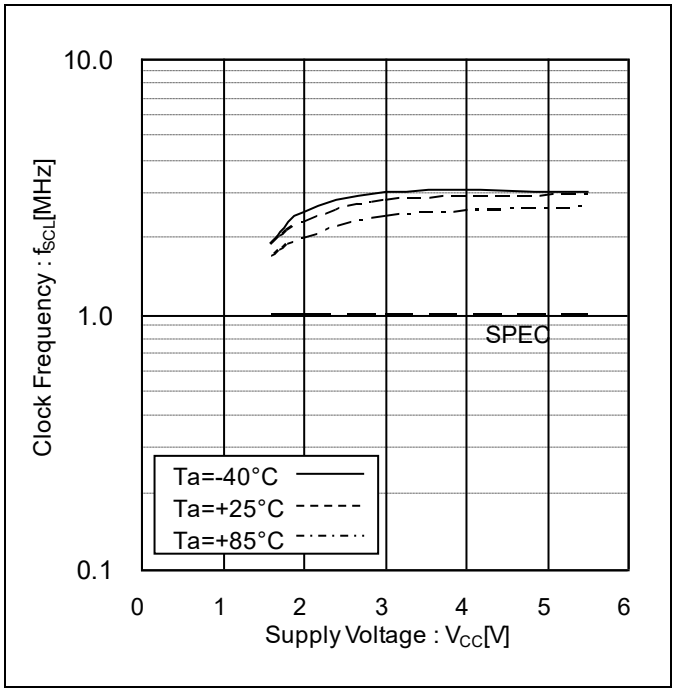


Figure 16. Clock Frequency vs Supply Voltage

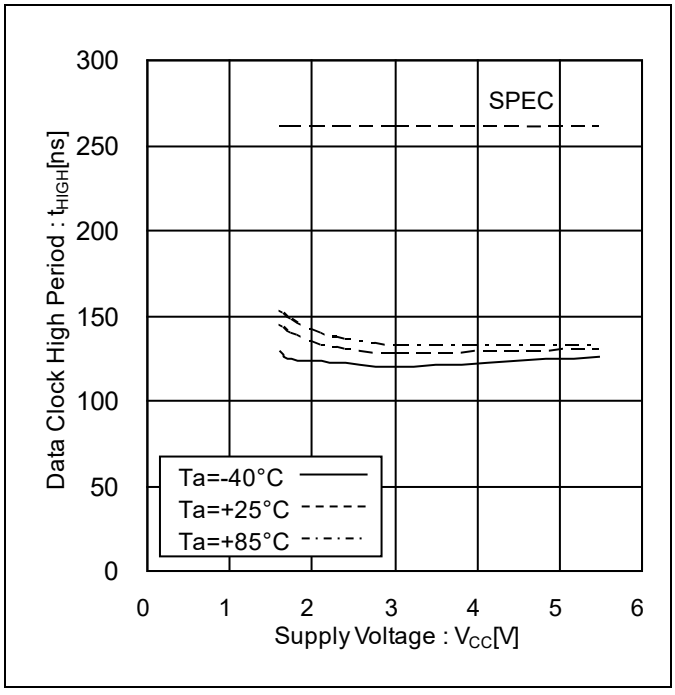


Figure 17. Data Clock High Period vs Supply Voltage

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Typical Performance Curves - continued

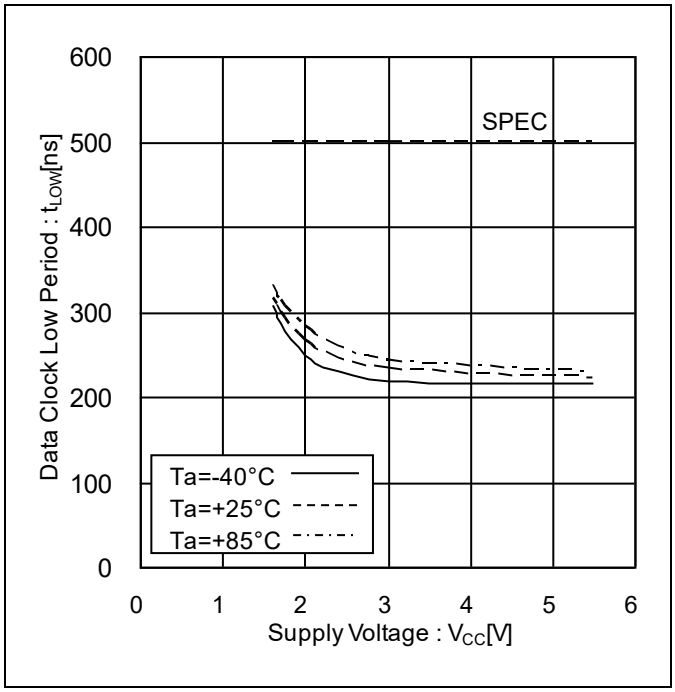


Figure 18. Data Clock Low Period vs Supply Voltage

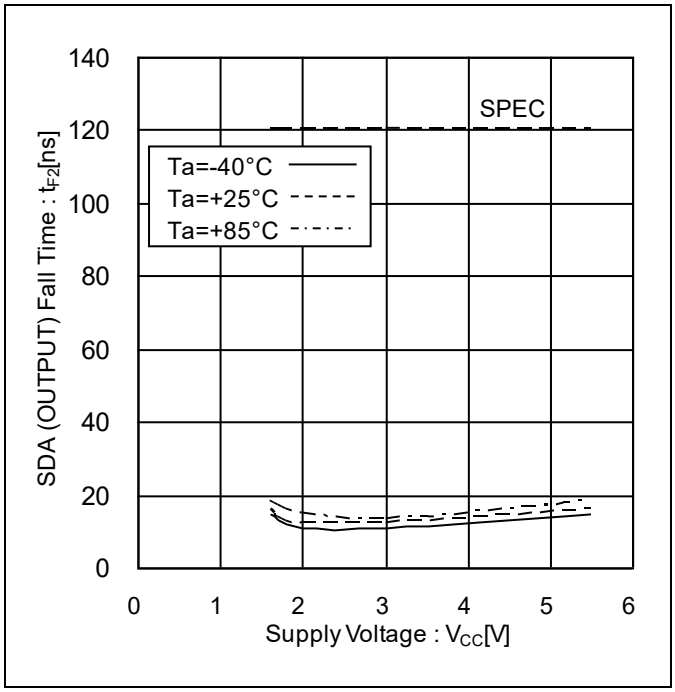


Figure 19. SDA (OUTPUT) Fall Time vs Supply Voltage

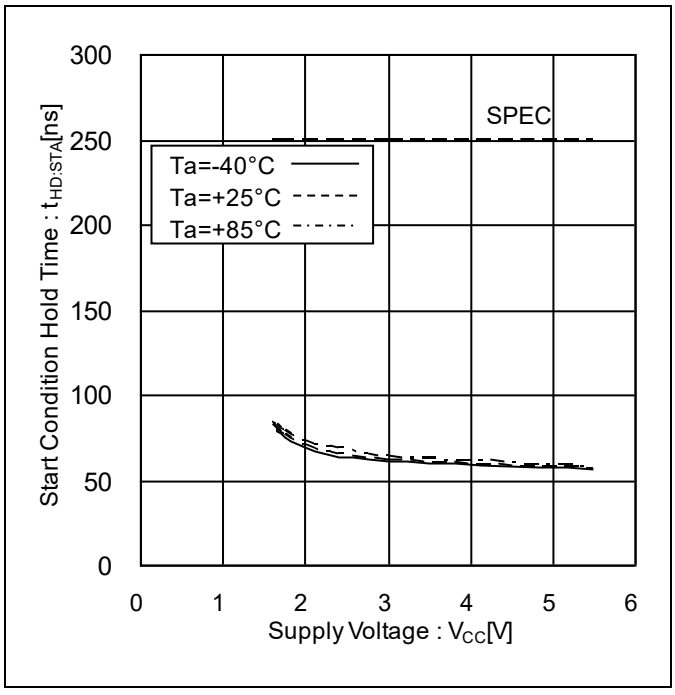


Figure 20. Start Condition Hold Time vs Supply Voltage

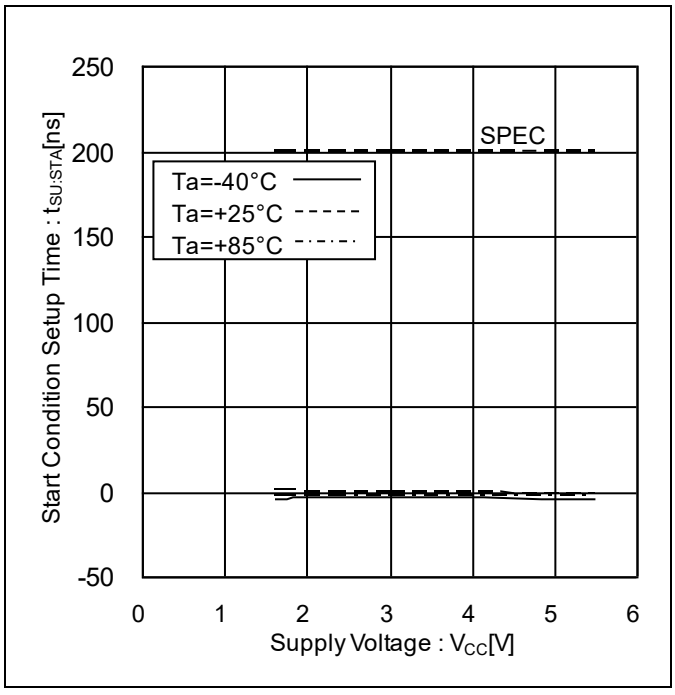


Figure 21. Start Condition Setup Time vs Supply Voltage

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Typical Performance Curves - continued

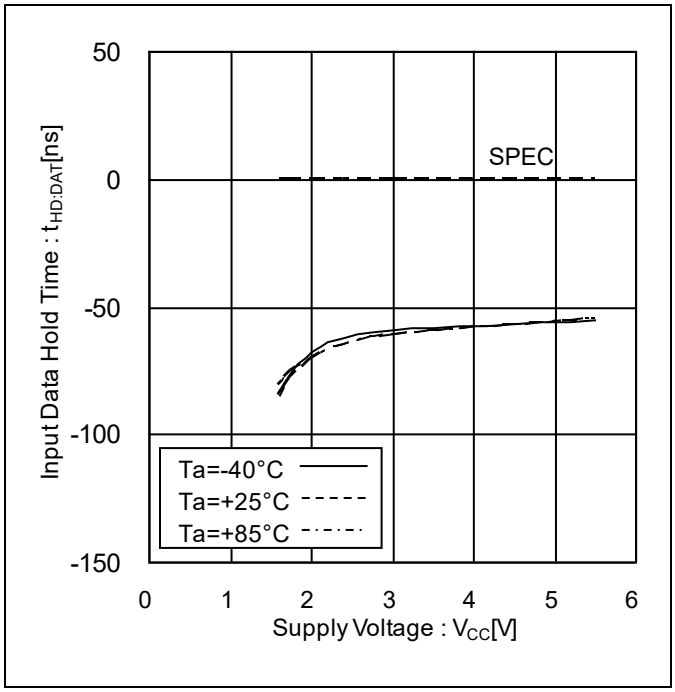


Figure 22. Input Data Hold Time vs Supply Voltage
(SDA 'LOW' to 'HIGH')

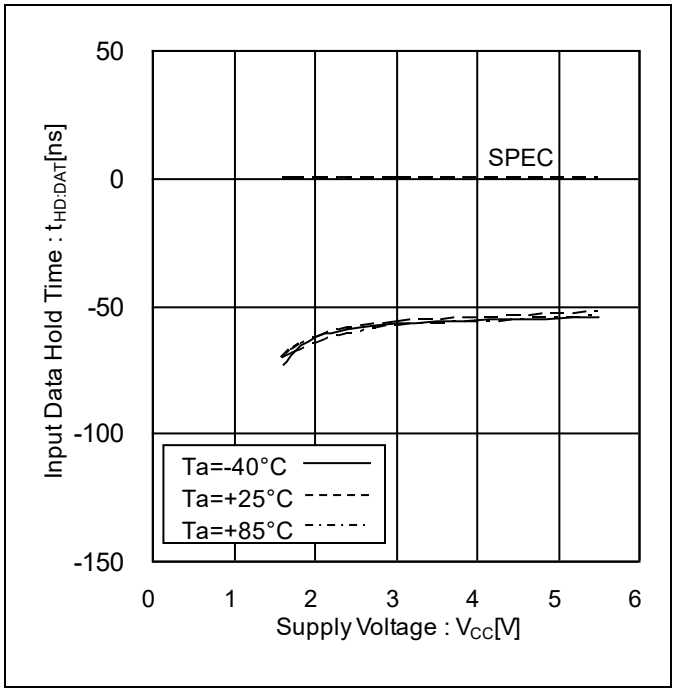


Figure 23. Input Data Hold Time vs Supply Voltage
(SDA 'HIGH' to 'LOW')

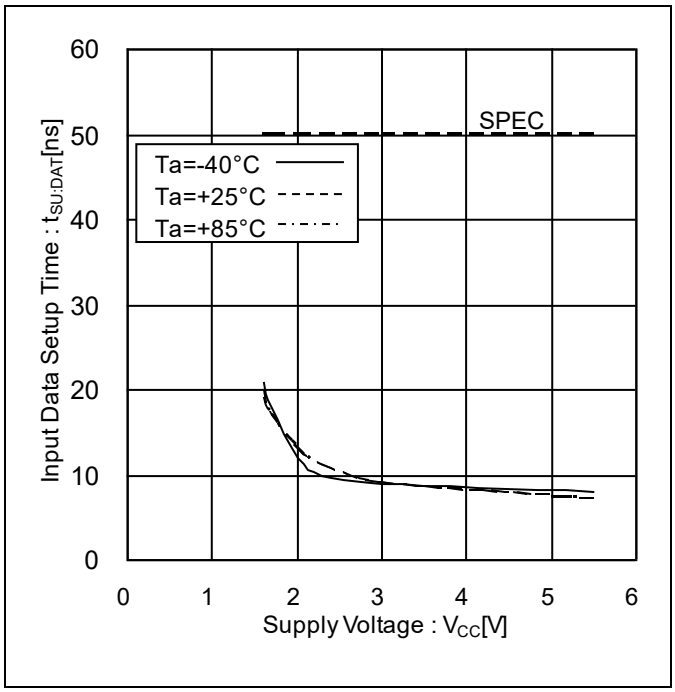


Figure 24. Input Data Setup Time vs Supply Voltage
(SDA 'LOW' to 'HIGH')

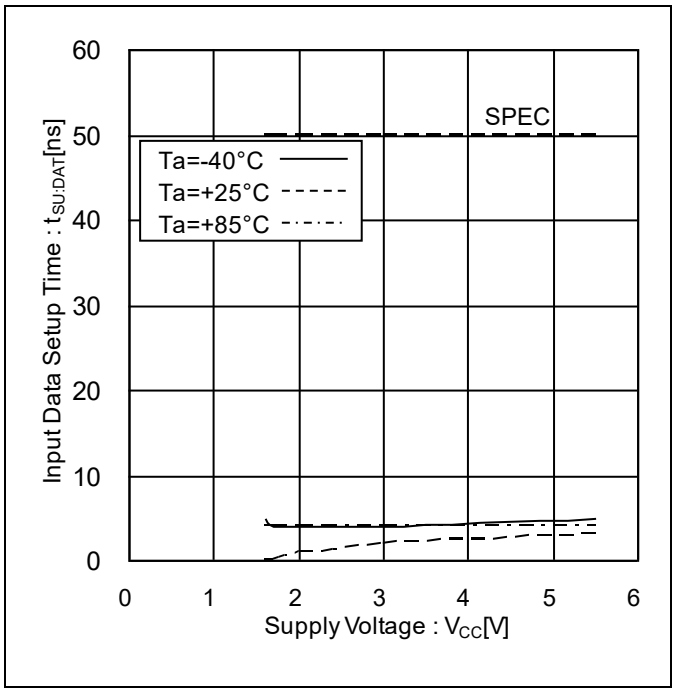


Figure 25. Input Data Setup Time vs Supply Voltage
(SDA 'HIGH' to 'LOW')

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Typical Performance Curves - continued

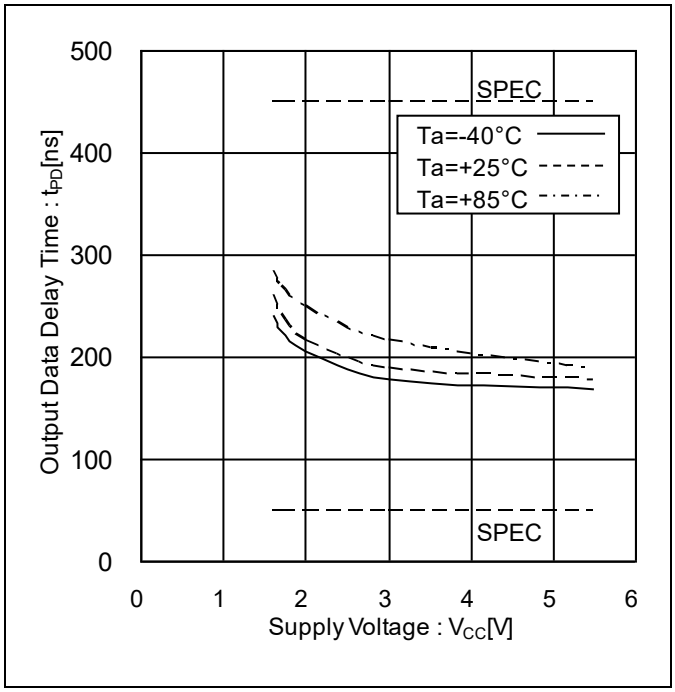


Figure 26. Output Data Delay Time vs Supply Voltage
(SDA 'LOW' to 'HIGH')

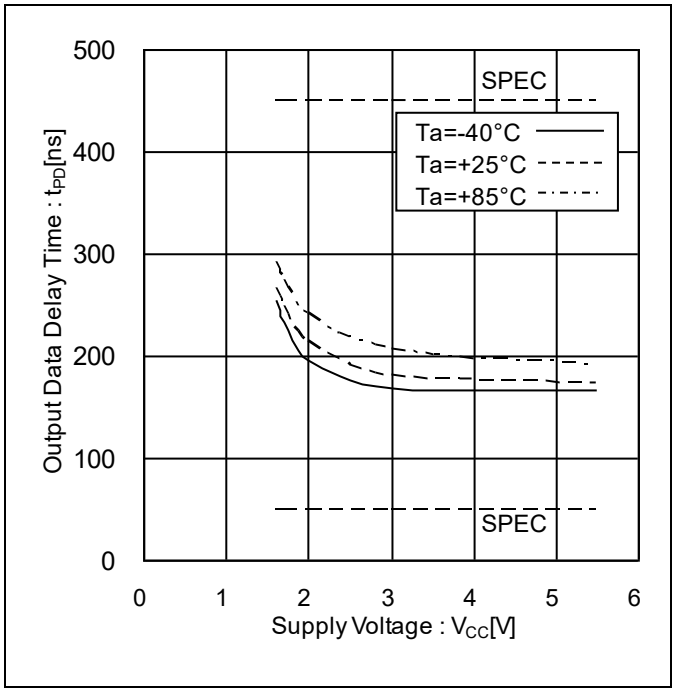


Figure 27. Output Data Delay Time vs Supply Voltage
(SDA 'HIGH' to 'LOW')

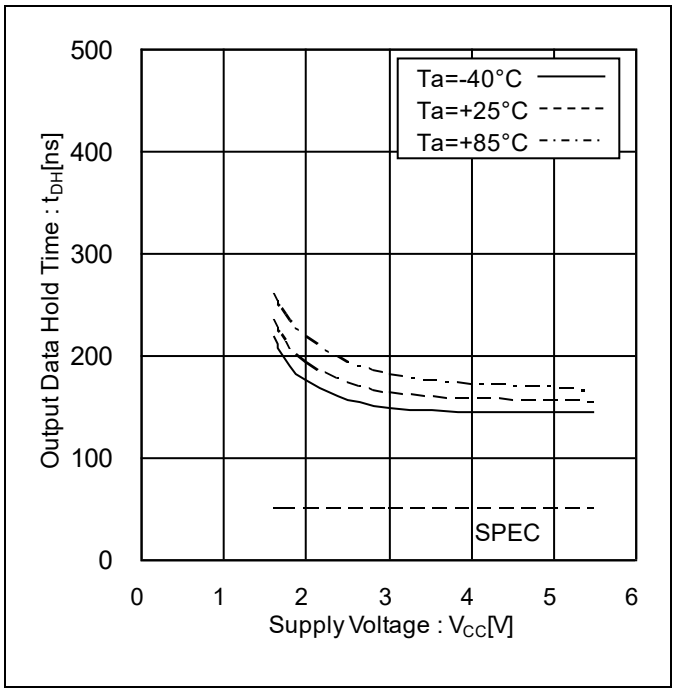


Figure 28. Output Data Hold Time vs Supply Voltage
(SDA 'LOW' to 'HIGH')

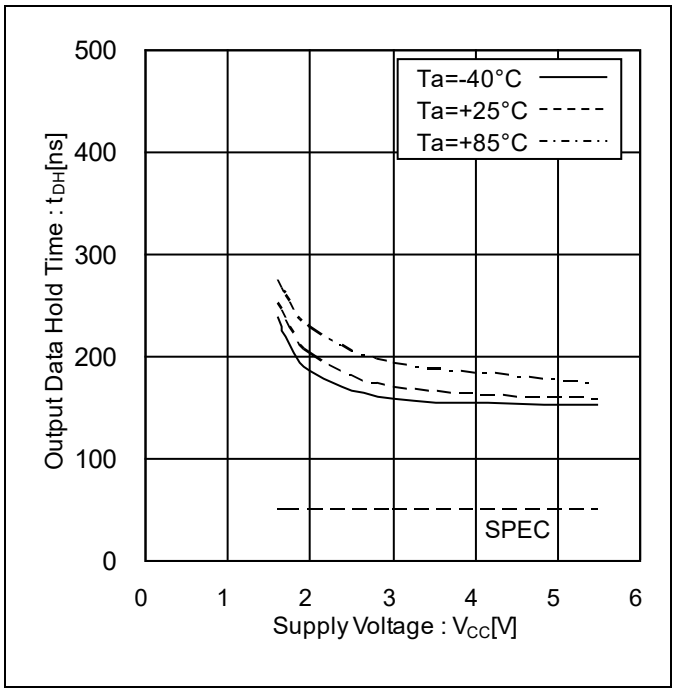


Figure 29. Output Data Hold Time vs Supply Voltage
(SDA 'HIGH' to 'LOW')

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Typical Performance Curves - continued

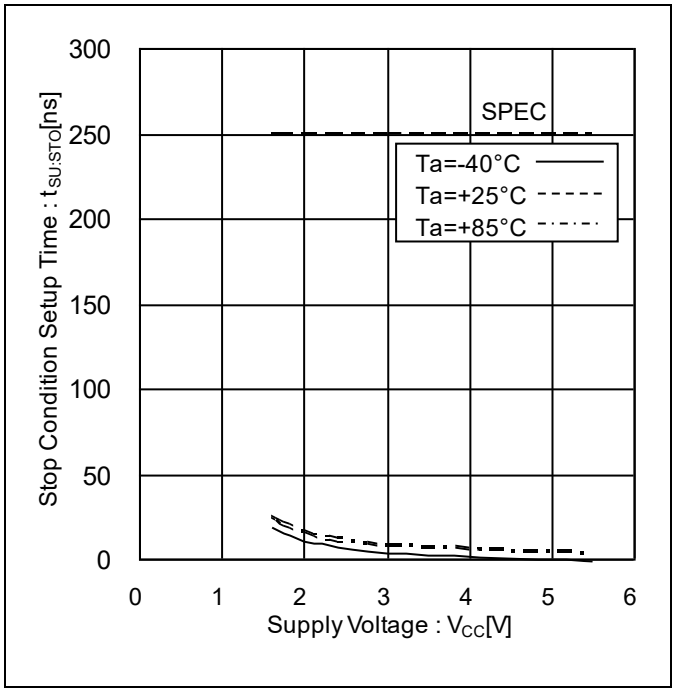


Figure 30. Stop Condition Setup Time vs Supply Voltage

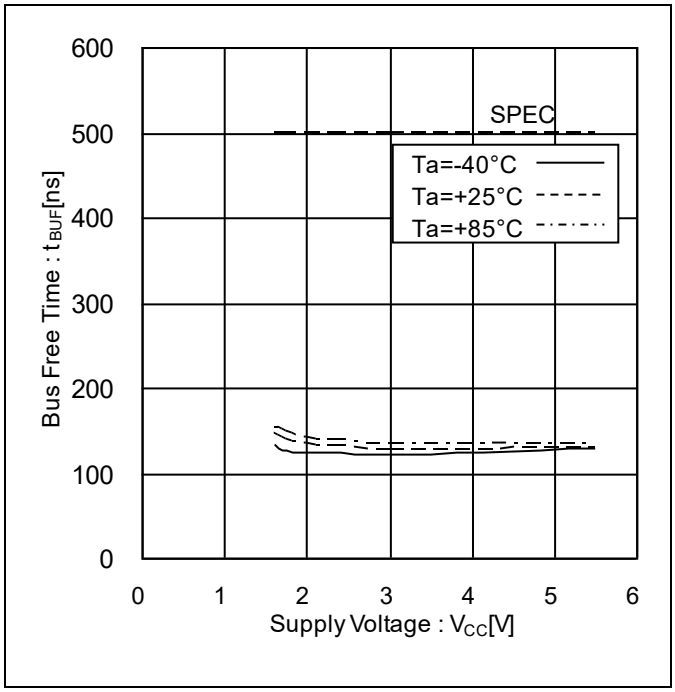


Figure 31. Bus Free Time vs Supply Voltage

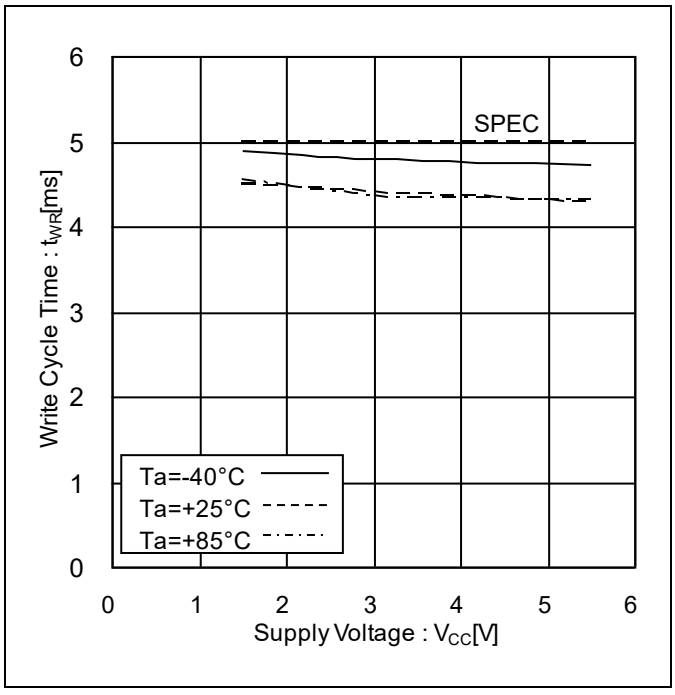


Figure 32. Write Cycle Time vs Supply Voltage

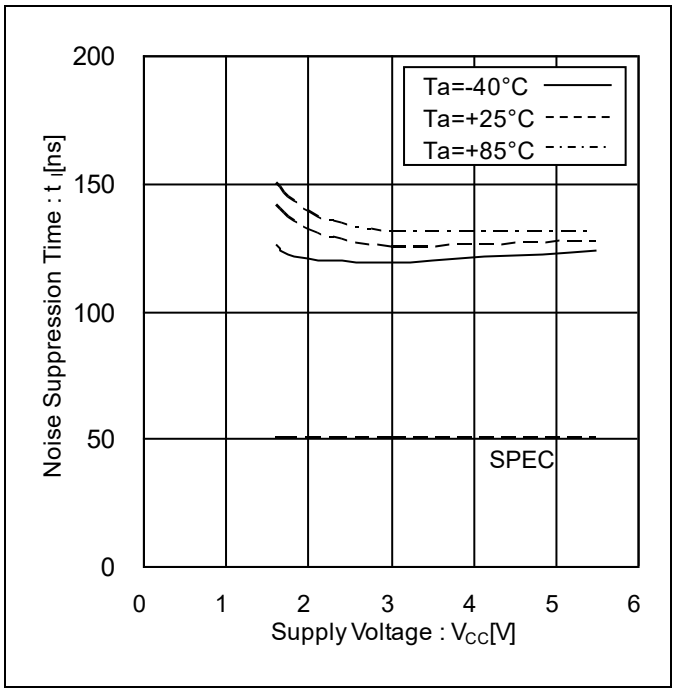


Figure 33. Noise Suppression Time vs Supply Voltage (SCL 'HIGH')

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Typical Performance Curves - continued

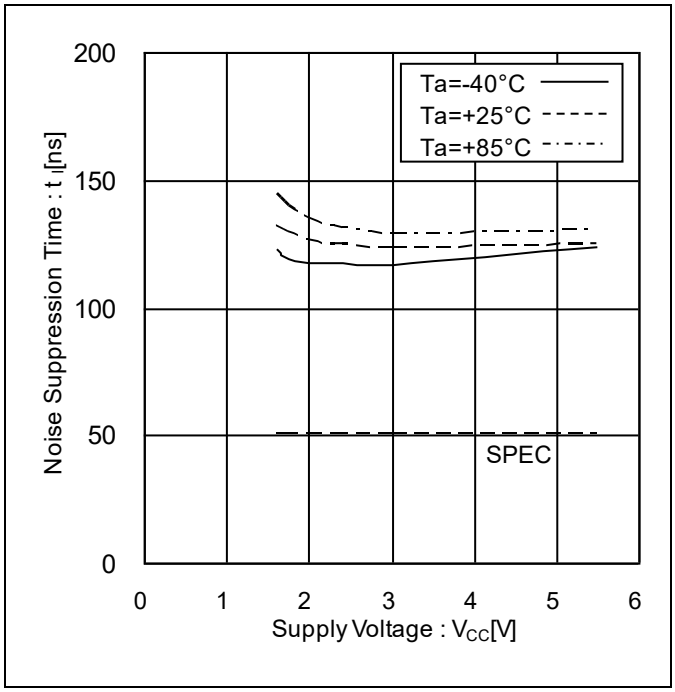


Figure 34. Noise Suppression Time vs Supply Voltage (SCL 'LOW')

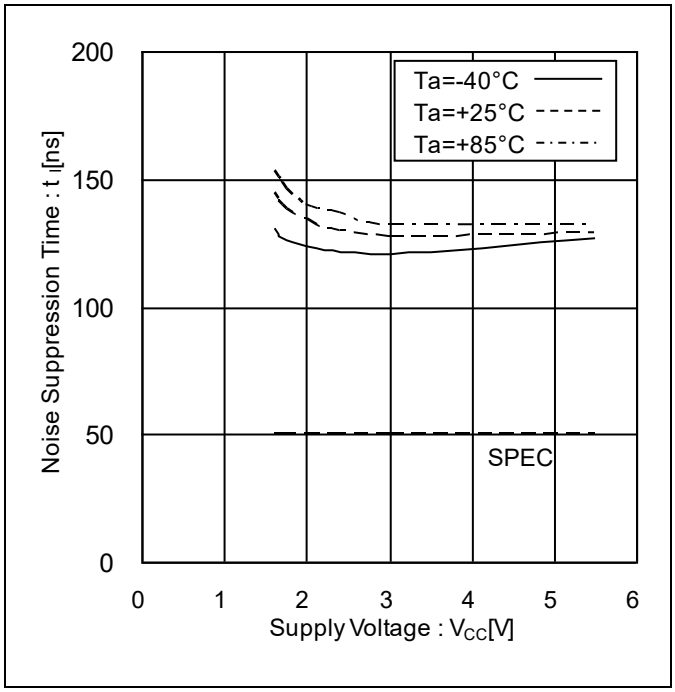


Figure 35. Noise Suppression Time vs Supply Voltage (SDA 'HIGH')

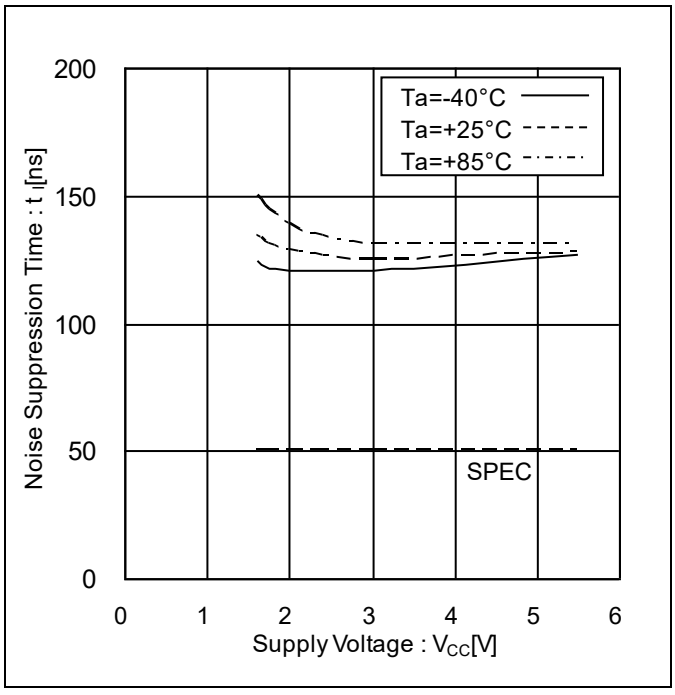


Figure 36. Noise Suppression Time vs Supply Voltage (SDA 'LOW')

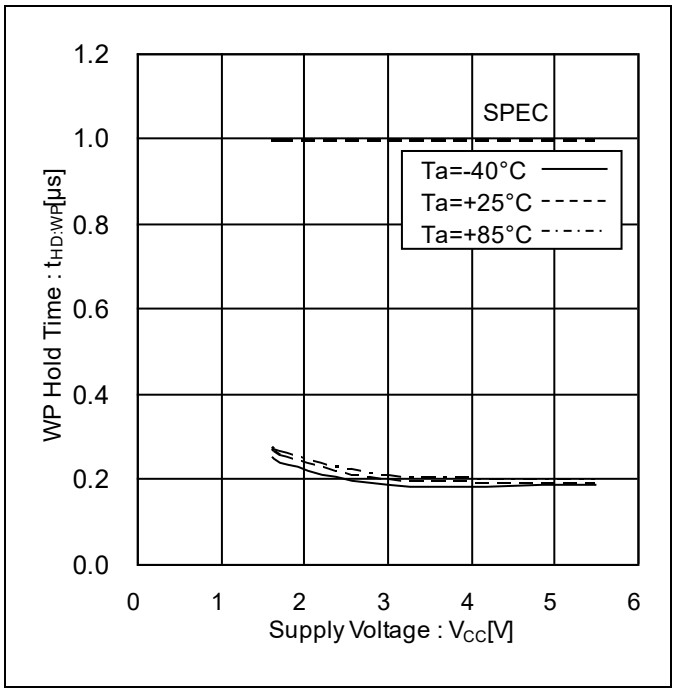


Figure 37. WP Hold Time vs Supply Voltage

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Typical Performance Curves - continued

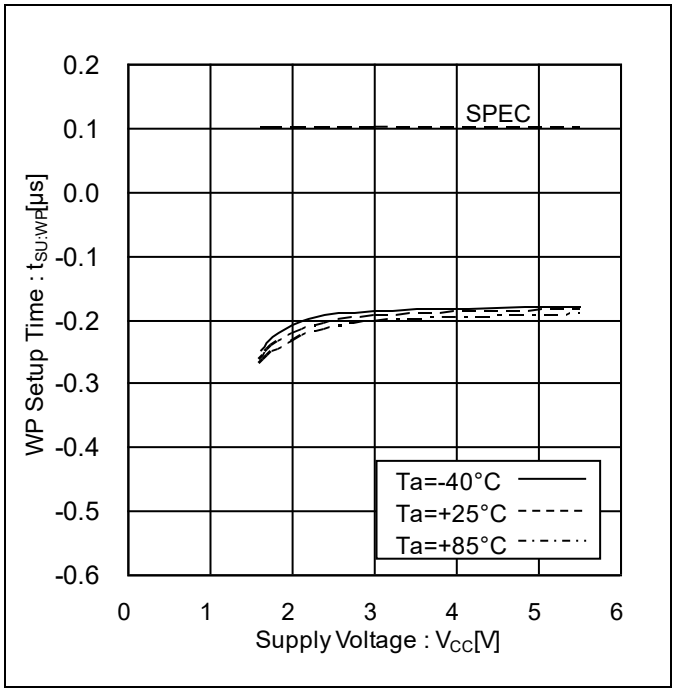


Figure 38. WP Setup Time vs Supply Voltage

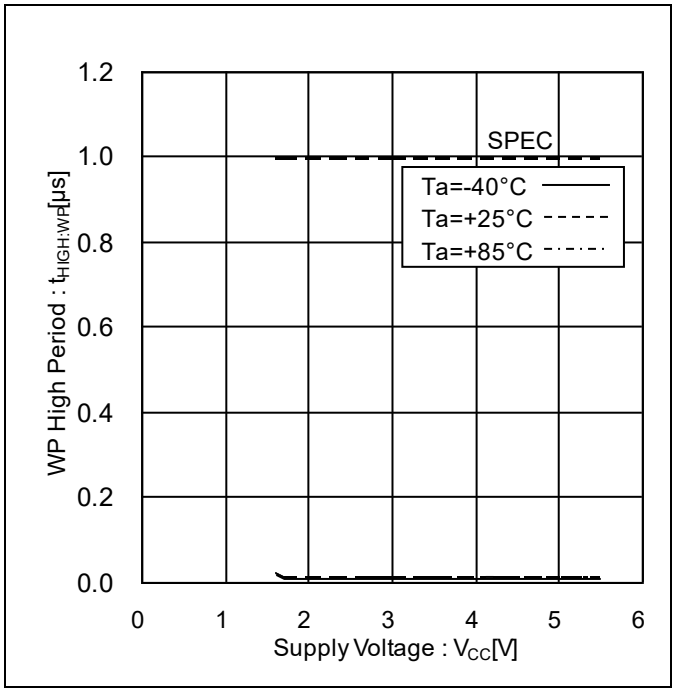


Figure 39. WP High Period vs Supply Voltage

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I²C BUS Communication

1. I²C BUS Data Communication

(1) I²C BUS data communication begins with start condition input, and ends at the stop condition input.
(2) The data is always 8bit long, and acknowledge is always required after each byte.
(3) I²C BUS data communication with several devices connected to the BUS is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).
(4) Among the devices, there is a “master” that generates clock and control communication start and end. The rest become “slave” which are controlled by an address peculiar to each device. EEPROM is a “slave”.
(5) The device that outputs data to the bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

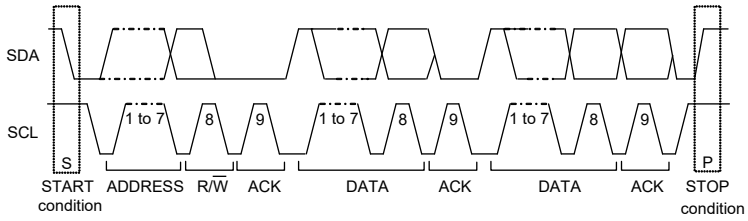


Figure 40. Data Transfer Timing

2. Start Condition (Start Bit Recognition)

(1) Before executing each command, start condition (start bit) where SDA goes down from ‘HIGH’ to ‘LOW’ while SCL is ‘HIGH’ is necessary.
(2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

Each command can be ended by a stop condition (stop bit) where SDA goes from ‘LOW’ to ‘HIGH’ while SCL is ‘HIGH’.

4. Acknowledge (ACK) Signal

(1) This acknowledge (ACK) signal is a software rule to indicate whether or not data transfer was performed normally. In both master and slave communication, the device at the transmitter (sending) side releases the bus after outputting 8-bit data. When a slave address of a write command or a read command is input, microcontroller is the device at the transmitter side. When data output for a read command, this IC is the device at the transmitter side.
(2) The device on the receiver (receiving) side sets SDA ‘LOW’ during the 9th clock cycle, and outputs an ACK signal showing that the 8-bit data has been received. When a slave address of a write command or a read command is input, this IC is the device at the receiver side. When data output for a read command, microcontroller is the device at the receiver side.
(3) This IC, after recognizing start condition and slave address (8bit), outputs ACK signal ‘LOW’.
(4) Each write operation outputs ACK signal ‘LOW’ every 8bit data (a word address and write data) reception.
(5) During read operation, this IC outputs 8bit data (read data) and detects the ACK signal ‘LOW’. When ACK signal is detected, and no stop condition is sent from the master (microcontroller) side, this IC will continue to output data. If the ACK signal is not detected, this IC stops data transfer, recognizes the stop condition (stop bit), and ends the read operation. Then this IC becomes ready for another transmission.

5. Device Addressing

(1) From the master, input the slave address after the start condition.
(2) The significant 4 bits of slave address are used for recognizing a device type.
The device code of this IC is fixed to ‘1010’.
(3) The next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and multiple devices can be used on a same bus according to the number of device addresses. It is possible to select and operate only device whose ‘VCC’ ‘GND’ input conditions of the A0, A1, A2 pin match the ‘HIGH’ ‘LOW’ input conditions of slave address sent from the master.
(4) The least significant bit ($R/\overline{W}$ --- READ/ $\overline{\text{WRITE}}$) of slave address is used for designating write or read operation, and is as shown below.

Setting $R/\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting $R/\overline{W}$ to 1 ------- read

Slave address								Maximum number of Connected buses
1	0	1	0	A2	A1	A0	$R/\overline{W}$	8

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Write Command

1. Write

(1) Arbitrary data can be written to EEPROM. When writing only 1 byte, Byte Write is normally used, and when writing continuous data of 2 bytes or more, simultaneous write is possible by Page Write. Up to 64 arbitrary bytes can be written.

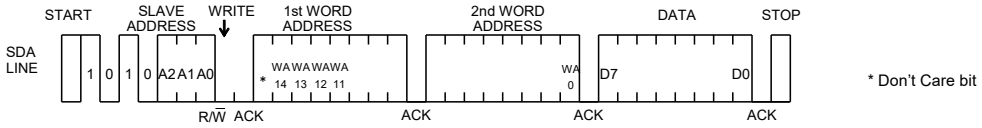


Figure 41. Byte Write

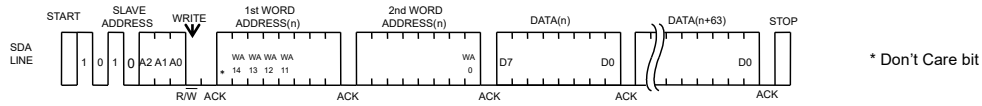


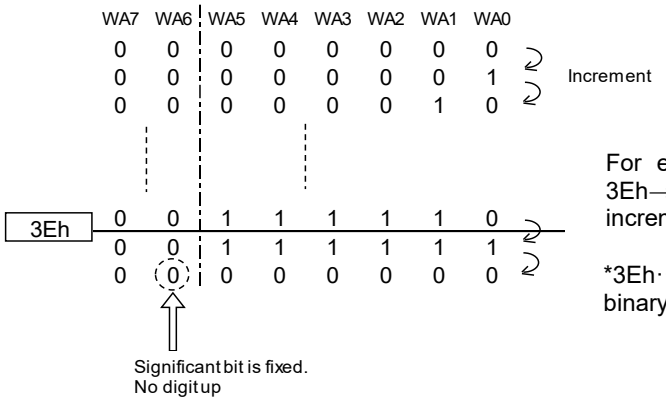
Figure 42. Page Write

(2) During internal write execution, all input commands are ignored, therefore ACK is not returned.
(3) Data is written to the address designated by word address (n-th address)
(4) By issuing stop bit after 8bit data input, internal write to memory cell starts.
(5) When internal write is started, command is not accepted for t_{WR} (5ms at maximum).
(6) Using page write, it is possible to write one lump sum up to 64 bytes. When data of more than 64 bytes is sent, the excess of the bytes is overwritten the data sent already from first byte. (Refer to "Internal Address Increment").
(7) As for page write where 2 or more bytes of data is intended to be written, after the word address are designated arbitrarily, only the value of 6 least significant bits in the address is incremented internally, so that data up to 64 bytes of memory only can be written.
(8) When V_{CC} is turned off during t_{WR}, data at the designated address is not guaranteed, please write it again.

1 page=64bytes, but the write time of page write is 5ms at maximum for 64byte batch write.
It is not equal to 5ms at maximum x 64byte=320ms(Max).

2. Internal Address Increment

Page write mode



For example, when starting from address 3Eh, then, 3Eh→3Fh→00h→01h⋯. Please take note that it will be incremented.

*3Eh⋯3E in hexadecimal, therefore, 00111110 becomes a binary number.

3. Write Protect (WP) Function

When WP pin is set at V_{CC} ('HIGH' level), data rewrite of all addresses is prohibited. When it is set GND ('LOW' level), data rewrite of all address is enabled. Be sure to connect this pin to VCC or GND, or control it to 'HIGH' level or 'LOW' level. If WP pin is open, this input is recognized as 'LOW'.
In case of using it as ROM, by connect it to pull-up or VCC, write error can be prevented.
At extremely low voltage at power ON/OFF, by setting the WP pin 'HIGH', write error can be prevented.

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4. ECC Function

This IC has ECC bits for Error Correction every 4 bytes with the same address bits of WA14 to WA2. In read operation, if 1 bit of error data exists in 4 bytes, this error data will be corrected by the ECC function and outputs the correct data. In write operation, only 1 byte of data is to be written, 4 bytes of data will be written as one group with the same address bits of WA14 to WA2 (the data to be written in the remaining 3 bytes will be the same as its previous stored data). Therefore, the number of write cycle times is guaranteed every 4 bytes with the same address bits of WA14 to WA2.

Initial Delivery State

Address	0000h	0001h	0002h	0003h	0004h	0005h	…
Number of remaining write cycles	4 Million Times	4 Million Times	4 Million Times	4 Million Times	4 Million Times	4 Million Times	…

After 1 Million Times using Byte Write in Address 0000h

Address	0000h	0001h	0002h	0003h	0004h	0005h	…
Number of remaining write cycles	3 Million Times	3 Million Times	3 Million Times	3 Million Times	4 Million Times	4 Million Times	…

Even if only 1 byte of data is to be written in address 0000h, the addresses 0000h to 0003h are written as one group. Therefore, the number of write cycle times at addresses 0001h to 0003h decreases.

Figure 43. Example of data write and number of remaining write cycles

Read Command

Read the EEPROM data. Read has a random read and a current read functions. Random read is commonly used in commands that specify addresses and read data. The current read is a command to read data of the internal address register without specifying an address. In both read functions, sequential read is possible where the next address data can be read in succession.

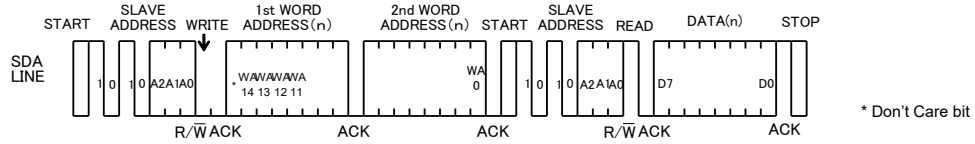


Figure 44. Random Read

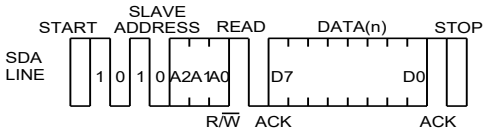


Figure 45. Current Read

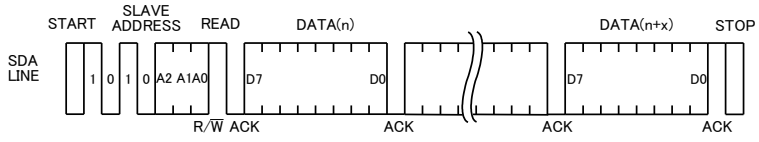


Figure 46. Sequential Read (in the Case of Current Read)

(1) In random read, data of designated word address can be read.
(2) When the command just before current read is random read or current read (each including sequential read), if last read address is (n)-th, data of the incremented address (n+1)-th is outputted.
(3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (microcontroller) side, the next address data can be read in succession.
(4) Read is ended by stop condition where 'HIGH' is input to ACK signal after D0 and SDA signal goes from 'LOW' to 'HIGH' while at SCL signal is 'HIGH'.
(5) When 'LOW' is input at ACK signal after D0 without 'HIGH' input, sequential read gets in, and the next data is outputted. Therefore, read command cannot be ended. To end read command, be sure to input 'HIGH' to ACK signal after D0, and the stop condition where SDA goes from 'LOW' to 'HIGH' while SCL signal is 'HIGH'.
(6) Sequential read is ended by stop condition where 'HIGH' is input to ACK signal after arbitrary D0 and SDA goes from 'LOW' to 'HIGH' while SCL signal is 'HIGH'.

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Method of Reset

This IC can be reset by sending the stop condition after executing the start condition. Please execute it when it is necessary to reset after power-up, or during command input timing. However, the start condition and stop condition could not be applied because 'HIGH' input of microcontroller and 'LOW' output of EEPROM collide when EEPROM is 'LOW' in ACK output section and data reading. In that case, input SCL clock until SDA bus is released ('HIGH' by pull-up). After confirming that SDA is released, send the stop condition after inputting the start condition. If SDA bus could not be confirmed whether released or not in microcontroller, input the software reset. If software reset is run, EEPROM can be reset without confirming the SDA state because SDA bus is always released in either of the two start conditions. The method of reset is shown in the table below.

Status of SDA	Method of reset
SDA bus released ('HIGH' by pull-up)	Send the stop condition after executing the start condition.
'LOW'	Input SCL clock until SDA bus is released, confirm that SDA bus is released, and send the stop condition after inputting start condition.
Microcontroller cannot confirm SDA bus is released or not	Using the software reset shown in the figure below, the start condition can be always excuted. Within the dummy clock input area, the SDA bus is needed to be released ('HIGH' by pull-up). For normal commands, start with the start condition input.

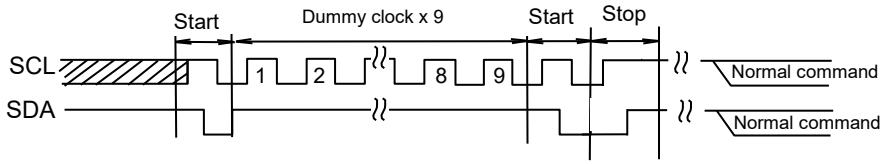


Figure 47. Input timing of software reset

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write input, next command (slave address) is sent. If the first ACK signal sends back 'LOW', then it means end of write operation, else 'HIGH' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for t_{WR} = 5ms.

To write continuously, slave address with R / $\overline{W}$ = 0, then to carry out current read after write, slave address with R / $\overline{W}$ = 1 is sent. If ACK signal sends back 'LOW', then execute word address input and data output and so forth.

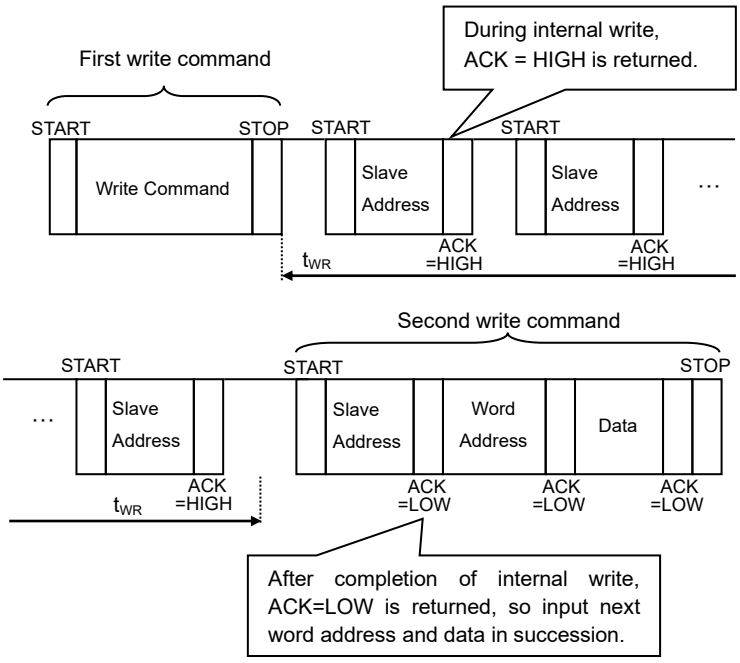


Figure 48. The Case of Continuous Write by Acknowledge Polling

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WP Valid Timing (Write Cancel)

WP is usually fixed to 'HIGH' or 'LOW', but when WP is controlled and used for write cancel and so on, pay attention to the following WP valid timing. Write can be cancelled by setting WP='HIGH' while it is executed and in WP valid area. In both byte write and page write, the area from the first start condition of command to the rise of clock which take in D0 of data(in page write, the first byte data) is the WP invalid area. WP input in this area becomes 'Don't care'. The area from the rise of clock to take in D0 to the stop condition input is the WP valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status.

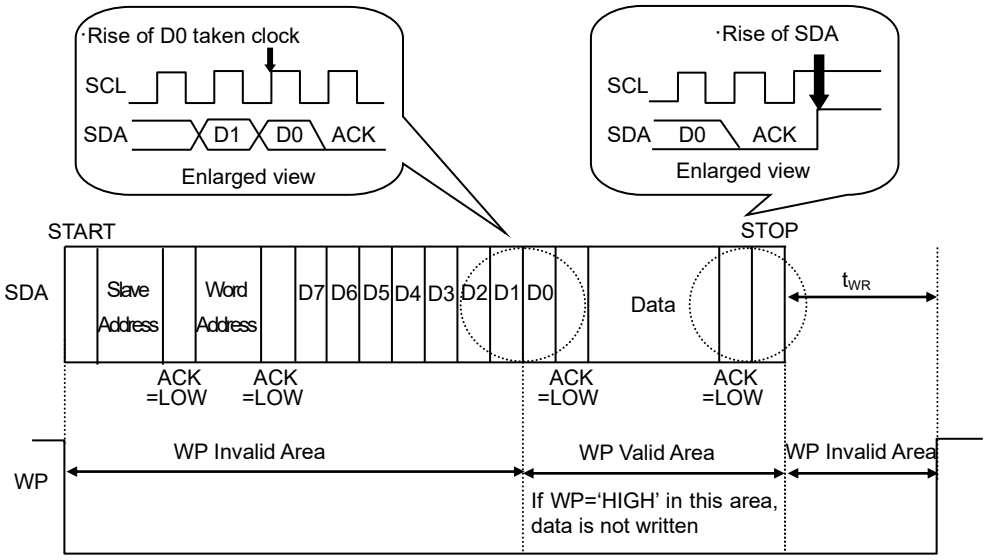


Figure 49. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. However, within ACK output area and during data read, SDA bus may output 'LOW'. In this case, start condition and stop condition cannot be inputted, so reset is not available. Therefore, execution of reset is needed referring "Method of Reset". When command is cancelled by start-stop condition during random read, sequential read, or current read, internal setting address is not determined. Therefore, it is not possible to carry out current read in succession. To carry out read in succession, carry out random read.

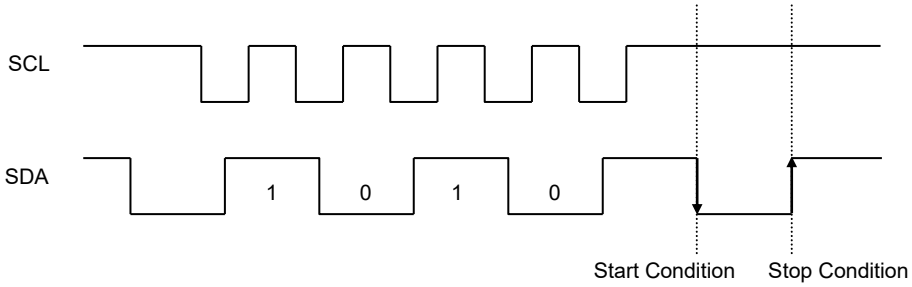


Figure 50. The Case of Cancel by Start, Stop Condition during Slave Address Input

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Application Examples

1. I/O Peripheral Circuit

(1) Pull-up Resistance of SDA Pin

SDA is NMOS open drain, so it requires a pull-up resistor. As for this resistor value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU} increases the supply current.

(2) Maximum Value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(a) SDA rise time determined by the capacitance (C_{BUS}) of bus line of SDA and R_{PU} should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(b) The bus electric potential Ⓐ to be determined by input current leak total (I_L) of the device connected to bus at output of 'HIGH' to SDA line and R_{PU} should sufficiently secure the input 'HIGH' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of $0.2V_{CC}$.

$$V_{CC} - I_L R_{PU} - 0.2V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.) V_{CC}=3V I_L=10μA V_{IH}=0.7V_{CC} from (b)

$$\therefore R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 30 \text{ [kΩ]}$$

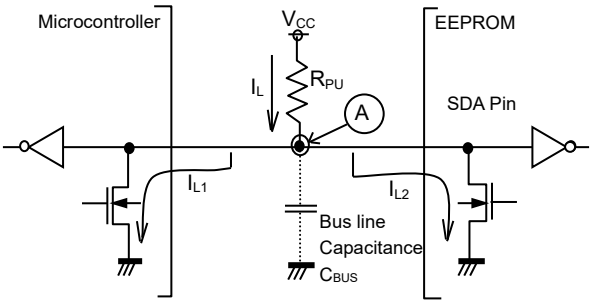


Figure 51. I/O Circuit Diagram

(3) Minimum Value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(a) When IC outputs 'LOW', the bus electric potential Ⓐ should be equal to or less than output 'LOW' level (V_{OL}) of EEPROM.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

Ex.) V_{CC}=3V, V_{OL}=0.4V, I_{OL}=3.2mA, microcontroller, EEPROM V_{IL}=0.3V_{CC}

$$\therefore R_{PU} \geq \frac{3 - 0.4}{3.2 \times 10^{-3}}$$

$$\geq 812.5 \text{ [Ω]}$$

(4) Pull-up Resistance of SCL Pin

When SCL control is made at the CMOS output port, there is no need for a pull-up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull-up resistor. As for the pull-up resistor value, decide with the balance with drive performance of output port of microcontroller.

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2. Cautions on Microcontroller Connection

(1) R_S

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input/output of tri state to SDA port, insert a series resistance R_S between the pull-up resistor R_{PU} and the SDA pin of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA pin against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.

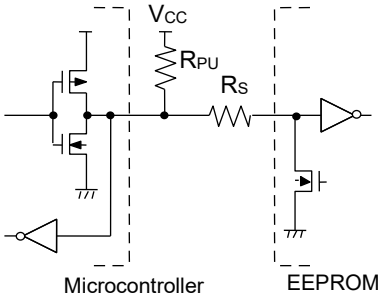


Figure 52. I/O Circuit Diagram

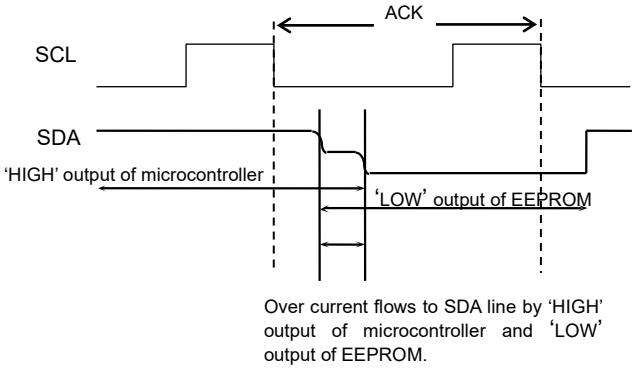


Figure 53. I/O Collision Timing

(2) Maximum Value of R_S

The maximum value of R_S is determined by the following relations.

(a) SDA rise time determined by the capacitance (C_{BUS}) of bus line of SDA and R_{PU} should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(b) The bus electric potential Ⓐ to be determined by R_{PU} and R_S when EEPROM outputs 'LOW' to SDA bus should sufficiently secure the input 'LOW' level (V_{IL}) of microcontroller including recommended noise margin of $0.1V_{CC}$.

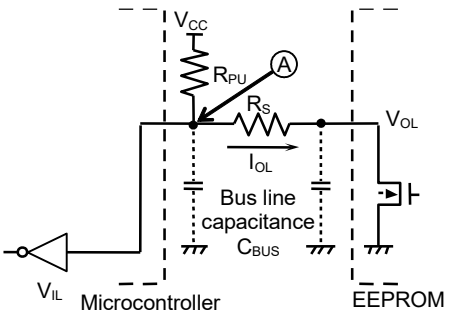


Figure 54. I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S}+V_{OL}+0.1V_{CC}\le V_{IL}$$

$$\therefore R_S \le \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}}\times R_{PU}$$

Ex.) V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \le \frac{0.3\times 3-0.4-0.1\times 3}{1.1\times 3-0.3\times 3}\times 20\times 10^3$$

$$\le 1.67\ [\mathrm{k\Omega}]$$

(3) Minimum Value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth.

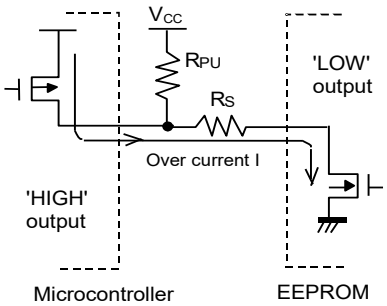


Figure 55. I/O Circuit Diagram

$$\frac{V_{CC}}{R_S}\le I$$

$$\therefore Rs \ge \frac{V_{CC}}{I}$$

Ex.) V_{CC}=3V I=10mA

$$Rs \ge \frac{3}{10\times 10^{-3}}$$

$$\ge 300\ [\Omega]$$

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Caution on Power-Up Conditions

At power-up, as the V_{CC} rises, the IC's internal circuits may go through unstable low voltage area, making the IC's internal circuit not completely reset, hence, malfunction like miswriting and misread may occur. To prevent it, this IC is equipped with Power-on Reset circuit. In order to ensure its operation, at power-up, please observe the conditions below. In addition, set the power supply rise so that the supply voltage constantly increases from Vbot to V_{CC} level. Furthermore, t_{INIT} is the time from the power become stable to the start of the first command input.

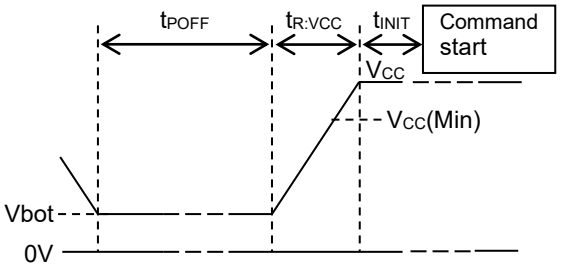


Figure 56. Rise Waveform Diagram

Power-Up Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage at Power OFF	Vbot	-	-	0.3	V
Power OFF Time*(Note 20)*	t_{POFF}	1	-	-	ms
Initialize Time*(Note 20)*	t_{INIT}	0.1	-	-	ms
Supply Voltage Rising Time*(Note 20)*	$t_{R:VCC}$	0.001	-	100	ms

(Note 20) Not 100% TESTED

If the above conditions are not followed, the POR circuit will not operate properly, the logic circuit of internal IC becomes undefined. At this time, there is a possibility that IC may not be able to input commands because EEPROM may output 'LOW' and it collide with 'HIGH' input of microcontroller. However, SDA bus can be released by resetting the IC. Refer to the page "Method of Reset" for reset details.

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

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I/O Equivalence Circuits

1. Input (A0, A1, A2, WP)

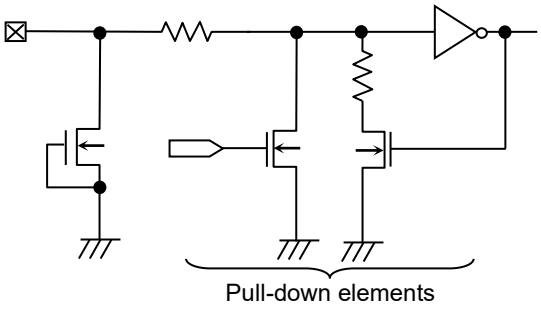


Figure 57. Input Pin Circuit Diagram (A0, A1, A2, WP)

2. Input (SCL)

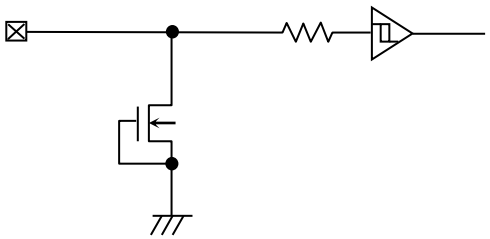


Figure 58. Input Pin Circuit Diagram (SCL)

3. Input / Output (SDA)

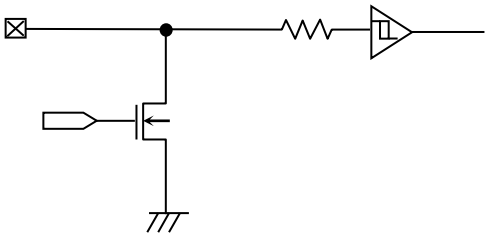


Figure 59. Input / Output Pin Circuit Diagram (SDA)

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

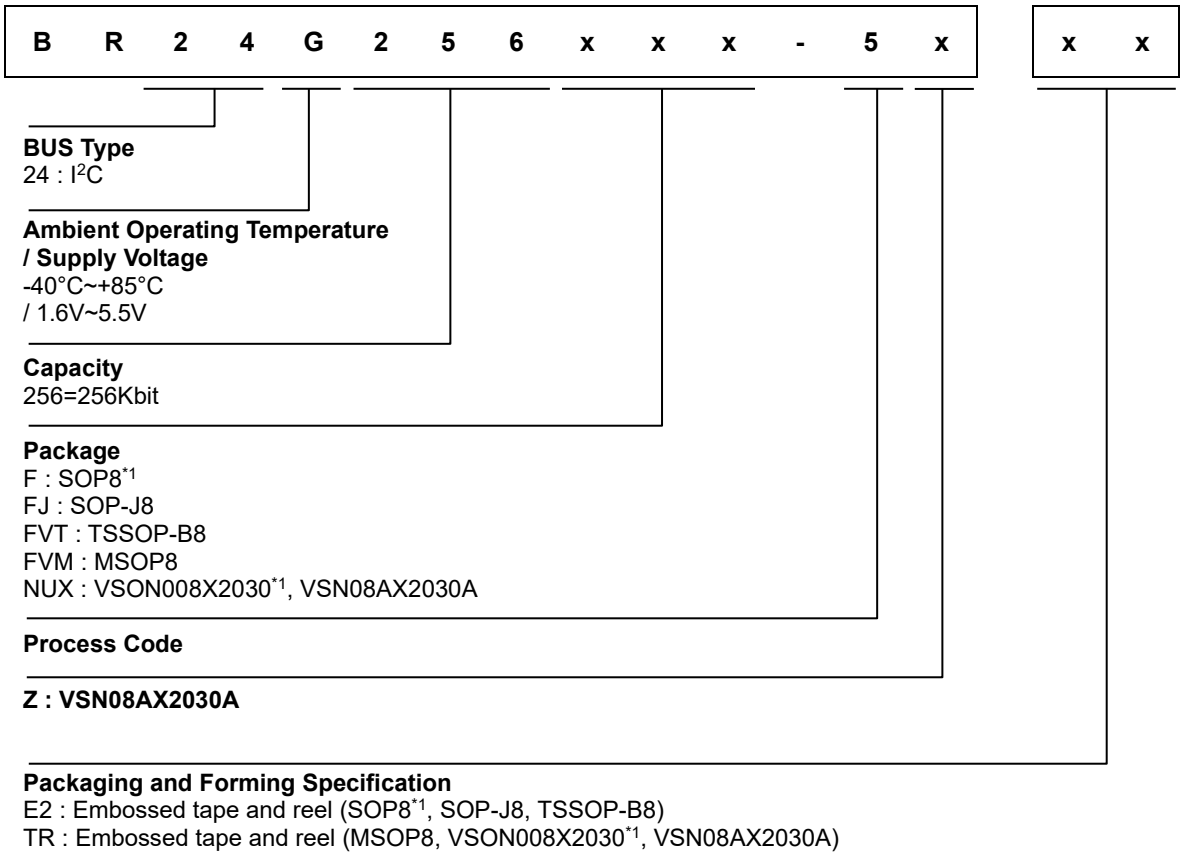
11. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

12. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Ordering Information



*1 Last Time Buy.

Lineup

Package		Orderable Part Number	
Type	Quantity		
SOP8*1	Reel of 2500	BR24G256F	-5E2
SOP-J8	Reel of 2500	BR24G256FJ	-5E2
TSSOP-B8	Reel of 3000	BR24G256FVT	-5E2
MSOP8	Reel of 3000	BR24G256FVM	-5TR
VSON008X2030*1	Reel of 4000	BR24G256NUX	-5TR
VSN08AX2030A	Reel of 4000	BR24G256NUX	-5ZTR

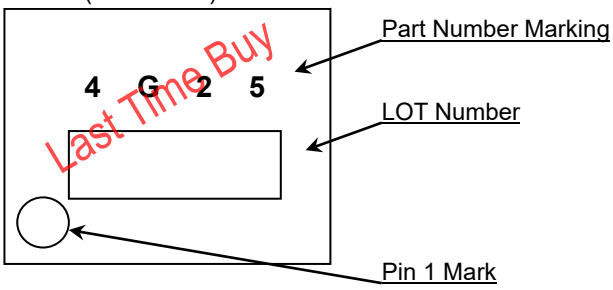
*1 Last Time Buy.

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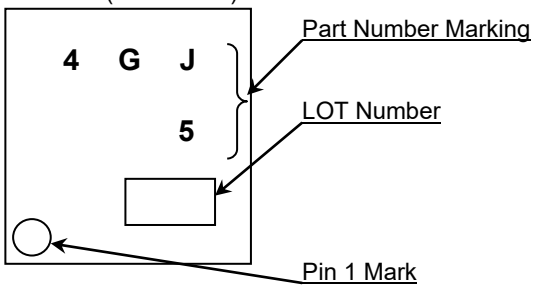
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Marking Diagrams

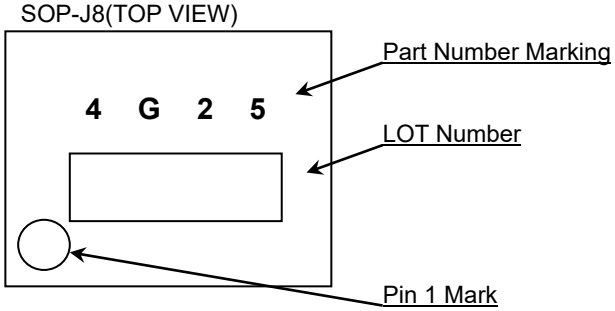
SOP8(TOP VIEW)



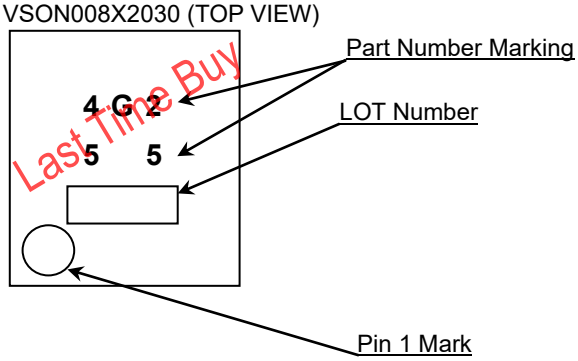
MSOP8(TOP VIEW)



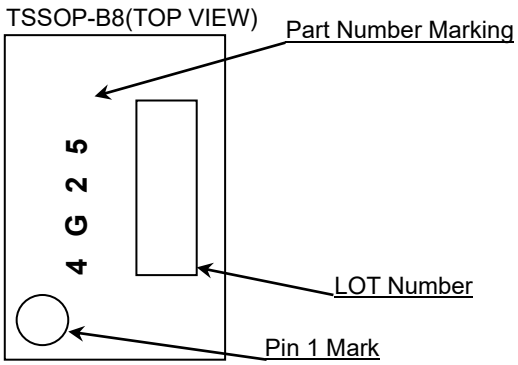
SOP-J8(TOP VIEW)



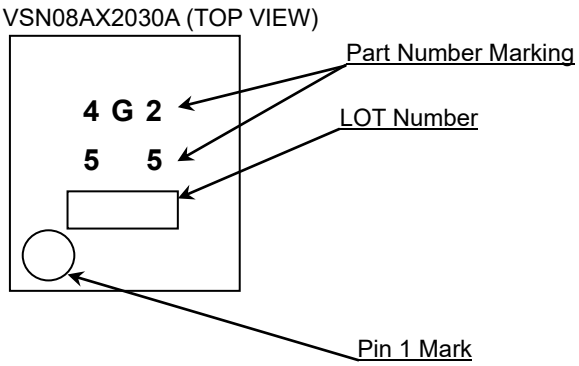
VSON008X2030 (TOP VIEW)



TSSOP-B8(TOP VIEW)



VSN08AX2030A (TOP VIEW)

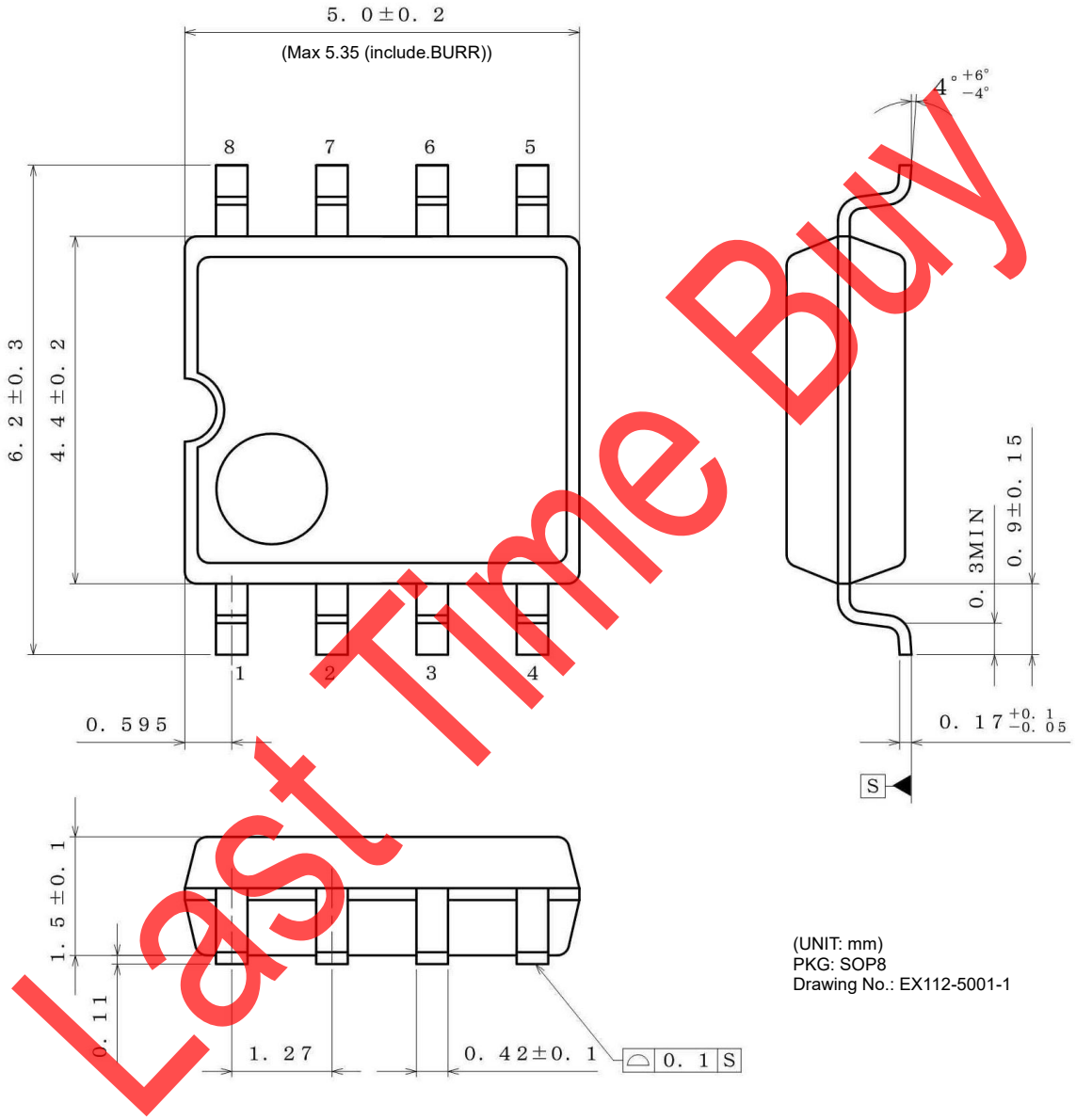


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Physical Dimension and Packing Information

Package Name	SOP8

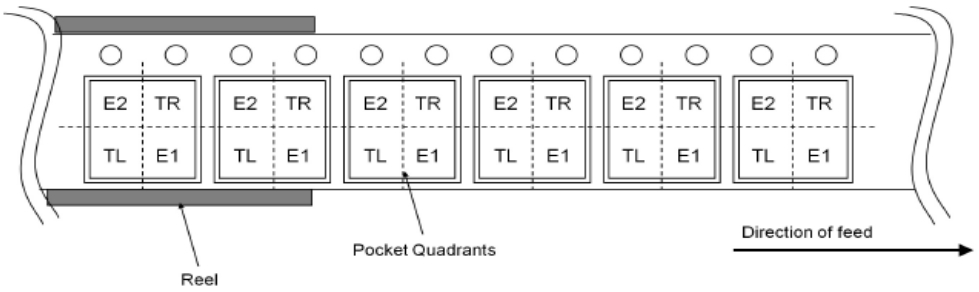


(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

Last Time Buy

<Tape and Reel information>

Tape	**Embossed carrier tape**
Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**

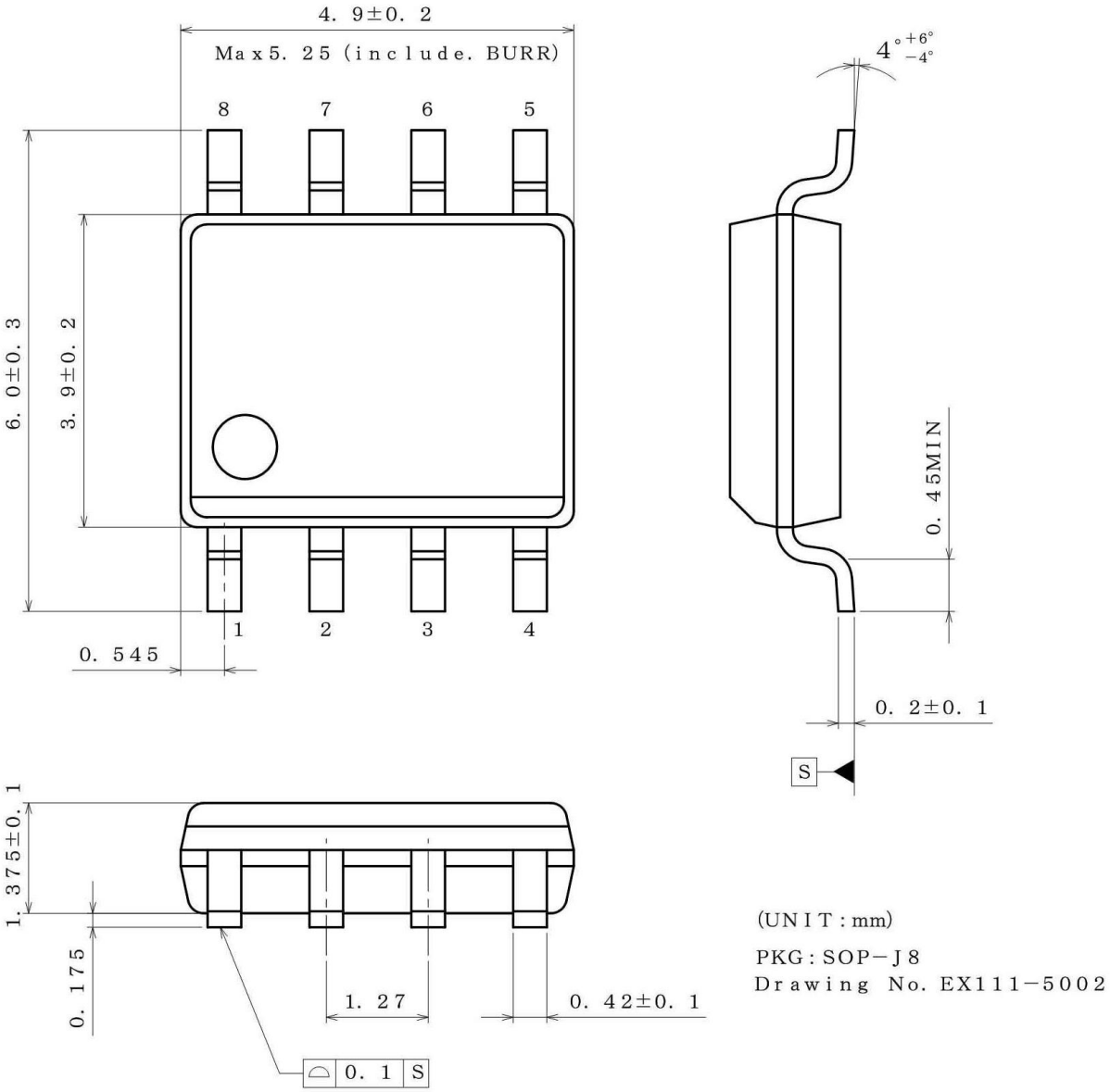


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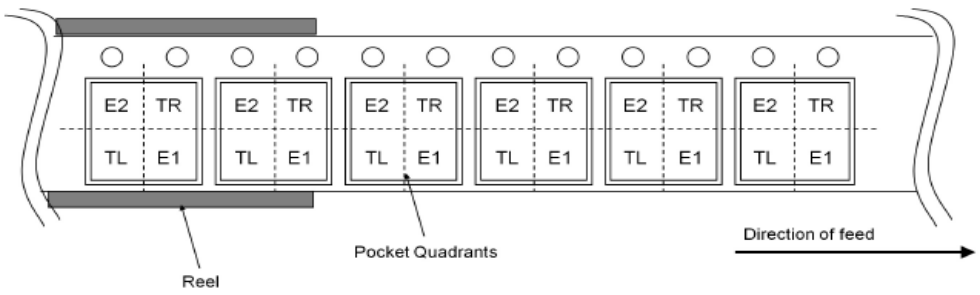
Physical Dimension and Packing Information - continued

Package Name	SOP-J8



<Tape and Reel information>

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Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**

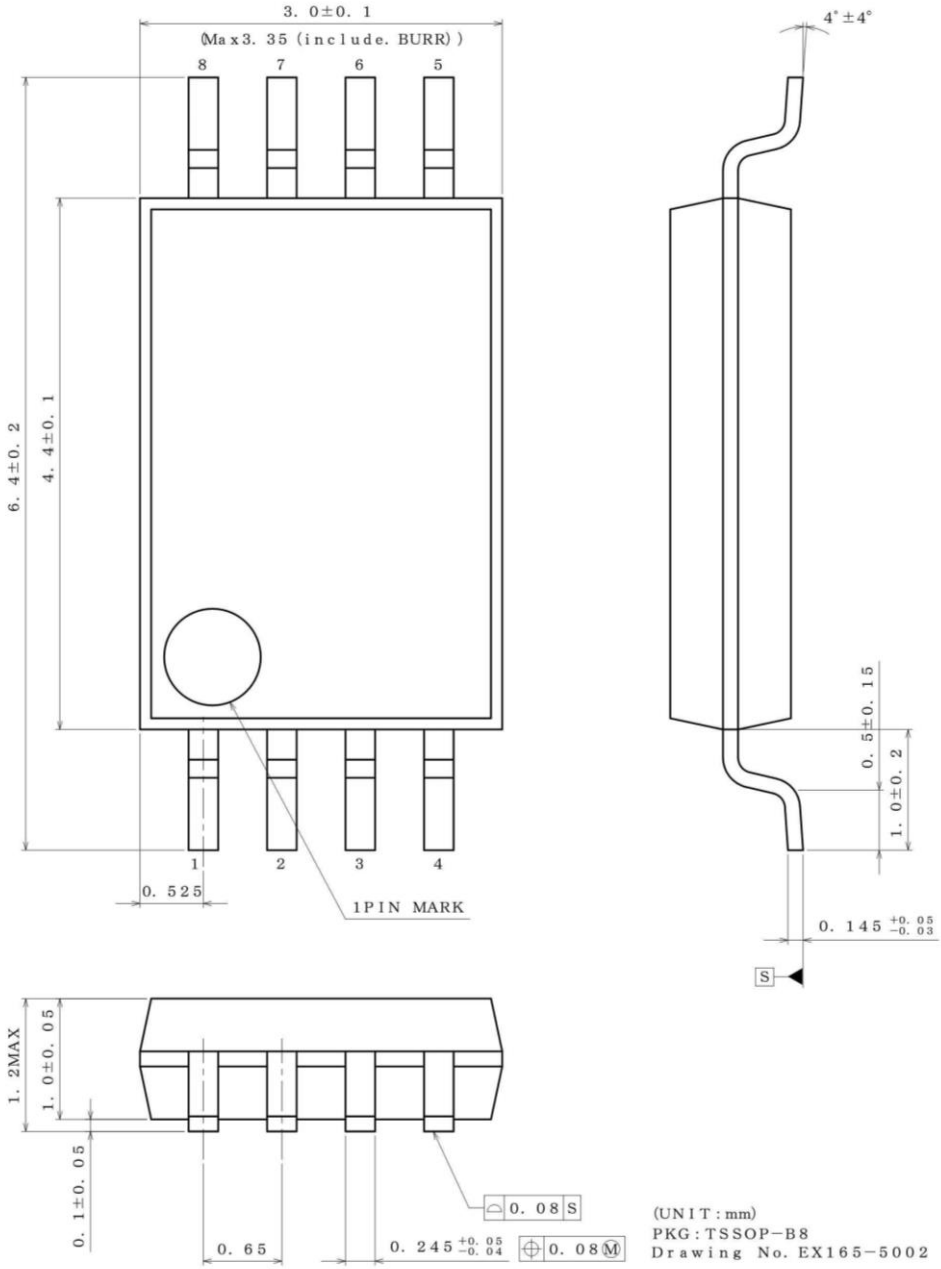


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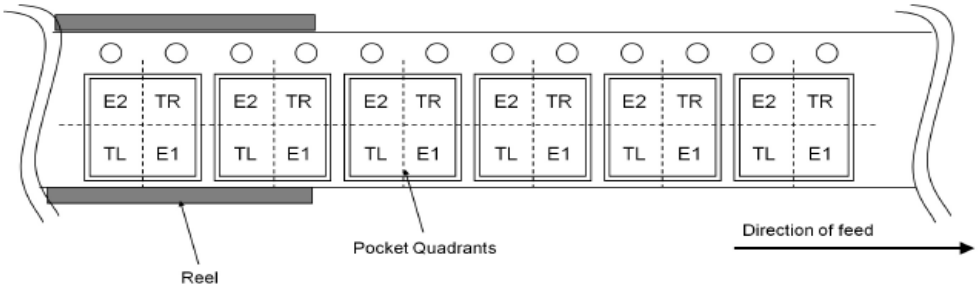
Physical Dimension and Packing Information - continued

Package Name	TSSOP-B8



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Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

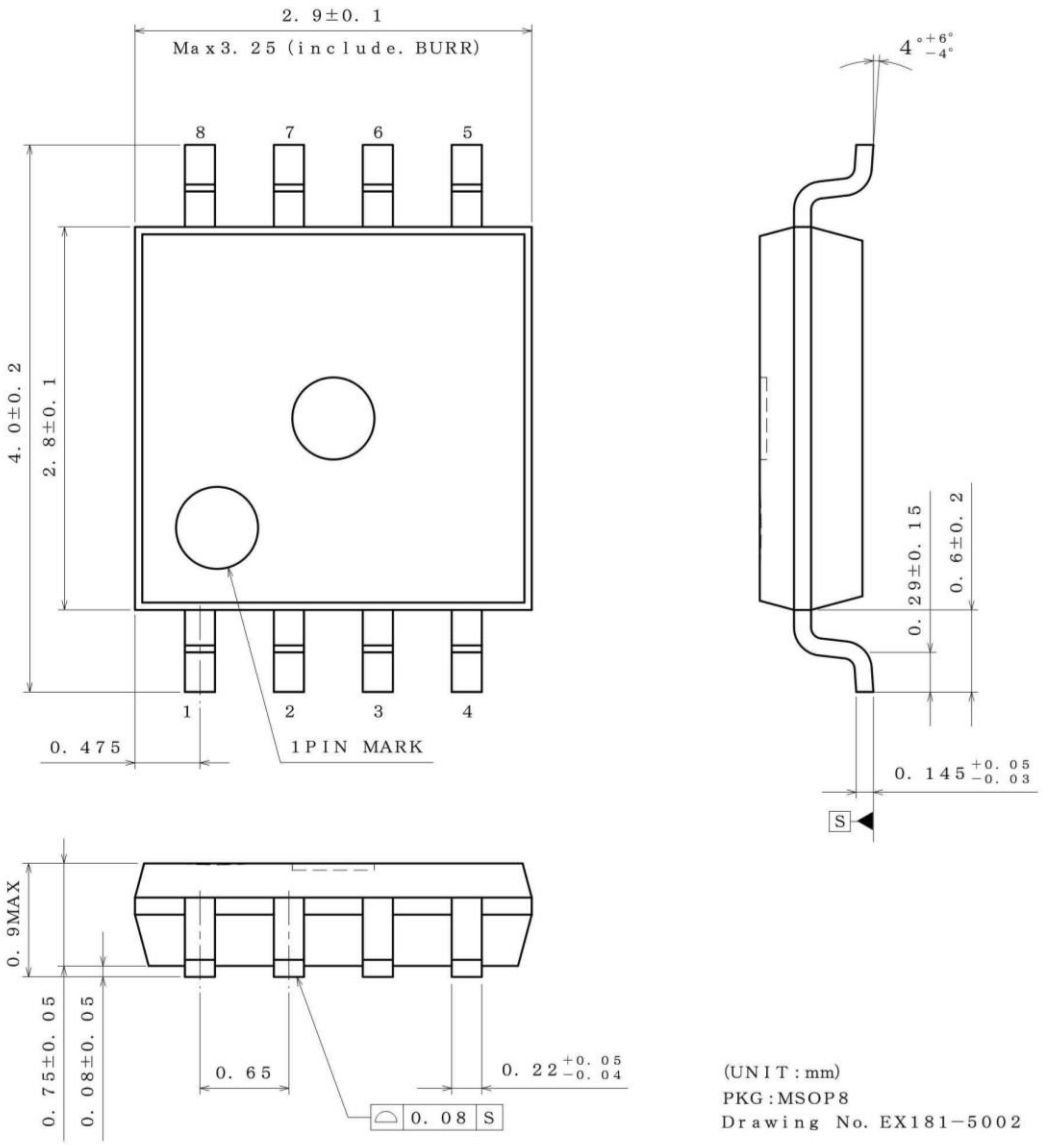


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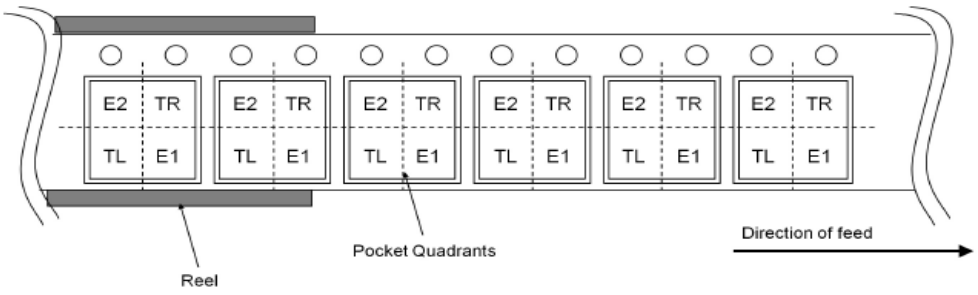
Physical Dimension and Packing Information - continued

Package Name	MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

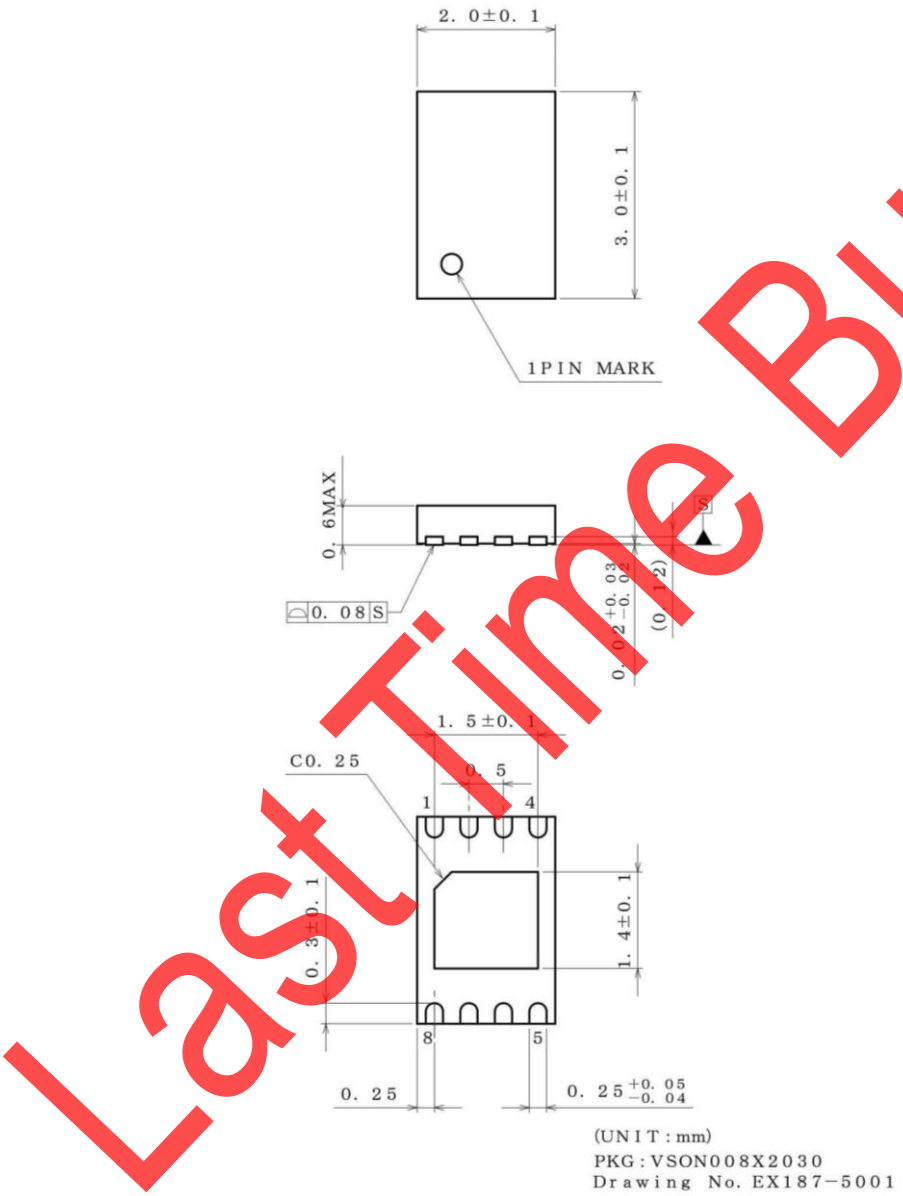


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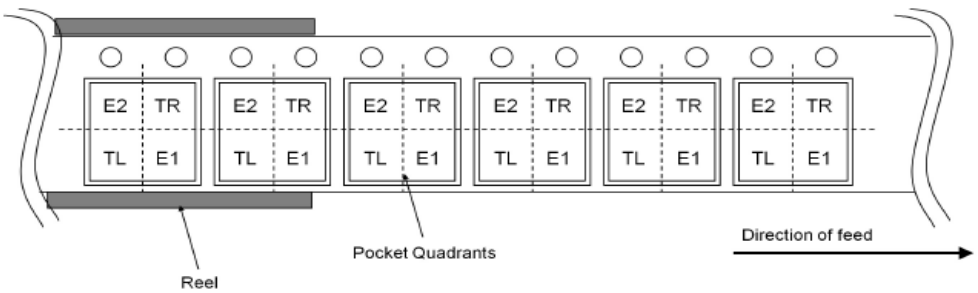
Package Name	VSON008X2030



Last Time Buy

<Tape and Reel information>

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Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

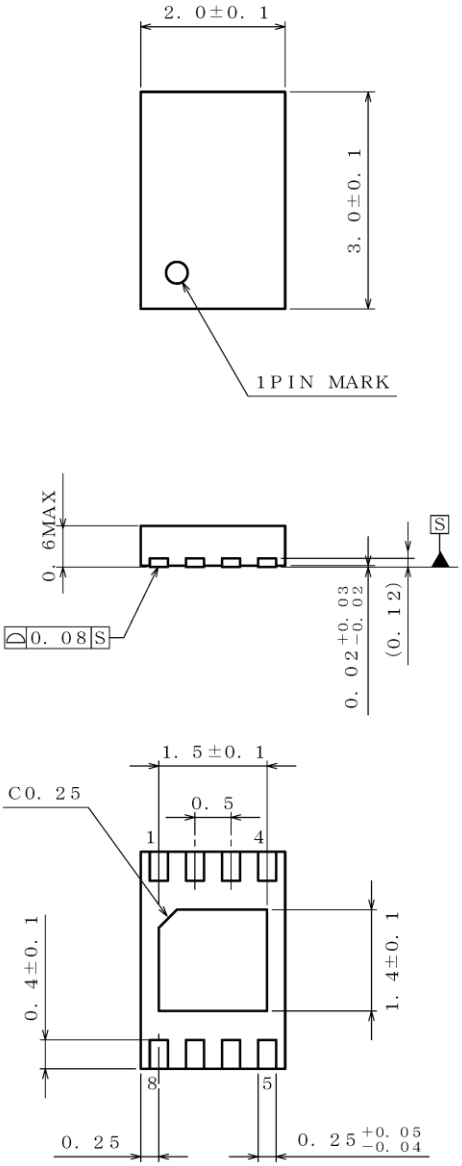


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Physical Dimension and Packing Information – continued

Package Name	VSN08AX2030A

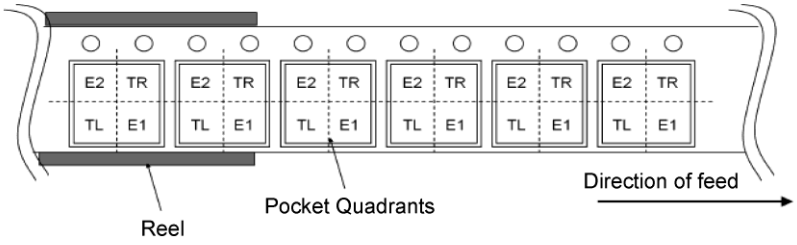


(UNIT : mm)

PKG : VSN08AX2030A
Drawing No. : EX001−0138

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
27.Sep.2017	001	New Release
24.Oct.2017	002	Package addition
13.Apr.2018	003	P.1 Add ambient operating temperature to key specifications P.1 Correction of error in package name P.24 Modify the caution on power-up conditions Change the fonts and format Improve the notation, implement grammar checking in all pages
19.Dec.2019	004	P.5 Deleted the comments on columns for condition of Input Impedance 1 and Input Impedance 2. Change the fonts and format.
05.Jun.2020	005	P.19 Correction of error in Number of remaining write cycles.
02.Mar.2021	006	P.6 Add Note.18.
19.Jul.2021	007	Updated packages and part numbers
26.Aug.2025	008	Change SOP8 to Not Recommended for New Designs. Change SDA, SCL (input) Rise Time. Change SDA, SCL (input) Fall Time.
01.Apr.2026	009	Change SOP8, SOP-J8A and VSON008X2030 to Last Time Buy. Add VSN08AX2030A Package.

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Ordering Information

B	R	2	4	G	2	5	6	F	J	-	5	Z		E	2

BUS Type
24 : I²C

Ambient Operating Temperature / Supply Voltage
-40°C~+85°C
/ 1.6V~5.5V

Capacity
256=256Kbit

Package
FJ : SOP-J8A

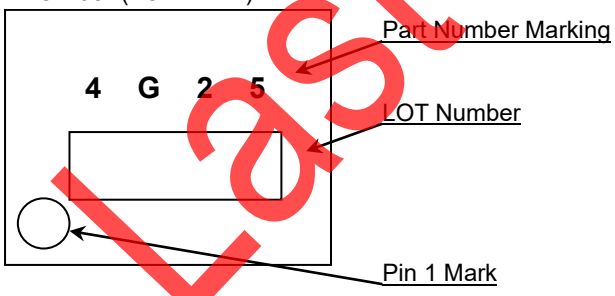
Process Code

Production Site
Z : Added

Packaging and Forming Specification
E2 : Embossed tape and reel

Marking Diagrams

SOP-J8A(TOP VIEW)



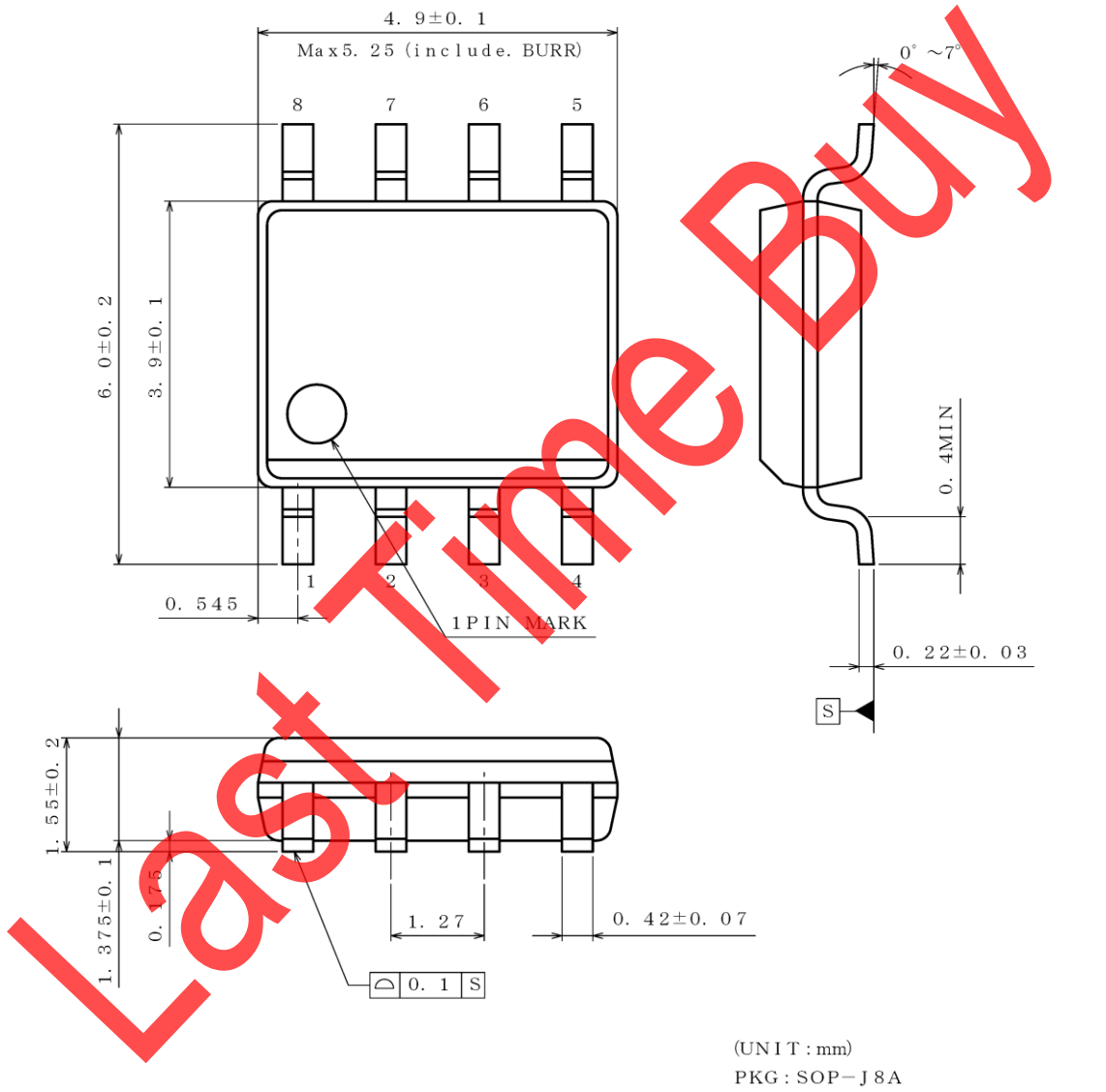
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Physical Dimension and Packing Information

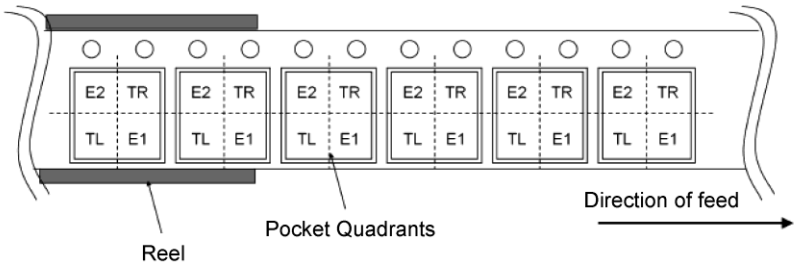
Package Name	SOP-J8A



(UNIT : mm)
PKG : SOP−J8A
Drawing No. EX001−0055−2

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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