



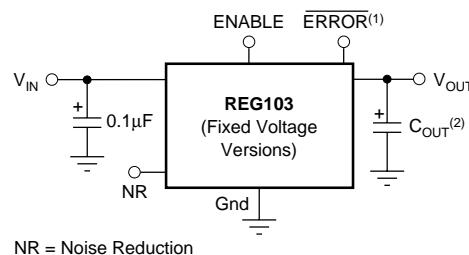
# DMOS 500mA Low-Dropout Regulator

## FEATURES

- **NEW DMOS TOPOLOGY:**  
Ultra Low Dropout Voltage:  
115mV Typ at 500mA and 3.3V Output  
Output Capacitor NOT Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 33 $\mu$ Vrms
- **HIGH ACCURACY:**  $\pm 2\%$  max
- **HIGH EFFICIENCY:**  
 $I_{GND} = 1\text{mA}$  at  $I_{OUT} = 500\text{mA}$   
Not Enabled:  $I_{GND} = 0.5\mu\text{A}$
- **2.5V, 2.7V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **OUTPUT VOLTAGE ERROR INDICATOR<sup>(1)</sup>**
- **SMALL SURFACE-MOUNT PACKAGES:**  
SOT223-5, DDPAK-5, SO-8

## APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**



NR = Noise Reduction

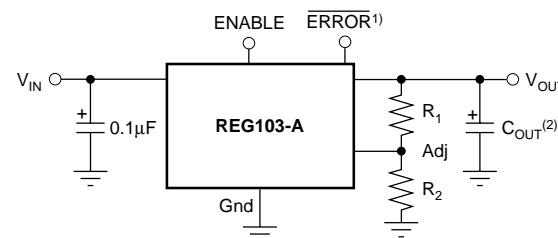
## DESCRIPTION

The REG103 is a family of low-noise, low-dropout, linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 115mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1 $\mu$ F.

Typical ground pin current is only 1mA (at  $I_{OUT} = 500\text{mA}$ ) and drops to 0.5 $\mu$ A in *not enabled* mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG103 has very low output noise (typically 33 $\mu$ Vrms for  $V_{OUT} = 3.3\text{V}$  with  $C_{NR} = 0.01\mu\text{F}$ ), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (-40°C to +85°C).

The SO-8 version of the REG103 has an **ERROR** pin that provides a *power good* flag, indicating the regulator is in regulation. The REG103 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. In addition to the SO-8 package, the REG103 is also available in the DDPAK and the SOT223-5.



NOTE: (1) SO-8 Package Only. (2) Optional.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Input Voltage, $V_{IN}$ .....	-0.3V to 16V
Enable Input Voltage, $V_{EN}$ .....	-0.3V to $V_{IN}$
Feedback Voltage, $V_{FB}$ .....	-0.3V to 6.0V
NR Pin Voltage, $V_{NR}$ .....	-0.3V to 6.0V
Error Flag Output .....	-0.3V to 6V
Error Flag Current .....	2mA
Output Short-Circuit Duration .....	Indefinite
Operating Temperature Range .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	-55°C to +150°C
Lead Temperature (soldering, 3s, SO-8, SOT, and DDPAK) .....	+240°C
ESD Rating: HBM ( $V_{OUT}$ to GND) .....	1.5kV
HBM (All other pins) .....	2kV
CDM .....	500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

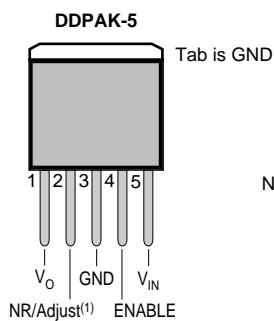
## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub>
<b>REG103xx-yyy/zzz</b>	<b>XX</b> is package designator. <b>YYYY</b> is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). <b>ZZZ</b> is package quantity.

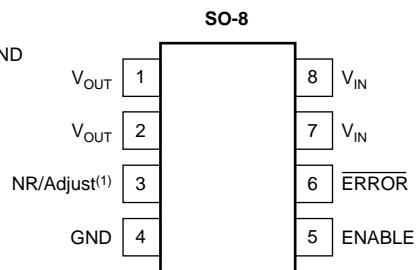
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS

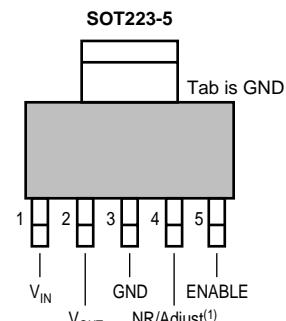
### Top View



(F Package)



(U Package)



(G Package)

NOTE: (1) For REG103A-A: voltage setting resistor pin.  
All other models: noise reduction capacitor pin.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_J = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

At  $T_J = +25^{\circ}\text{C}$ ,  $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$  ( $V_{\text{OUT}} = 3.0\text{V}$  for REG103-A),  $V_{\text{ENABLE}} = 2\text{V}$ ,  $I_{\text{OUT}} = 10\text{mA}$ ,  $C_{\text{NR}} = 0.01\mu\text{F}$ , and  $C_{\text{OUT}} = 0.1\mu\text{F}^{(1)}$ , unless otherwise noted.

PARAMETER	CONDITION	REG103GA, UA, FA			UNITS	
		MIN	TYP	MAX		
<b>OUTPUT VOLTAGE</b>						
Output Voltage Range REG103-2.5 REG103-2.7 REG103-3.0 REG103-3.3 REG103-5 REG103-A	$V_{\text{OUT}}$					
Reference Voltage Adjust Pin Current	$V_{\text{REF}}$ $I_{\text{ADJ}}$					
Accuracy $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$dV_{\text{OUT}}/dT$	$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $I_{\text{OUT}} = 10\text{mA}$ to $500\text{mA}$ , $V_{\text{IN}} = (V_{\text{OUT}} + 0.7\text{V})$ to $15\text{V}$ $V_{\text{IN}} = (V_{\text{OUT}} + 0.9\text{V})$ to $15\text{V}$	$V_{\text{REF}}$	2.5 2.7 3.0 3.3 5 1.295 0.2 $\pm 0.5$ <b>70</b> $\pm 0.5$	5.5 $\pm 2$ $\pm 2.8$	V V V V V V $\mu\text{A}$ %
vs Temperature vs Line and Load $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$					ppm/ $^{\circ}\text{C}$ % %	
<b>DC DROPOUT VOLTAGE<sup>(2, 3)</sup></b>	$V_{\text{DROP}}$	$I_{\text{OUT}} = 10\text{mA}$ $I_{\text{OUT}} = 500\text{mA}$ $I_{\text{OUT}} = 500\text{mA}$ $I_{\text{OUT}} = 500\text{mA}$		3 115 160	25 200 250 <b>230</b> <b>280</b>	mV mV mV mV mV
For all models except 5V For 5V model For all models except 5V $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$						
For 5V models $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$						
<b>VOLTAGE NOISE</b> $f = 10\text{Hz}$ to $100\text{kHz}$	$V_n$					
Without $C_{\text{NR}}$ (all models) With $C_{\text{NR}}$ (all fixed voltage models)		$C_{\text{NR}} = 0$ , $C_{\text{OUT}} = 0$ $C_{\text{NR}} = 0.01\mu\text{F}$ , $C_{\text{OUT}} = 10\mu\text{F}$		$30\mu\text{Vrms}/\text{V} \cdot V_{\text{OUT}}$ $10\mu\text{Vrms}/\text{V} \cdot V_{\text{OUT}}$		$\mu\text{Vrms}$ $\mu\text{Vrms}$
<b>OUTPUT CURRENT</b> Current Limit <sup>(4)</sup>	$I_{\text{CL}}$			550 <b>500</b>	700 <b>1000</b>	mA mA
$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$						
<b>RIPPLE REJECTION</b> $f = 120\text{Hz}$				65		dB
<b>ENABLE CONTROL</b>						
$V_{\text{ENABLE}}$ HIGH (output enabled) $V_{\text{ENABLE}}$ LOW (output disabled)	$V_{\text{ENABLE}}$					
$I_{\text{ENABLE}}$ HIGH (output enabled) $I_{\text{ENABLE}}$ LOW (output disabled)	$I_{\text{ENABLE}}$	$V_{\text{ENABLE}} = 2\text{V}$ to $V_{\text{IN}}$ , $V_{\text{IN}} = 2.1\text{V}$ to $6.5^{(5)}$ $V_{\text{ENABLE}} = 0\text{V}$ to $0.5\text{V}$		2 -0.2	$V_{\text{IN}}$ 0.5 100 2 50 1.5	V V nA nA us ms
Output Disable Time Output Enable Soft Start Time						
<b>ERROR FLAG<sup>(6)</sup></b> Current, Logic HIGH (open drain)—Normal Operation Voltage, Logic LOW—On Error		$V_{\text{IN}} = V_{\text{ERROR}} = V_{\text{OUT}} + 1\text{V}$ Sinking $500\mu\text{A}$		0.1 0.2	10 0.4	$\mu\text{A}$ V
<b>THERMAL SHUTDOWN</b>						
Junction Temperature Shutdown Reset from Shutdown					150 130	$^{\circ}\text{C}$ $^{\circ}\text{C}$
<b>GROUND PIN CURRENT</b>						
Ground Pin Current ENABLE Pin LOW	$I_{\text{GND}}$	$I_{\text{OUT}} = 10\text{mA}$ $I_{\text{OUT}} = 500\text{mA}$ $V_{\text{ENABLE}} \leq 0.5\text{V}$		0.5 1 0.5	0.7 1.3	mA mA $\mu\text{A}$
<b>INPUT VOLTAGE</b>	$V_{\text{IN}}$					
Operating Input Voltage Range <sup>(7)</sup> Specified Input Voltage Range $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$V_{\text{IN}} > 2.7\text{V}$ $V_{\text{IN}} > 2.9\text{V}$		2.1 $V_{\text{OUT}} + 0.7$ $V_{\text{OUT}} + 0.9$	15 15 <b>15</b>	V V V
<b>TEMPERATURE RANGE</b>						
Specified Range Operating Range Storage Range	$T_J$					
Thermal Resistance DDPAK-5 Surface-Mount SO-8 Surface-Mount SOT223-5 Surface-Mount	$\theta_{\text{JC}}$ $\theta_{\text{JA}}$ $\theta_{\text{JC}}$	Junction-to-Case Junction-to-Ambient Junction-to-Case		-40 -55 -65	+85 +125 +150	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$

NOTES: (1) The REG103 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at  $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$  at fixed load.

(3) Not applicable for  $V_{\text{OUT}}$  less than  $2.7\text{V}$ .

(4) Current limit is the output current that produces a 10% change in output voltage from  $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$  and  $I_{\text{OUT}} = 10\text{mA}$ .

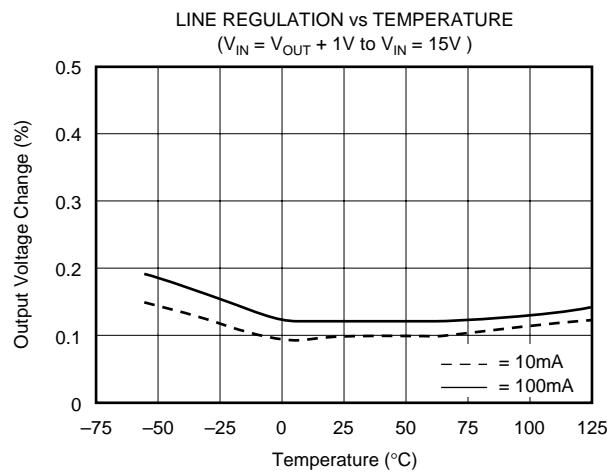
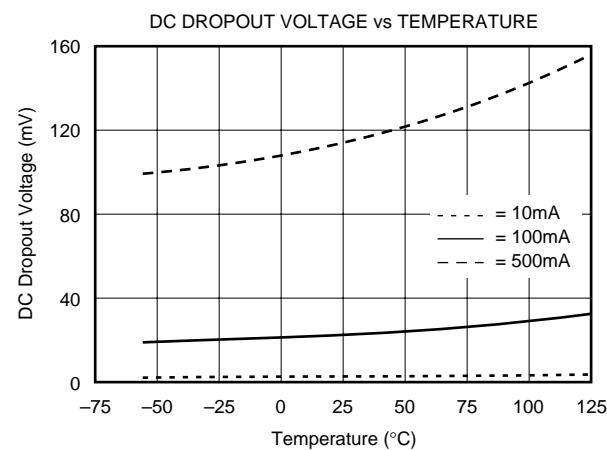
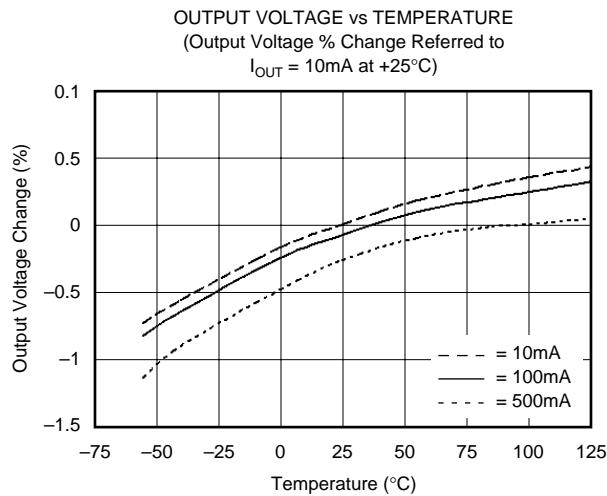
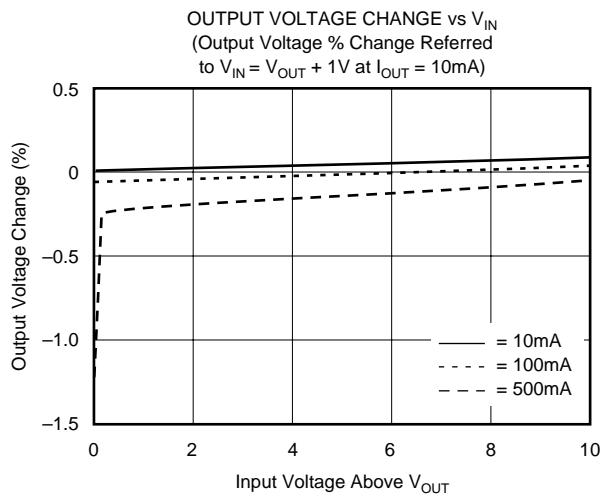
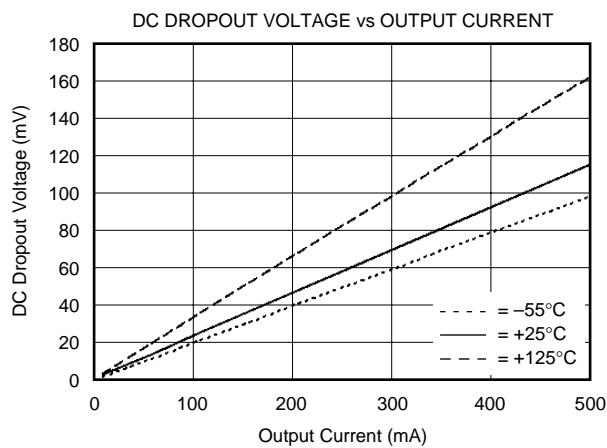
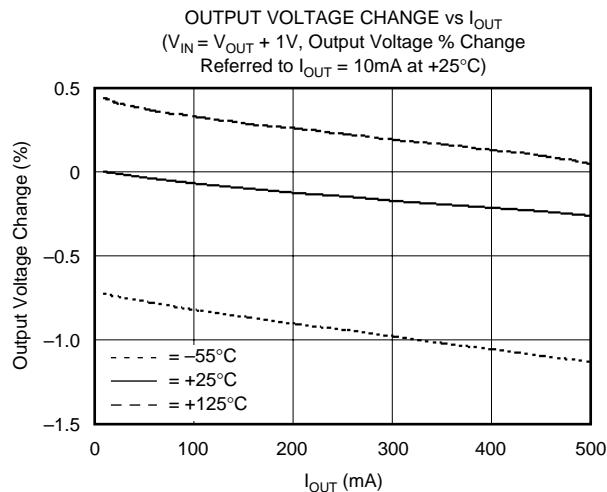
(5) For  $V_{\text{IN}} > 6.5\text{V}$ , see typical characteristic  $V_{\text{ENABLE}}$  vs  $I_{\text{ENABLE}}$ .

(6) Logic low indicates out-of-regulation condition by approximately 10%, or thermal shutdown.

(7) The REG103 no longer regulates when  $V_{\text{IN}} < V_{\text{OUT}} + V_{\text{DROP}}(\text{MAX})$ . In drop-out or when the input voltage is between  $2.7\text{V}$  and  $2.1\text{V}$ , the impedance from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  is typically less than  $1\Omega$  at  $T_J = +25^{\circ}\text{C}$ . See typical characteristic.

# TYPICAL CHARACTERISTICS

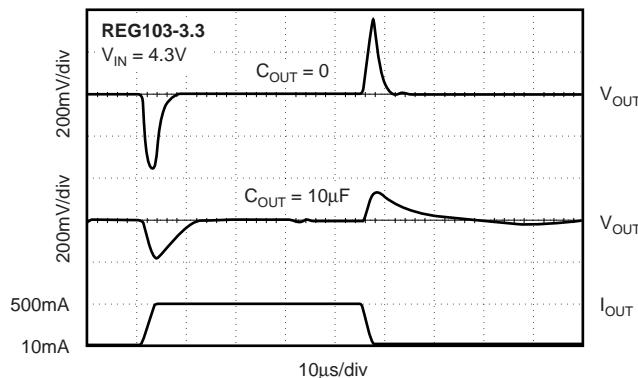
For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.



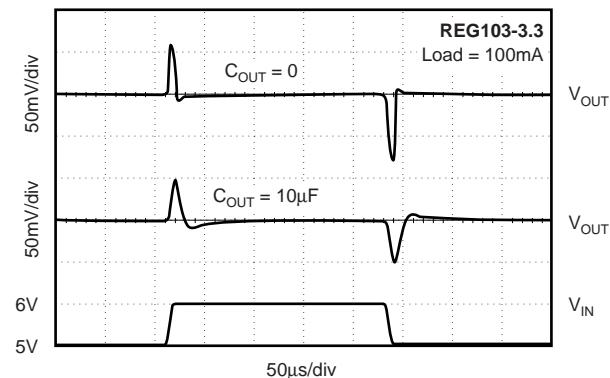
## TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.

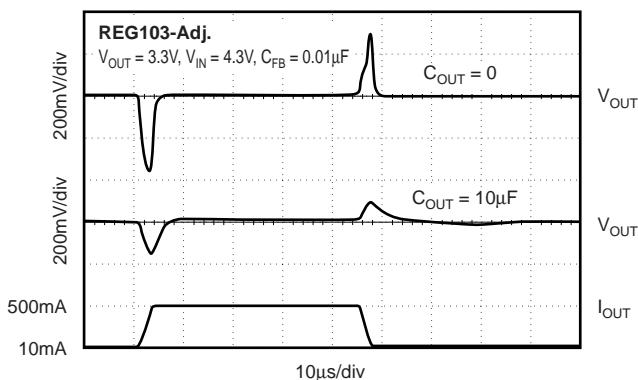
LOAD TRANSIENT RESPONSE



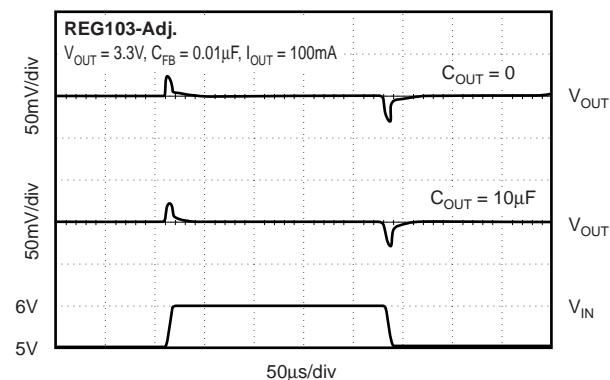
LINE TRANSIENT RESPONSE



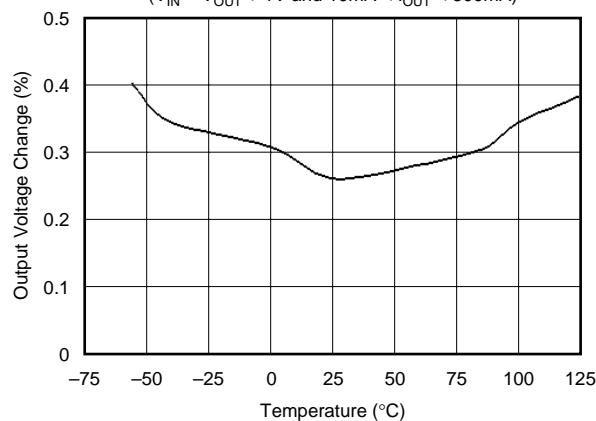
LOAD TRANSIENT RESPONSE



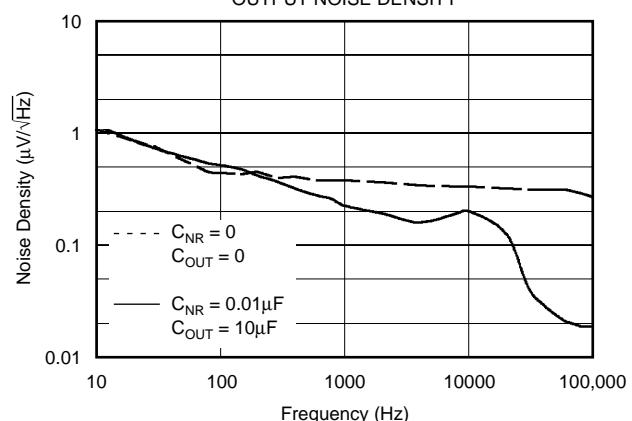
LINE TRANSIENT RESPONSE



LOAD REGULATION vs TEMPERATURE  
 $(V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$  and  $10\text{mA} < I_{\text{OUT}} < 500\text{mA}$ )

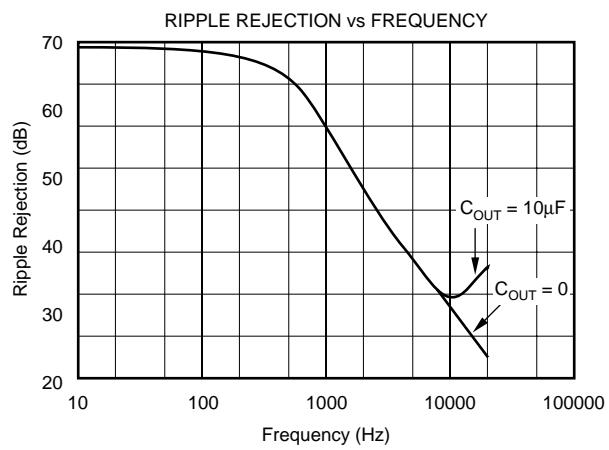
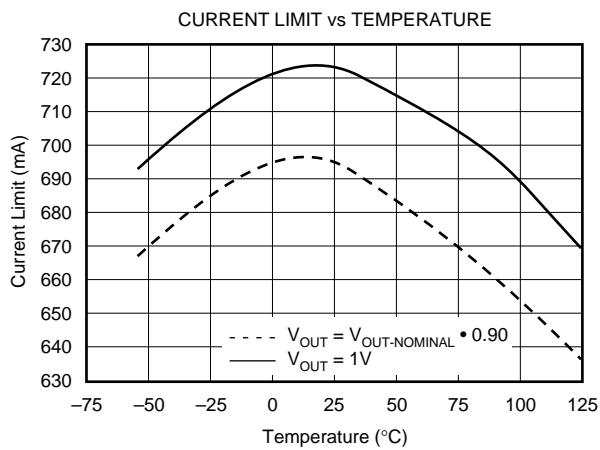
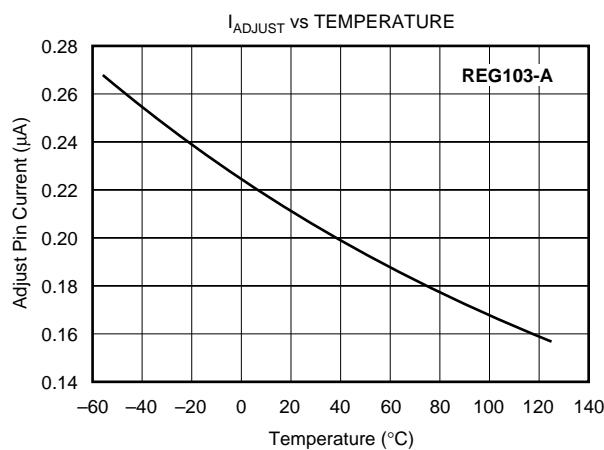
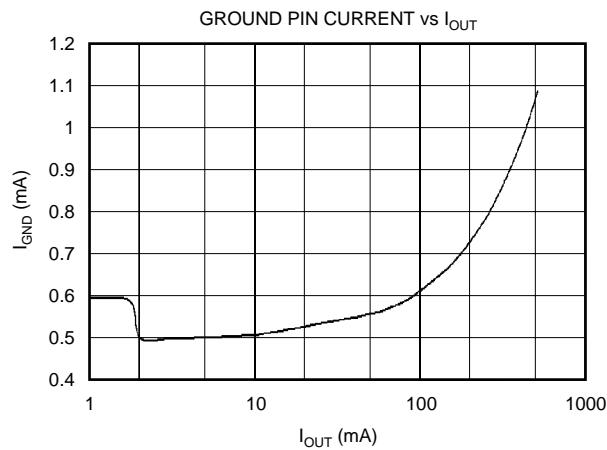
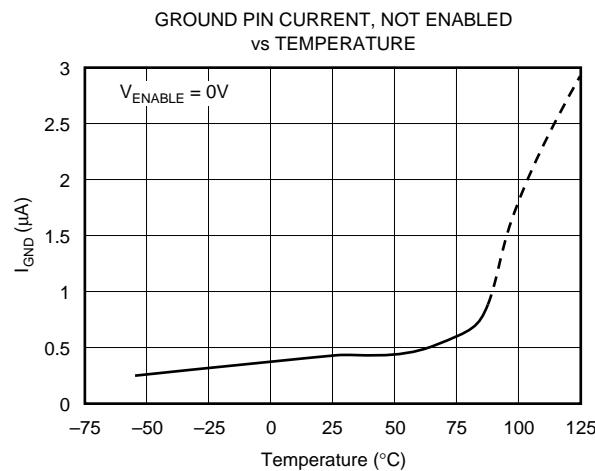
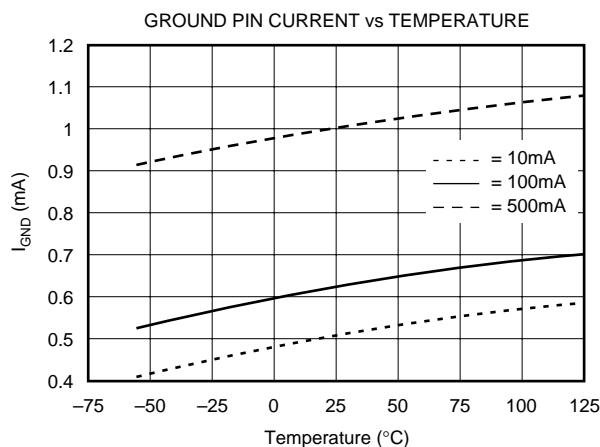


OUTPUT NOISE DENSITY



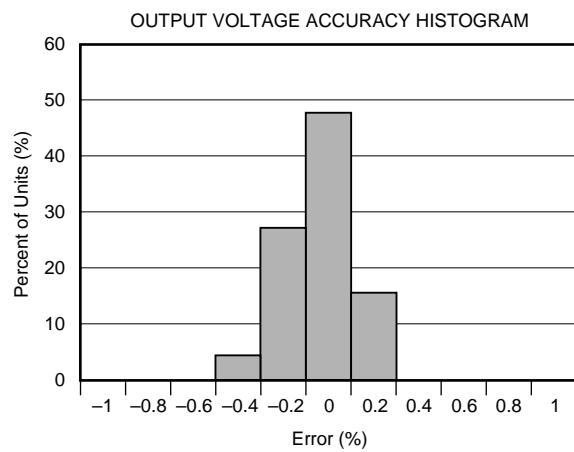
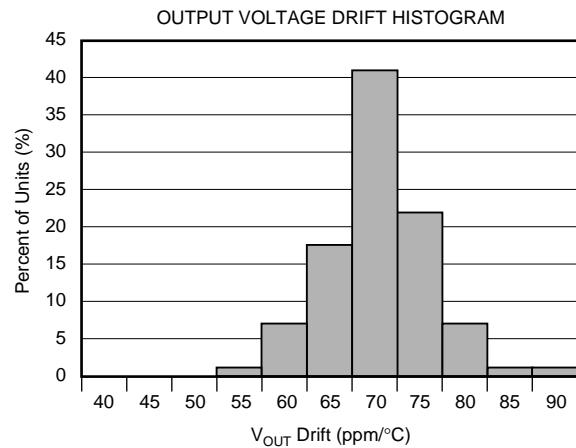
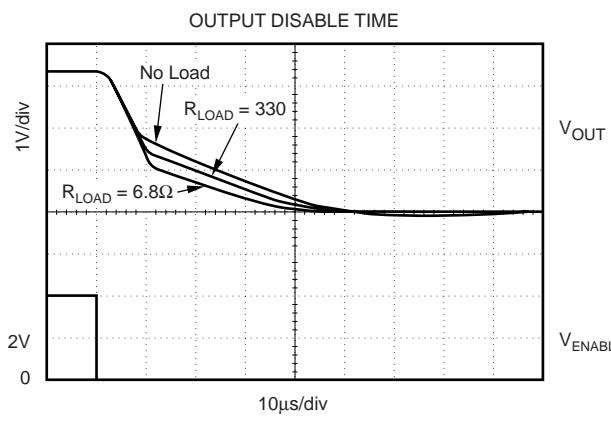
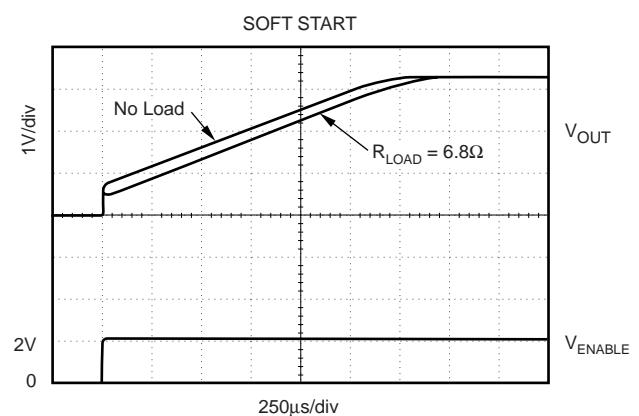
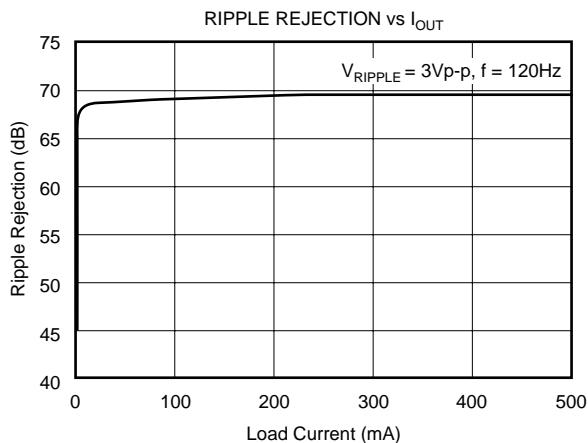
## TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.



# BASIC OPERATION

The REG103 series is a family of LDO (Low Drop-Out) linear regulators. The family includes five fixed output versions (2.5V to 5.0V) and an adjustable output version. An internal DMOS power device provides low dropout regulation with near constant ground pin current (largely independent of load and drop-out conditions) and very fast line and load transient response. All versions include internal current limit and thermal shutdown circuitry.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG103A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2. The SO-8 package provides two pins each for  $V_{IN}$  and  $V_{OUT}$ . Both sets of pins **MUST** be used and connected adjacent to the device.

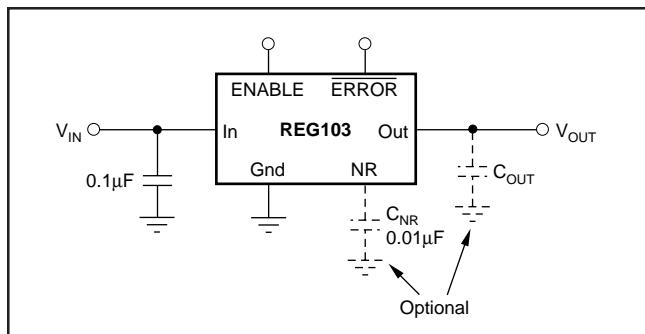


FIGURE 1. Fixed Voltage Nominal Circuit for REG103.

None of the versions require an output capacitor for regulator stability. The REG103 will accept any output capacitor type less than 1µF. For capacitance values larger than 1µF, the effective ESR should be greater than 0.1Ω. This minimum ESR value includes parasitics such as printed circuit board traces, solder joints, and sockets. A minimum 0.1µF low ESR capacitor connected to the input supply voltage is recommended.

## INTERNAL CURRENT LIMIT

The REG103 internal current limit has a typical value of 700mA. A fold-back feature limits the short-circuit current to a typical short-circuit value of 40mA. This circuit will protect the regulator from damage under all load conditions. A typical characteristic of  $V_{OUT}$  versus  $I_{OUT}$  is given in Figure 3a.

Care should be taken in high current applications to avoid ground currents flowing in the circuit board traces causing voltage drops between points on the circuit. If voltage drops occur on the circuit board ground that causes the load ground voltage to be much lower than the ground voltage seen by the ground pin on the REG103, the foldback current may approach zero and the REG103 may not start up. In these types of applications, a large value resistor can be placed between  $V_{IN}$  and  $V_{OUT}$  to help "boost" up the output of the REG103 during start-up, see Figure 3b. The value for the "boost" resistor should be chosen so that the current through the "boost" resistor is less than the minimum load current:  $R_{BOOST} > (V_{IN} - V_{OUT})/I_{LOAD}$ . Typically, a good value for a "boost" resistor is 5kΩ.

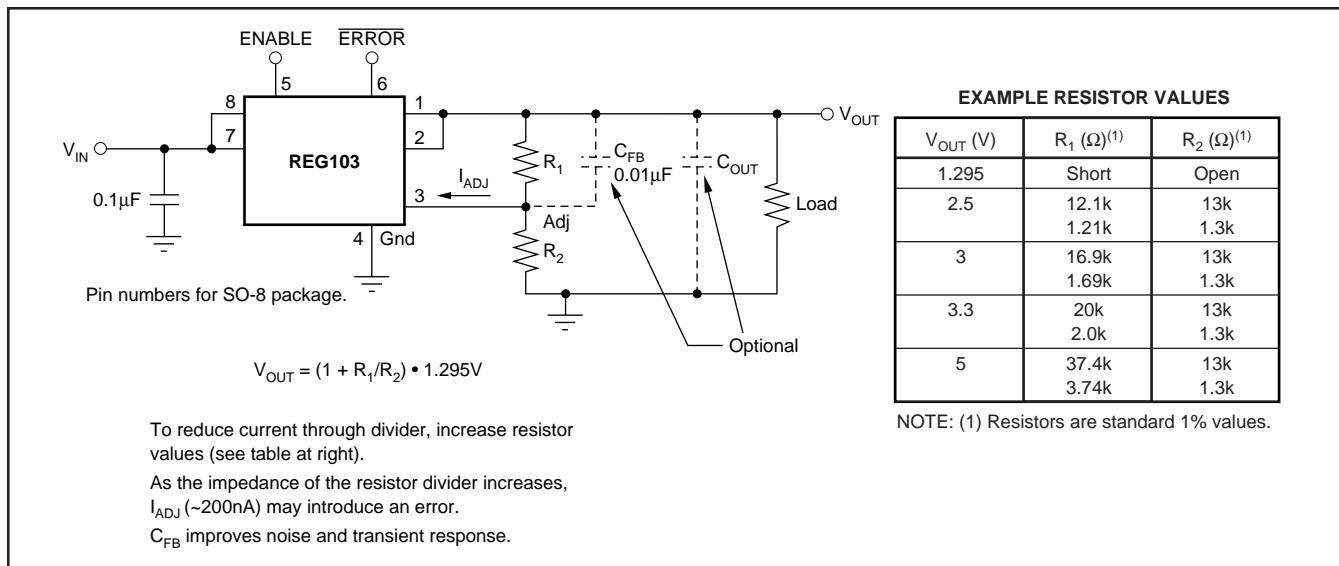


FIGURE 2. Adjustable Voltage Circuit for REG103A.

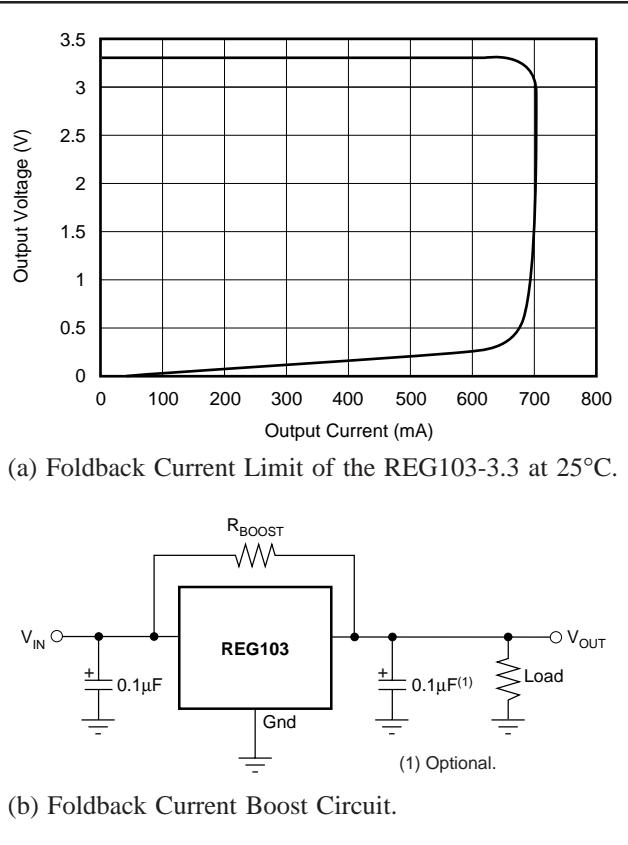


FIGURE 3. Foldback Current Limit and Boost Circuit.

## ENABLE

The ENABLE pin allows the regulator to be turned on and off. This pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 0.5µA. When not used, the ENABLE pin may be connected to  $V_{IN}$ .

Internal to the part, the ENABLE pin is connected to an input resistor-zener diode circuit, as shown in Figure 4, creating a nonlinear input impedance. The ENABLE Pin Current versus Applied Voltage relationship is shown in Figure 5. When the ENABLE pin is connected to a voltage greater than 10V, a series resistor may be used to limit the current.

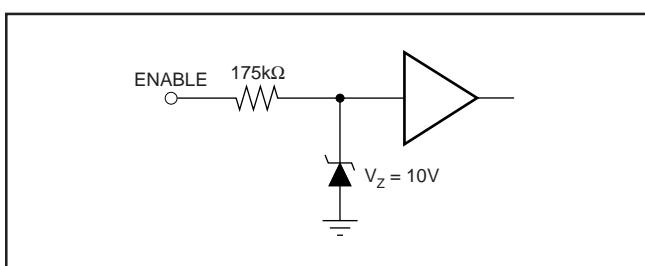


FIGURE 4. ENABLE Pin Equivalent Input Circuit.

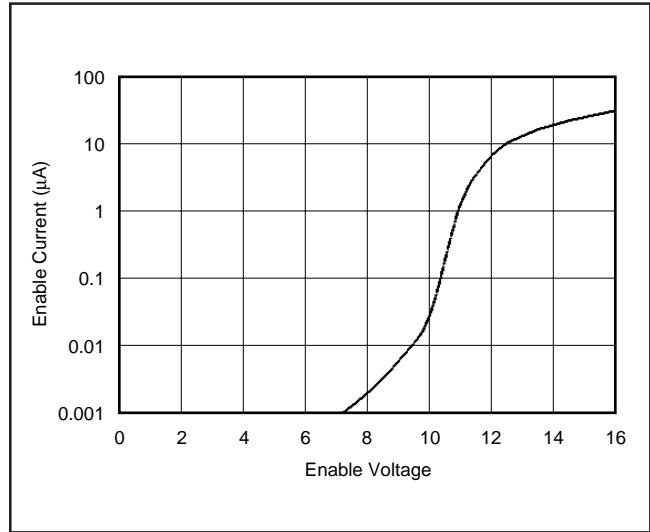


FIGURE 5. ENABLE Pin Current versus Applied Voltage.

## ERROR FLAG

The error indication pin, only available on the SO-8 package version, provides a fault indication out-of-regulation condition. During a fault condition,  $\overline{ERROR}$  is pulled LOW by an open drain output device. The pin voltage, in the fault state, is typically less than 0.2V at 500µA.

A fault condition is indicated when the output voltage differs (either above or below) from the specified value by approximately 10%. Figure 6 shows a typical fault-monitoring application.

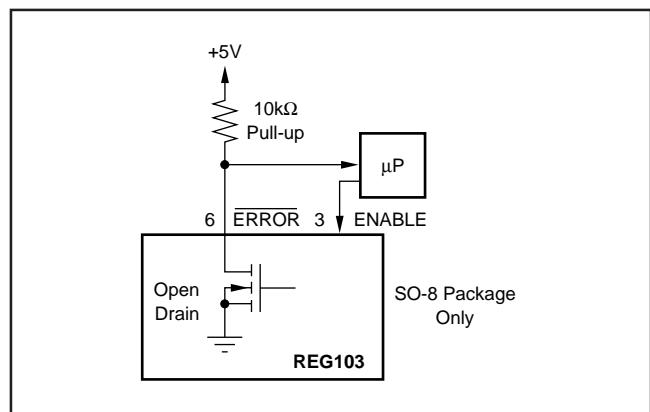


FIGURE 6. ERROR Pin Typical Fault-Monitoring Circuit.

## OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage,  $V_{REF}$ , for the REG103. This reference is the dominant noise source within the REG103. It generates approximately 45µVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 45\mu\text{Vrms} \frac{R_1 + R_2}{R_2} = 45\mu\text{Vrms} \cdot \frac{V_{OUT}}{V_{REF}}$$

Since the value of  $V_{REF}$  is 1.295V, this relationship reduces to:

$$V_N = 35 \frac{\mu V_{rms}}{V} \cdot V_{OUT}$$

Connecting a capacitor,  $C_{NR}$ , from the Noise-Reduction (NR) pin to ground, can reduce the output noise voltage. Adding  $C_{NR}$ , as shown in Figure 7, forms a low-pass filter for the voltage reference. For  $C_{NR} = 10nF$ , the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 3.5, as shown in Figure 8.

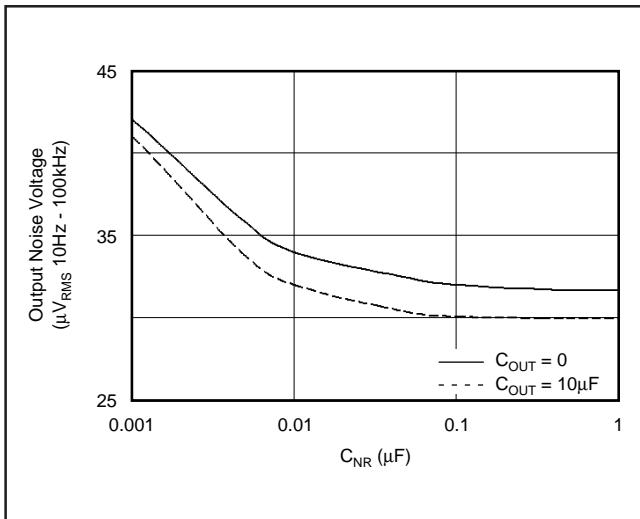


FIGURE 8. Output Noise versus Noise-Reduction Capacitor.

The REG103 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor,  $C_{FB}$ , connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. Figure 9 shows improved output noise performance for two capacitor combinations.

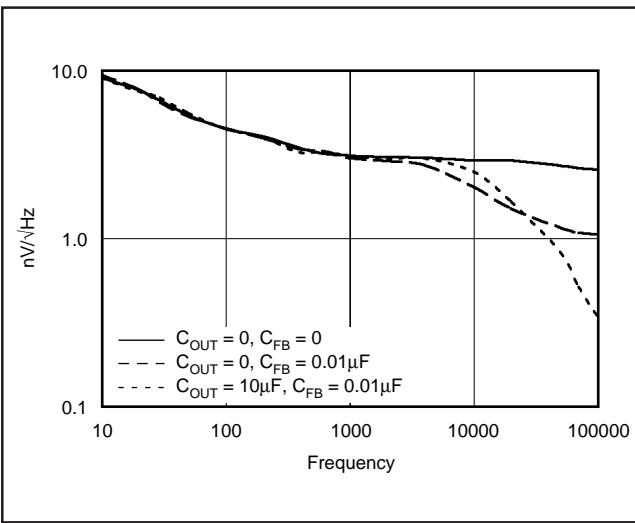


FIGURE 9. Output Noise Density on Adjustable Versions.

The REG103 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above  $V_{IN}$ . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator.

## DROP-OUT VOLTAGE

The REG103 uses an N-channel DMOS as the “pass” element. When the input voltage is within a few hundred millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of  $V_{IN}$  to  $V_{OUT}$ , the regulator’s input-to-output resistance is the  $R_{DS(on)}$  of the DMOS pass element (typically 230mΩ). For static (DC) loads, the REG103 will typically maintain regulation down to  $V_{IN}$  to  $V_{OUT}$  voltage drop of 115mV at full-rated output current. In Figure 10, the bottom line (DC dropout) shows the minimum  $V_{IN}$  to  $V_{OUT}$  voltage drop required to prevent drop-out under DC load conditions.

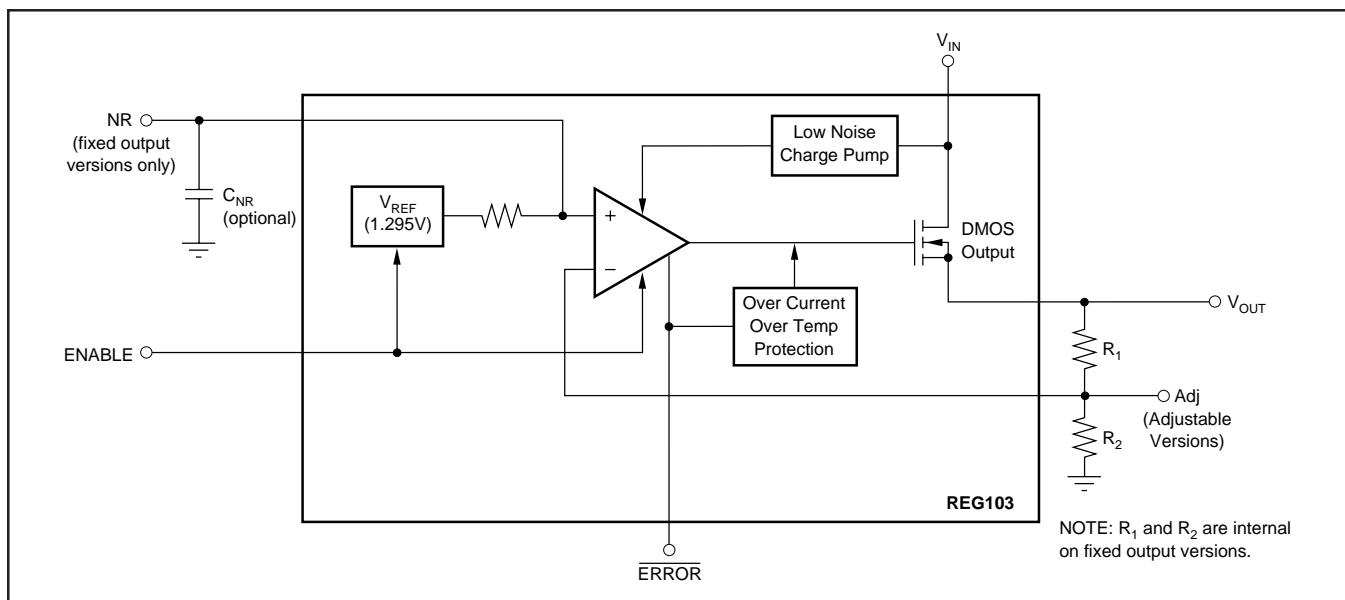


FIGURE 7. Block Diagram.

For large step changes in load current, the REG103 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this “transient drop-out” region is shown as the top line in Figure 10. Values of  $V_{IN}$  to  $V_{OUT}$  voltage drop above this line insure normal transient response.

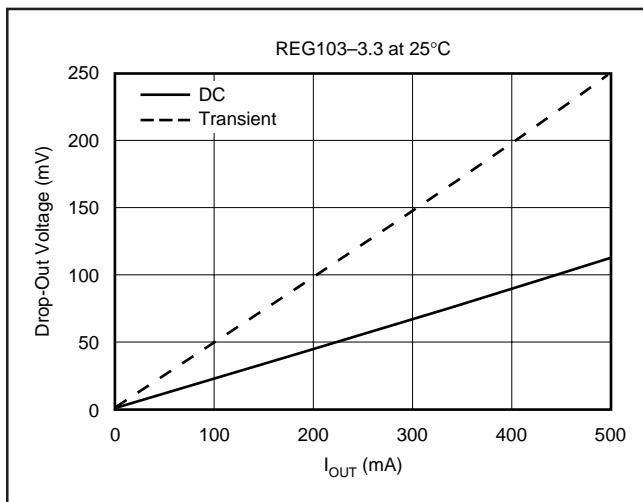


FIGURE 10. Transient and DC Dropout.

In the transient dropout region between “DC” and “Transient”, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available “headroom”  $V_{IN}$  to  $V_{OUT}$  voltage drop. Under worst-case conditions (full-scale load change with  $V_{IN}$  to  $V_{OUT}$  voltage drop close to DC dropout levels), the REG103 can take several hundred microseconds to re-enter the specified window of regulation.

## TRANSIENT RESPONSE

The REG103 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 10nF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor,  $C_{FB}$  (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

## THERMAL PROTECTION

Power dissipated within the REG103 will cause the junction temperature to rise. The REG103 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 150°C, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be

limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG103 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG103 into thermal shutdown will degrade reliability.

## POWER DISSIPATION

The REG103 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 11. In all cases, the PCB copper area is bare copper, free of solder-resist mask, and not solder plated. All examples are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

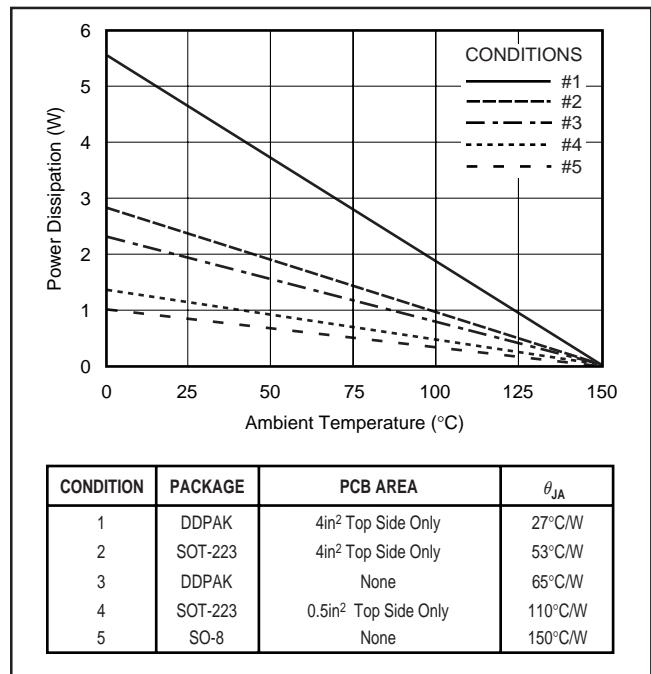


FIGURE 11. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the average output current times the voltage across the output element,  $V_{IN}$  to  $V_{OUT}$  voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

## REGULATOR MOUNTING

The tab of both packages is electrically connected to ground. For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit-

board copper area. Increasing the copper area improves heat dissipation. Figure 12 shows typical thermal resistance from junction to ambient as a function of the copper area for the DDPAK.

Although the tabs of the DDPAK and the SOT-223 are electrically grounded, they are not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG103 devices are presented in the Application Bulletin "Solder Pad Recommendations for Surface-Mount Devices" (SBFA015), available from the Texas Instruments web site (www.ti.com).

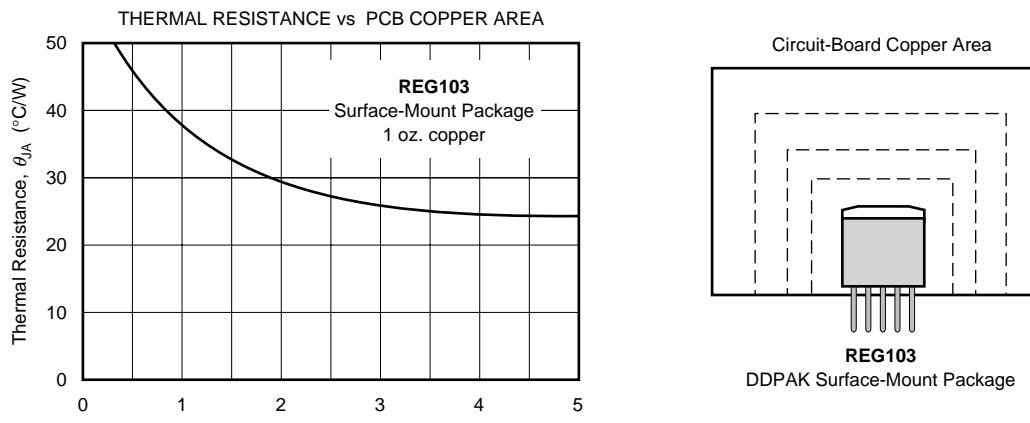


FIGURE 12. Thermal Resistance versus PCB Area for the Five-Lead DDPAK.

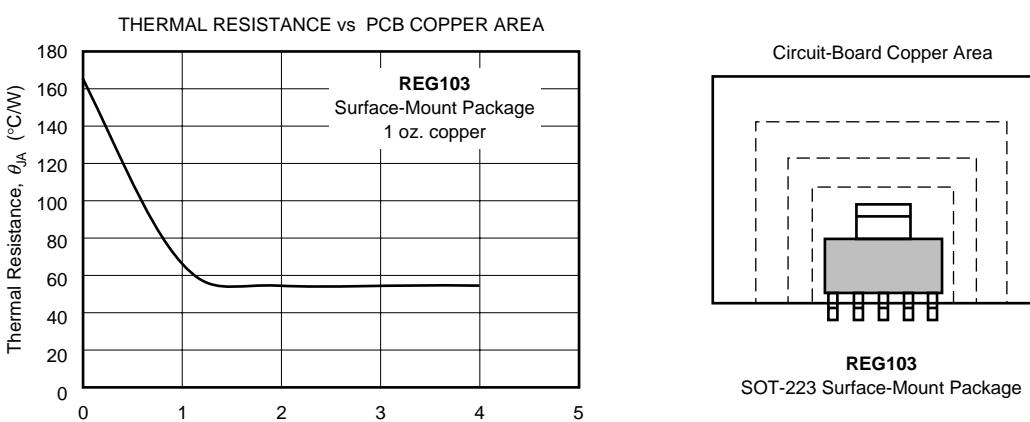


FIGURE 13. Thermal Resistance versus PCB Area for the Five-Lead SOT-223.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REG103FA-2.5KTTT	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5
REG103FA-2.5KTTT.A	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5
REG103FA-2.5KTTT.B	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5
REG103FA-2.5KTTTG3	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5
REG103FA-3.3KTTT	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-3.3
REG103FA-3.3KTTT.A	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-3.3
REG103FA-3.3KTTT.B	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-3.3
REG103FA-5KTTT	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-5
REG103FA-5KTTT.B	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-5
REG103FA-5KTTTG3	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-5
REG103FA-A/500	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103FA-A/500.A	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103FA-A/500.B	Active	Production	DDPAK/ TO-263 (KTT)   5	500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103FA-AKTTT	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103FA-AKTTT.A	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103FA-AKTTT.B	Active	Production	DDPAK/ TO-263 (KTT)   5	50   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A
REG103GA-2.5	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G25

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REG103GA-2.5.A	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G25
REG103GA-2.5.B	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G25
<b>REG103GA-3.3</b>	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
REG103GA-3.3.A	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
REG103GA-3.3.B	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
<b>REG103GA-3.3/2K5</b>	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
REG103GA-3.3/2K5.A	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
REG103GA-3.3/2K5.B	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33
<b>REG103GA-5</b>	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G50
REG103GA-5.B	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G50
<b>REG103GA-5/2K5</b>	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	R103G50
REG103GA-5/2K5.B	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	R103G50
REG103GA-5G4	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G50
<b>REG103GA-A</b>	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
REG103GA-A.A	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
REG103GA-A.B	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
<b>REG103GA-A/2K5</b>	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
REG103GA-A/2K5.A	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
REG103GA-A/2K5.B	Active	Production	SOT-223 (DCQ)   6	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
REG103GA-AG4	Active	Production	SOT-223 (DCQ)   6	78   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA
<b>REG103UA-2.5</b>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25
REG103UA-2.5.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25
REG103UA-2.5.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25
<b>REG103UA-2.5/2K5</b>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25
REG103UA-2.5/2K5.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25
REG103UA-2.5/2K5.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">REG103UA-3.3</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
REG103UA-3.3.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
REG103UA-3.3.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
<a href="#">REG103UA-3.3/2K5</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
REG103UA-3.3/2K5.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
REG103UA-3.3/2K5.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4
<a href="#">REG103UA-5</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50
REG103UA-5.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50
<a href="#">REG103UA-5/2K5</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50
REG103UA-5/2K5.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50
<a href="#">REG103UA-A</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
REG103UA-A.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
REG103UA-A.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
<a href="#">REG103UA-A/2K5</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
REG103UA-A/2K5.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
REG103UA-A/2K5.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A
REG103UA-AG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

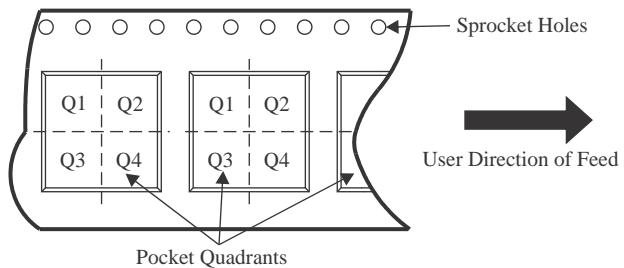
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


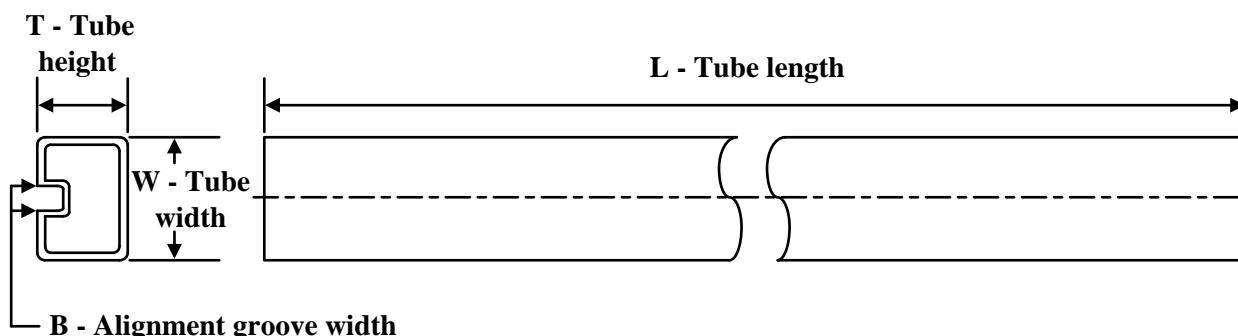
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG103GA-3.3/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG103GA-5/2K5	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
REG103GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG103UA-2.5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-3.3/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-A/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG103GA-3.3/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG103GA-5/2K5	SOT-223	DCQ	6	2500	356.0	356.0	36.0
REG103GA-A/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG103UA-2.5/2K5	SOIC	D	8	2500	356.0	356.0	35.0
REG103UA-3.3/2K5	SOIC	D	8	2500	356.0	356.0	35.0
REG103UA-5/2K5	SOIC	D	8	2500	356.0	356.0	35.0
REG103UA-A/2K5	SOIC	D	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

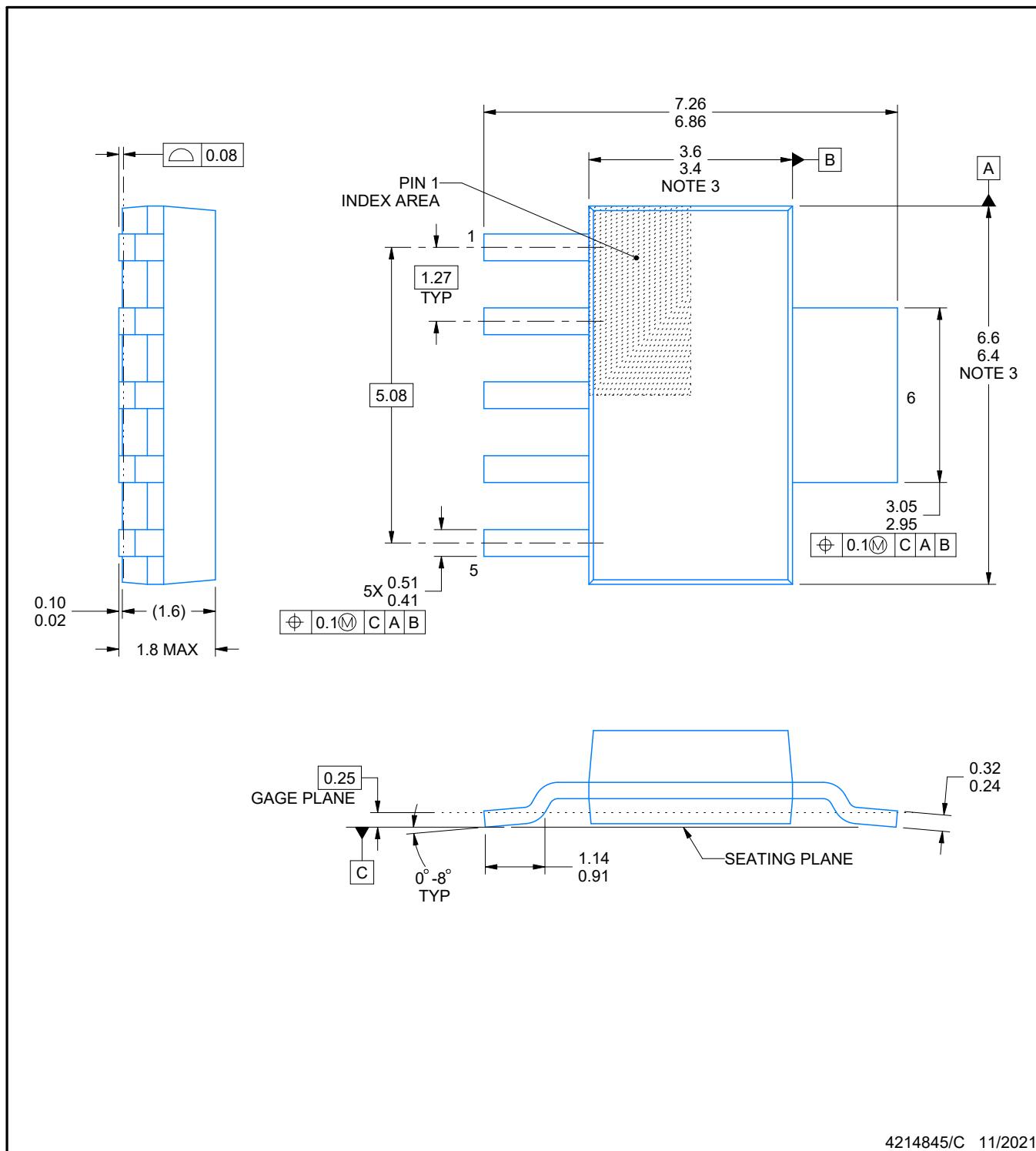
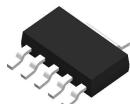
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
REG103GA-2.5	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-2.5.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-2.5.B	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-3.3	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-3.3.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-3.3.B	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-5	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-5.B	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-5G4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-A.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-A.B	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103GA-AG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG103UA-2.5	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-2.5.A	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-2.5.B	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-3.3	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-3.3.A	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-3.3.B	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-5	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-5.B	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-A	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-A.A	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-A.B	D	SOIC	8	75	506.6	8	3940	4.32
REG103UA-AG4	D	SOIC	8	75	506.6	8	3940	4.32

## PACKAGE OUTLINE

## SOT - 1.8 mm max height

## PLASTIC SMALL OUTLINE

**DCQ0006A**



4214845/C 11/2021

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

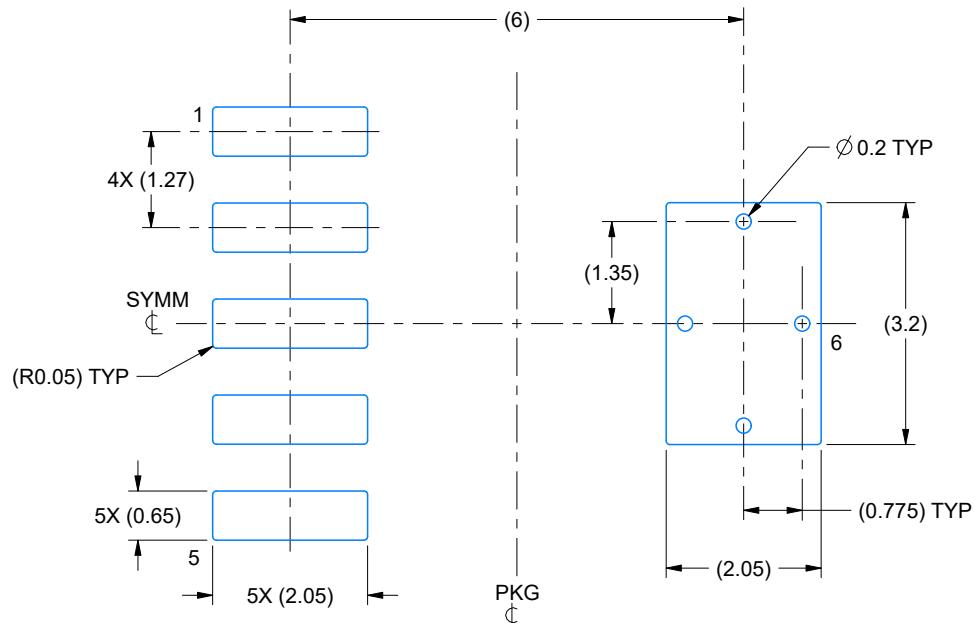


## EXAMPLE BOARD LAYOUT

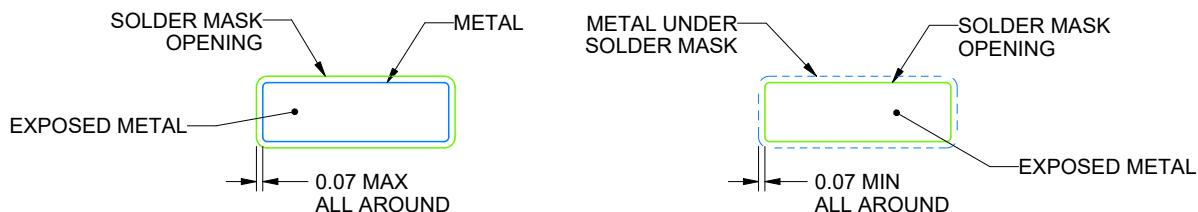
**DCQ0006A**

**SOT - 1.8 mm max height**

## PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4214845/C 11/2021

#### NOTES: (continued)

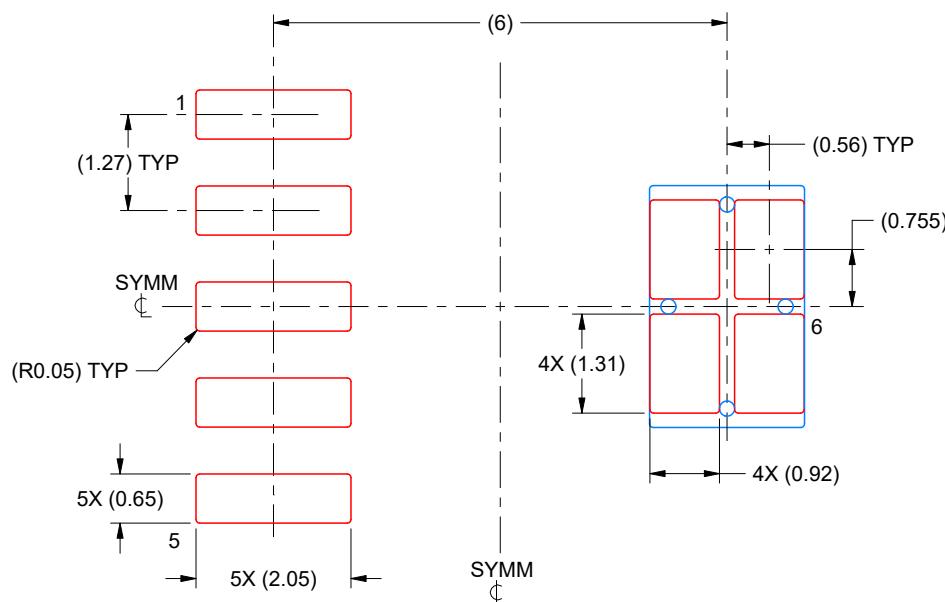
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

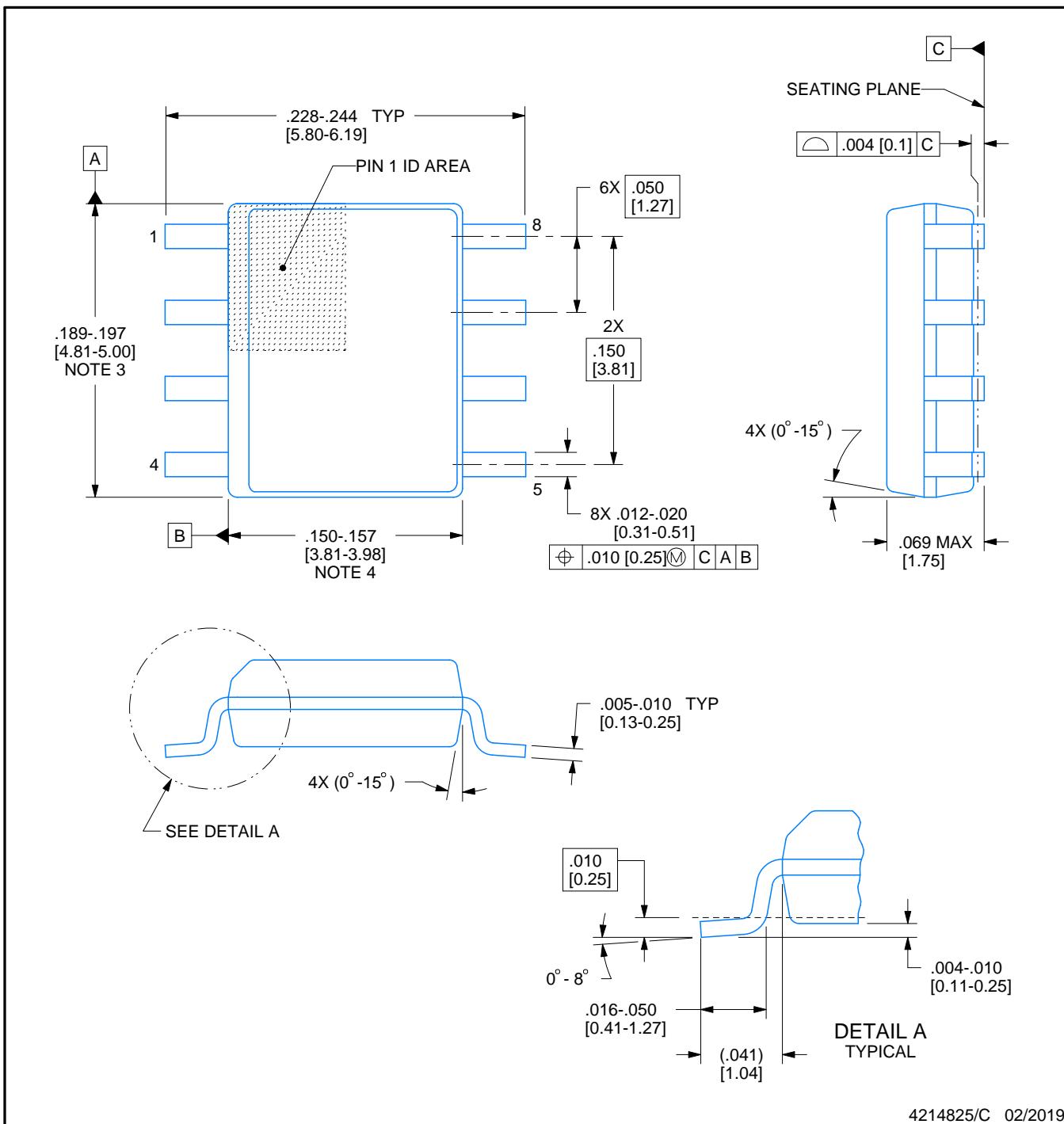
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

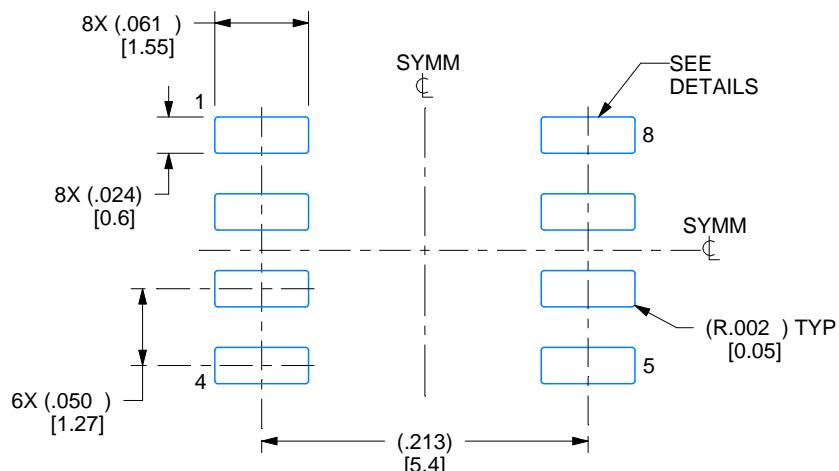
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

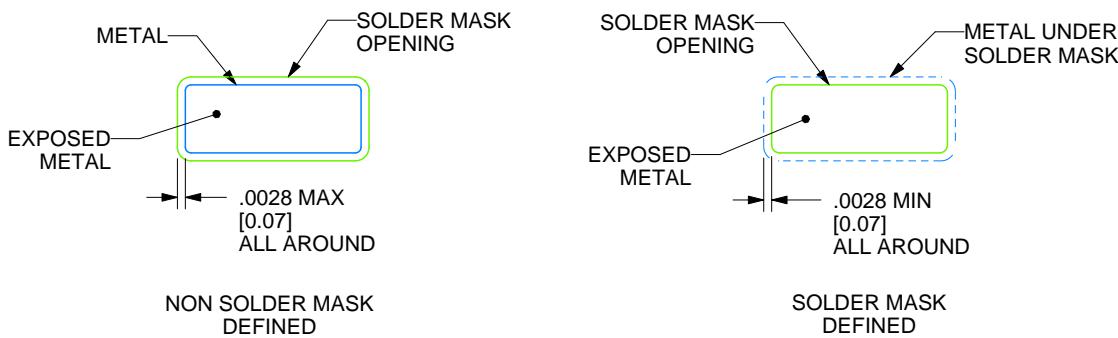
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

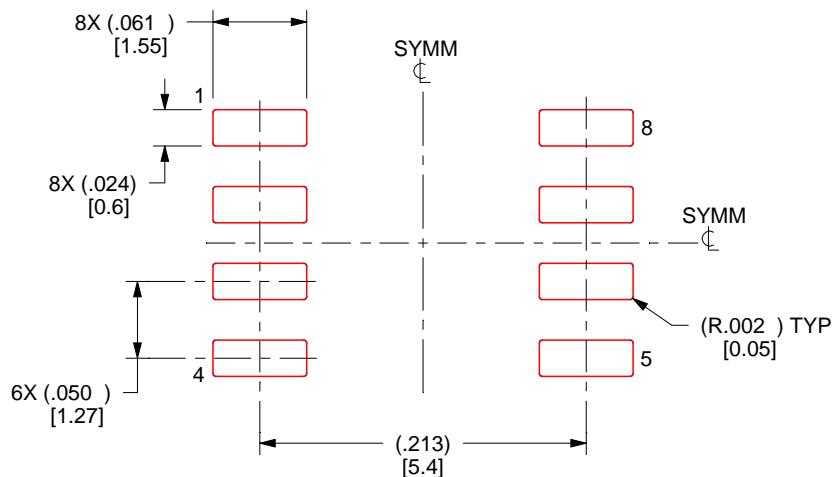
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

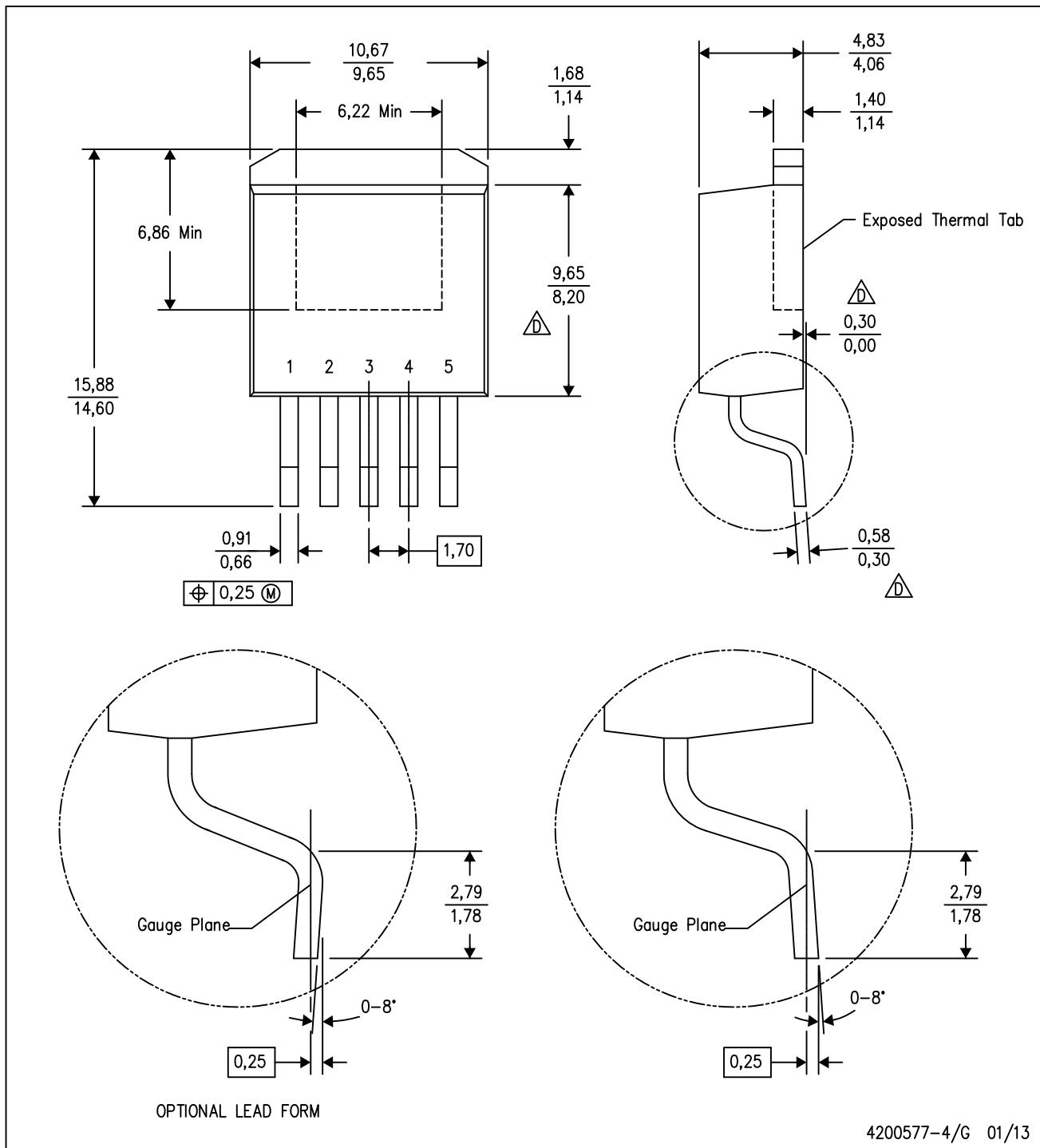
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE



4200577-4/G 01/13

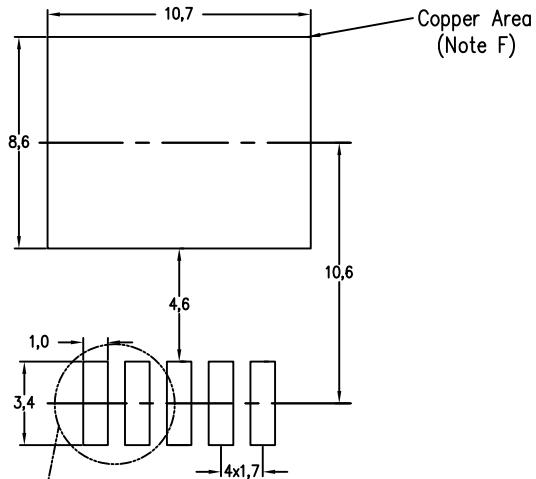
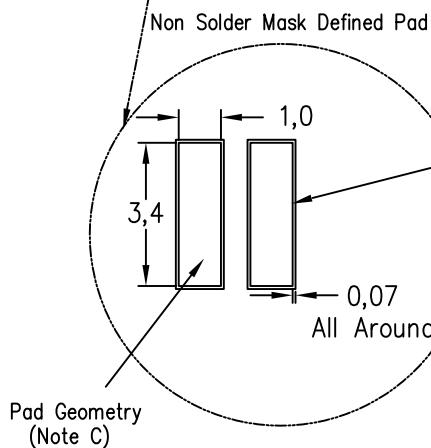
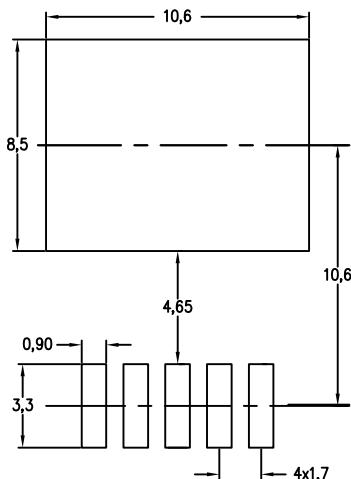
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.

$\Delta$  Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

Example Board Layout  
(Note C)Example Stencil Design  
(Note D)Example  
Solder Mask Opening  
(Note E)

4208208-3/C 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-SM-782 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated