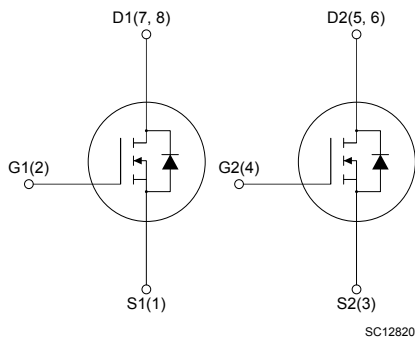
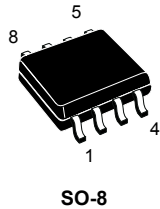


Dual N-channel 450 V, 4.1 Ω typ., 0.4 A SuperMESH Power MOSFET in a SO-8 package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS1DNC45	450 V	4.5 Ω	0.4 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance

Application

- Switch mode low-power supplies (SMPS)
- DC-DC converters
- Low power, low-cost CFL (compact fluorescent lamps)
- Low-power battery chargers

Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STS1DNC45](#)

Product summary

Order code	STS1DNC45
Marking	1DC45)
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	450	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	450	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	0.4	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.25	
$I_{DM}^{(1)}$	Drain current (pulsed)	1.6	A
P_{TOT}	Total power dissipation at $T_A = 25\text{ }^\circ\text{C}$, dual operation	1.6	W
	Total power dissipation at $T_A = 25\text{ }^\circ\text{C}$, single operation	2	
$dv/dt^{(2)}$	Peak diode recovery voltage slope	3	V/ns
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 0.4\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction-to-ambient, single operation	62.5	$^\circ\text{C}/\text{W}$
	Thermal resistance, junction-to-ambient, dual operation	78	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	0.4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	30	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	450			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 450\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 450\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.3	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$		4.1	4.5	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25\text{ V}$, $I_D = 0.5\text{ A}$	-	1.1		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	160		pF
C_{oss}	Output capacitance		-	27.5		pF
C_{rss}	Reverse transfer capacitance		-	4.7		pF
Q_g	Total gate charge	$V_{DD} = 360\text{ V}$, $I_D = 1.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	7	$10^{(2)}$	nC
Q_{gs}	Gate-source charge		-	1.3		nC
Q_{gd}	Gate-drain charge		-	3.2		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 225\text{ V}$, $I_D = 0.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	6.7	-	ns
t_r	Rise time		-	4	-	ns
$t_{r(off)}$	Turn-off rise time	$V_{DD} = 360\text{ V}$, $I_D = 1.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	8.5	-	ns
t_f	Fall time			12		ns
t_c	Cross-over time		-	18	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		1.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.4 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 0.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	225		ns
Q_{rr}	Reverse recovery charge		-	530		nC
I_{RRM}	Reverse recovery current		-	4.7		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

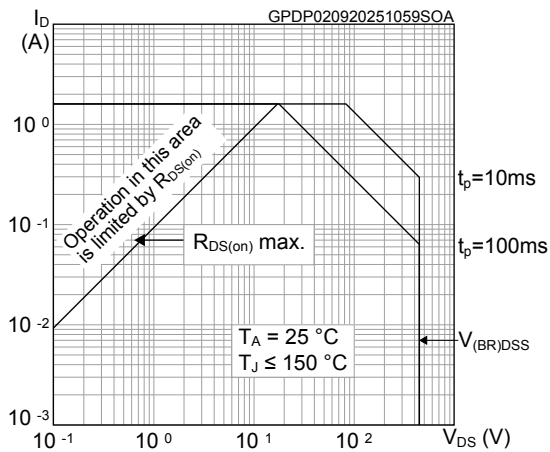


Figure 2. Normalized transient thermal impedance

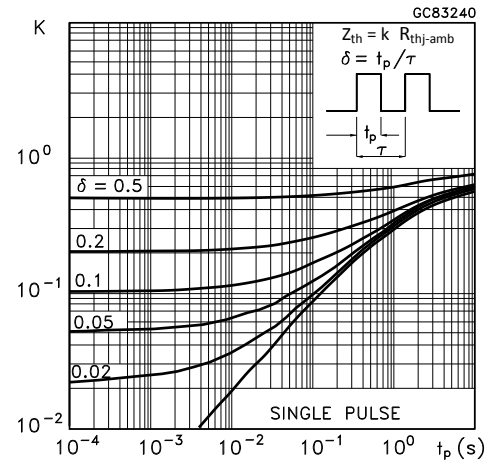


Figure 3. Typical output characteristics

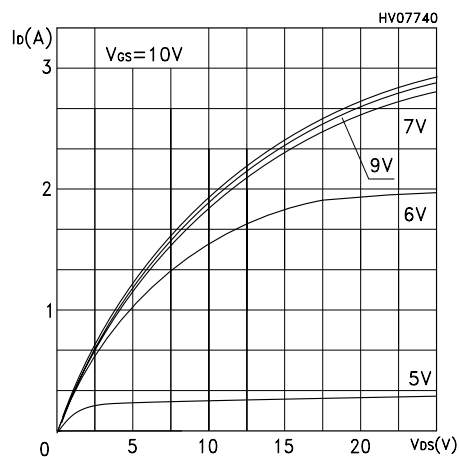


Figure 4. Typical transfer characteristics

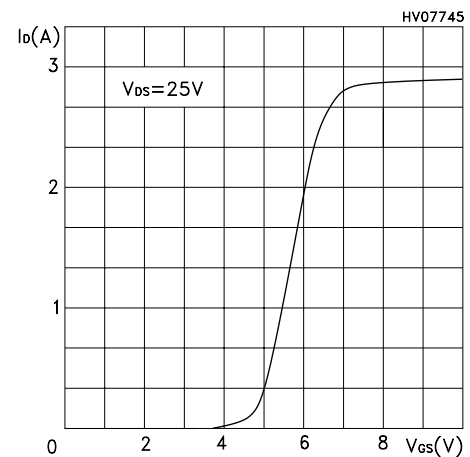


Figure 5. Typical transconductance characteristics

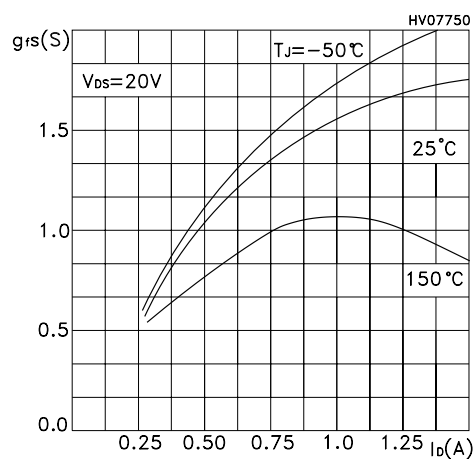


Figure 6. Typical gate charge characteristics

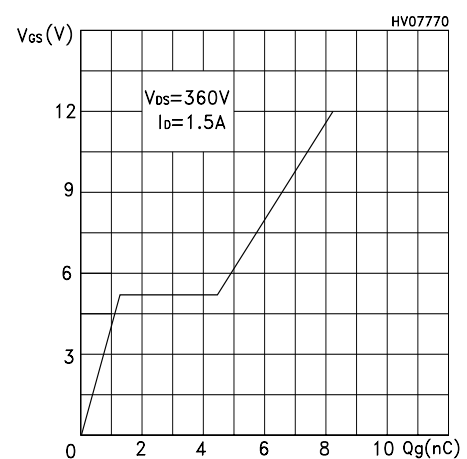


Figure 7. Typical capacitance characteristics

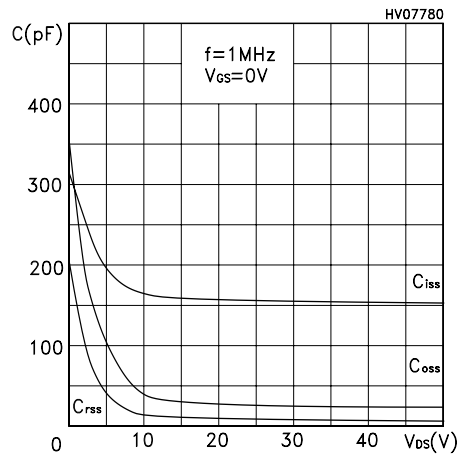


Figure 8. Typical drain-source on-resistance

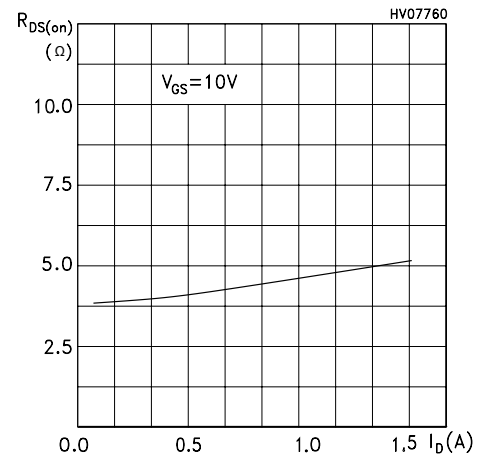


Figure 9. Normalized breakdown voltage vs temperature

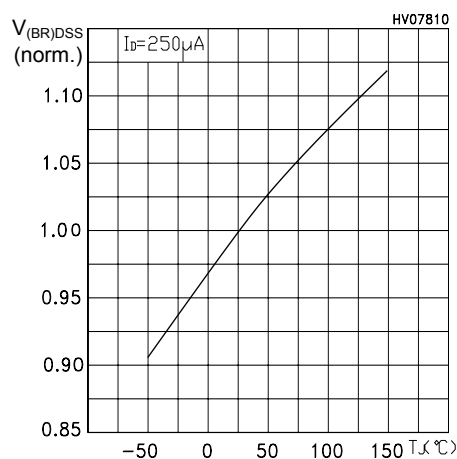


Figure 10. Normalized gate threshold vs temperature

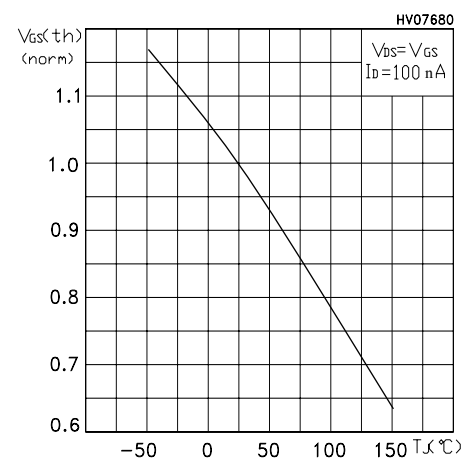


Figure 11. Normalized on-resistance vs temperature

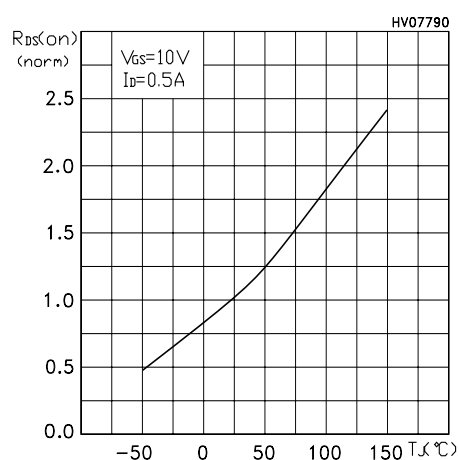


Figure 12. Typical reverse diode forward characteristics

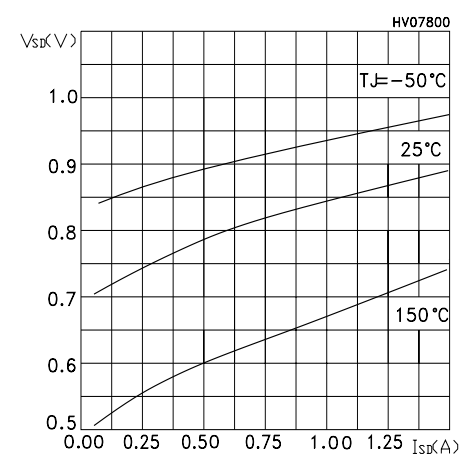


Figure 13. Maximum I_D current vs T_C

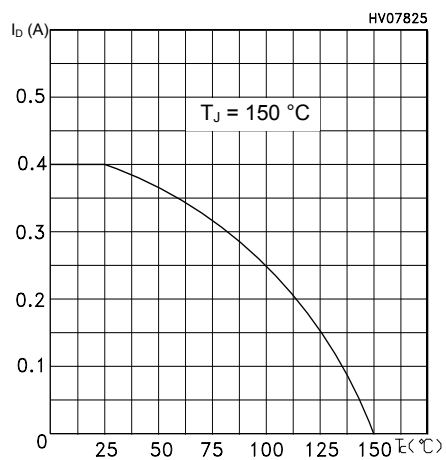
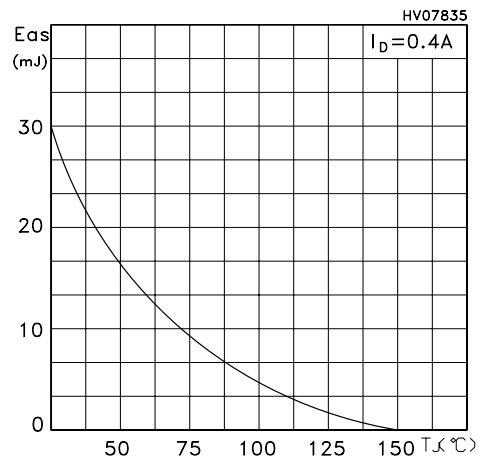
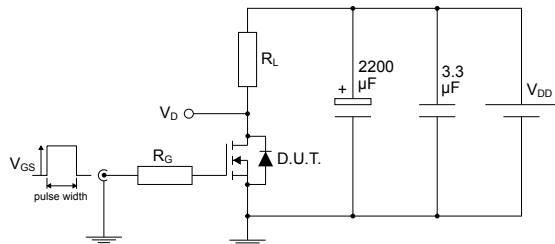


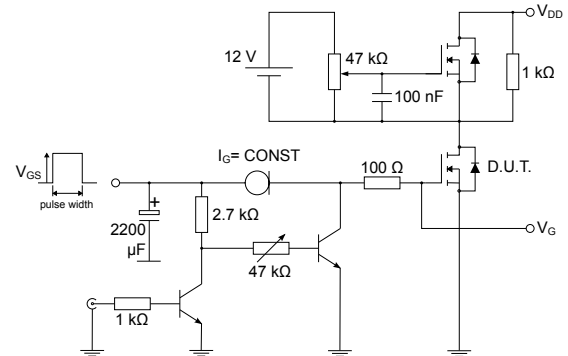
Figure 14. Maximum avalanche energy vs temperature



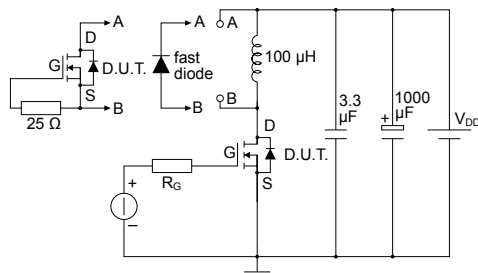
3 Test circuits

Figure 15. Test circuit for resistive load switching times


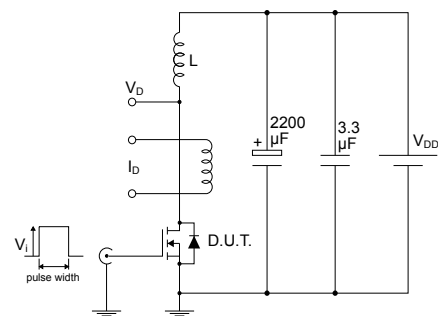
AM01468v1

Figure 16. Test circuit for gate charge behavior


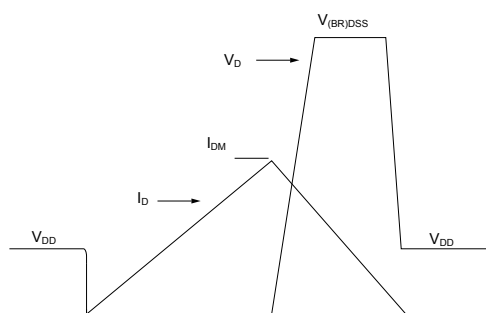
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Figure 17. Test circuit for inductive load switching and diode recovery times


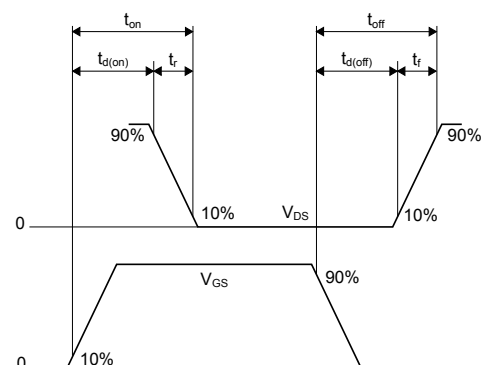
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Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


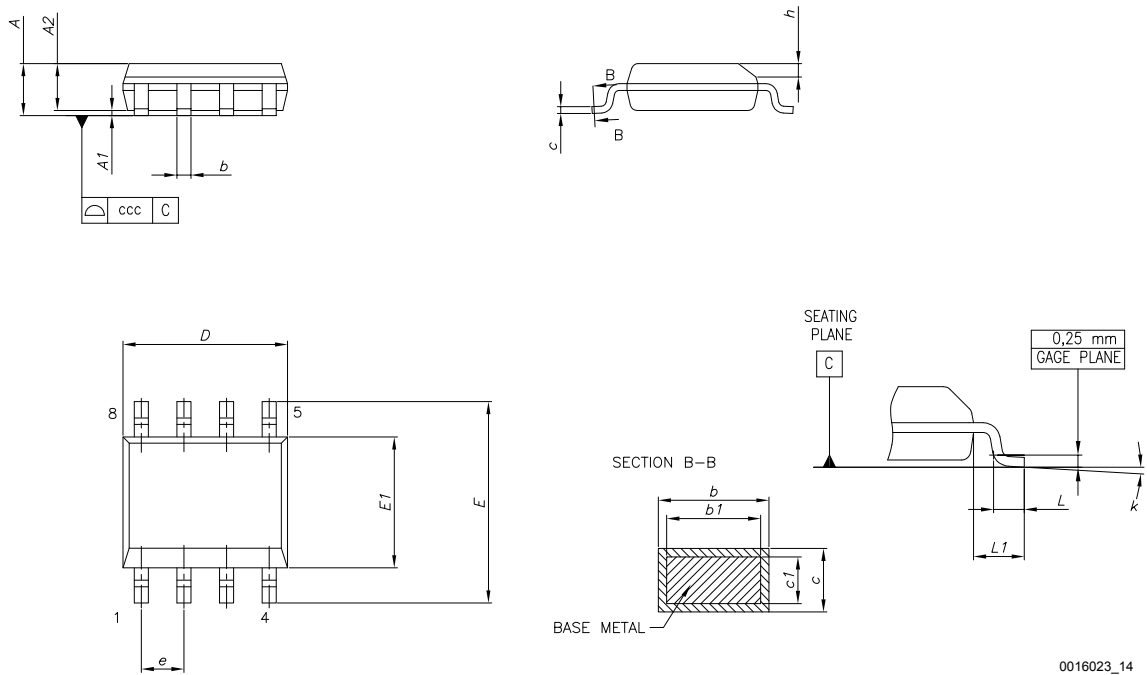
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

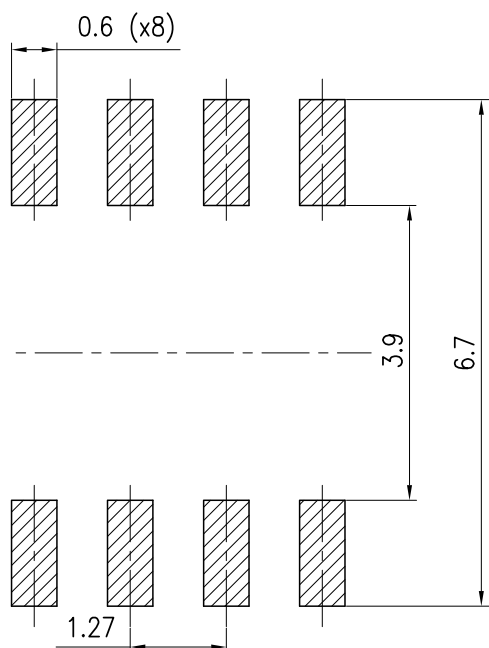
Figure 21. SO-8 package outline



0016023_14

Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 22. SO-8 recommended footprint (dimensions are in mm)


4.2 SO-8 packing information

Figure 23. SO-8 tape and reel dimensions

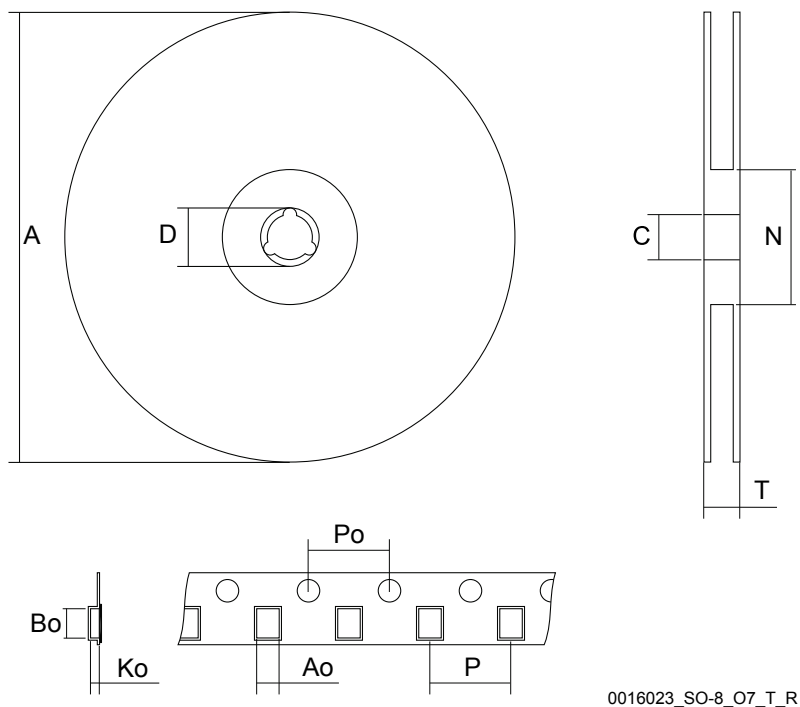


Figure 24. Tape orientation

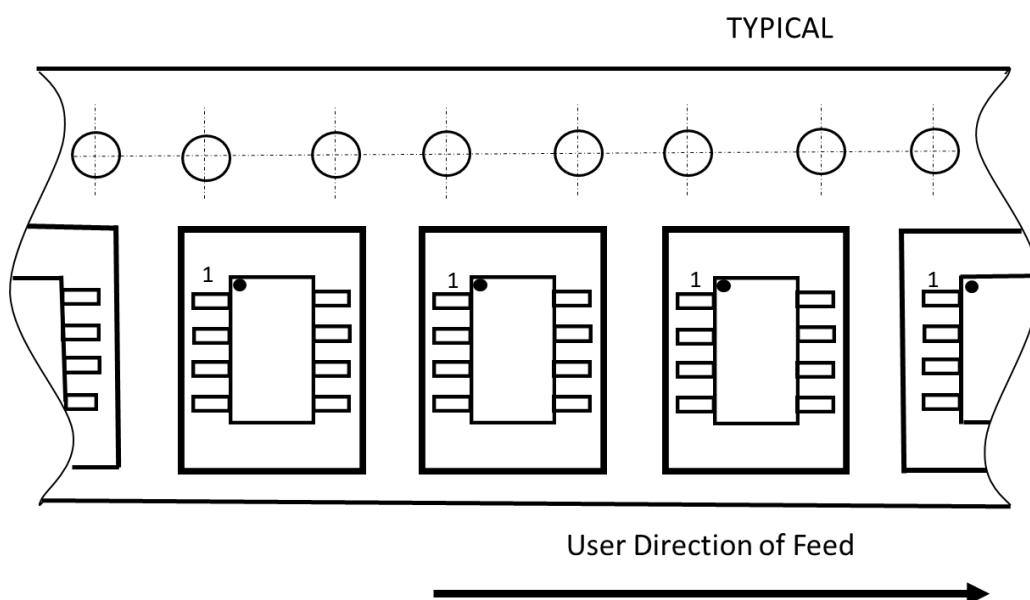


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5		6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Sep-2025	3	Updated Figure 1. Safe operating area. Updated Section 4: Package information. Minor text changes.

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