Bi-CMOS IC

LED Boost Driver with PWM Dimming



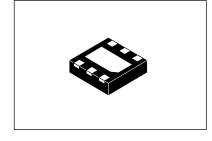
www.onsemi.com

Overview

The LV52205MU is a high voltage boost driver for LED drive. LED current is set by the external resistor R1 and LED dimming can be done by changing FB voltage with PWM control.

Feature

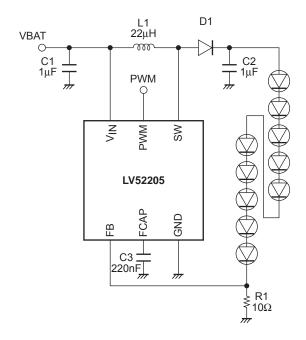
- Operating Voltage from 2.7V to 5.5V
- Integrated 42V MOSFET
- PWM dimming for Brightness Control
- 600kHz Switching Frequency



UDFN6 2×2, 0.65P

Typical Applications

• LED Display Backlight Control



ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	V _{CC}	5.5	V
Maximum pin voltage1	V1 max	SW	42	V
Maximum pin voltage2	V2 max	Other pin	5.5	V
Allowable power dissipation	Pd max	Ta = 25°C *1	2.05	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

^{*1} Mounted on a specified board: 70mm×50mm×1.2mm (4 layer glass epoxy)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommendation Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range1	V _{CC} op	VCC	2.7 to 5.5	V
PWM frequency	Fpwm		300 to 100k	Hz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics Analog block at Ta = 25°C, V_{CC} = 3.6V, unless otherwise specified

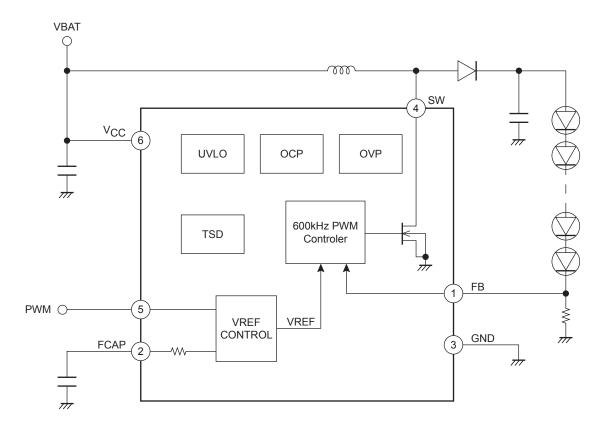
Davarantan	Ourshall Conditions	Ratings			l lait	
Parameter Symbol		Conditions	min	typ	max	Unit
Standby current dissipation	I _{CC} 1	SHUTDOWN		0	5	μА
DC/DC current dissipation	I _{CC} 2	V _{OUT} = 30V, I _{LED} = 20mA			1	mA
FB voltage	Vfb	PWM duty 100%	0.19	0.2	0.21	V
FB pin leak current	Ifb				1	μА
OVP voltage	Vovp	SW	40	41	42	V
SWOUT ON resistance	Ron	IL = 100mA		700		mΩ
NMOS switch current limit	ILIM	Vfb = 200mV		0.7		Α
OSC frequency	Fosc			600		kHz
High level input voltage	V _{IN} H	PWM	1.5		VCC	V
Low level input voltage	V _{IN} L	PWM	0		0.4	V
Under voltage lockout	Vuvlo	V _{IN} falling		2.2		V
PWM setup time from shutdown	Ton		20			us
PWM low time to shutdown	Toff		8.9			ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

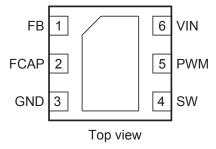
Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Block Diagram

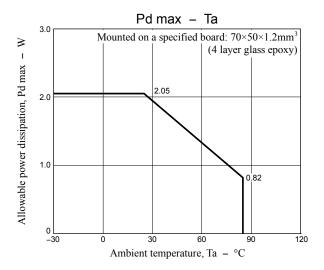


Pin Connections



Pin Function

PIN#	Pin Name	Description
1	FB	Feedback pin.
2	FCAP	Filtering capacitor terminal for PWM signal.
3	GND	Ground
4	SW	Switch pin. Drain of the internal power FET.
5	PWM	PWM dimming input (active High).
6	V _{CC}	Supply voltage.
	Expose-pad	Connect to GND on PCB.



LED Current Setting

LED current is set by an external resistor connected between the FB pin and ground.

$$I_{LED} = V_{FB}/R_{FB}$$
.

The V_{FB} can be controlled by PWM signal. PWM input is converted into a near DC current by the internal resistor R that was equivalent to $60k\Omega$ ($\pm 10\%$) and the external capacitor C_{FCAP} as a low pass filter with a cut-off frequency fc = $1/2\pi RC_{FCAP}$. The V_{FB} can be adjusted by altering the duty cycle of the PWM signal (See Fig.1).

$$V_{FB} = 200 \text{ (mV)} \times \text{PWM Duty (\%)}$$

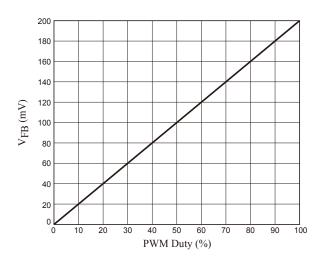


Fig1. VFB vs. PWM Duty

PWM Control

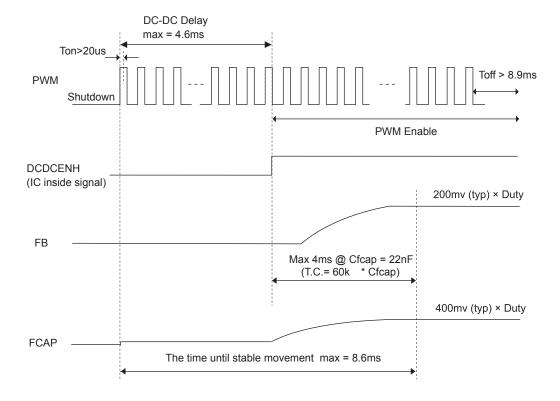


Fig2. Timing Diagram in PWM signal

Open LED Protection

If SW terminal voltage exceeds a threshold Vovp (41V typ) for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, PWM setup signal is required again.

Over Current Protection

Current limit value for built-in power MOS is around 0.7A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

Under Voltage Lock Out (UVLO)

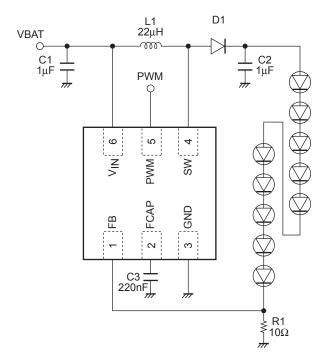
UVLO operation works when V_{IN} terminal voltage is below 2.2V.

Thermal Shutdown

When chip temperature is too high, boost converter is stopped.

Application Circuit Diagram

10LEDs

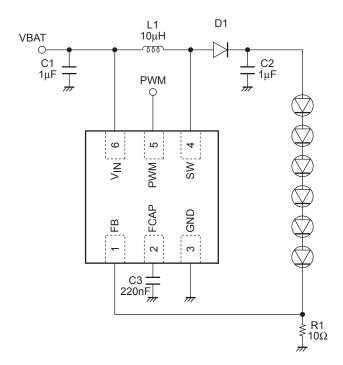


L1: VLS3012T-220M49 (TDK), VLF504015MT-220M (TDK)

D1: MBR0540T1 (ONsemi), NSR05F40 (ONsemi)

C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

6LEDs

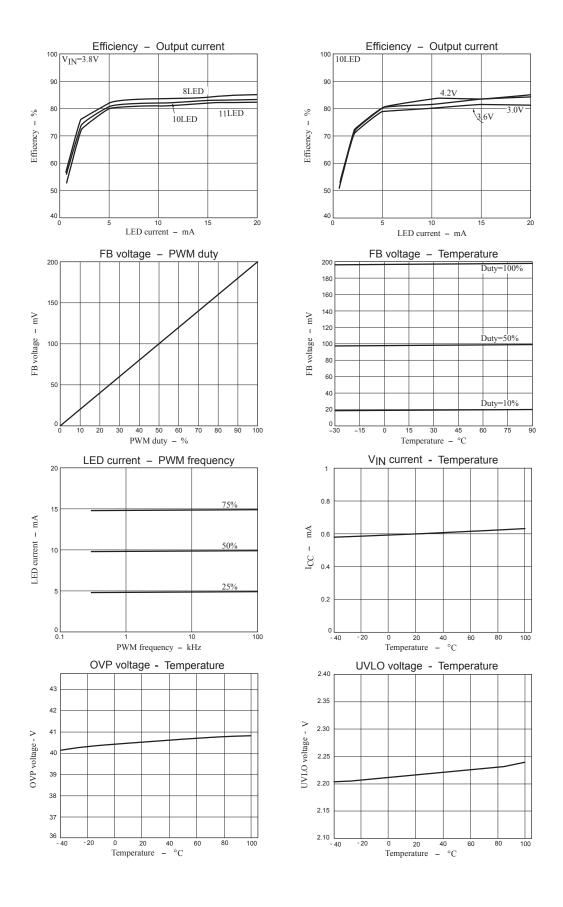


L1: VLS3012T-100M72 (TDK), VLF302512M-100M (TDK)

D1: MBR0540T1 (ONsemi), NSR05F40 (ONsemi)

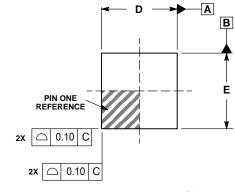
C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

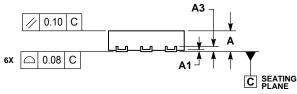
Typical Characteristics ($V_{IN} = 3.6V$, $L = 22\mu H$, T = 25°C, unless otherwise specified)

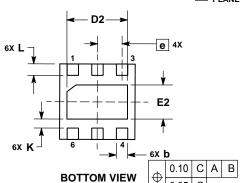


PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P CASE 517AB







0.05 С

- NOTES:

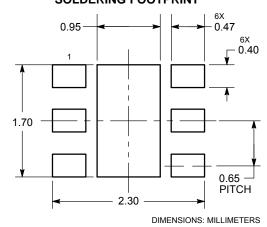
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS			
DIM	MIN MAX			
Α	0.45	0.55		
A1	0.00 0.05			
A3	0.127 REF			
b	0.25 0.35			
D	2.00 BSC			
D2	1.50 1.70			
E	2.00 BSC			
E2	0.80	1.00		
е	0.65 BSC			
K	0.20			
L	0.25 0.35			

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LV52205MU is as follows.

MARKING DIAGRAM



= Device Code T5

= Date Code

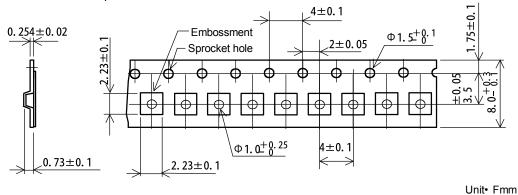
= Pb-Free Package

(Note: Microdot may be in either location)

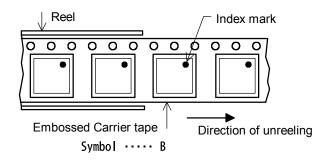
Packing Specification of Embossed Carrier Taping UDFN6 (2.0×2.0) 3,000 pcs/reel

1.EMBOSSED CARRIER TAPING

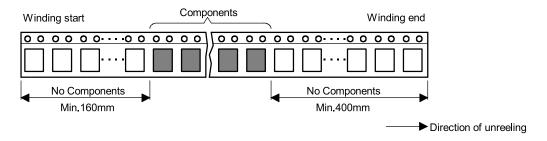
1 - 1. Embossed carrier tape dimensions



1 - 2 . Tape mounting direction



1 - 3 .Reel winding start and reel winding end



2.TAPE STRENGTH

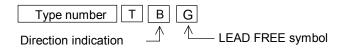
2 - 1 . Tensile strength of the carrier tape : Min. 10N

2 - 2 . Peel strength of the top cover tape

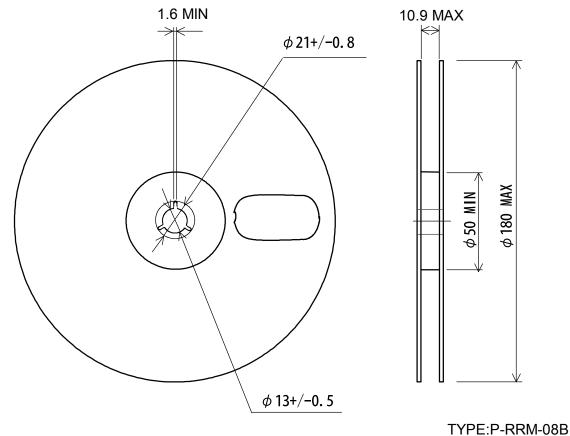
(a) Peel angle: 165° to 180° relative to the tape adhesive surface

(b)Peel rate: 300mm / minute (c)Peel of strength: 0.1N to 1.0N

3 .PARTS No. ON BAR CODE LABEL

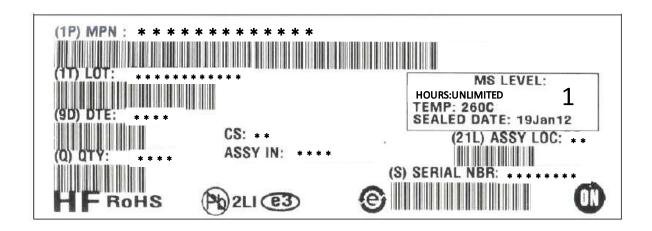


4.REEL DIMENSIONS

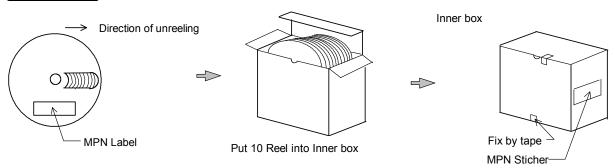


Carrier tape type number	SANYO Package code	Maximum number of ICs contained (pcs.)		Packing form
		Reel	Inner box	Inner box. B50766P001
N22986D001	UDFN6(2.0*2.0)	3,000	30,000	10 Reels contained Dimensions:mm 190 × 136 × 186

MPN Label



Packing Method



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV52205MUTBG	UDFN6 (2x2) (Pb-Free)	3000 / Tape & Reel

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent re