

NTMFD4C20N

MOSFET – Power, Dual, N-Channel, SO8FL

30 V, High Side 18 A / Low Side 27 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

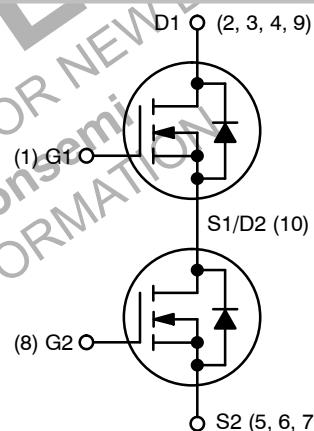
- DC-DC Converters
- System Voltage Rails
- Point of Load



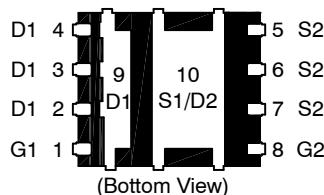
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
Q1 Top FET 30 V	7.3 m Ω @ 10 V	18 A
	10.8 m Ω @ 4.5 V	
Q2 Bottom FET 30 V	3.4 m Ω @ 10 V	27 A
	5.2 m Ω @ 4.5 V	



PIN CONNECTIONS



MARKING DIAGRAM



4C20N = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTMFD4C20N

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Drain-to-Source Voltage					
Gate-to-Source Voltage	V_{GS}	± 20	V		
Gate-to-Source Voltage					
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	12	A
		$T_A = 85^\circ\text{C}$		8.6	
		$T_A = 25^\circ\text{C}$	I_D	18	
		$T_A = 85^\circ\text{C}$		13	
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^\circ\text{C}$	P_D	1.88	W
		$T_A = 85^\circ\text{C}$		1.97	
Continuous Drain Current $R_{\theta JA} \leq 10 \text{ s}$ (Note 1)		$T_A = 25^\circ\text{C}$	I_D	18.2	A
		$T_A = 85^\circ\text{C}$		13.1	
		$T_A = 25^\circ\text{C}$		27.4	
		$T_A = 85^\circ\text{C}$		19.8	
Power Dissipation $R_{\theta JA} \leq 10 \text{ s}$ (Note 1)		$T_A = 25^\circ\text{C}$	P_D	4.37	W
		$T_A = 85^\circ\text{C}$		4.6	
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$	I_D	9.1	A
		$T_A = 85^\circ\text{C}$		6.6	
		$T_A = 25^\circ\text{C}$		13.7	
		$T_A = 85^\circ\text{C}$		9.9	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$	P_D	1.09	W
		$T_A = 85^\circ\text{C}$		1.15	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$	Q1	I_{DM}	55	A
		Q2		82	
Operating Junction and Storage Temperature	Q1	T_J, T_{STG}		-55 to +150	°C
Source Current (Body Diode)	Q1	I_S		4.0	A
				4.2	
Drain to Source DV/DT		dV/dt		6	V/ns
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $L = 0.1 \text{ mH}$, $R_G = 25 \Omega$)	$I_L = 18 \text{ A}_{\text{pk}}$	Q1	EAS	16	mJ
		Q2	EAS	42	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	FET	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	Q1	$R_{\theta JA}$	66.5	$^{\circ}\text{C}/\text{W}$
	Q2		63.3	
Junction-to-Ambient – Steady State (Note 4)	Q1	$R_{\theta JA}$	114.3	$^{\circ}\text{C}/\text{W}$
	Q2		108.7	
Junction-to-Ambient – ($t \leq 10 \text{ s}$) (Note 3)	Q1	$R_{\theta JA}$	28.6	$^{\circ}\text{C}/\text{W}$
	Q2		27.2	
Junction-to-Case – (Drain)	Q1	$R_{\theta JC}$	5.4	$^{\circ}\text{C}/\text{W}$
	Q2		3.7	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
 4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	Q1	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
	Q2		$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	30			
Drain-to-Source Breakdown Voltage Temperature Coefficient	Q1	$V_{(BR)DSS}/T_J$			14.5		mV/ $^{\circ}\text{C}$
	Q2				12		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	$V_{GS} = 0 \text{ V}, V_{DS} = 24 \text{ V}$	$T_J = 25^{\circ}\text{C}$		1	μA
	Q2		$V_{GS} = 0 \text{ V}, V_{DS} = 24 \text{ V}$	$T_J = 125^{\circ}\text{C}$		10	
Gate-to-Source Leakage Current	Q1	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
	Q2					± 100	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.3		2.1	V
	Q2			1.3		2.1	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)}/T_J$			4.7		mV/ $^{\circ}\text{C}$
	Q2				5.1		
Drain-to-Source On Resistance	Q1	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$	5.8	7.3	$\text{m}\Omega$
			$V_{GS} = 4.5 \text{ V}$	$I_D = 10 \text{ A}$	8.7	10.8	
	Q2		$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$	2.7	3.4	
			$V_{GS} = 4.5 \text{ V}$	$I_D = 20 \text{ A}$	4.0	5.2	
Forward Transconductance	Q1	g_{FS}	$V_{DS} = 1.5 \text{ V}, I_D = 10 \text{ A}$		43		S
	Q2				68		

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit	
CHARGES, CAPACITANCES & GATE RESISTANCE								
Input Capacitance	Q1	C_{ISS}	$V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}, V_{DS} = 15 \text{ V}$		970		pF	
	Q2				1950			
Output Capacitance	Q1	C_{OSS}			430		pF	
	Q2				990			
Reverse Capacitance	Q1	C_{RSS}			125		pF	
	Q2				50			
Total Gate Charge	Q1	$Q_{G(TOT)}$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}; I_D = 10 \text{ A}$		9.3		nC	
	Q2				13			
Threshold Gate Charge	Q1	$Q_{G(TH)}$			1.6			
	Q2				3.3			
Gate-to-Source Charge	Q1	Q_{GS}			3.3		nC	
	Q2				6.0			
Gate-to-Drain Charge	Q1	Q_{GD}			4.2		nC	
	Q2				3.0			
Total Gate Charge	Q1	$Q_{G(TOT)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 15 \text{ V}; I_D = 10 \text{ A}$		19		nC	
	Q2				29			
SWITCHING CHARACTERISTICS (Note 6)								
Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}, I_D = 15 \text{ A}, R_G = 3.0 \Omega$		9.0		ns	
	Q2				11			
Rise Time	Q1	t_r			33			
	Q2				32			
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			15			
	Q2				20			
Fall Time	Q1	t_f			5.0			
	Q2				5.0			
SWITCHING CHARACTERISTICS (Note 6)								
Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 15 \text{ V}, I_D = 15 \text{ A}, R_G = 3.0 \Omega$		6.0		ns	
	Q2				8.0			
Rise Time	Q1	t_r			26			
	Q2				26			
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			18			
	Q2				25			
Fall Time	Q1	t_f			4.0			
	Q2				4.0			
DRAIN-SOURCE DIODE CHARACTERISTICS								
Forward Voltage	Q1	V_{SD}	$V_{GS} = 0 \text{ V}, I_S = 3 \text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.0	V
	Q2			$T_J = 125^\circ\text{C}$		0.62		
	Q1		$V_{GS} = 0 \text{ V}, I_S = 3 \text{ A}$	$T_J = 25^\circ\text{C}$		0.45	0.70	
	Q2			$T_J = 125^\circ\text{C}$		0.37		

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit	
DRAIN-SOURCE DIODE CHARACTERISTICS								
Reverse Recovery Time	Q1	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		23		ns	
	Q2				38			
Charge Time	Q1	t _a			11.6		ns	
	Q2				18.6			
Discharge Time	Q1	t _b			11.4		ns	
	Q2				19.4			
Reverse Recovery Charge	Q1	Q _{RR}			10		nC	
	Q2				25			

PACKAGE PARASITIC VALUES

Source Inductance	Q1	L _S	T _A = 25°C		0.38		nH	
	Q2				0.65			
Drain Inductance	Q1	L _D			0.054		nH	
	Q2				0.007			
Gate Inductance	Q1	L _G			1.5		nH	
	Q2				1.5			
Gate Resistance	Q1	R _G		0.3	1.0	2.0	Ω	
	Q2			0.3	1.0	2.0		

5. Pulse Test: pulse width \leq 300 μs, duty cycle \leq 2%.

6. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFD4C20NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

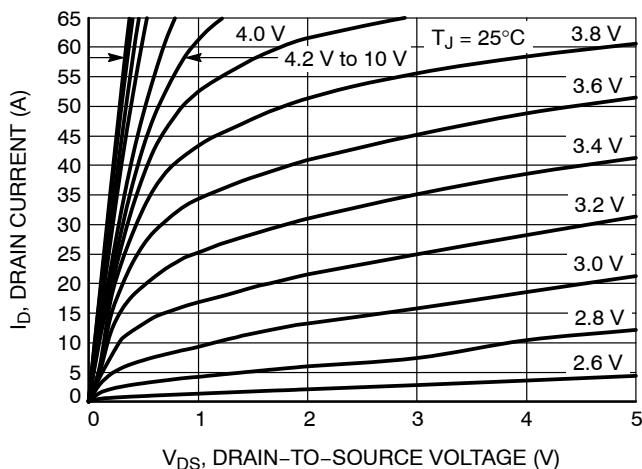


Figure 1. On-Region Characteristics

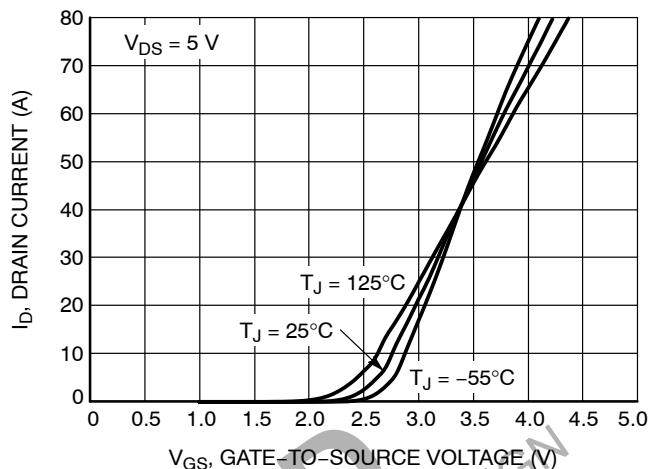


Figure 2. Transfer Characteristics

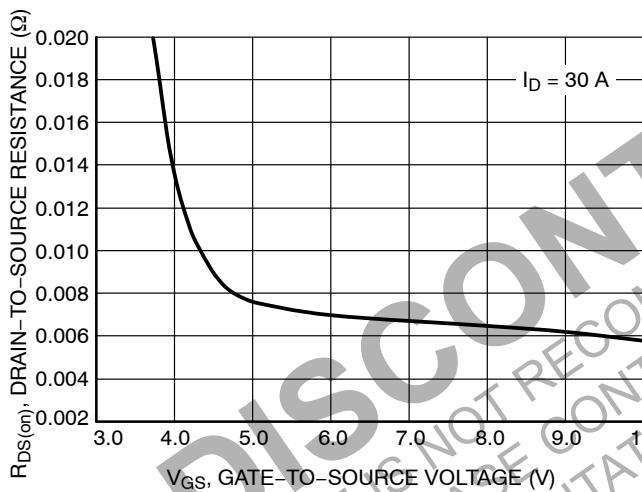
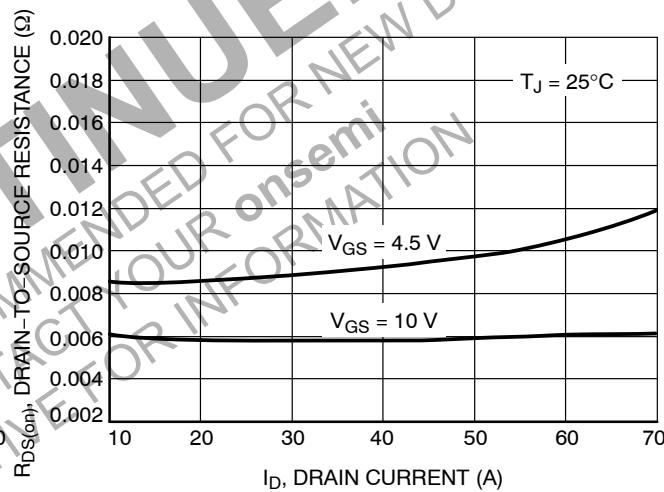
Figure 3. On-Resistance vs. V_{GS} 

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

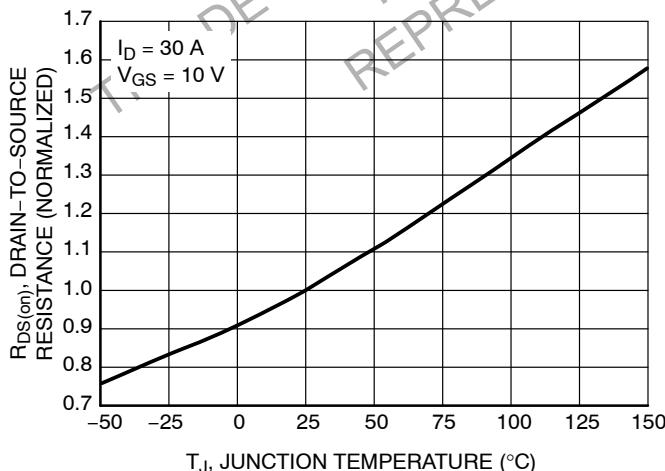


Figure 5. On-Resistance Variation with Temperature

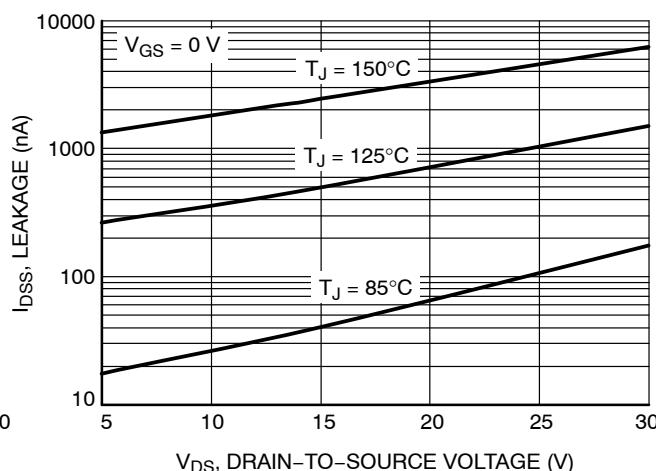
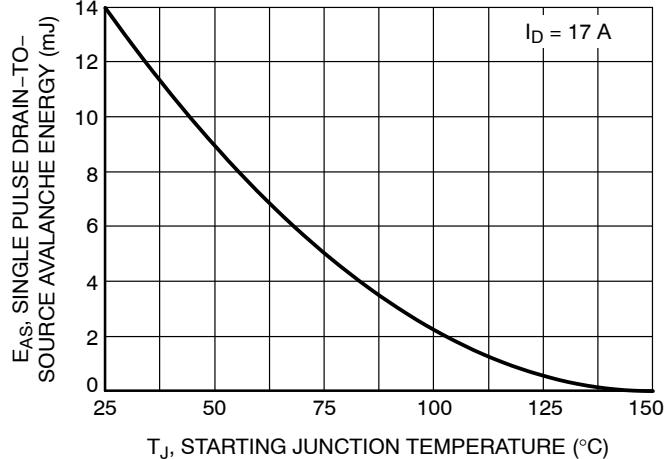
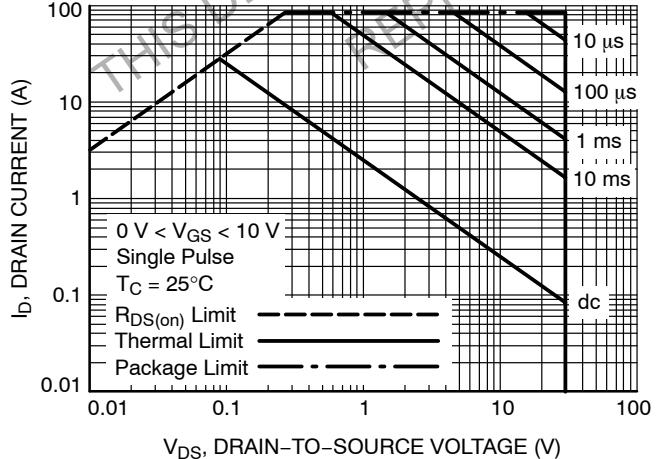
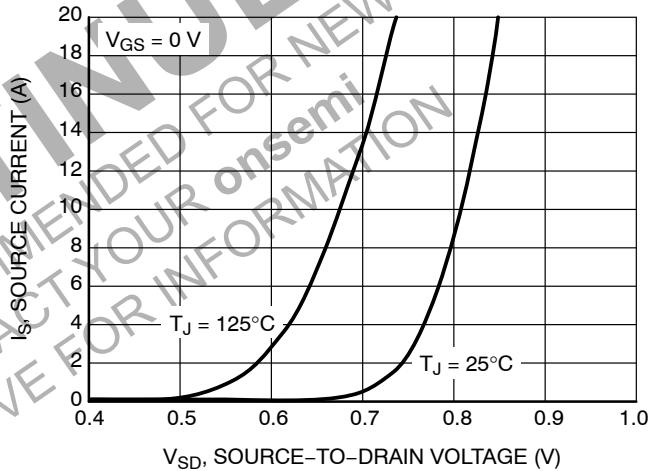
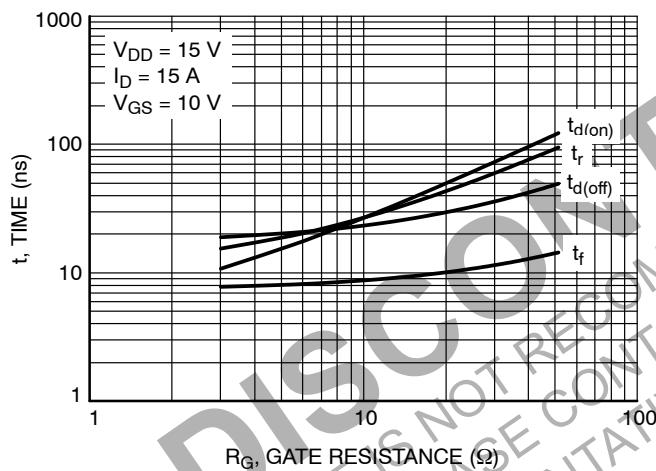
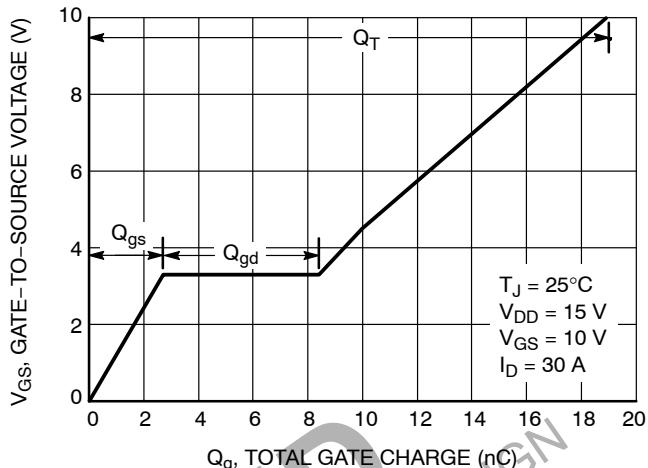
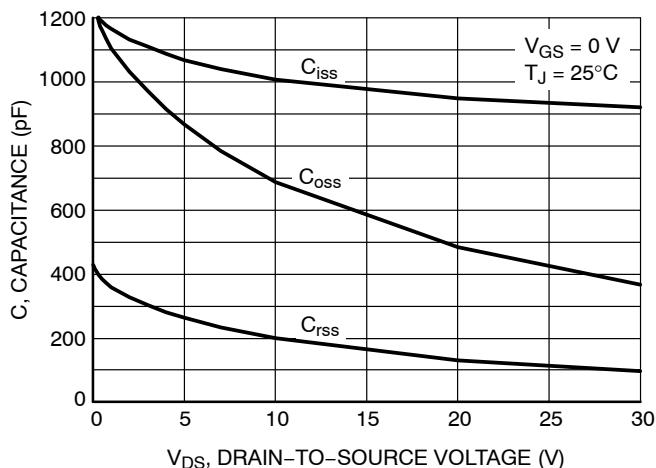


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1



TYPICAL CHARACTERISTICS – Q1

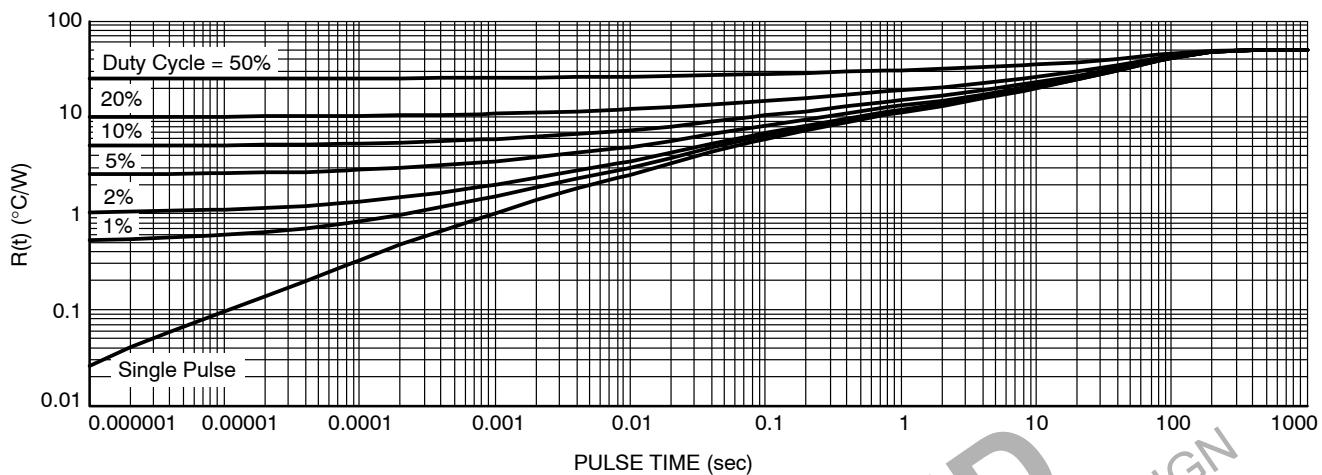


Figure 13. Thermal Response

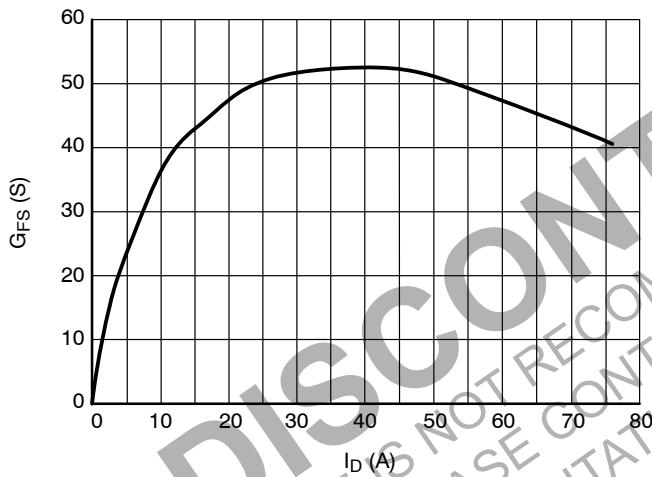
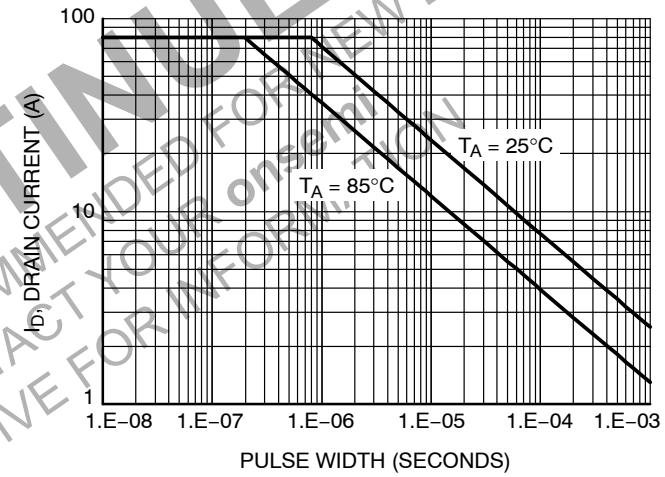
Figure 14. G_{FS} vs. I_D 

Figure 15. Avalanche Characteristics

TYPICAL CHARACTERISTICS – Q2

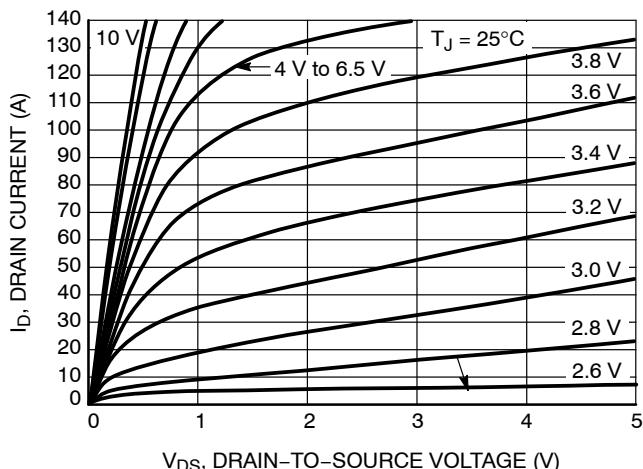


Figure 16. On-Region Characteristics

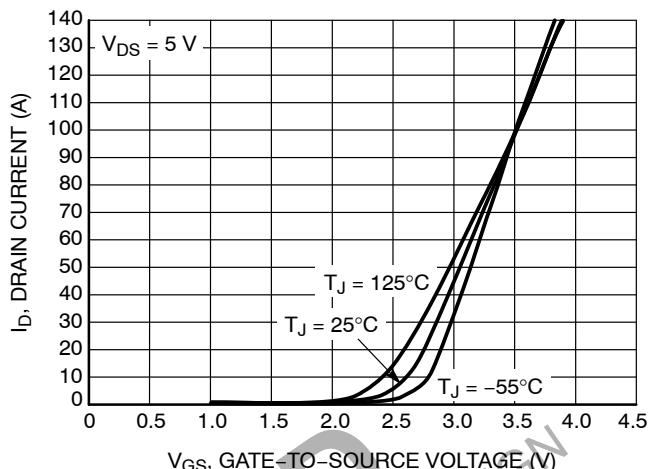


Figure 17. Transfer Characteristics

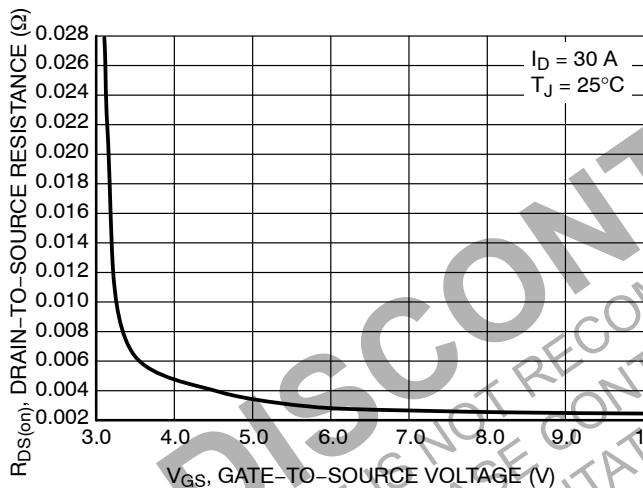
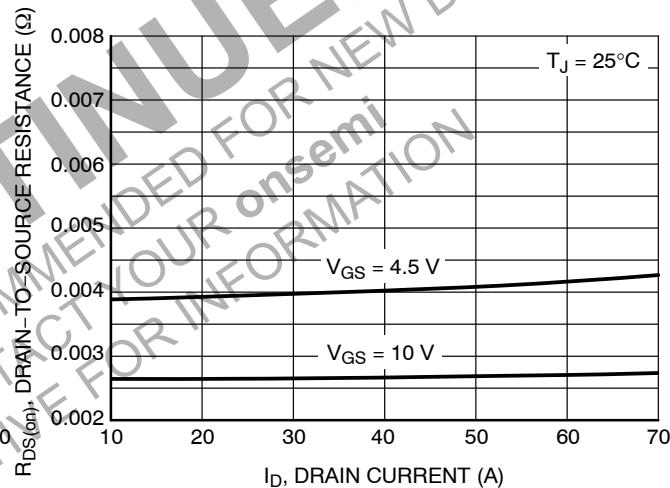
Figure 18. On-Resistance vs. V_{GS} 

Figure 19. On-Resistance vs. Drain Current and Gate Voltage

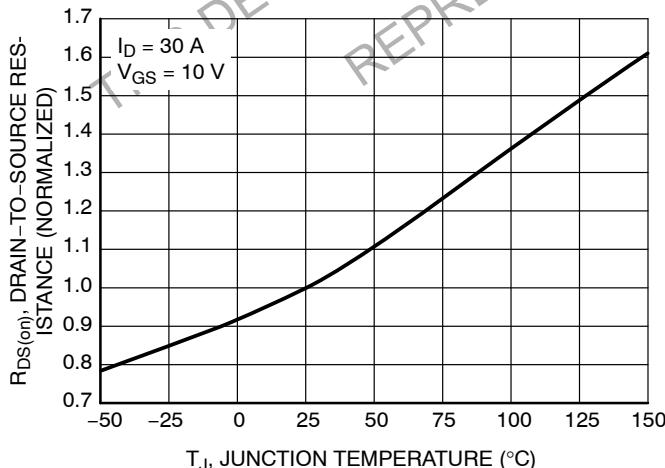


Figure 20. On-Resistance Variation with Temperature

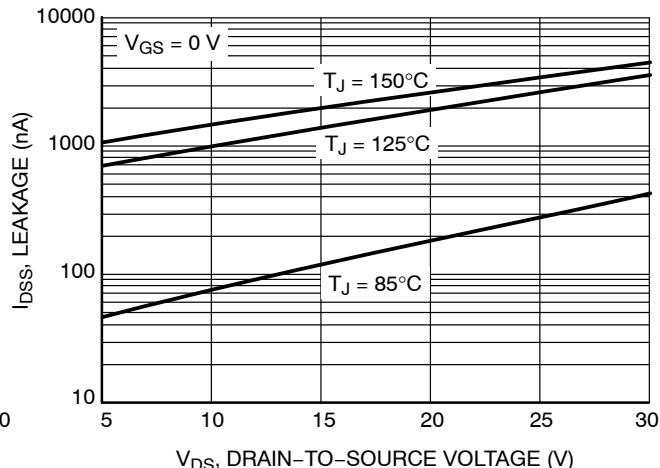


Figure 21. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

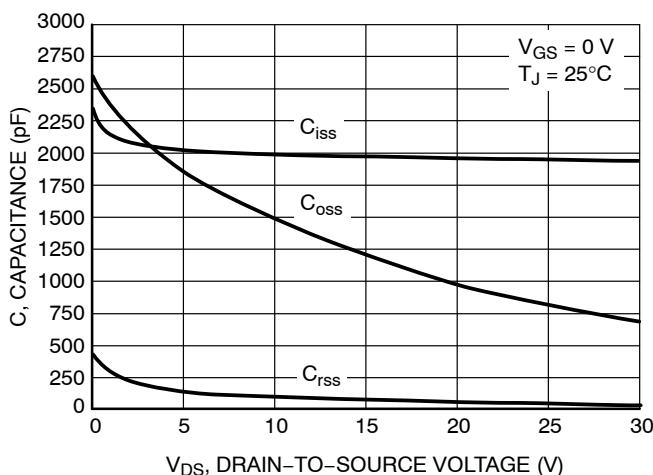


Figure 22. Capacitance Variation

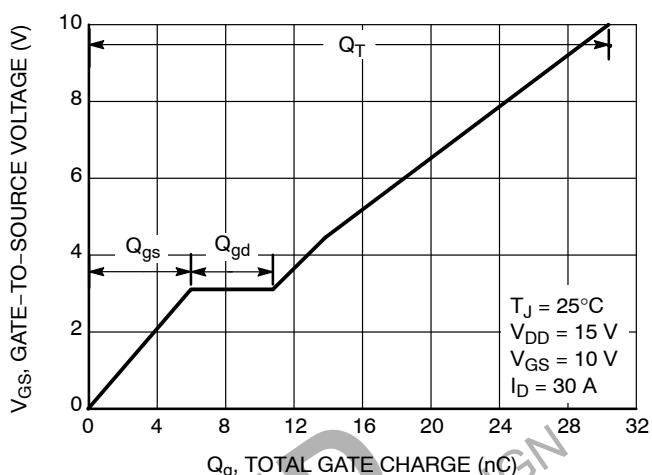


Figure 23. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

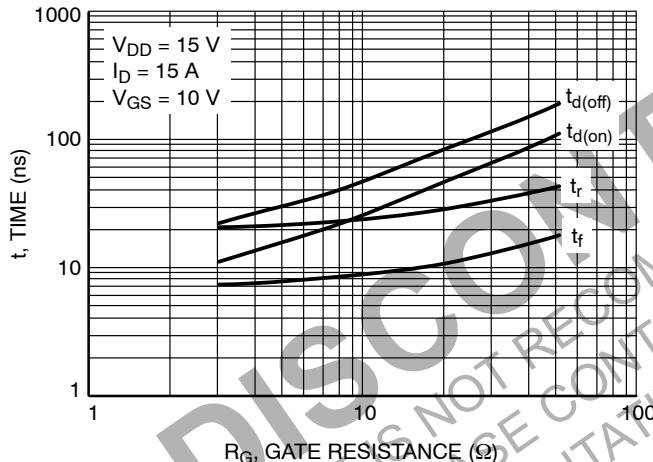


Figure 24. Resistive Switching Time Variation vs. Gate Resistance

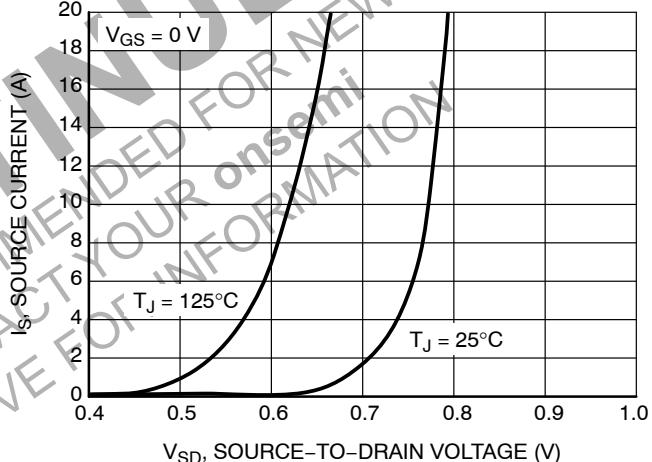


Figure 25. Diode Forward Voltage vs. Current

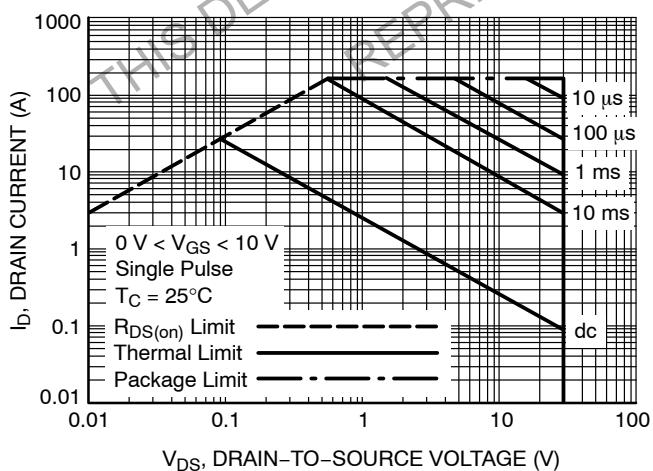


Figure 26. Maximum Rated Forward Biased Safe Operating Area

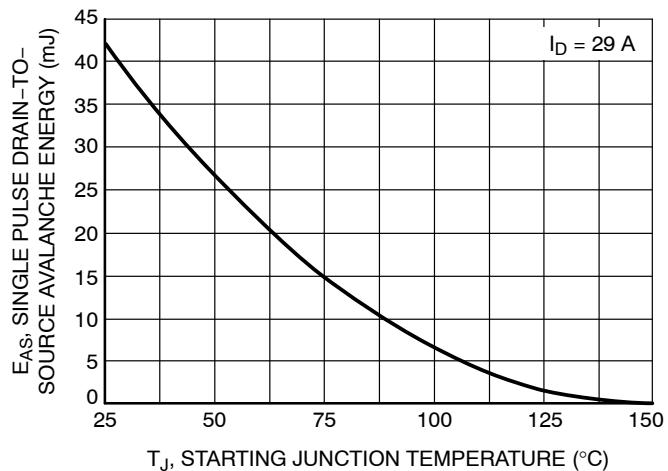


Figure 27. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS – Q2

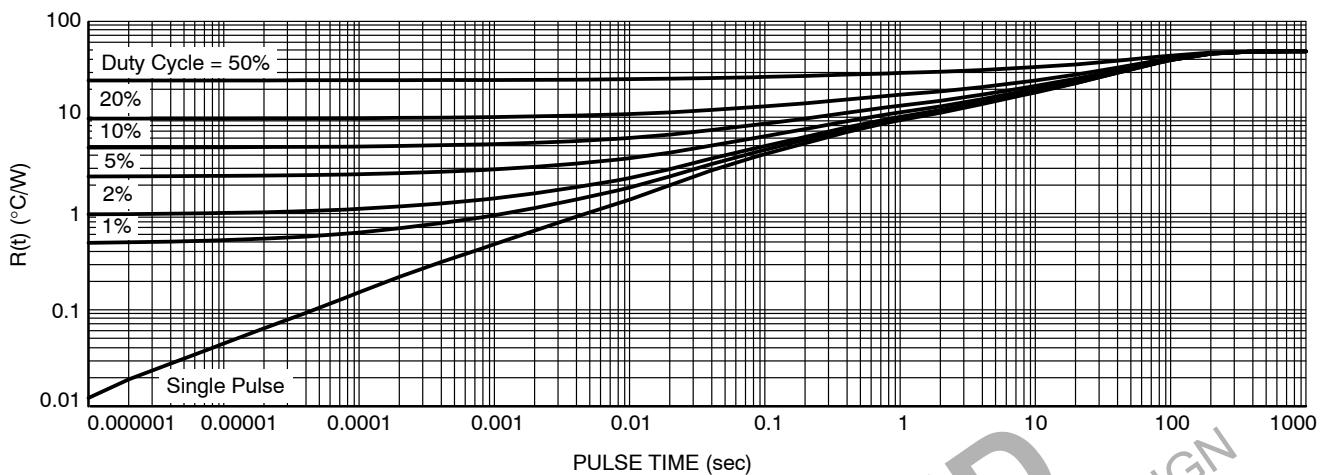


Figure 28. Thermal Response

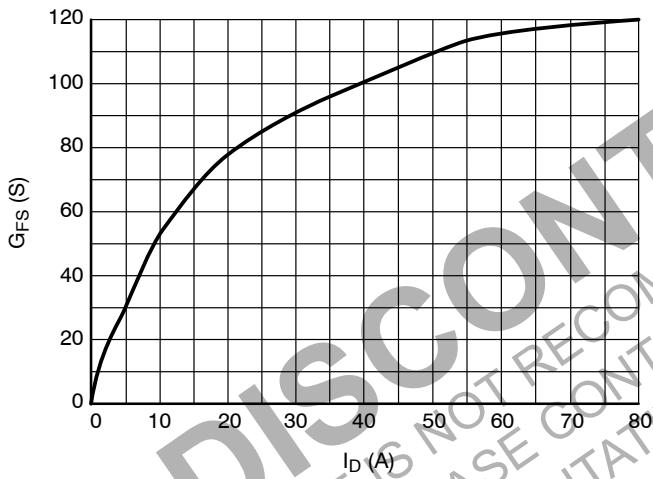
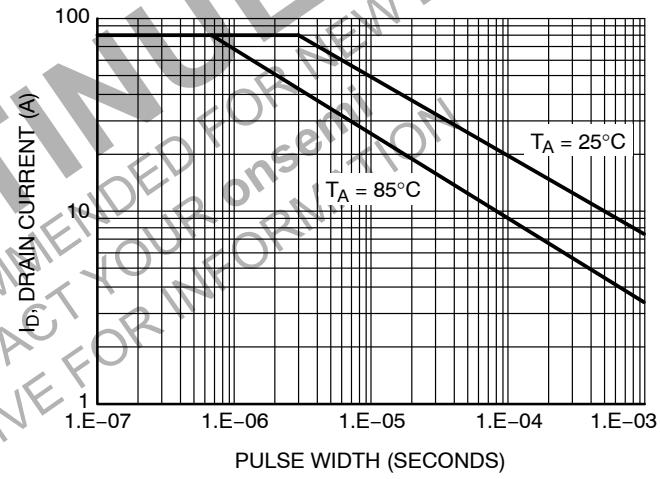
Figure 29. G_{FS} vs. I_D 

Figure 30. Avalanche Characteristics



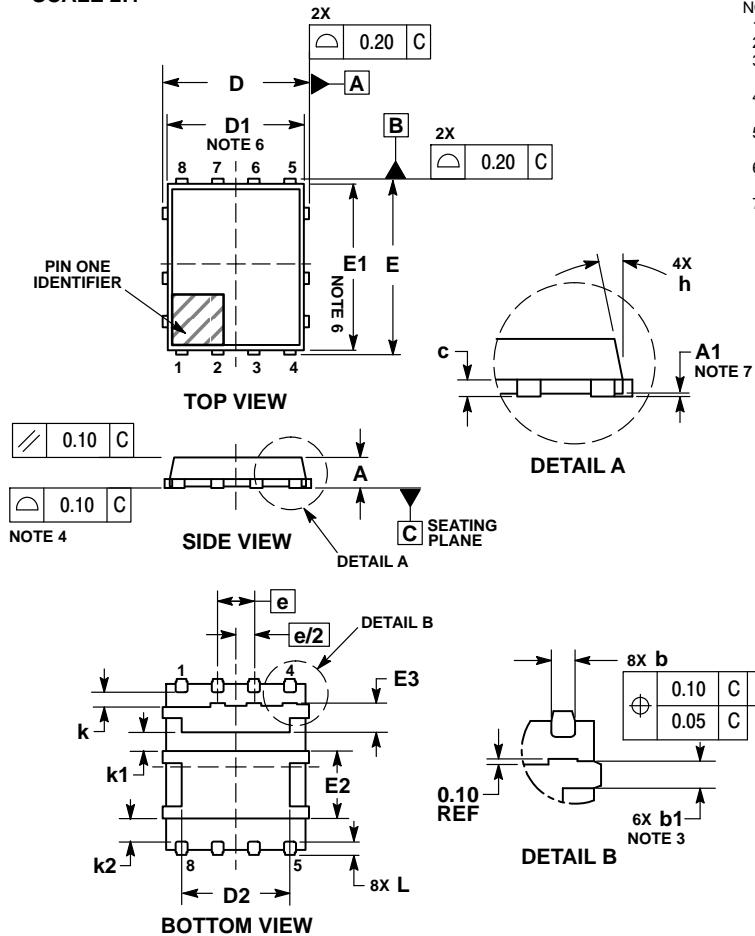
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual-Asymmetrical)

CASE 506BX

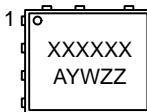
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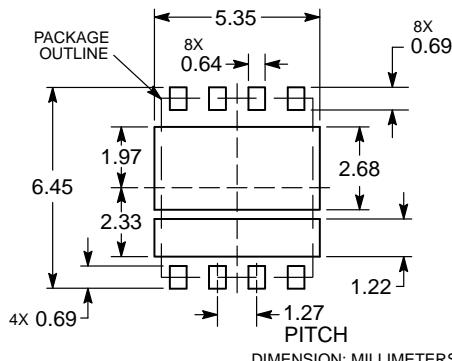
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS b AND L ARE MEASURED AT THE PACKAGE SURFACE
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
7. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

GENERIC
MARKING DIAGRAM*

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED
SOLDERING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON54291E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL-ASYMMETRICAL)	PAGE 1 OF 1

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