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FAIRCHILD SEMICONDUCTOR®

June 1993
Revised April 2005

74LVX373
Low Voltage Octal Transparent Latch with 3-STATE Outputs

General Description

The LVX373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

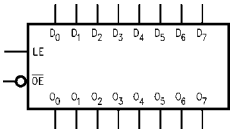
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

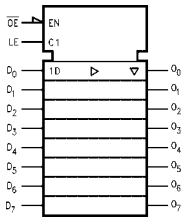
Order Number	Package Number	Package Description
74LVX373M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX373SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDED J-STD-020B.

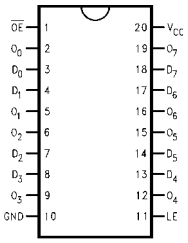
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Latch Outputs

Truth Table

Inputs			Outputs
LE	**$\overline{OE}$**	**D_n**	**O_n**
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

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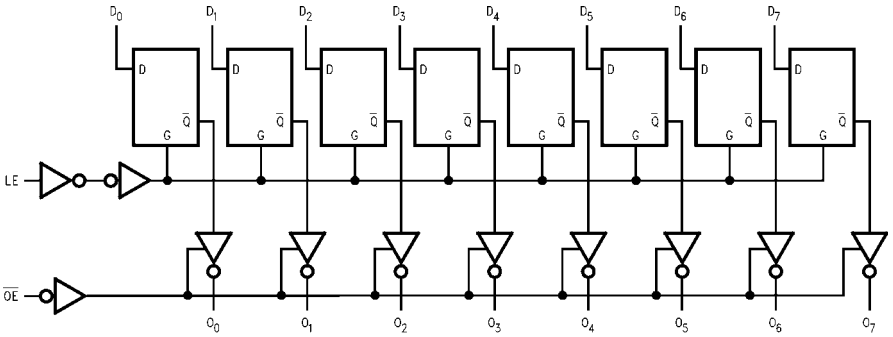
Functional Description

The LVX373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level	2.0	1.5			1.5				
	Input Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
V_{IL}	LOW Level	2.0			0.5		0.5			
	Input Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9			V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
	Output Voltage	3.0	2.9	3.0		2.9		V		I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
	Output Voltage	3.0		0.0	0.1		0.1	V		I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{OZ}	3-STATE Output	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}	
	Off-State Current								V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

Note 3: Input t_r = t_f = 3 ns.

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AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Time	2.7		7.7	15.0	1.0	18.5	ns	$C_L = 15$ pF
t_{PHL}	D_n to O_n			10.2	18.5	1.0	22.0		$C_L = 50$ pF
		3.3 ± 0.3		6.0	9.7	1.0	11.5		$C_L = 15$ pF
				8.5	13.2	1.0	15.0		$C_L = 50$ pF
t_{PLH}	Propagation Delay Time	2.7		7.5	14.5	1.0	17.5	ns	$C_L = 15$ pF
t_{PHL}	LE to O_n			10.0	18.0	1.0	21.0		$C_L = 50$ pF
		3.3 ± 0.3		5.8	9.3	1.0	11.0		$C_L = 15$ pF
				8.3	12.8	1.0	14.5		$C_L = 50$ pF
t_{PZL}	3-STATE Output	2.7		7.7	15.0	1.0	18.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
t_{PZH}	Enable Time			10.2	18.5	1.0	22.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ± 0.3		6.0	9.7	1.0	11.5		$C_L = 15$ pF, $R_L = 1$ kΩ
				8.5	13.2	1.0	15.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ}	3-STATE Output	2.7		9.8	18.0	1.0	21.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PHZ}	Disable Time	3.3 ± 0.3		8.2	12.8	1.0	14.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_W	LE Pulse Width, HIGH	2.7	6.5			7.5		ns	
		3.3 ± 0.3	5.0			5.0			
t_S	Setup Time, D_n to LE	2.7	6.0			6.0		ns	
		3.3 ± 0.3	4.0			4.0			
t_H	Hold Time, D_n to LE	2.7	1.0			1.0		ns	
		3.3 ± 0.3	1.0			1.0			
t_{OSLH}	Output to Output Skew	2.7			1.5		1.5	ns	$C_L = 50$ pF
t_{OSHL}	(Note 4)	3.3			1.5		1.5		

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 5)		27				pF

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per Latch)}}$

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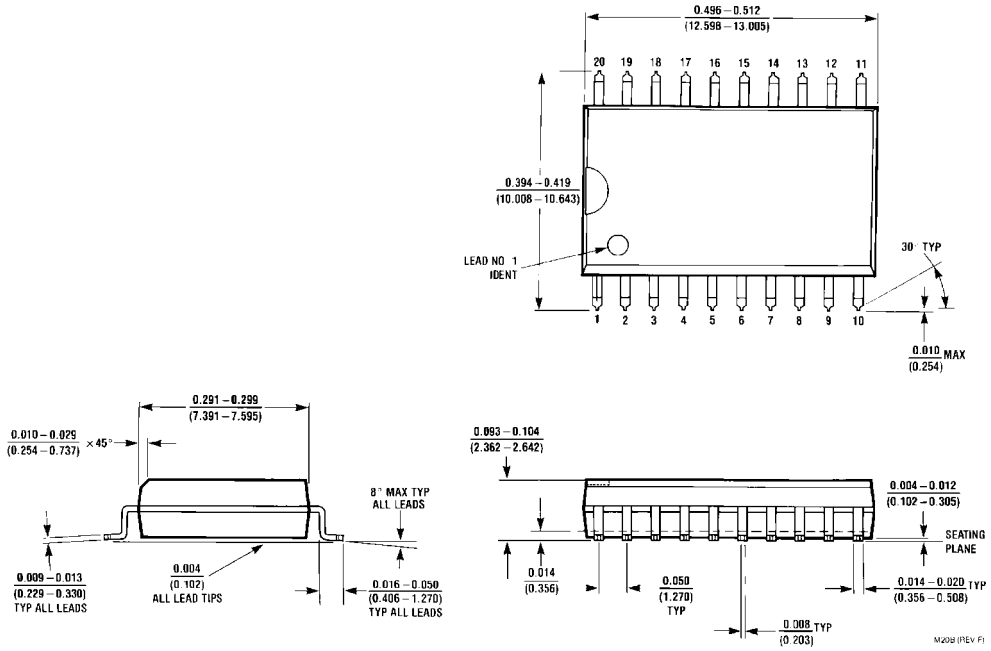
Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

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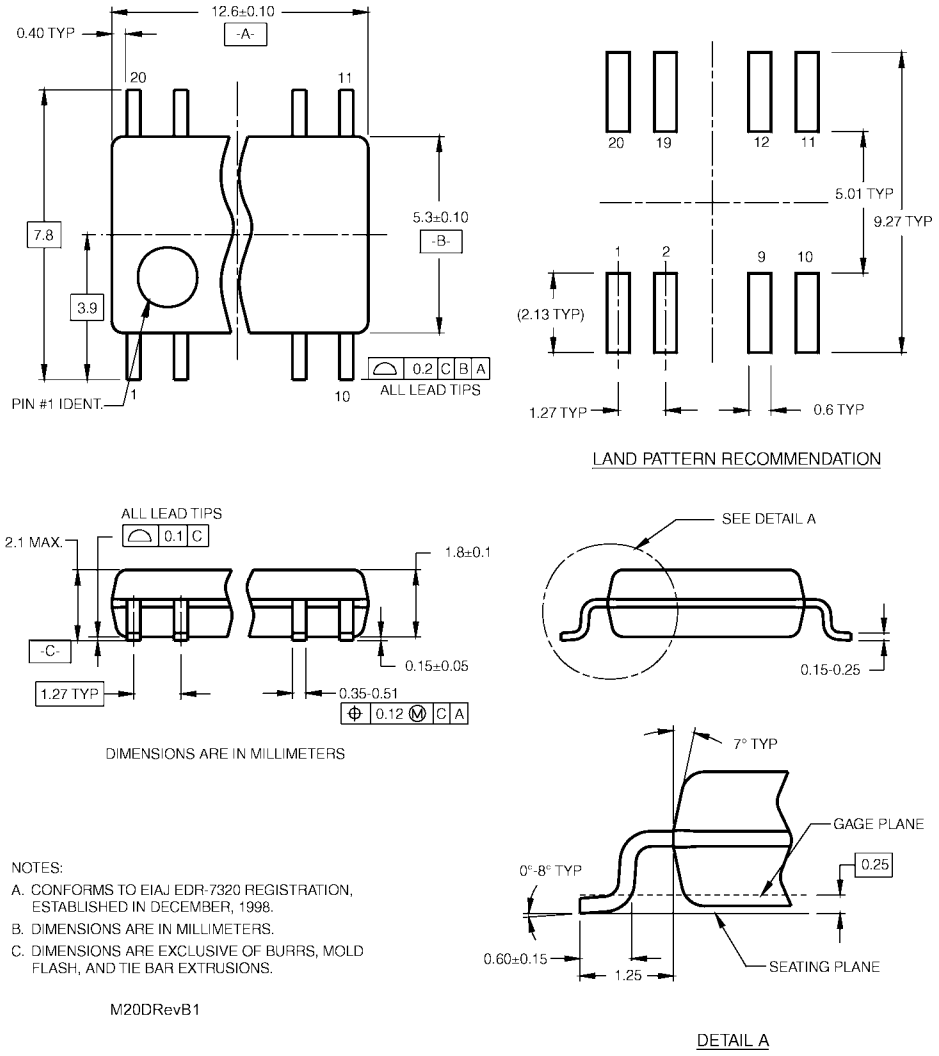

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M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
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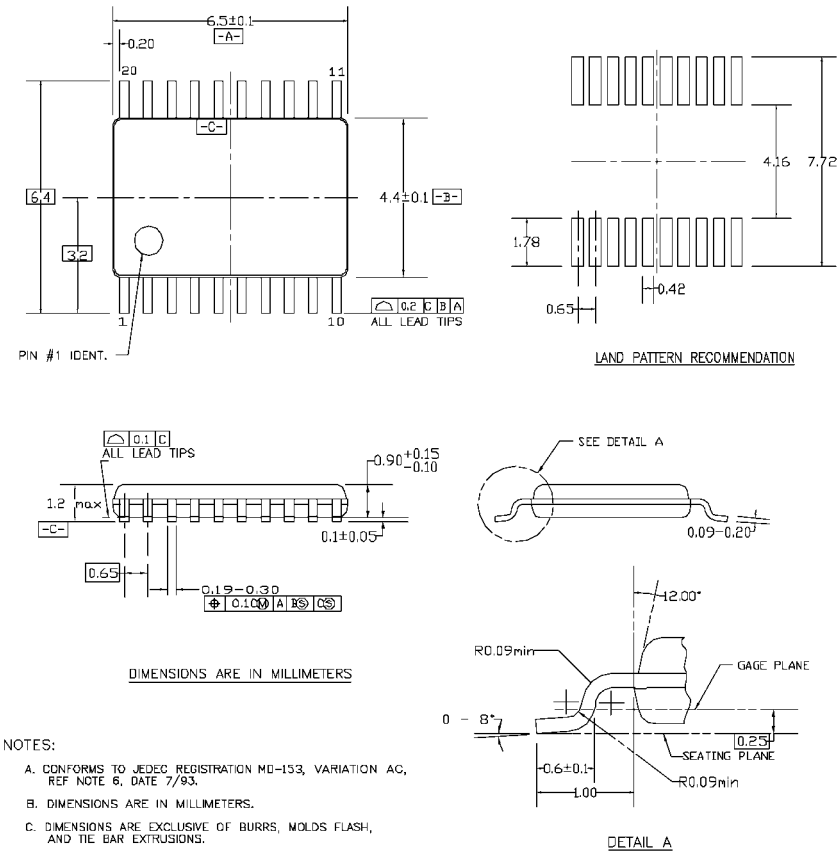

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MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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