# 8-Bit, 250 MSPS 3.3 V A/D Converter

# AD9481

## FEATURES

**DNL = ±0.35 LSB**
**INL = ±0.26 LSB**
**Single 3.3 V supply operation (3.0 V to 3.6 V)**
**Power dissipation of 439 mW at 250 MSPS**
**1 V p-p analog input range**
**Internal 1.0 V reference**
**Single-ended or differential analog inputs**
**De-multiplexed CMOS outputs**
**Power-down mode**
**Clock duty cycle stabilizer**

## APPLICATIONS

**Digital oscilloscopes**
**Instrumentation and measurement**
**Communications**
**Point-to-point radios**
**Digital predistortion loops**

## FUNCTIONAL BLOCK DIAGRAM

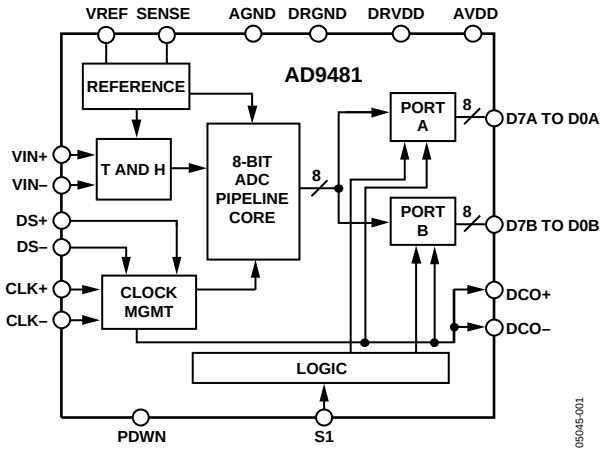


*Figure 1.*

## GENERAL DESCRIPTION

The AD9481 is an 8-bit, monolithic analog-to-digital converter (ADC) optimized for high speed and low power consumption. Small in size and easy to use, the product operates at a 250 MSPS conversion rate, with excellent linearity and dynamic performance over its full operating range.

To minimize system cost and power dissipation, the AD9481 includes an internal reference and track-and-hold circuit. The user only provides a 3.3 V power supply and a differential encode clock. No external reference or driver components are required for many applications.

The digital outputs are TTL/CMOS-compatible with an option of twos complement or binary output format. The output data bits are provided in an interleaved fashion along with output clocks that simplifies data capture.

The AD9481 is available in a Pb-free, 44-lead, surface-mount package (TQFP-44) specified over the industrial temperature range (−40°C to +85°C).

## PRODUCT HIGHLIGHTS

1. Superior linearity. A DNL of ±0.35 makes the AD9481 suitable for many instrumentation and measurement applications
2. Power-down mode. A power-down function may be exercised to bring total consumption down to 15 mW.
3. De-multiplexed CMOS outputs allow for easy interfacing with low cost FPGAs and standard logic.

**Rev. 0**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.326.8703** 

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- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
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- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
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- MS-2210: Designing Power Supplies for High Speed ADC

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## REVISION HISTORY

**10/04—Revision 0: Initial Version**

# DC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V; $T_{MIN}$ = −40°C, $T_{MAX}$ = +85°C, $A_{IN}$ = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

**Table 1.**

| | | | AD9481-250 | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Temp** | **Test Level** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | | | 8 | | Bits |
| ACCURACY | | | | | | |
| No Missing Codes | Full | VI | | Guaranteed | | |
| Offset Error | 25°C | I | −40 | | 40 | mV |
| Gain Error[1] | 25°C | I | −6.0 | | 6.0 | % FS |
| Differential Nonlinearity (DNL) | Full | VI | −0.85 | ±0.35 | 0.85 | LSB |
| Integral Nonlinearity (INL) | Full | VI | −0.9 | ±0.26 | 0.9 | LSB |
| TEMPERATURE DRIFT | | | | | | |
| Offset Error | Full | V | | 30 | | µV/°C |
| Gain Error | Full | V | | 0.03 | | % FS/°C |
| Reference | Full | V | | ±0.025 | | mV/°C |
| REFERENCE | | | | | | |
| Internal Reference Voltage | Full | VI | 0.97 | 1.0 | 1.03 | V |
| Output Current[2] | 25°C | IV | | | 1.5 | mA |
| $I_{VREF}$ Input Current[3] | 25°C | I | | | 100 | µA |
| $I_{SENSE}$ Input Current[2] | 25°C | I | | | 10 | µA |
| ANALOG INPUTS (VIN+, VIN−) | | | | | | |
| Differential Input Voltage Range[4] | Full | V | | 1 | | V p-p |
| Common-Mode Voltage | Full | VI | 1.6 | 1.9 | 2.1 | V |
| Input Resistance | Full | VI | 8.4 | 10 | 11.2 | kΩ |
| Input Capacitance | 25°C | V | | 4 | | pF |
| Analog Bandwidth, Full Power | 25°C | V | | 750 | | MHz |
| POWER SUPPLY | | | | | | |
| AVDD | Full | IV | 3.0 | 3.3 | 3.6 | V |
| DRVDD | Full | IV | 3.0 | 3.3 | 3.6 | V |
| Supply Currents | | | | | | |
| IAVDD[5] | Full | VI | | 133 | 145 | mA |
| IDRVDD[5] | Full | VI | | 39 | 42.5 | mA |
| Power Dissipation[5] | 25°C | V | | 439 | | mW |
| Power-Down Dissipation | 25°C | V | | 15 | 37 | mW |
| Power Supply Rejection Ratio (PSRR) | 25°C | V | | −4.2 | | mV/V |

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1 V external reference and 1 V p-p input range).
[2] Internal reference mode; SENSE = AGND.
[3] External reference mode; VREF driven by external 1.0 V reference; SENSE = AVDD.
[4] In FS = 1 V, both analog inputs are 500 mV p-p and out of phase with each other.
[5] Supply current measured with rated encode and a 20 MHz analog input. Power dissipation measured with dc input, see the Terminology section for power vs. clock rate.

# DIGITAL SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V; $T_{MIN}$ = −40°C, $T_{MAX}$ = +85°C, $A_{IN}$ = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

**Table 2.**

| | | | AD9481-250 | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Temp** | **Test Level** | **Min** | **Typ** | **Max** | **Unit** |
| CLOCK AND DS INPUTS (CLK+, CLK–, DS+, DS–) | | | | | | |
| Differential Input | Full | IV | 200 | | | mV p-p |
| Common-Mode Voltage[1] | Full | VI | 1.38 | 1.5 | 1.68 | V |
| Input Resistance | Full | VI | 4.2 | 5.5 | 6.0 | kΩ |
| Input Capacitance | 25°C | V | | 4 | | pF |
| LOGIC INPUTS (PDWN, S1) | | | | | | |
| Logic 1 Voltage | Full | IV | 2.0 | | | V |
| Logic 0 Voltage | Full | IV | | | 0.8 | V |
| Logic 1 Input Current | Full | VI | | | ±160 | µA |
| Logic 0 input Current | Full | VI | | | 10 | µA |
| Input Resistance | 25°C | V | | 30 | | kΩ |
| Input Capacitance | 25°C | V | | 4 | | pF |
| DIGITAL OUTPUTS | | | | | | |
| Logic 1 Voltage[2] | Full | VI | DRVDD – 0.05 | | | mV |
| Logic 0 Voltage | Full | VI | | | 0.05 | V |
| Output Coding | Full | IV | Twos complement or binary | | | |

[1] The common mode for CLOCK inputs can be externally set, such that 0.9 V < CLK ± < 2.6 V.
[2] Capacitive loading only.

# AC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V; $T_{MIN}$ = −40°C, $T_{MAX}$ = +85°C, $A_{IN}$ = −1 dBFS, full scale = 1.0 V, internal reference, differential analog and clock inputs, unless otherwise noted.

**Table 3.**

| | | | AD9481-250 | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Temp** | **Test Level** | **Min** | **Typ** | **Max** | **Unit** |
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | 46 | | dB |
| $f_{IN}$ = 70.1 MHz | 25°C | I | 44.5 | 45.7 | | dB |
| SIGNAL-TO-NOISE AND DISTORTION (SINAD) | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | 45.9 | | dB |
| $f_{IN}$ = 70.1 MHz | 25°C | I | 44.4 | 45.7 | | dB |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | 7.5 | | Bits |
| $f_{IN}$ = 70.1 MHz | 25°C | I | 7.2 | 7.5 | | Bits |
| WORST SECOND OR THIRD HARMONIC DISTORTION | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | −64.8 | | dBc |
| $f_{IN}$ = 70.1 MHz | 25°C | I | | −64.8 | −54 | dBc |
| WORST OTHER | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | −68 | | dBc |
| $f_{IN}$ = 70.1 MHz | 25°C | I | | −65.8 | −56 | dBc |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR)[1] | | | | | | |
| $f_{IN}$ = 19.7 MHz | 25°C | V | | −64.8 | | dBc |
| $f_{IN}$ = 70.1 MHz | 25°C | I | | −64.8 | −54 | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD) | | | | | | |
| $f_{IN1}$ = 69.3 MHz, $f_{IN2}$ = 70.3 MHz | 25°C | V | | −64.9 | | dBc |

[1] DC and Nyquist bin energy ignored.

# SWITCHING SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V; differential encode input, duty cycle stabilizer enabled, unless otherwise noted.

**Table 4.**

| | | | AD9481-250 | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Temp** | **Test Level** | **Min** | **Typ** | **Max** | **Unit** |
| CLOCK | | | | | | |
| Maximum Conversion Rate | Full | VI | 250 | | | MSPS |
| Minimum Conversion Rate | Full | IV | | | 20 | MSPS |
| Clock Pulse-Width High ($t_{EH}$) | Full | IV | 1.2 | 2 | | ns |
| Clock Pulse-Width Low ($t_{EL}$) | Full | IV | 1.2 | 2 | | ns |
| DS Input Setup Time ($t_{SDS}$) | Full | IV | 0.5 | | | ns |
| DS Input Hold Time ($t_{HDS}$) | Full | IV | 0.5 | | | ns |
| OUTPUT PARAMETERS[1] | | | | | | |
| Valid Time ($t_V$)[2] | Full | VI | 2.5 | | | ns |
| Propagation Delay ($t_{PD}$) | Full | VI | | 4 | 5.4 | ns |
| Rise Time ($t_R$) 10% to 90% | Full | V | | 670 | | ps |
| Fall Time ($t_F$) 10% to 90% | Full | V | | 360 | | ps |
| DCO Propagation Delay ($t_{CPD}$)[3] | Full | VI | 2.5 | 3.9 | 5.3 | ns |
| Data-to-DCO Skew ($t_{PD} - t_{CPD}$)[4] | Full | VI | −0.5 | | +0.5 | ns |
| A Port Data to DCO− Rising ($t_{SKA}$)[5] | Full | IV | | 4 | | ns |
| B Port Data to DCO+ Rising ($t_{SKB}$) | Full | IV | | 4 | | ns |
| Pipeline Latency (A, B) | Full | IV | | 8 | | Cycles |
| APERTURE | | | | | | |
| Aperture Delay ($t_A$) | 25°C | V | | 1.5 | | ns |
| Aperture Uncertainty (Jitter) | 25°C | V | | 0.25 | | ps rms |
| OUT-OF-RANGE RECOVERY TIME | 25°C | V | | 1 | | Cycle |

[1] $C_{LOAD}$ equals 5 pF maximum for all output switching specifications.
[2] Valid time is approximately equal to minimum $t_{PD}$.
[3] $T_{CPD}$ equals clock rising edge to DCO (+ or −) rising edge delay.
[4] Data changing to (DCO+ or DCO−) rising edge delay.
[5] $T_{SKA}$, $T_{SKB}$ are both clock rate dependent delays equal to $T_{CYCLE}$ − (Data to DCO skew).

## TIMING DIAGRAM

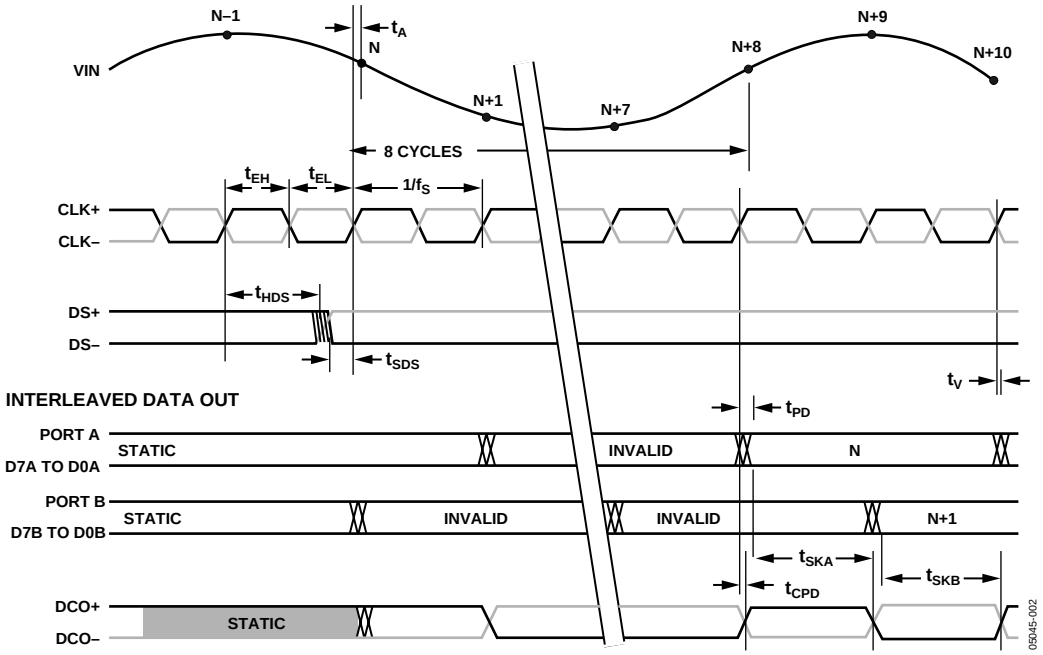



*Figure 2. Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

Thermal impedance ($\theta_{JA}$) = 46.4°C/W (4-layer PCB).

**Table 5.**

| Parameter | Min. Rating | Max. Rating |
|---|---|---|
| ELECTRICAL | | |
| AVDD (With respect to AGND) | −0.5 V | +4.0 V |
| DRVDD (With respect to DRGND) | −0.5 V | +4.0 V |
| AGND (With respect to DRGND) | −0.5 V | +0.5 V |
| Digital I/0 (With respect to DRGND) | −0.5 V | DRVDD + 0.5 V |
| Analog Inputs (With respect to AGND) | −0.5 V | AVDD + 0.5 V |
| ENVIRONMENTAL | | |
| Operating Temperature | −40°C | +85°C |
| Junction Temperature | | 150°C |
| Storage Temperature | | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## EXPLANATION OF TEST LEVELS

**Table 6.**

| Level | Description |
|---|---|
| I | 100% production tested. |
| II | 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures. |
| III | Sample tested only. |
| IV | Parameter is guaranteed by design and characterization testing. |
| V | Parameter is a typical value only. |
| VI | 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range. |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

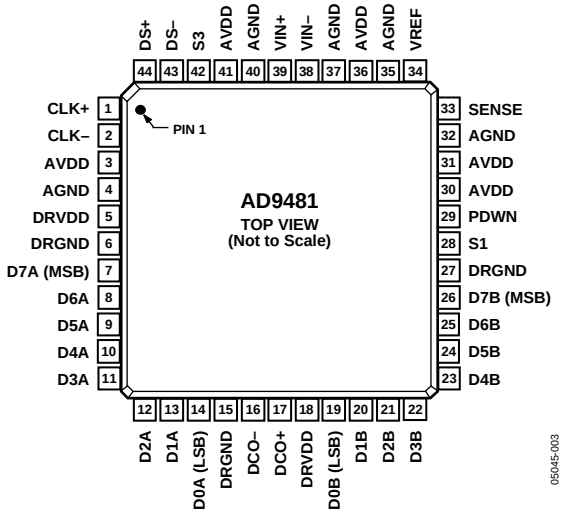



*Figure 3. Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Name | Description |
|---|---|---|
| 1 | CLK+ | Input Clock—True |
| 2 | CLK– | Input Clock—Complement |
| 3 | AVDD | 3.3 V Analog Supply |
| 4 | AGND | Analog Ground |
| 5 | DRVDD | 3.3 V Digital Output Supply |
| 6 | DRGND | Digital Ground |
| 7 | D7A | Data Output Bit 7—Channel A (MSB) |
| 8 | D6A | Data Output Bit 6—Channel A |
| 9 | D5A | Data Output Bit 5—Channel A |
| 10 | D4A | Data Output Bit 4—Channel A |
| 11 | D3A | Data Output Bit 3—Channel A |
| 12 | D2A | Data Output Bit 2—Channel A |
| 13 | D1A | Data Output Bit 1—Channel A |
| 14 | D0A | Data Output Bit 0—Channel A (LSB) |
| 15 | DRGND | Digital Ground |
| 16 | DCO– | Data Clock Output—Complement |
| 17 | DCO+ | Data Clock Output—True |
| 18 | DRVDD | 3.3 V Digital Output Supply |
| 19 | D0B | Data Output Bit 0—Channel B (LSB) |
| 20 | D1B | Data Output Bit 1—Channel B |
| 21 | D2B | Data Output Bit 2—Channel B |
| 22 | D3B | Data Output Bit 3—Channel B |
| 23 | D4B | Data Output Bit 4—Channel B |
| 24 | D5B | Data Output Bit 5—Channel B |
| 25 | D6B | Data Output Bit 6—Channel B |
| 26 | D7B | Data Output Bit 7—Channel B (MSB) |
| 27 | DRGND | Digital Ground |
| 28 | S1 | Data Format Select and Duty Cycle Stabilizer Select |
| 29 | PDWN | Power-Down Selection |
| 30 | AVDD | 3.3 V Analog Supply |
| 31 | AVDD | 3.3 V Analog Supply |
| 32 | AGND | Analog Ground |
| 33 | SENSE | Reference Mode Selection |
| 34 | VREF | Voltage Reference Input/Output |
| 35 | AGND | Analog Ground |
| 36 | AVDD | 3.3 V Analog Supply |
| 37 | AGND | Analog Ground |
| 38 | VIN– | Analog Input—Complement |
| 39 | VIN+ | Analog Input—True |
| 40 | AGND | Analog Ground |
| 41 | AVDD | 3.3 V Analog Supply |
| 42 | S3 | DCO Enable Select (Tie to AVDD for DCO Active) |
| 43 | DS– | Data Sync Complement (If Unused, Tie to DRVDD) |
| 44 | DS+ | Data Sync True (If Unused, Tie to DGND) |

# TERMINOLOGY

**Analog Bandwidth**
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

**Aperture Delay**
The delay between the 50% point of the rising edge of the encode command and the instant the analog input is sampled.

**Aperture Uncertainty (Jitter)**
The sample-to-sample variation in aperture delay.

**Clock Pulse-Width/Duty Cycle**
Pulse-width high is the minimum amount of time that the clock pulse should be left in a Logic 1 state to achieve rated performance; pulse-width low is the minimum time clock pulse should be left in a low state. See timing implications of changing $t_{EH}$ in the Clocking the AD9481 section. At a given clock rate, these specifications define an acceptable clock duty cycle.

**Crosstalk**
Coupling onto one channel being driven by a low level (−40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

**Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance**
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

**Differential Analog Input Voltage Range**
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

**Differential Nonlinearity**
The deviation of any code width from an ideal 1 LSB step.

**Effective Number of Bits (ENOB)**
ENOB is calculated from the measured SINAD based on the equation (assuming full-scale input)

$$ENOB = \frac{SINAD_{MEASURED} - 1.76\ \text{dB}}{6.02}$$

**Full-Scale Input Power**
Expressed in dBm. Computed using the following equation

$$Power_{FULLSCALE} = 10 \log \left( \frac{\frac{V^2{}_{FULLSCALE}\ rms}{Z_{INPUT}}}{0.001} \right)$$

**Gain Error**
Gain error is the difference between the measured and ideal full-scale input voltage range of the ADC.

**Harmonic Distortion, Second**
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

**Harmonic Distortion, Third**
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

**Integral Nonlinearity**
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

**Minimum Conversion Rate**
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

**Maximum Conversion Rate**
The encode rate at which parametric testing is performed.

**Output Propagation Delay**
The delay between a differential crossing of CLK+ and CLK− and the time when all output data bits are within valid logic levels.

**Noise (for Any Range within the ADC)**
This value includes both thermal and quantization noise.

$$V_{noise} = \sqrt{\text{Z} \times 0.001 \times 10 \left( \frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}$$

where:

*Z* is the input impedance.

*FS* is the full scale of the device for the frequency in question.

*SNR* is the value for the particular input level.

*Signal* is the signal level within the ADC reported in dB below full scale.

**Power Supply Rejection Ratio**
The ratio of a change in input offset voltage to a change in power supply voltage.

**Signal-to-Noise and Distortion (SINAD)**
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

**Signal-to-Noise Ratio (without Harmonics)**
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

**Spurious-Free Dynamic Range (SFDR)**
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (degrades as signal level is lowered) or dBFS (always related back to converter full scale).

**Two-Tone Intermodulation Distortion Rejection**
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product, in dBc.

**Two-Tone SFDR**
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (degrades as signal level is lowered) or in dBFS (always relates back to converter full scale).

**Worst Other Spur**
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic), reported in dBc.

**Transient Response Time**
The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

**Out-of-Range Recovery Time**
This is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DRVDD = 3.3 V, T = 25°C, $A_{IN}$ differential drive, FS = 1, internal reference mode, unless otherwise noted.

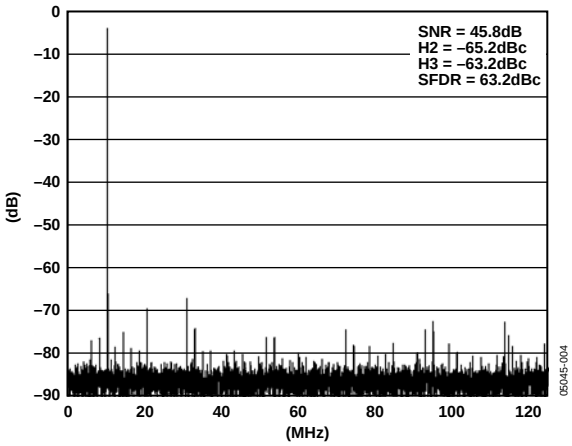



Figure 4. FFT: $f_S$ = 250 MSPS, $A_{IN}$ = 10.3 MHz @ –1 dBFS

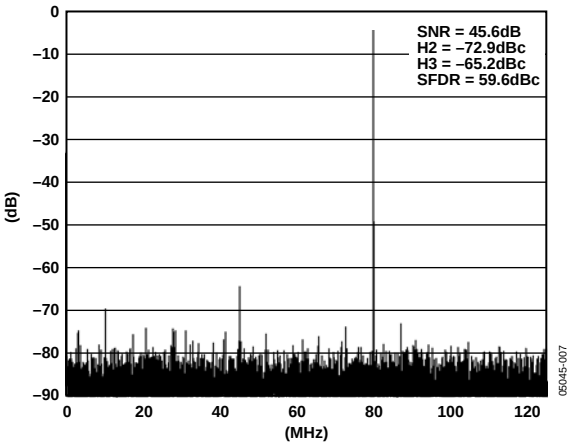



Figure 7. FFT: $f_S$ = 250 MSPS, $A_{IN}$ = 170 MHz @ –1 dBFS

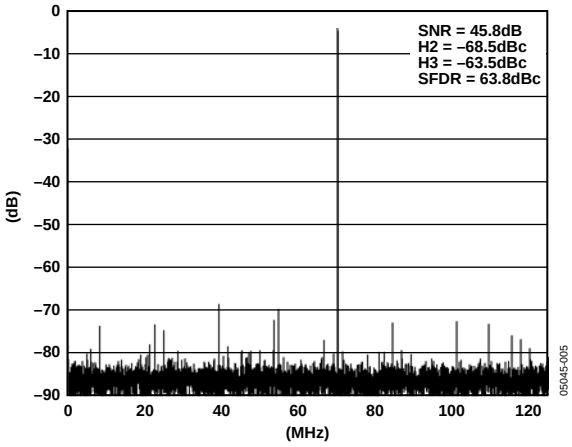



Figure 5. FFT: $f_S$ = 250 MSPS, $A_{IN}$ = 70 MHz @ –1 dBFS

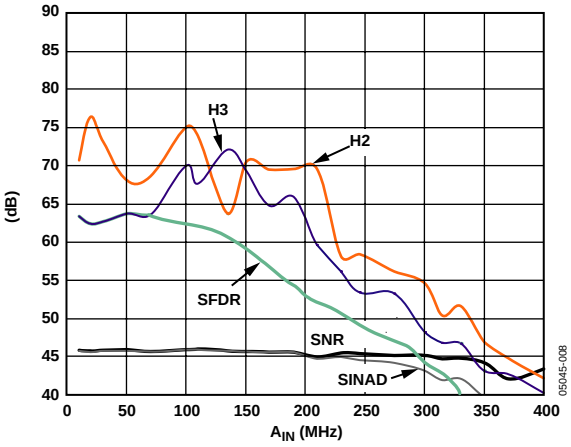



Figure 8. Analog Input Frequency Sweep, $A_{IN}$ = –1 dBFS, FS = 1 V, $f_S$ = 250 MSPS

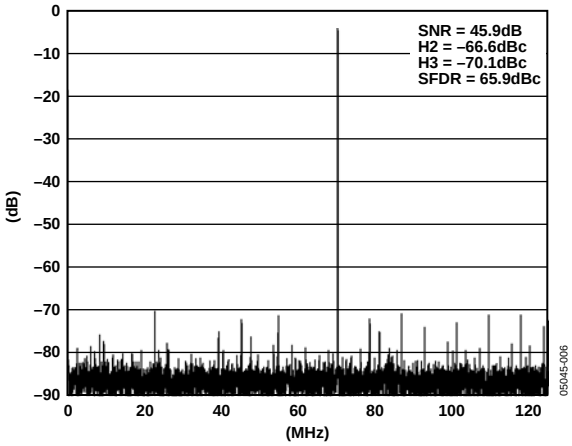



Figure 6. FFT: $f_S$ = 250 MSPS, $A_{IN}$ = 70 MHz @ –1 dBFS, Single-Ended Input

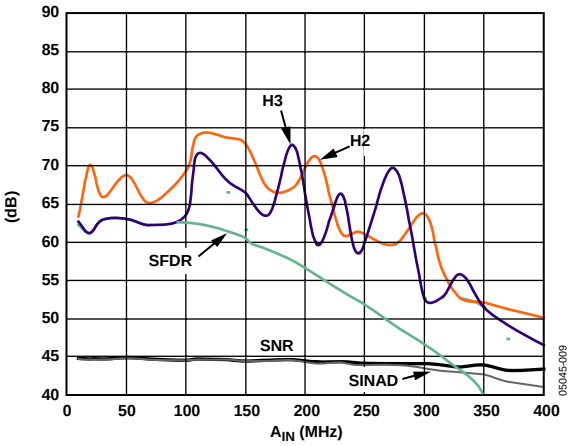



Figure 9. Analog Input Frequency Sweep, $A_{IN}$ = –1 dBFS, FS = 0.75 V, $f_S$ = 250 MSPS, External VREF Mode

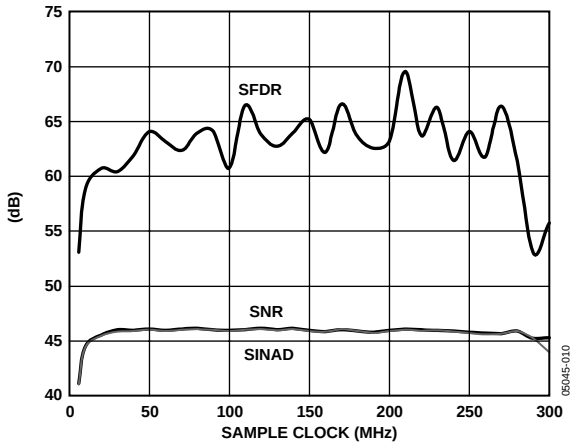



Figure 10. SNR, SINAD, SFDR vs. Sample Clock Frequency, $A_{IN}$ = 70 MHz @ −1 dB

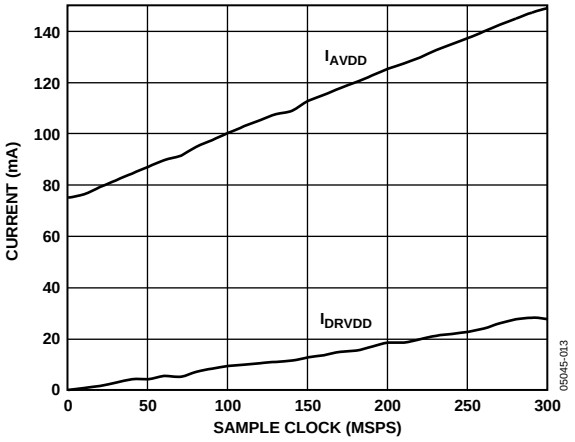



Figure 13. $I_{AVDD}$ and $I_{DRVDD}$ vs. Clock Rate, $C_{LOAD}$ = 5 pF $A_{IN}$ = 70 MHz @ −1 dBFS

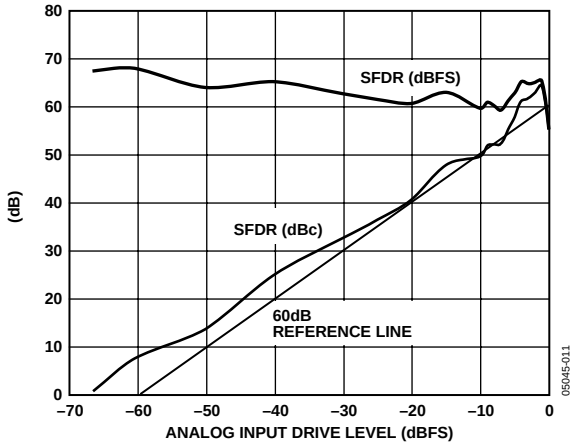



Figure 11. SFDR vs. $A_{IN}$ Input Level; $A_{IN}$ = 70 MHz @ 250 MSPS

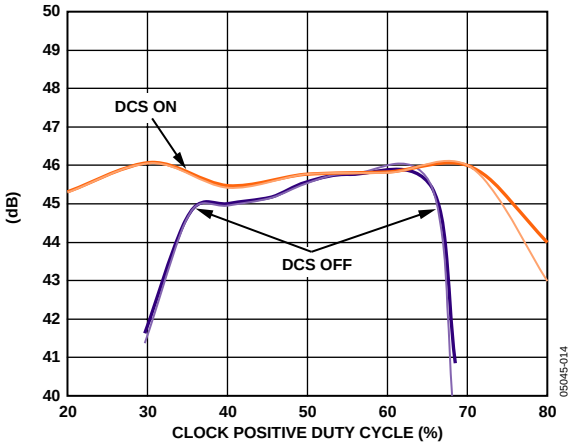



Figure 14. SNR, SINAD vs. Clock Pulse-Width High, $A_{IN}$ = 70 MHz @ −1 dBFS, 250 MSPS, DCS On/Off

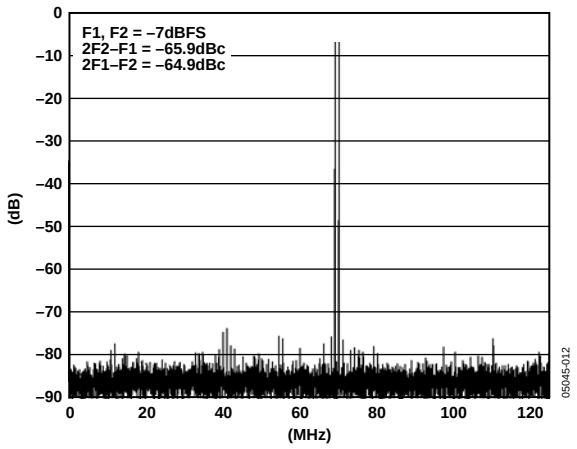



Figure 12. Two-Tone Intermodulation Distortion (69.3 MHz and 70.3 MHz; $f_S$ = 250 MSPS)

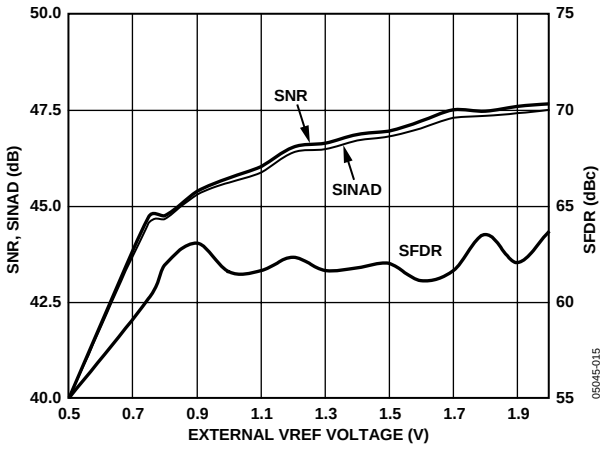



Figure 15. SNR, SINAD, and SFDR vs. VREF in External Reference Mode, $A_{IN}$ = 70 MHz @ −1 dBFS, 250 MSPS

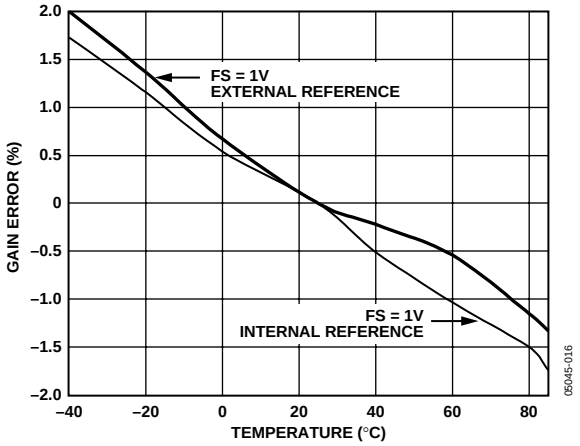



Figure 16. Full-Scale Gain Error vs. Temperature, $A_{IN}$ = 70.3 MHz @ −0.5 dBFS, 250 MSPS

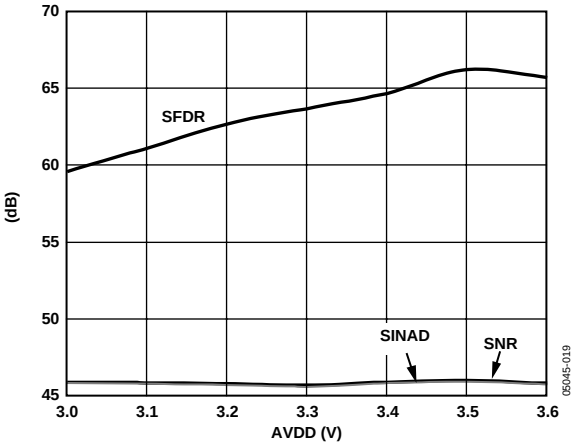



Figure 19. SNR, SINAD, and SFDR vs. Supply Voltage, $A_{IN}$ = 70.3 MHz @ −1 dBFS, 250 MSPS

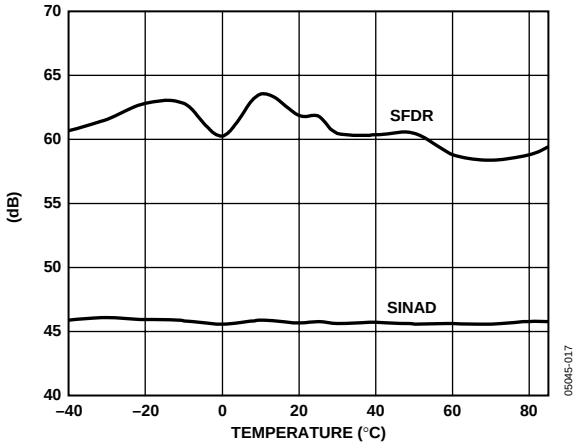



Figure 17. SINAD, SFDR vs. Temperature, $A_{IN}$ = 70 MHz @ −1 dBFS, 250 MSPS

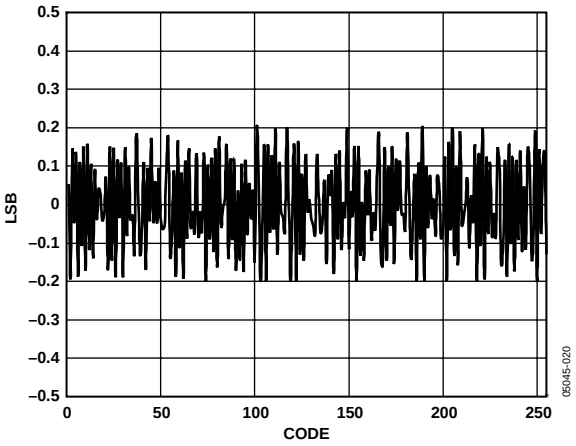



Figure 20. Typical DNL Plot, $A_{IN}$ = 10.3 MHz @ −0.5 dBFS, 250 MSPS

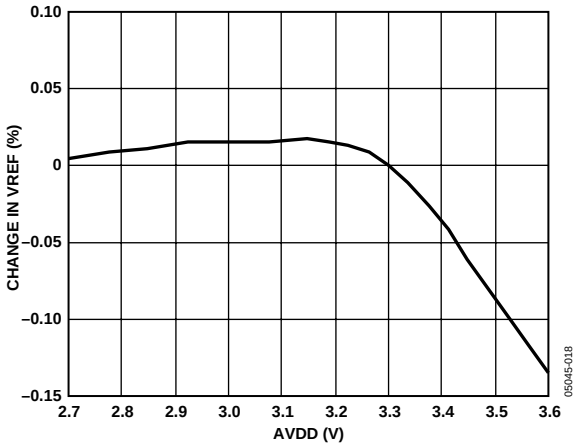



Figure 18. VREF Sensitivity to AVDD

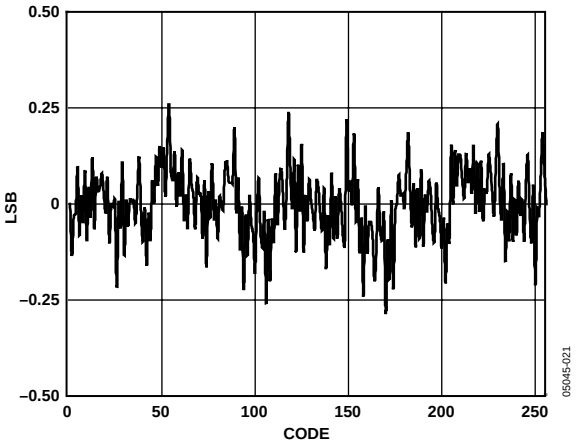



Figure 21. Typical INL Plot, $A_{IN}$ = 10.3 MHz @ −0.5 dBFS, 250 MSPS

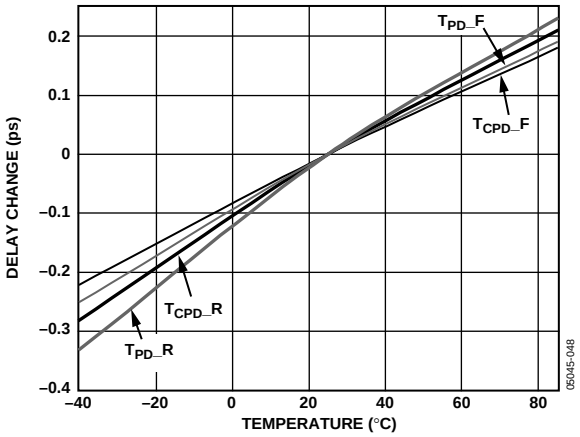



*Figure 22. Propagation Delay Sensitivity vs. Temperature*

# EQUIVALENT CIRCUITS

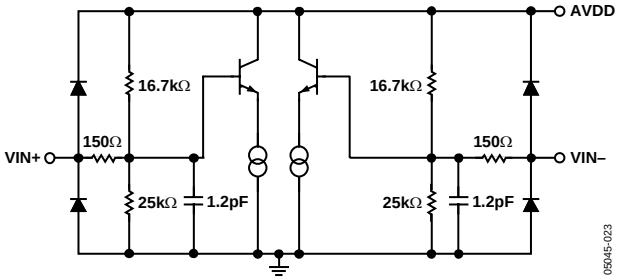



Figure 23. Analog Inputs

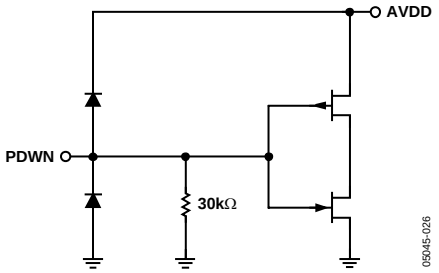



Figure 26. Power-Down Input

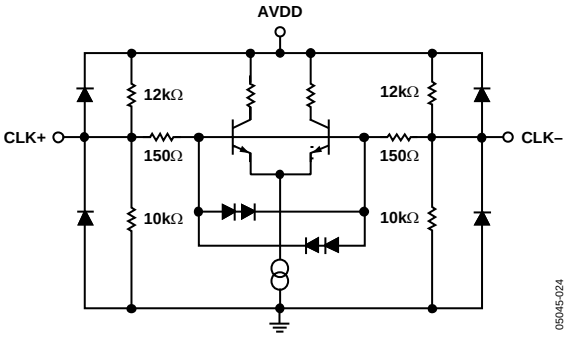



Figure 24. Clock Inputs

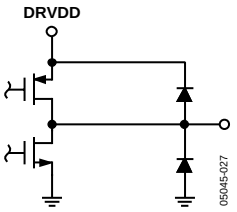



Figure 27. Data, DCO Outputs

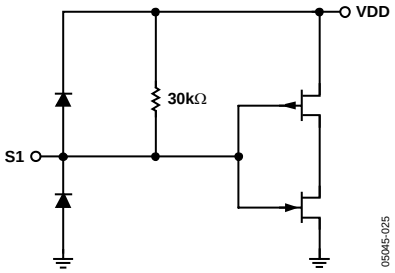



Figure 25. S1 Input

# APPLICATIONS

The AD9481 uses a 1.5 bit per stage architecture. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 8-bit core. For ease of use, the part includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are CMOS-compatible.

## ANALOG INPUTS

The analog input to the AD9481 is a differential buffer. For best dynamic performance, impedances at VIN+ and VIN− should match. Optimal performance is obtained when the analog inputs are driven differentially. SNR and SINAD performance can degrade if the analog input is driven with a single-ended signal. The analog inputs self-bias to approximately 1.9 V; this common-mode voltage can be externally overdriven by approximately ±300 mV if required.

A wideband transformer, such as the Mini-Circuits ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Note that the filter and center-tap capacitor on the secondary side is optional and dependent on application requirements. An RC filter at the secondary side helps reduce any wideband noise getting aliased by the ADC.

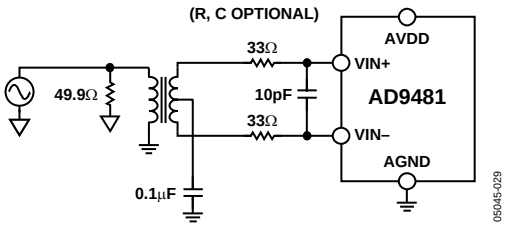



*Figure 28. Driving the ADC with an RF Transformer*

For dc-coupled applications, the AD8138/AD8139 or AD8351 can serve as a convenient ADC driver, depending on requirements. Figure 29 shows an example with the AD8138. The AD9481 PCB has an optional AD8351 on board, as shown in Figure 39 and Figure 40. The AD8351 typically yields better performance for frequencies greater than 30 MHz to 40 MHz. The AD9481's linearity and SFDR start to degrade at higher analog frequencies (see the Typical Performance Characteristics section). For higher frequency applications, the AD9480 with LVDS outputs and superior AC performance should be considered.

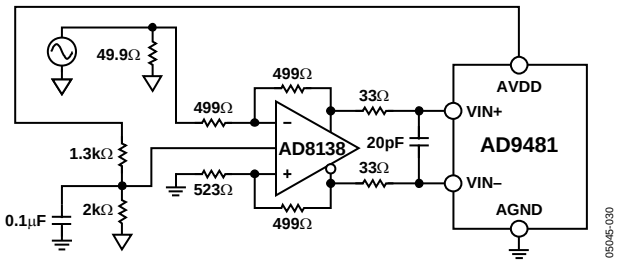



*Figure 29. Driving the ADC with the AD8138*

The AD9481 can be easily configured for different full-scale ranges. See the Voltage Reference section for more information. Optimal performance is achieved with a 1 V p-p analog input.

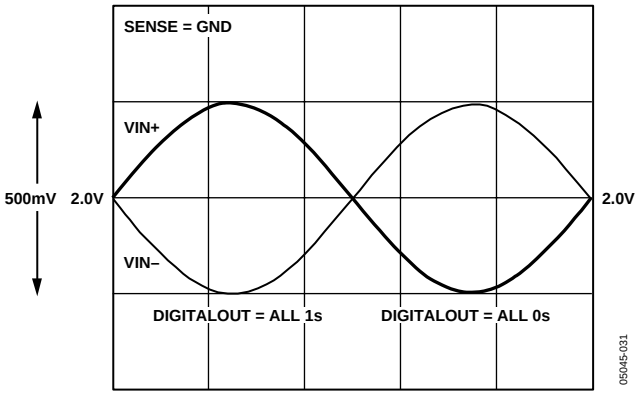



*Figure 30. Analog Input Full Scale*

## VOLTAGE REFERENCE

A stable and accurate 1.0 V reference is built into the AD9481. Users can choose this internal reference or provide an external reference for greater accuracy and flexibility. Figure 32 shows the typical reference variation with temperature. Table 8 summarizes the available reference configurations.

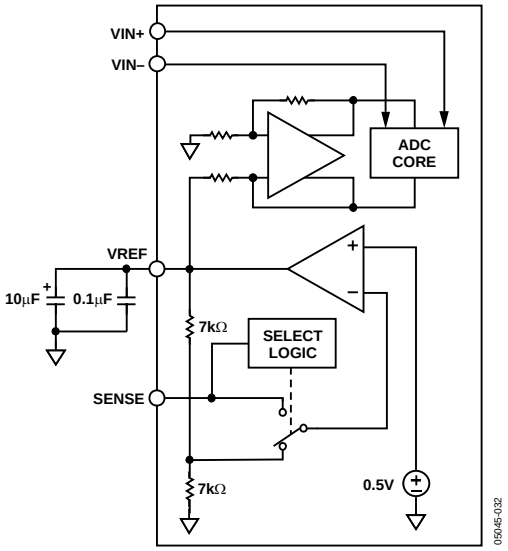



*Figure 31. Internal Reference Equivalent Circuit*

### *Fixed Reference*

The internal reference can be configured for a differential span of 1 V p-p (see Figure 34). It is recommended to place a 0.1 µF capacitor as close as possible to the VREF pin; a 10 µF capacitor is also required (see the PCB layout for guidance). If the internal reference of the AD9481 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 34 depicts how the internal reference voltage is affected by loading.

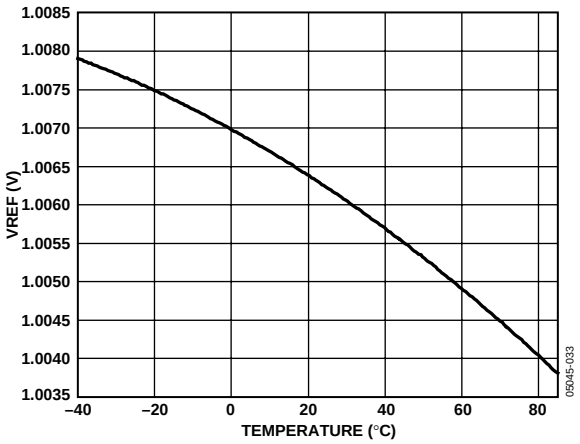



*Figure 32. Typical Reference Variation with Temperature*

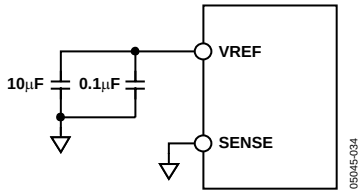



*Figure 33. Internal Fixed Reference (1 V p-p)*

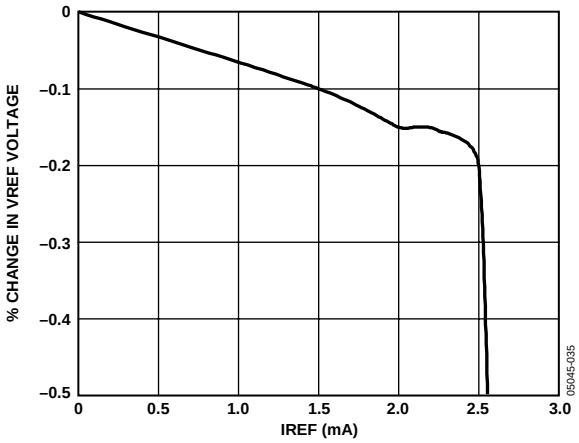



*Figure 34. Internal VREF vs. Load Current*

**Table 8. Reference Configurations**

| SENSE Voltage | Resulting VREF | Reference | Differential Span |
|---|---|---|---|
| AVDD | N/A (external reference input) | External | 1 × external reference voltage |
| 0.5 V (Self-Biased) | 0.5 × (1 + R1/R2) V | Programmable | 1 × VREF (0.75 V p-p to 1.5 V p-p) |
| AGND to 0.2 V | 1.0 V | Internal fixed | 1 V p-p |

### *External Reference*

An external reference can be used for greater accuracy and temperature stability when required. The gain of the AD9481 can also be varied using this configuration. A voltage output DAC can be used to set VREF, providing for a means to digitally adjust the full-scale voltage. VREF can be externally set to voltages from 0.75 V to 1.5 V; optimum performance is typically obtained at VREF = 1 V. (See the Typical Performance Characteristics section.)

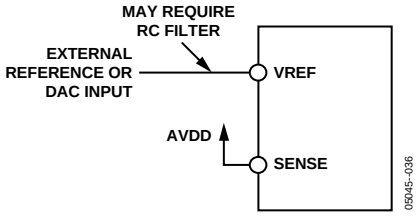



*Figure 35. External Reference*

### *Programmable Reference*

The programmable reference can be used to set a differential input span anywhere between 0.75 V p-p and 1.5 V p-p by using an external resistor divider. The SENSE pin self-biases to 0.5 V, and the resulting VREF is equal to 0.5 × (1 + R1/R2). It is recommended to keep the sum of R1 + R2 ≥ 10 kΩ to limit VREF loading (for VREF = 1.5 V, set R1 equal to 7 kΩ and R2 equal to 3.5 kΩ).

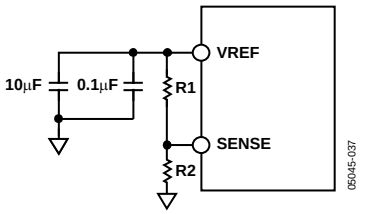



*Figure 36. Programmable Reference*

## CLOCKING THE AD9481

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. Considerable care has been taken in the design of the CLOCK input of the AD9481, and the user is advised to give commensurate thought to the clock source.

The AD9481 has an internal clock duty cycle stabilization circuit that locks to the rising edge of CLOCK and optimizes timing internally for sample rates between 100 MSPS and 250 MSPS. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter on the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 70 MHz nominally. The loop has a time constant associated with it that needs to be considered in applications where the clock rate can change dynamically, requiring a wait time of 5 µs after a dynamic clock frequency increase before valid data is available. The clock duty cycle stabilizer can be disabled at Pin 28 (S1).

The clock inputs are internally biased to 1.5 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. An MC100LVEL16 performs well in the circuit to drive the clock inputs (ac coupling is optional). If the clock buffer is greater than two inches from the ADC, a standard LVPECL termination may be required instead of the simple pull-down termination shown in Figure 37.

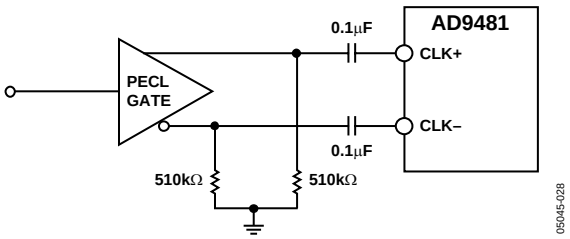



*Figure 37. Clocking the AD9481*

## DS INPUTS

The data sync inputs (DS+, DS–) can be used in applications which require that a given sample appear at a specific output port (A or B) relative to a given external timing signal.

The DS inputs can also be used to synchronize two or more ADCs in a system to maintain phasing between Ports A and B on separate ADCs (in effect, synchronizing multiple DCO outputs).

The DS inputs are internally biased to 1.5 V (nominal) and support either differential or single-ended signals. When DS+ is held high (DS– low), the ADC data outputs and DCO outputs do not switch and are held static. Synchronization is accomplished by the assertion (falling edge) of DS+ within the timing constraints $t_{SDS}$ and $t_{HDS}$, relative to a clock rising edge. (On initial synchronization, $t_{HDS}$ is not relevant.) If DS+ falls within the required setup time ($t_{SDS}$) before a given clock rising edge N, the analog value at that point in time is digitized and available at Port A, eight cycles later in interleaved mode. The next sample, N + 1, is sampled by the next rising clock edge and available at Port B, eight cycles after that clock edge.

Driving each ADC's DS inputs by the same sync signal accomplishes synchronization between multiple ADCs. In applications which require synchronization, one-shot synchronization is recommended. An easy way to accomplish synchronization is by a one-time sync at power-on reset.

**Table 9. S1 Voltage Levels**

| S1 Voltage | Data Format | Duty Cycle Stabilizer |
|---|---|---|
| (0.9 × *AVDD*) → *AVDD* | Offset binary | Disabled |
| (2/3 × *AVDD*) ± (0.1 × *AVDD*) | Offset binary | Enabled |
| (1/3 × *AVDD*) ± (0.1 × *AVDD*) | Twos complement | Enabled |
| *AGND* → (0.1 × *AVDD*) | Twos complement | Disabled |

## DIGITAL OUTPUTS

The CMOS digital outputs are TTL-/CMOS-compatible for lower power consumption. The outputs are biased from a separate supply (DRVDD), allowing easy interface to external logic. The outputs are CMOS devices that swing from ground to DRVDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (< 2 inch, for a total $C_{LOAD}$ < 5 pF). When operating in CMOS mode, it is also recommended to place low value series damping resistors on the data lines close to the ADC to reduce switching transient effects on performance.

**Table 10. Output Coding (FS = 1 V)**

| Code | (VIN+) – (VIN–) | Offset Binary | Twos Complement |
|---|---|---|---|
| 255 | > +0.512 V | 1111 1111 | 0111 1111 |
| 255 | +0.512 V | 1111 1111 | 0111 1111 |
| 254 | +0.508 V | 1111 1110 | 0111 1110 |
| • | • | • | • |
| • | • | • | • |
| 129 | +0.004 V | 1000 0001 | 0000 0001 |
| 128 | +0.0 V | 1000 0000 | 0000 0000 |
| 127 | −0.004 V | 0111 1111 | 1111 1111 |
| • | • | • | • |
| • | • | • | • |
| 2 | −0.504 V | 0000 0010 | 1000 0010 |
| 1 | −0.508 V | 0000 0001 | 1000 0001 |
| 0 | −0.512 V | 0000 0000 | 1000 0000 |
| 0 | < −0.512 V | 0000 0000 | 1000 0000 |

## INTERLEAVING TWO AD9481s

Instrumentation applications may prefer to interleave (or ping-pong) two AD9481s to achieve twice the sample rate, or 500 MSPS. In these applications, it is important to match the gain and offset of the two ADCs. Varying the reference voltage allows the gain of the ADCs to be adjusted; external dc offset compensation can be used to reduce offset mismatch between two ADCs. The sampling phase offset between the two ADCs is extremely important as well and requires very low skew between clock signals driving the ADCs (< 2 ps clock skew for a 100 MHz analog input frequency).

## DATA CLOCK OUT

A data clock is available at DCO+ and DCO−. These clocks can facilitate latching off-chip, providing a low skew clocking solution. The on-chip delay of the DCO clocks tracks with the on-chip delay of the data bits, (under similar loading) such that the variation between $t_{PD}$ and $t_{CPD}$ is minimized. It is recommended to keep the trace lengths on the data and DCO pins matched and 2 inches maximum. A series damping resistor at the clock outputs is also recommended. The DCO outputs can be disabled and placed in a high impedance state by tying S3 to ground (tie to AVDD for DCO active). Switching both into and out of high impedance is accomplished in 4 ns from S3 switching.

## POWER-DOWN INPUT

The ADC can be placed into a low power state by setting the PDWN pin to AVDD. Time to go into (or come out of) power down equals 30 ns typically from PDWN switching.

# AD9481 EVALUATION BOARD

The AD9481 evaluation board offers an easy way to test the device. It requires a clock source, an analog input signal, and a 3.3 V power supply. The clock source is buffered on the board to provide the clocks for the ADC and a data-ready signal. The digital outputs and output clocks are available at an 80-pin output connector, P3, P23. (Note that P3, P23 are represented schematically as two 40-pin connectors, and this connector is implemented as one 80-pin connector on the PCB.) The board has several different modes of operation and is shipped in the following configuration:

- Offset binary
- Internal voltage reference

## POWER CONNECTOR

Power is supplied to the board via two detachable 4-pin power strips.

**Table 11. Power Connector**

| Terminal | Comments |
|---|---|
| VDL (3.3 V) | Output supply for external latches and data ready clock buffer ~ 30 mA |
| AVDD[1] 3.3 V | Analog supply for ADC ~ 140 mA |
| DRVDD[1] 3.3 V | Output supply for ADC ~ 30 mA |
| VCTRL[1] 3.3 V | Supply for support clock circuitry ~ 60 mA |
| Op amp, ext. ref | Optional supply for op amp and ADR510 reference |

[1] AVDD, DRVDD, VDL, and VCTRL are the minimum required power connections.

## ANALOG INPUTS

The evaluation board accepts a 700 mV p-p analog input signal centered at ground at SMB Connector J3. This signal is terminated to ground through 50 Ω by R22. The input can be alternatively terminated at the T1 transformer secondary by R21 and R28. T1 is a wideband RF transformer that provides the single-ended-to-differential conversion, allowing the ADC to be driven differentially, minimizing even-order harmonics. An optional transformer, T4, can be placed if desired (remove T1, as shown in Figure 39 and Figure 40).

The analog signal can be low-pass filtered by R21, C8 and R28, C9 at the ADC input.

## GAIN

Full scale is set by the sense jumper. This jumper applies a bias to the SENSE pin to vary the full-scale range; the default position is SENSE = ground, setting the full scale to 1 V p-p.

## OPTIONAL OPERATIONAL AMPLIFIER

The PCB has been designed to accommodate an optional AD8351 op amp that can serve as a convenient solution for dc-coupled applications. To use the AD8351 op amp, remove R29, R31, and C3. Populate R12, R17, and R36 with 25 Ω resistors, and populate C1, C21, C23, C31, C39, and C30 with 0.1 µF capacitors. Populate R54, R10, and R11 with 10 Ω resistors, and R34 and R32 with 1 kΩ resistors. Populate R15 with a 1.2 kΩ resistor and R14 with a 100 Ω resistor. Populate R37 with a 10 kΩ resistor.

## CLOCK

The clock input is terminated to ground through 50 Ω at SMA Connector J1. The input is ac-coupled to a high speed differential receiver (LVEL16) that provides the required low jitter, fast edge rates needed for best performance. J1 input should be > 0.5 V p-p. Power to the LVEL16 is set to VCTRL (default) or AVDD by jumper placement at the device.

## OPTIONAL CLOCK BUFFER

The PCB has been designed to accommodate the SNLVDS1 line driver. The SNLVDS1 is used as a high speed LVDS-level optional encode clock. To use this clock, please remove C2, C5, and C6. Place 0.1 µF capacitors on C34, C35, and C26. Place a 10 Ω resistor on R48, and place a 100 Ω resistor on R6. Place a 0 Ω resistor on both R49 and R53. For best results using the line driver, J1 input should be > 2.5 V p-p.

## DS

The DS inputs are available on the PCB at J2 and J4. If driving DS+ externally, place a 0 Ω resistor at C48 and remove R53.

## OPTIONAL XTAL

The PCB has been designed to accommodate an optional crystal oscillator that can serve as a convenient clock source. The footprint can accept both through-hole and surface-mount devices, including Vectron XO-400 and Vectron VCC6 family oscillators.

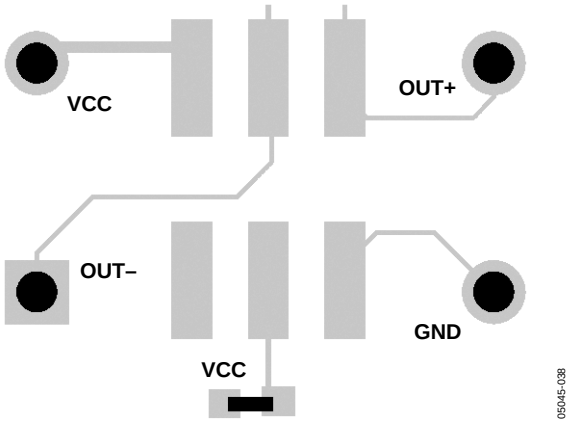



*Figure 38. XTAL Footprint*

To use either crystal, populate C38 and C40 with 0.1 µF capacitors. Populate R48 and R49 with 0 Ω resistors. Place R50, R51, R59, and R60 with 1 kΩ resistors. Remove C6 and C5. If the Vectron VCC6 family crystal is being used, populate R57 with a 10 Ω resistor. If using the XO-400 crystal, place jumper E21 or E22 to E23.

## VOLTAGE REFERENCE

The AD9481 has an internal 1 V reference mode. The ADC uses the internal 1 V reference as the default when sense is set to ground. An optional on-board external 1.0 V reference (ADR510) can be used by setting the sense jumper to AVDD, by placing a jumper on E5 to E3, and by placing a 0 Ω resistor on R55. When using an external programmable reference, (R20, R30) remove the sense jumper.

## DATA OUTPUTS

The ADC outputs are buffered on the PCB by LVT574 latches on the data outputs. The latch outputs have series terminating resistors at the output pins to minimize reflections.

# EVALUATION BOARD BILL OF MATERIALS (BOM)

**Table 12.**

| No. | Quantity | Reference Designator | Device | Package | Value |
|---|---|---|---|---|---|
| 1 | 24 | C1 to C6, C10 to C12, C14 to C15, C17 to C19, C22 to C29, C31, C48 to C49 | Capacitors | 0402 | 0.1 µF |
| 2 | 1 | C13 | Capacitor | Tantalum (3528) | 10 µF |
| 3 | 5 | C32 to C36 | Capacitors | Tantalum (6032) | 10 µF |
| 4 | 4 | J1 to J4 | SMA | SMA | Degrees |
| 5 | 3 | P1, P12 to P13 | 4-pin power connectors | Post | Z5.531.3425.0 |
| 6 | 3 | P1, P12 to P13 | 4-pin power connectors | Detachable connector | 25.602.5453.0 |
| 7 | 2 | P3, P23 | 80-pin connectors | Connector | TSW-140-08-L-D-RA |
| 8 | 7 | R1, R5, R19, R22, R27, R35, R53 | Resistors | 0603 | 50 Ω |
| 9 | 8 | R2 to R4, R6 to R9, R18, R14 | Resistors | 0603 | 100 Ω |
| 10 | 7 | R13, R42 to R45, R32, R34 | Resistors | 0603 | 1 kΩ |
| 11 | 2 | R16, R52 | Resistors | 0603 | 130 Ω |
| 12 | 2 | R23, R24 | Resistors | 0603 | 510 Ω |
| 13 | 2 | R25, R26 | Resistors | 0603 | 82 Ω |
| 14 | 2 | R29, R31 | Resistors | 0603 | 00 Ω |
| 15 | 2 | R33, R37 | Resistors | 0603 | 10 kΩ |
| 16 | 1 | R46 | Resistor | 0603 | 2 kΩ |
| 17 | 3 | R12, R17, R36 | Resistors | 0603 | 25 Ω |
| 18 | 1 | R15 | Resistor | 0603 | 1.2 kΩ |
| 19 | 3 | R54, R10 to R11 | Resistors | 0603 | 10 Ω |
| 20 | 2 | RP1 to RP2 | Resistor Pack | 100 Ω Res. Array | 742C163100JTR |
| 21 | 4 | U3, U5 to U6, U8 | Resistor Pack 100 Ω | 100 Ω Res. Array | EXB-38V101JV |
| 22 | 2 | U4, U7 | 74LVT574 | SO20 | 74LVT574WM |
| 23 | 1 | T1 | Transformer | CD542 | ADT1-1WT |
| 24 | 1 | U1 | AD8351 | MSOP-10 | Op Amp |
| 25 | 1 | U2 | 74VCX86 | SO-14 | XOR |
| 26 | 1 | U10[1] | ADR510 | SOT-23 | Voltage Regulator |
| 27 | 1 | U9[1] | VCC6PECL6 | VCC6-QAB-250M000 | Vectron Crystal |
| 28 | 1 | U12 | AD9481 | TQFP-44 | ADC |
| 29 | 1 | U11 | MC100-LVEL16D | S08NB | Clock Buffer |
| 30 | 1 | T2[1] | ETC1-1-13 | 1-1 TX | M/A-COM/ETC 1-1-13 |
| 31 | 11 | C1, C7 to C9, C16, C20, C30, C31, C38 to C40 | Capacitors | 0402 | X[1] |
| 32 | 18 | R20 to R21, R28, R30, R38 to R41, R48 to R51, R55 to R60 | Resistors | 0603 | X[1] |
| 33 | 16 | E98 to E102, E73 to E84 | Jumpers | | |

[1] Not placed.

# PCB SCHEMATICS

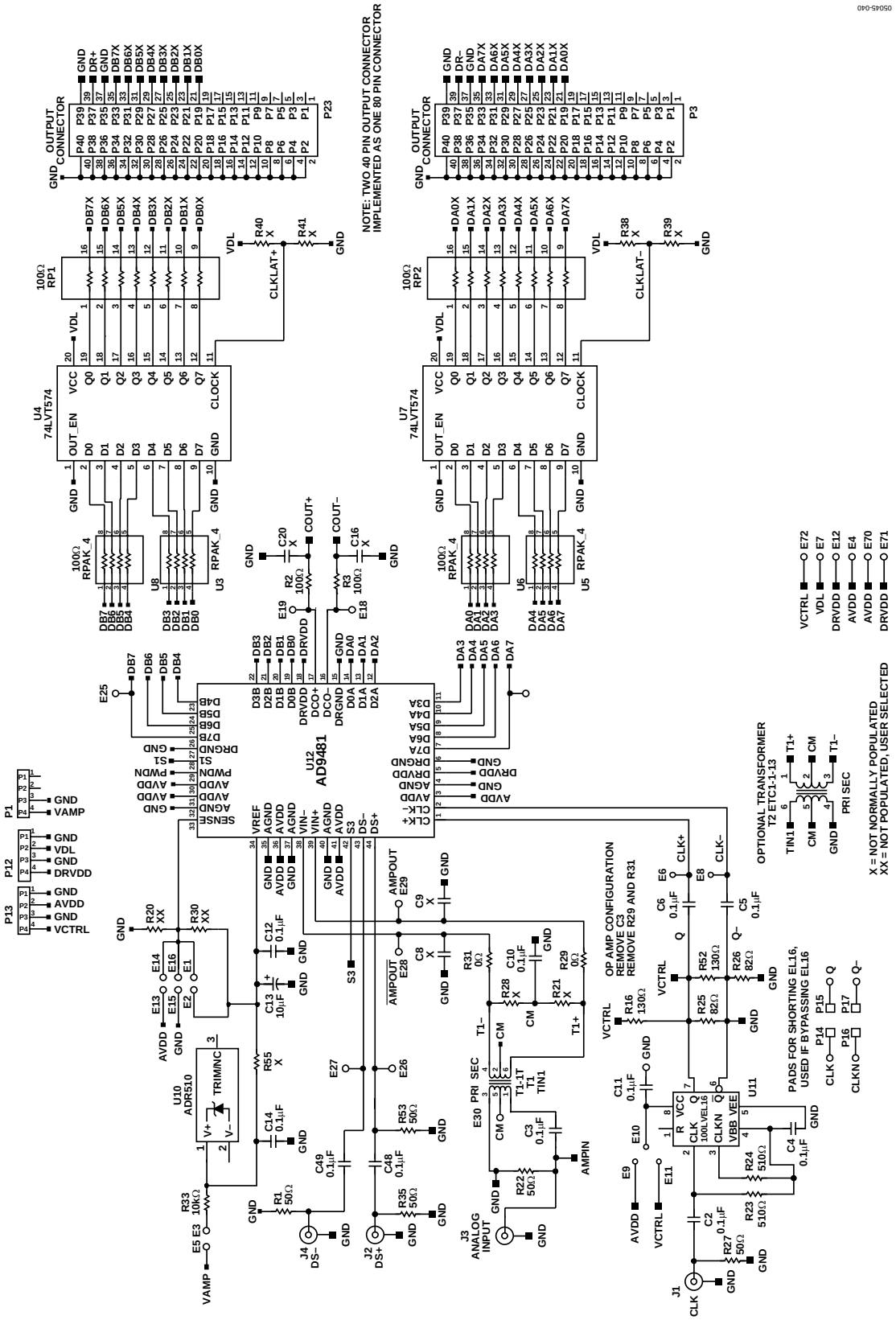


*Figure 39. PCB Schematic (1 of 2)*

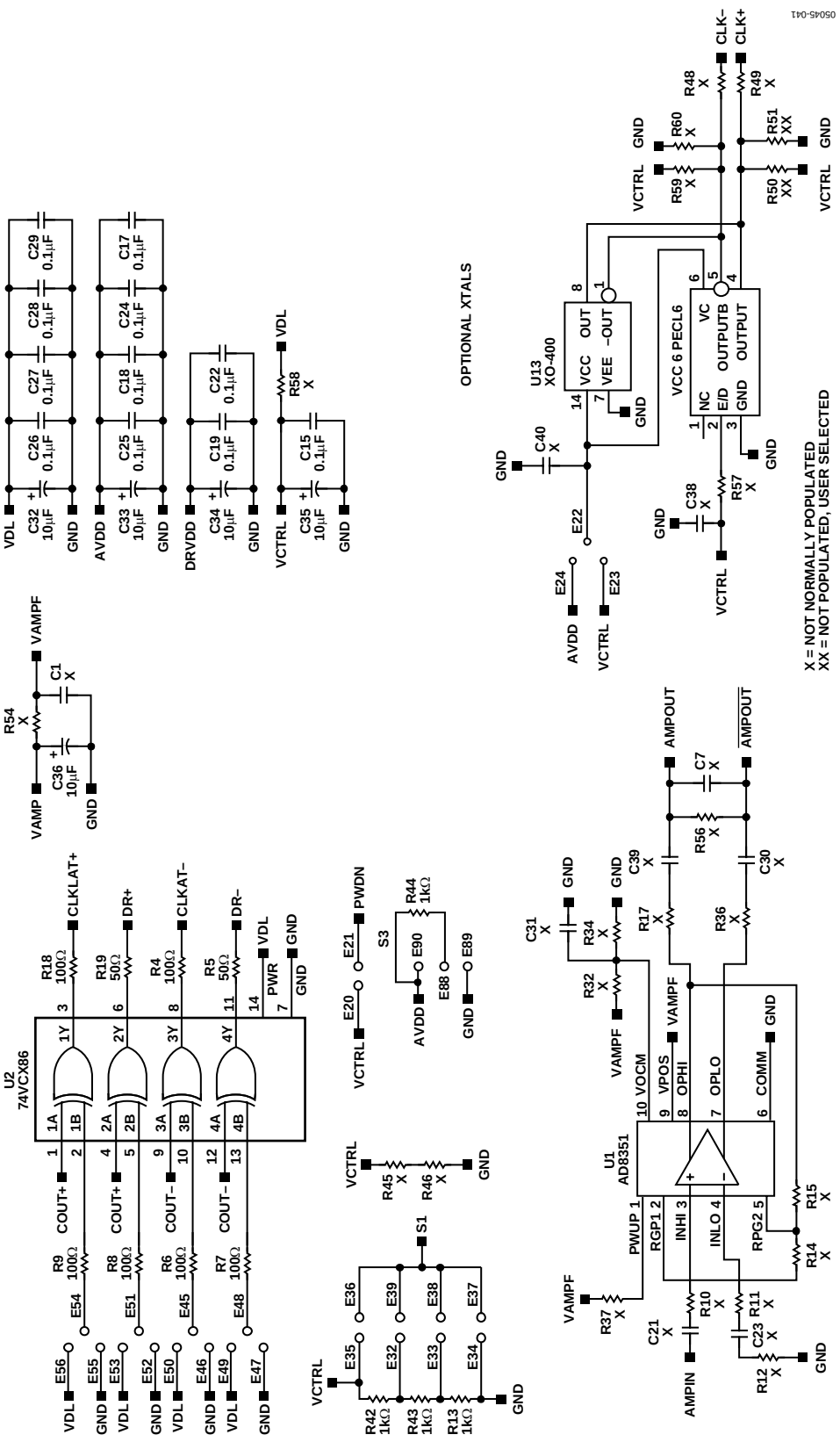



*Figure 40. PCB Schematic (2 of 2)*

# PCB LAYERS

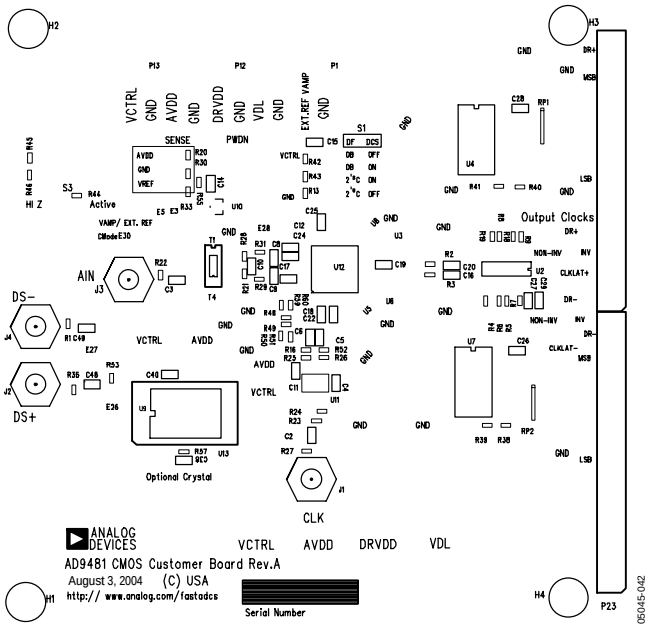



Figure 41. PCB Top-Side Silkscreen

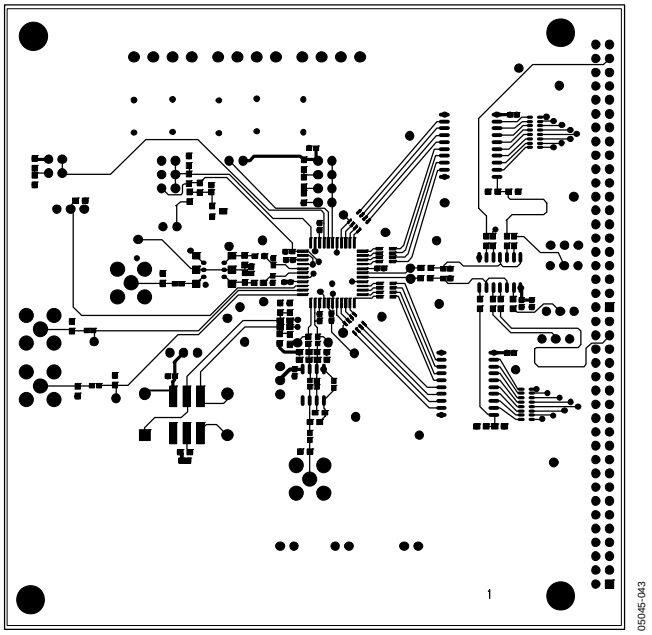



Figure 42. PCB Top-Side Copper Routing

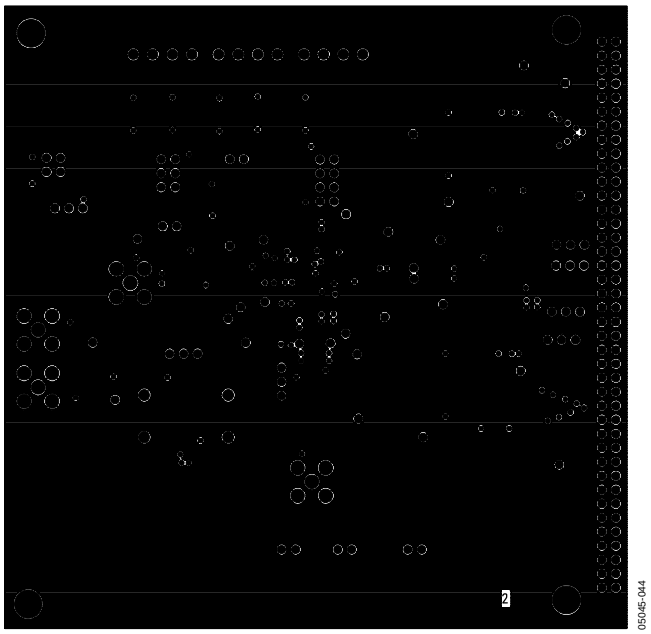



Figure 43. PCB Ground Layer

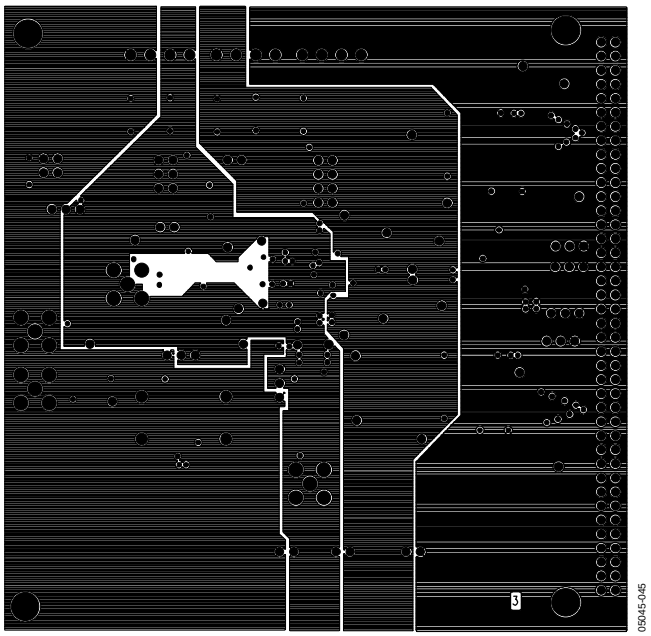



Figure 44. PCB Split Power Plane

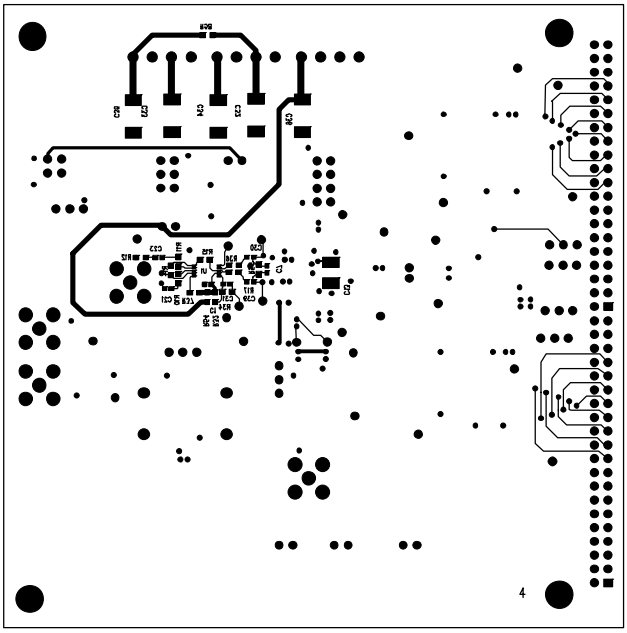



Figure 45. PCB Bottom-Side Copper Routing

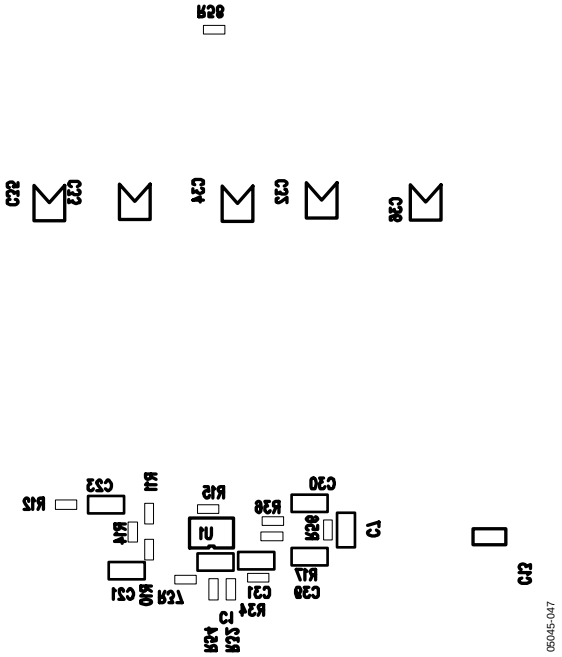
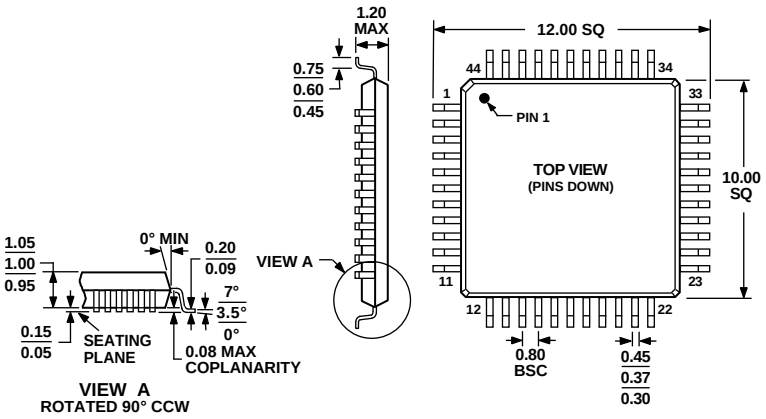



Figure 46. PCB Bottom-Side Silkscreen

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-026ACB

*Figure 47. 44-Lead Thin Plastic Quad Flat Package [TQFP] (SU-44)—Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9481BSUZ-250[1] | –40°C to +85°C | 44-Lead Thin Plastic Quad Flat Package (TQFP) | SU-44 |
| AD9481-PCB[2] | | Evaluation Board | |

[1] Z = Pb-free part.
[2] Evaluation board shipped with AD9481BSUZ-250 installed.