# TCAN1057A-Q1 and TCAN1057AV-Q1 Automotive Fault-Protected CAN FD Transceiver

## 1 Features

- AEC-Q100 (Grade 1) Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2016 physical layer standard
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8 Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- TCAN1057AV I/O voltage range supports 1.7 V to 5.5 V
- Support for 12-V and 24-V battery applications
- Receiver common mode input voltage: ±12 V
- Protection features:
  - Bus fault protection: ±58 V
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
    - Data rates down to 9.2 kbps
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Silent mode
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power up/down glitch free operation on bus and RXD output
- Junction temperature from: –40°C to 150°C
- Available in SOIC (8), small footprint SOT-23 (8), and leadless VSON (8) package with improved automated optical inspection (AOI) capability

## 2 Applications

- Automotive and transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

## 3 Description

The TCAN1057A-Q1 and TCAN1057AV-Q1 are high speed controller area network (CAN) transceivers that meet the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

The transceivers have certified electromagnetic compatibility (EMC) operation making it an ideal choice for classical CAN and CAN FD networks up to 5 megabits per second (Mbps). Upto 8 Mbps operation in simpler networks is possible with these devices. The transceivers support two modes of operation; normal mode and silent mode. The transceivers also include many protection and diagnostic features including thermal shutdown (TSD), TXD-dominant timeout (DTO), and bus fault protection up to ±58 V. The device has defined fail-safe behavior in supply under-voltage or floating pin scenarios.

The transceiver features an integrated level shifter on the $V_{IO}$ pin which supplies internal logic-level translation for interfacing the transceiver I/Os directly to 1.8-V, 2.5-V, 3.3-V, or 5-V logic level.

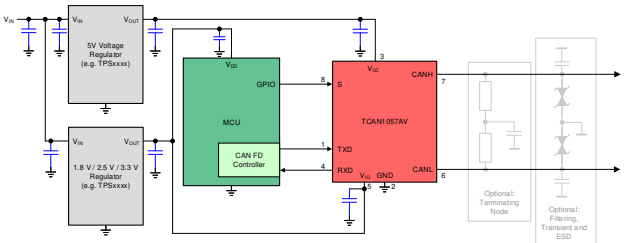
**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TCAN1057A-Q1<br>TCAN1057AV-Q1 | SOT-23 (DDF) (8) | 2.90 mm x 1.60 mm |
| | VSON (DRB) (8) | 3.00 mm x 3.00 mm |
| | SOIC (D) (8) | 4.90 mm x 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Table 3-1. Device Comparison Table**

| Device number | Low voltage I/O logic support on Pin5 | Pin8 Mode selection |
|---|---|---|
| TCAN1057A-Q1 | No | Silent mode |
| TCAN1057AV-Q1 | Yes | Silent mode |




**Simplified Schematic**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (May 2021) to Revision B (November 2021) | Page |
|---|---|
| • Removed Product Preview from the DFF and D packages in the *Device Information* table | 1 |

| Changes from Revision * (February 2021) to Revision A (May 2021) | Page |
|---|---|
| • Changed the document status from: *Advanced Information* to: *Production* data | 1 |

## 5 Pin Configuration and Functions

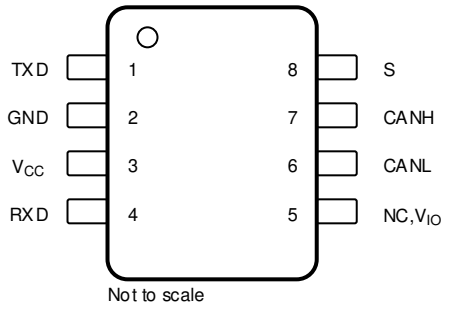



**Figure 5-1. DDF Package, 8-Pin SOT, Top View**

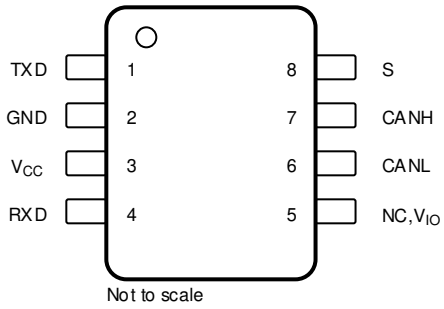



**Figure 5-2. D Package, 8-Pin SOIC, Top View**

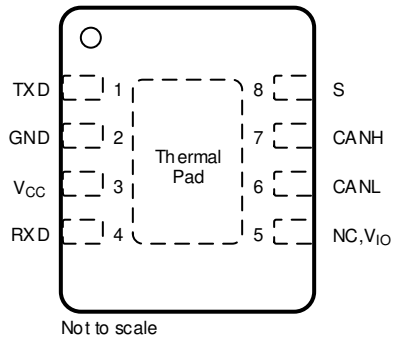



**Figure 5-3. DRB Package, 8-Pin VSON, Top View**

**Table 5-1. Pin Functions**

| Pins | | Type | Description |
|---|---|---|---|
| Name | No. | | |
| TXD | 1 | Digital Input | CAN transmit data input, integrated pull-up |
| GND | 2 | GND | Ground connection |
| $V_{CC}$ | 3 | Supply | 5-V supply voltage |
| RXD | 4 | Digital Output | CAN receive data output, tri-state when powered off |
| NC | 5 | — | No connect (not internally connected); devices without $V_{IO}$ |
| $V_{IO}$ | | Supply | I/O supply voltage |
| CANL | 6 | Bus IO | Low-level CAN bus input/output line |
| CANH | 7 | Bus IO | High-level CAN bus input/output line |
| S | 8 | Digital Input | Silent mode control input, integrated pull-up |
| Thermal Pad (VSON only) | | — | Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.3 | 6 | V |
| $V_{IO}$ | Supply voltage I/O level shifter | –0.3 | 6 | V |
| $V_{BUS}$ | CAN Bus I/O voltage | –58 | 58 | V |
| $V_{DIFF}$ | Max differential voltage between CANH and CANL | –45 | 45 | V |
| $V_{Logic\_Input}$ | Logic input terminal voltage | –0.3 | 6 | V |
| $V_{RXD}$ | RXD output terminal voltage range | –0.3 | 6 | V |
| $I_{O(RXD)}$ | RXD output current | –8 | 8 | mA |
| $T_J$ | Junction temperature | –40 | 165 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | HBM classification level 3A for all pins | ±4000 | V |
| | | | HBM classification level 3B for global pins CANH and CANL with respect to GND | ±10000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins | | ±750 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 ESD Ratings Table — IEC Specifications

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | System level Electrostatic discharge(1) | CAN bus terminals (CANH and CANL) to GND | Unpowered contact discharge per ISO10605 (1) | ±8000 | V |
| | | | SAE J2962-2 per ISO 10605 Powered Contact Discharge (2) | ±8000 | V |
| | | | SAE J2962-2 per ISO 10605 Powered Air Discharge (2) | ±15000 | V |
| $V_{Tran}$ | Transient voltage per ISO 7637-2(3) | | Pulse 1 | –100 | V |
| | | | Pulse 2a | 75 | V |
| | | | Pulse 3a | –150 | V |
| | | | Pulse 3b | 100 | V |
| | Transient voltage per ISO 7637-3(4) | | DCC slow transient pulse | ±30 | V |

(1) Tested according to IEC 62228-3:2019 CAN Transceivers.
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.
(3) Tested according to IEC 62228-3:2019 CAN Transceivers.
(4) Tested according to SAE J2962-2.

## 6.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |

## 6.4 Recommended Operating Conditions (continued)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IO}$ | Supply voltage for I/O level shifter | 1.7 | | 5.5 | V |
| $I_{OH(RXD)}$ | RXD terminal high-level output current, Devices with $V_{IO}$ | –1.5 | | | mA |
| $I_{OL(RXD)}$ | RXD terminal low-level output current, Devices with $V_{IO}$ | | | 1.5 | mA |
| $I_{OH(RXD)}$ | RXD terminal high-level output current, Devices without $V_{IO}$ | –2 | | | mA |
| $I_{OL(RXD)}$ | RXD terminal low-level output current, Devices without $V_{IO}$ | | | 2 | mA |
| $T_J$ | Operating junction temperature | -40 | | 150 | ℃ |

## 6.5 Thermal Characteristics

| THERMAL METRIC(1) | | TCAN1057Ax-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DDF (SOT) | DRB (VSON) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 127.5 | 122 | 55.2 | ℃/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 67.6 | 63 | 62.4 | ℃/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 70.9 | 42.4 | 27.5 | ℃/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 19.3 | 2.4 | 2.3 | ℃/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 70.2 | 42.2 | 27.4 | ℃/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | -- | -- | 11.5 | ℃/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.6 Supply Characteristics

Over recommended operating conditions with $T_J$ = -40℃ to 150℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current Normal mode | Dominant | TXD = 0 V, S = 0 V, $R_L$ = 60 Ω, $C_L$ = open; See Figure 7-1 | | 45 | 70 | mA |
| | | | TXD = 0 V, S = 0 V, $R_L$ = 50 Ω, $C_L$ = open; See Figure 7-1 | | 49 | 80 | mA |
| | | Recessive | TXD = $V_{CC}$ or $V_{IO}$, S = 0 V, $R_L$ = 50 Ω, $C_L$ = open; See Figure 7-1 | | 4.5 | 7.5 | mA |
| | | Dominant with bus fault | TXD = 0 V, S = 0 V, CANH = CANL = ±25 V, $R_L$ = open, $C_L$ = open; See Figure 7-1 | | | 130 | mA |
| | Supply current Silent mode | | TXD = S = $V_{CC}$ or $V_{IO}$, $R_L$ = 50 Ω, $C_L$ = open; See Figure 7-1 | | | 2.1 | mA |
| $I_{IO}$ | I/O supply current Normal mode, Devices with $V_{IO}$ | Dominant | S = 0 V, TXD = 0 V RXD floating | | 125 | 300 | µA |
| | | Recessive | TXD = $V_{IO}$ , S = 0 V RXD floating | | 25 | 48 | µA |
| $UV_{CC}$ | Rising undervoltage detection on $V_{CC}$ for protected mode | | | | 4.2 | 4.4 | V |
| | Falling undervoltage detection on $V_{CC}$ for protected mode | | | 3.5 | 4 | 4.25 | V |
| $V_{HYS(UVCC)}$ | Hysteresis voltage on $UV_{CC}$ | | | | 200 | | mV |
| $UV_{VIO}$ | Rising undervoltage detection on $V_{IO}$ (Devices with $V_{IO}$) | | | | 1.56 | 1.65 | V |
| | Falling undervoltage detection on $V_{IO}$ (Devices with $V_{IO}$) | | | 1.4 | 1.51 | 1.59 | V |
| $V_{HYS(UVIO)}$ | Hysteresis voltage on $UV_{IO}$ | | | | 40 | | mV |

## 6.7 Dissipation Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Average power dissipation Normal mode | $V_{CC}$ = 5 V, $V_{IO}$ = 1.8 V, $T_J$= 27°C, $R_L$ = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 95 | | mW |
| | | $V_{CC}$ = 5 V, $V_{IO}$ = 3.3 V, $T_J$= 27°C, $R_L$ = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 95 | | mW |
| | | $V_{CC}$ = 5 V, $V_{IO}$ = 5 V, $T_J$= 27°C, $R_L$ = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 95 | | mW |
| | | $V_{CC}$ = 5.5 V, $V_{IO}$ = 1.8 V, $T_A$= 150°C, $R_L$ = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 120 | | mW |
| | | $V_{CC}$ = 5.5 V, $V_{IO}$ = 3.3 V, $T_A$= 150°C, $R_L$ = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 120 | | mW |
| | | $V_{CC}$ = 5.5 V, $V_{IO}$ = 5 V, $T_A$= 150°C, $R_L$ = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 120 | | mW |
| $T_{TSD}$ | Thermal shutdown temperature | | 175 | 195 | 210 | °C |
| $T_{TSD(HYS)}$ | Thermal shutdown hysteresis | | | 12 | | °C |

## 6.8 Electrical Characteristics

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver Electrical Characteristics** | | | | | | | |
| $V_{O(DOM)}$ | Dominant output voltage Normal mode | CANH | S = 0 V, TXD = 0 V<br>50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open, $R_{CM}$ = open;<br>See Figure 7-2 | 2.75 | | 4.5 | V |
| | | CANL | | 0.5 | | 2.25 | V |
| $V_{O(REC)}$ | Recessive output voltage Normal or silent mode | CANH and CANL | S = 0 V, TXD = $V_{IO}$<br>$R_L$ = open (no load), $R_{CM}$ = open<br>See Figure 7-2 | 2 | 0.5 $V_{CC}$ | 3 | V |
| $V_{SYM}$ | Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/$V_{CC}$ | | S = 0 V, TXD = 250 kHz, 1 MHz, 2.5 MHz<br>$R_L$ = 60 Ω, $C_{SPLIT}$ = 4.7 nF, $C_L$ = open,<br>$R_{CM}$ = open;<br>See Figure 7-2 and Figure 9-2 | 0.9 | | 1.1 | V/V |
| $V_{SYM\_DC}$ | DC output symmetry ($V_{CC}$ - $V_{O(CANH)}$ - $V_{O(CANL)}$) | | S = 0 V<br>$R_L$ = 60 Ω, $C_L$ = open;<br>See Figure 7-2 | –400 | | 400 | mV |
| $V_{OD(DOM)}$ | Differential output voltage Normal mode Dominant | CANH - CANL | S = 0 V, TXD = 0 V<br>50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open;<br>See Figure 7-2 | 1.5 | | 3 | V |
| | | | S = 0 V, TXD = 0 V<br>45 Ω ≤ $R_L$ ≤ 70 Ω, $C_L$ = open;<br>See Figure 7-2 | 1.4 | | 3.3 | V |
| | | | S = 0 V, TXD = 0 V<br>$R_L$ = 2240 Ω, $C_L$ = open;<br>See Figure 7-2 | 1.5 | | 5 | V |
| $V_{OD(REC)}$ | Differential output voltage Normal mode Recessive | CANH - CANL | S = 0 V, TXD = $V_{IO}$<br>$R_L$ = 60 Ω, $C_L$ = open;<br>See Figure 7-2 | –120 | | 12 | mV |
| | | | S = 0 V, TXD = $V_{IO}$<br>$R_L$ = open, $C_L$ = open;<br>See Figure 7-2 | –50 | | 50 | mV |
| $I_{OS(SS\_DOM)}$ | Short-circuit steady-state output current, dominant Normal mode | | S = 0 V, TXD = 0 V<br>$V_{(CANH)}$ = -15 V to 40 V, CANL = open;<br>See Figure 7-7 | –115 | | | mA |
| | | | S = 0 V, TXD = 0 V<br>$V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open;<br>See Figure 7-7 | | | 115 | mA |

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OS(SS\_REC)}$ | Short-circuit steady-state output current, recessive<br>Normal mode | S = 0 V, TXD = $V_{IO}$<br>–27 V ≤ $V_{BUS}$ ≤ 32 V, where $V_{BUS}$ = CANH = CANL;<br>See Figure 7-7 | –5 | | 5 | mA |
| **Receiver Electrical Characteristics** | | | | | | |
| $V_{IT}$ | Input threshold voltage<br>Normal and silent mode | S = 0 V, -12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-6 | 500 | | 900 | mV |
| $V_{DOM}$ | Dominant state differential input voltage range<br>Normal and silent mode | S = 0 V, -12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-6 | 0.9 | | 9 | V |
| $V_{REC}$ | Recessive state differential input voltage range<br>Normal and silent mode | S = 0 V, -12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-6 | -4 | | 0.5 | V |
| $V_{HYS}$ | Hysteresis voltage for input threshold<br>Normal mode | S = 0 V, -12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-6 | | 115 | | mV |
| $V_{CM}$ | Common-mode range<br>Normal and silent mode | See Figure 7-3 and Table 8-6 | –12 | | 12 | V |
| $I_{LKG(IOFF)}$ | Unpowered bus input leakage current | CANH = CANL = 5 V, $V_{CC}$ = $V_{IO}$ = GND | | | 5 | µA |
| $C_I$ | Input capacitance to ground (CANH or CANL) | TXD = $V_{IO}$ (1) | | | 20 | pF |
| $C_{ID}$ | Differential input capacitance | | | | 10 | pF |
| $R_{ID}$ | Differential input resistance | TXD = $V_{IO}$ (1), S = 0 V, -12 V ≤ $V_{CM}$ ≤ 12 V | 40 | | 90 | kΩ |
| $R_{IN}$ | Single-ended input resistance (CANH or CANL) | | 20 | | 45 | kΩ |
| $R_{IN(M)}$ | Input resistance matching<br>[1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 % | $V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V | –1 | | 1 | % |
| **TXD Terminal (CAN Transmit Data Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | Devices without $V_{IO}$ | 0.7 $V_{CC}$ | | | V |
| $V_{IH}$ | High-level input voltage | Devices with $V_{IO}$ | 0.7 $V_{IO}$ | | | V |
| $V_{IL}$ | Low-level input voltage | Devices without $V_{IO}$ | | | 0.3 $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | Devices with $V_{IO}$ | | | 0.3 $V_{IO}$ | V |
| $I_{IH}$ | High-level input leakage current | TXD = $V_{CC}$ = $V_{IO}$ = 5.5 V | –2.5 | 0 | 1 | µA |
| $I_{IL}$ | Low-level input leakage current | TXD = 0 V<br>$V_{CC}$= $V_{IO}$ = 5.5 V | –200 | -100 | –20 | µA |
| $I_{LKG(OFF)}$ | Unpowered leakage current | TXD = 5.5 V<br>$V_{CC}$= $V_{IO}$ = 0 V | –1 | 0 | 1 | µA |
| $C_I$ | Input capacitance | $V_{IN}$ = 0.4×sin(2×π×2×$10^6$×t)+2.5 V | | 5 | | pF |
| **RXD Terminal (CAN Receive Data Output)** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_O$ = –2 mA<br>Devices without $V_{IO}$;<br>See Figure 7-3 | 0.8 $V_{CC}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_O$ = –1.5 mA<br>Devices with $V_{IO}$;<br>See Figure 7-3 | 0.8 $V_{IO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 2mA<br>Devices without $V_{IO}$;<br>See Figure 7-3 | | | 0.2 $V_{CC}$ | V |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 1.5mA<br>Devices with $V_{IO}$;<br>See Figure 7-3 | | | 0.2 $V_{IO}$ | V |
| $I_{LKG(OFF)}$ | Unpowered leakage current | RXD = 5.5 V<br>$V_{CC}$ = $V_{IO}$ = 0 V | –1 | 0 | 1 | µA |
| **S Terminal (Silent Mode Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | Devices without $V_{IO}$ | 0.7 $V_{CC}$ | | | V |
| $V_{IH}$ | High-level input voltage | Devices with $V_{IO}$ | 0.7 $V_{IO}$ | | | V |
| $V_{IL}$ | Low-level input voltage | Devices without $V_{IO}$ | | | 0.3 $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | Devices with $V_{IO}$ | | | 0.3 $V_{IO}$ | V |
| $I_{IH}$ | High-level input leakage current | $V_{CC}$ = $V_{IO}$ = S = 5.5 V | –2 | | 2 | µA |

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with $T_J$ = -40℃ to 150℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Low-level input leakage current | S = 0 V<br>$V_{CC}$ = $V_{IO}$ = 5.5 V, | –20 | | –2 | µA |
| $I_{LKG(OFF)}$ | Unpowered leakage current | S = 5.5V<br>$V_{CC}$ = $V_{IO}$ = 0 V | –1 | 0 | 1 | µA |

(1) $V_{IO}$ = $V_{CC}$ in non-V variants of device

## 6.9 Switching Characteristics

Over recommended operating conditions with $T_J$ = -40℃ to 150℃ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Device Switching Characteristics** | | | | | | |
| $t_{PROP(LOOP1)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), recessive to dominant | S = 0 V, $V_{IO}$ = 2.8 V to 5.5 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 125 | 210 | ns |
| $t_{PROP(LOOP1)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), recessive to dominant | S = 0 V, $V_{IO}$ = 1.7 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 165 | 255 | ns |
| $t_{PROP(LOOP2)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), dominant to recessive | S = 0 V, $V_{IO}$ = 2.8 V to 5.5 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 150 | 210 | ns |
| $t_{PROP(LOOP2)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), dominant to recessive | S = 0 V, $V_{IO}$ = 1.7 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 180 | 255 | ns |
| $t_{MODE}$ | Mode change time, from normal to standby or from standby to normal | See Figure 7-5 | | | 20 | µs |
| **Driver Switching Characteristics** | | | | | | |
| $t_{pHR}$ | Propagation delay time, high TXD to driver recessive (dominant to recessive) | S = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF;<br>See Figure 7-2 | | 80 | | ns |
| $t_{pLD}$ | Propagation delay time, low TXD to driver dominant (recessive to dominant) | | | 70 | | ns |
| $t_{sk(p)}$ | Pulse skew (\|tpHR - tpLD\|) | | | 14 | | ns |
| $t_R$ | Differential output signal rise time | | | 25 | | ns |
| $t_F$ | Differential output signal fall time | | | 50 | | ns |
| $t_{TXD\_DTO}$ | Dominant timeout | S = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF;<br>See Figure 7-6 | 1.2 | | 4.0 | ms |
| **Receiver Switching Characteristics** | | | | | | |
| $t_{pRH}$ | Propagation delay time, bus recessive input to high output (dominant to recessive) | S = 0 V<br>$C_{L(RXD)}$ = 15 pF;<br>See Figure 7-3 | | 81 | | ns |
| $t_{pDL}$ | Propagation delay time, bus dominant input to low output (recessive to dominant) | | | 66 | | ns |
| $t_R$ | RXD output signal rise time | | | 10 | | ns |
| $t_F$ | RXD output signal fall time | | | 10 | | ns |
| **FD Timing Characteristics** | | | | | | |

## 6.9 Switching Characteristics (continued)

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{BIT(BUS)}$ | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 500 ns | S = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF<br>$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ ;<br>See Figure 7-4 | 450 | | 525 | ns |
| | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 200 ns | | 160 | | 205 | ns |
| | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 125 ns(1) | | 85 | | 130 | ns |
| $t_{BIT(RXD)}$ | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 500 ns | | 410 | | 540 | ns |
| | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 200 ns | | 130 | | 210 | ns |
| | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 125 ns(1) | | 75 | | 135 | ns |
| $\Delta t_{REC}$ | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 500 ns | | -50 | | 20 | ns |
| | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 200 ns | | -40 | | 10 | ns |
| | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 125 ns(1) | | -40 | | 10 | ns |

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

# 7 Parameter Measurement Information

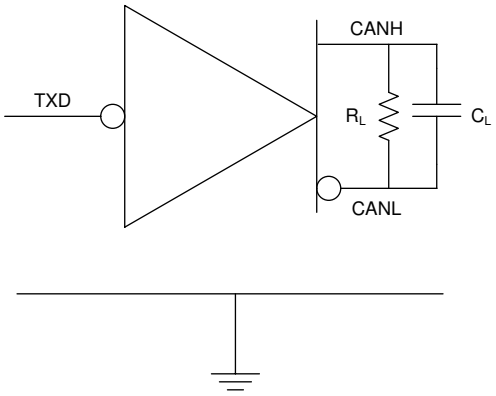
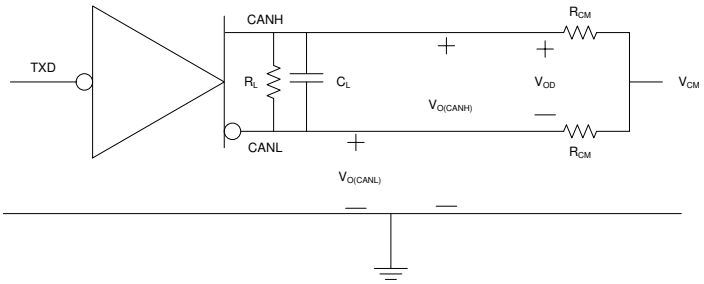



**Figure 7-1. $I_{CC}$ Test Circuit**



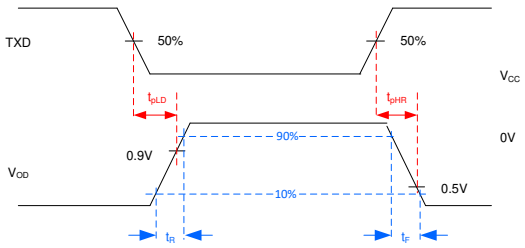
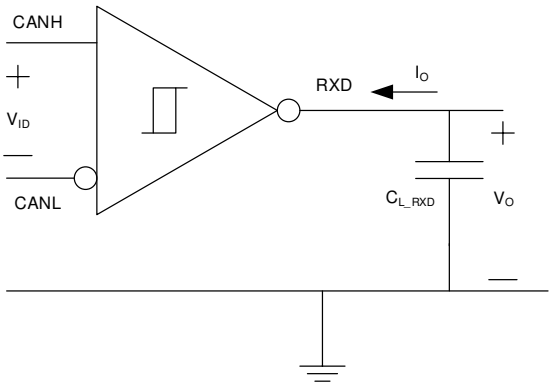




**Figure 7-2. Driver Test Circuit and Measurement**



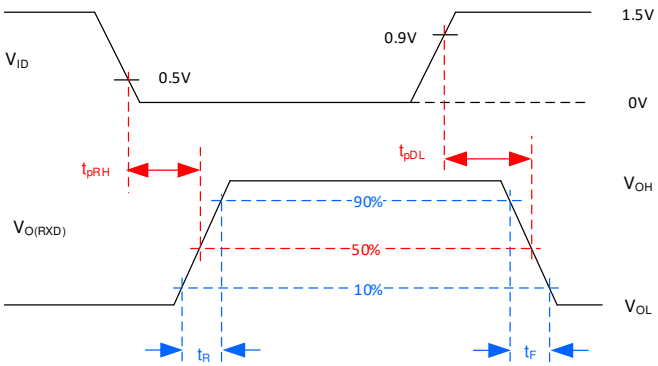




**Figure 7-3. Receiver Test Circuit and Measurement**

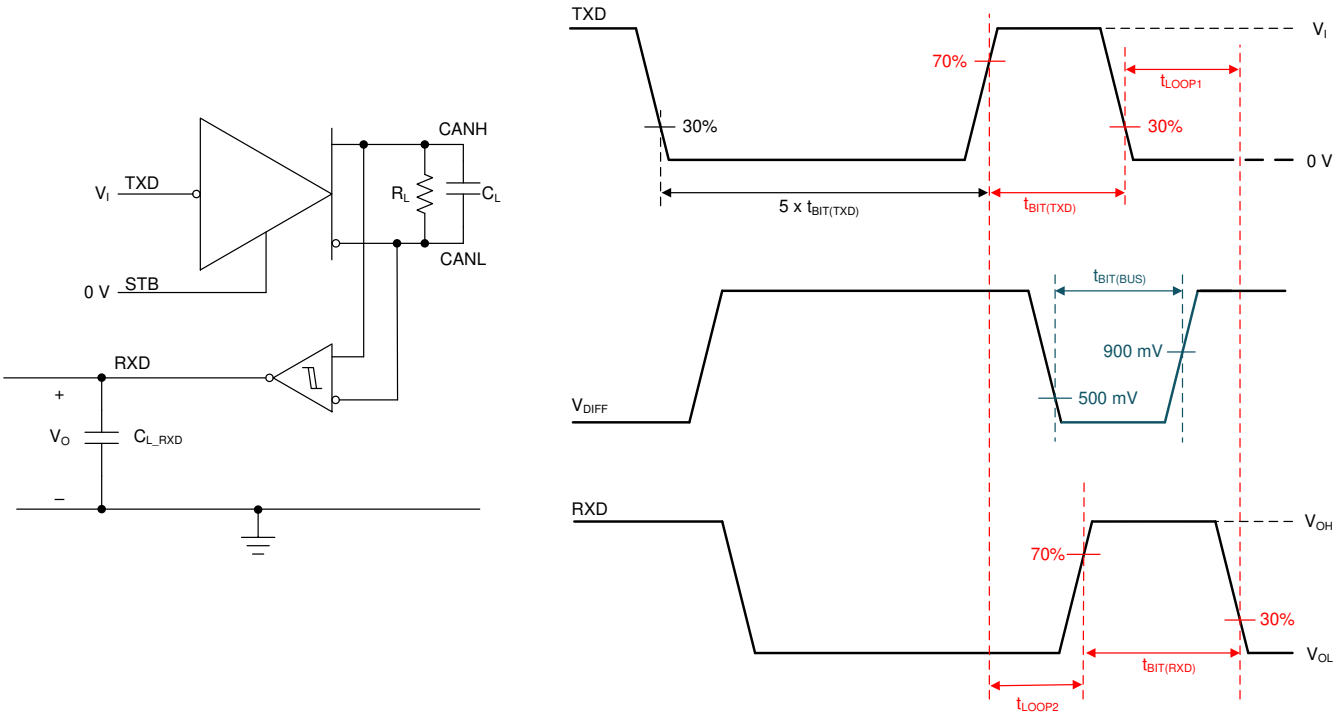



**Figure 7-4. Transmitter and Receiver Timing Test Circuit and Measurement**

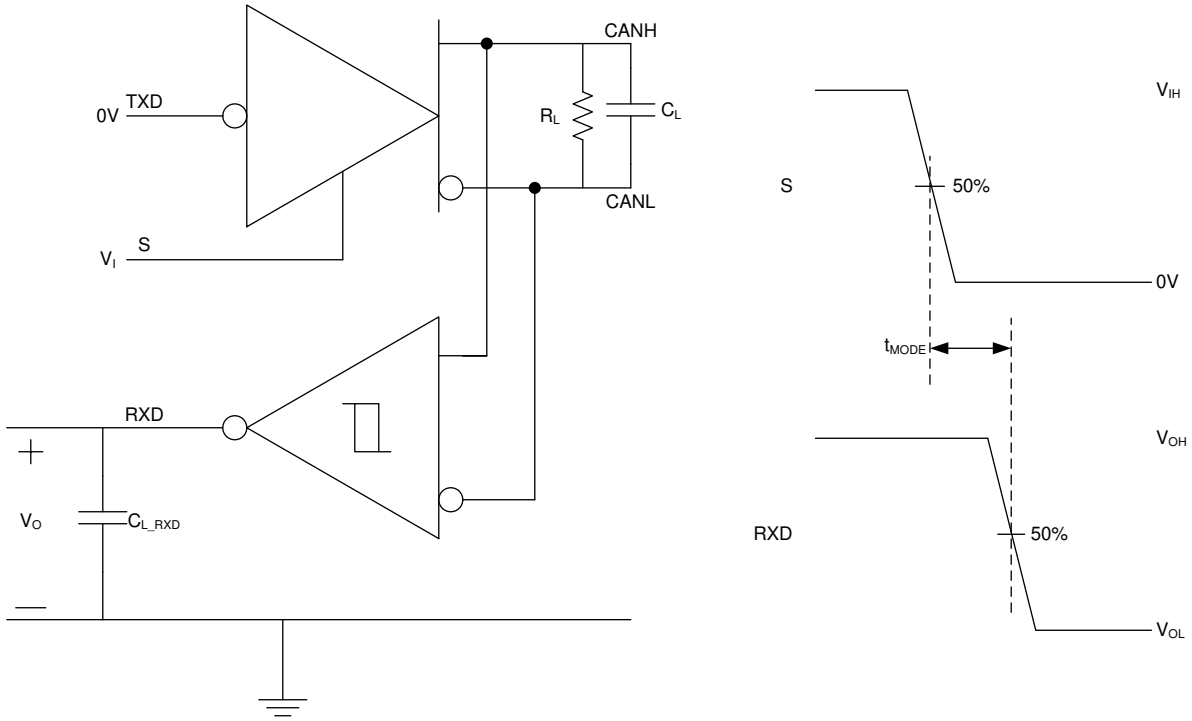



**Figure 7-5. $t_{MODE}$ Test Circuit and Measurement**

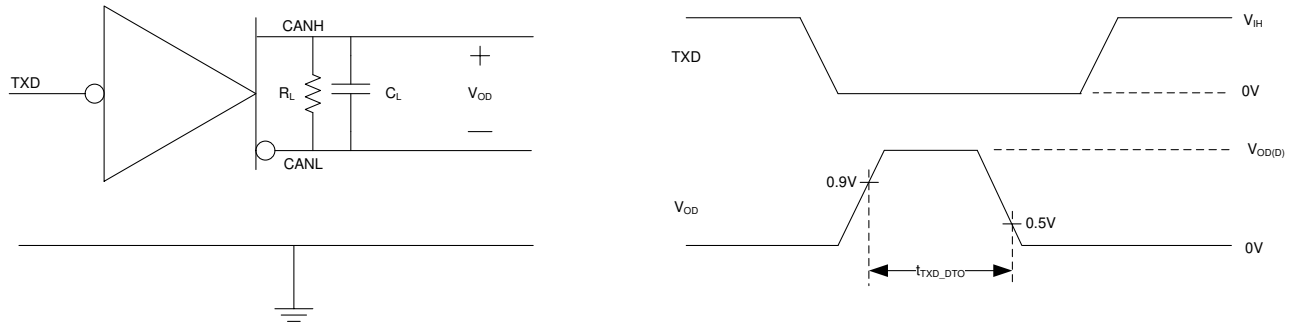



**Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement**

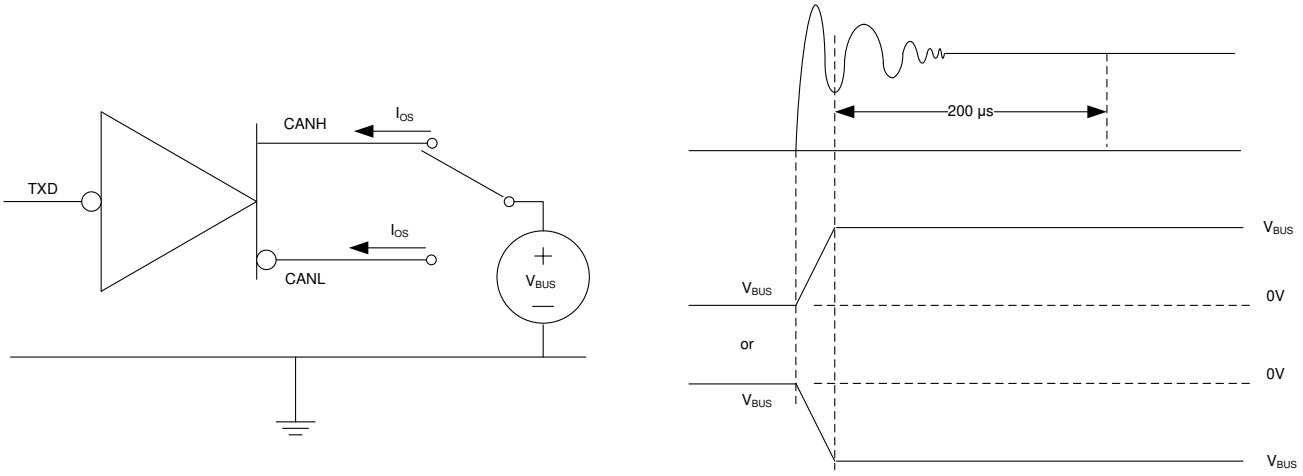



**Figure 7-7. Driver Short-Circuit Current Test and Measurement**

# 8 Detailed Description

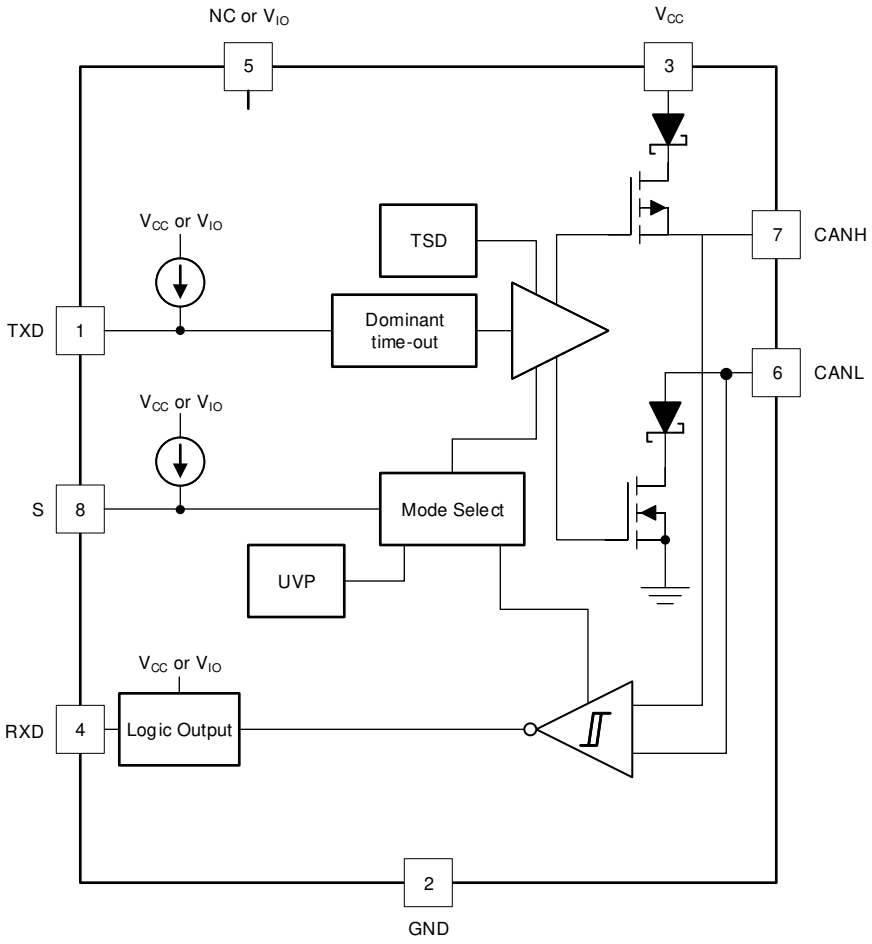
## 8.1 Overview

The TCAN1057A(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The devices support the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance Test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Pin Description

#### *8.3.1.1 TXD*

The TXD input is a logic-level signal, referenced to either $V_{CC}$ or $V_{IO}$ from a CAN controller to the transceivers.

#### *8.3.1.2 GND*

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

#### *8.3.1.3 $V_{CC}$*

$V_{CC}$ provides the 5-V power supply to the CAN transceiver.

#### *8.3.1.4 RXD*

The RXD output is a logic-level signal, referenced to either $V_{CC}$ or $V_{IO}$, from the transceivers to the CAN controller. RXD is only driven once $V_{IO}$ is present.

#### *8.3.1.5 $V_{IO}$*

The $V_{IO}$ pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. The $V_{IO}$ pin should be connected to the controller's I/O voltage source.

#### *8.3.1.6 CANH and CANL*

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

#### *8.3.1.7 S (Silent)*

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation than the S pin can be tied directly to system GND using a pull-down resistor. If silent mode is the only intended mode of operation than the S pin can be tied directly to a static system voltage source using a pull-up resistor.

### 8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors $R_{IN}$) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

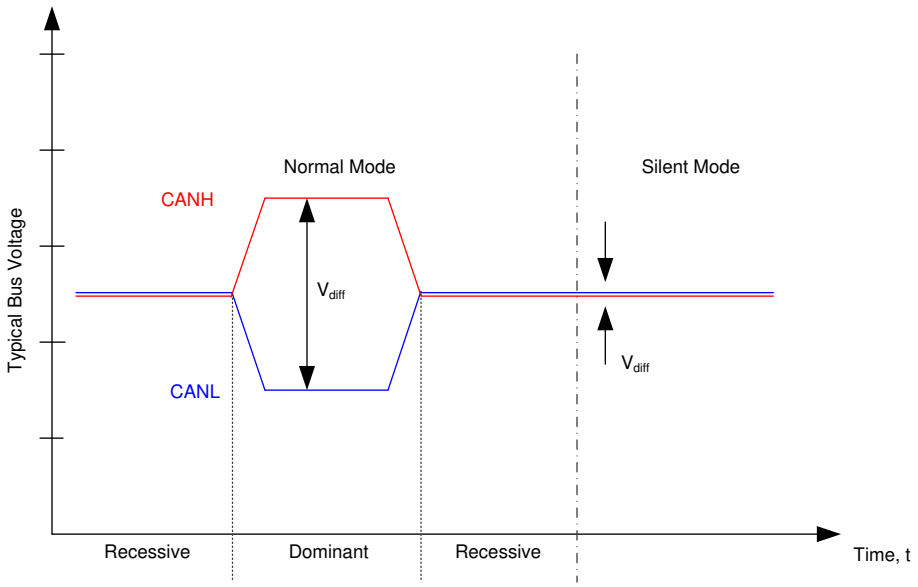



**Figure 8-1. Bus States**

### 8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period $t_{TXD\_DTO}$. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, $t_{TXD\_DTO}$, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

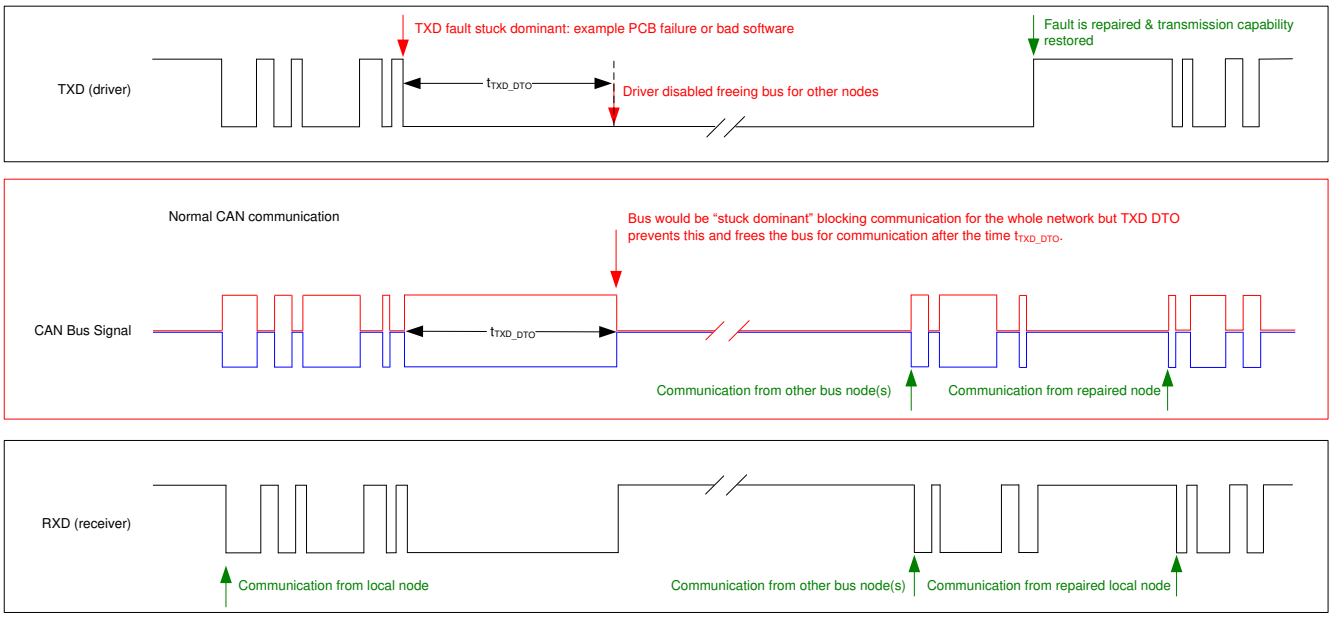



**Figure 8-2. Example Timing Diagram for TXD Dominant Timeout**

### 8.3.4 CAN Bus short-circuit current limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers $V_{CC}$ supply.

### 8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold, $T_{TSD}$, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below $T_{TSD}$. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

### 8.3.6 Undervoltage Lockout

The supply pins, $V_{CC}$ and $V_{IO}$, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

**Table 8-1. Undervoltage Lockout - TCAN1057A-Q1**

| $V_{CC}$ | DEVICE STATE | BUS | RXD PIN |
|---|---|---|---|
| > $UV_{VCC}$ | Normal | Per TXD | Mirrors bus |
| < $UV_{VCC}$ | Protected | High impedance<br>Weak pull-down to ground(1) | High impedance |

(1) $V_{CC}$ = GND, see $I_{LKG(OFF)}$

**Table 8-2. $V_{IO}$ Undervoltage Lockout - TCAN1057AV-Q1**

| $V_{CC}$ | $V_{IO}$ | DEVICE STATE | BUS | RXD PIN |
|---|---|---|---|---|
| > $UV_{VCC}$ | > $UV_{VIO}$ | Normal | Per TXD | Mirrors bus |
| < $UV_{VCC}$ | > $UV_{VIO}$ | S = $V_{IO}$: Silent mode | High impedance<br>Weak pull-down to ground(1) | Recessive |
| | | S = GND: Protected mode | | |
| > $UV_{VCC}$ | < $UV_{VIO}$ | Protected | | High impedance |
| < $UV_{VCC}$ | < $UV_{VIO}$ | Protected | | High impedance |

(1) $V_{CC}$ = GND, see $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and $t_{MODE}$ has expired the device transitions to normal mode and the host controller can send and receive CAN traffic again.

### 8.3.7 Unpowered Device

The device is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

### 8.3.8 Floating pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 8-3 for details on pin bias conditions.

**Table 8-3. Pin Bias**

| Pin | Pull-up or Pull-down | Comment |
|---|---|---|
| TXD | Pull-up | Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering |
| S | Pull-up | Weakly biases S towards low-power silent mode to prevent excessive system power |

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

The device has two main operating modes; normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

**Table 8-4. Operating Modes**

| S | Device Mode | Driver | Receiver | RXD Pin |
|---|---|---|---|---|
| High | Silent mode | Disabled | Enabled | Mirrors bus state |
| Low | Normal Mode | Enabled | Enabled | |

### 8.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

### 8.4.3 Silent Mode

In silent mode the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN1057A(V)-Q1 is reduced in silent mode due to the CAN driver being disabled.

### 8.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to either $V_{CC}$ or $V_{IO}$.

**Table 8-5. Driver Function Table**

| Device Mode | TXD Input(1) | Bus Outputs | | Driven Bus State(2) |
|---|---|---|---|---|
| | | CANH | CANL | |
| Normal | Low | High | Low | Dominant |
| | High or open | High impedance | High impedance | Biased recessive |
| Silent | X | High impedance | High impedance | Biased recessive |

(1) X = irrelevant
(2) For bus state see Figure 8-1

**Table 8-6. Receiver Function Table Normal and Silent Mode**

| Device Mode | CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$ | Bus State | RXD Pin |
|---|---|---|---|
| Normal or Silent | $V_{ID} \geq 0.9$ V | Dominant | Low |
| | 0.5 V < $V_{ID}$ < 0.9 V | Undefined | Undefined |
| | $V_{ID} \leq 0.5$ V | Recessive | High |
| Any | Open ($V_{ID} \approx 0$ V) | Open | High |

# 9 Application Information Disclaimer

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

## 9.2 Typical Application

Figure 9-1 shows a typical configuration for 5 V system using the device. The bus termination is shown for illustrative purposes.

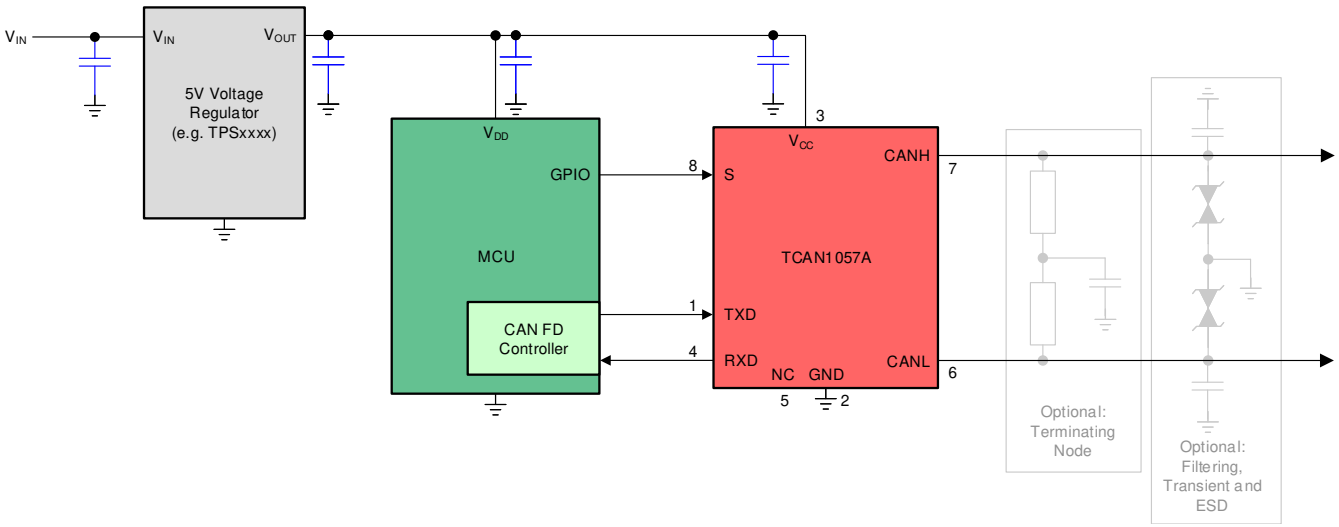



**Figure 9-1. Transceiver Application Using 5 V I/O Connections**

### 9.2.1 Design Requirements

#### *9.2.1.1 CAN Termination*

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

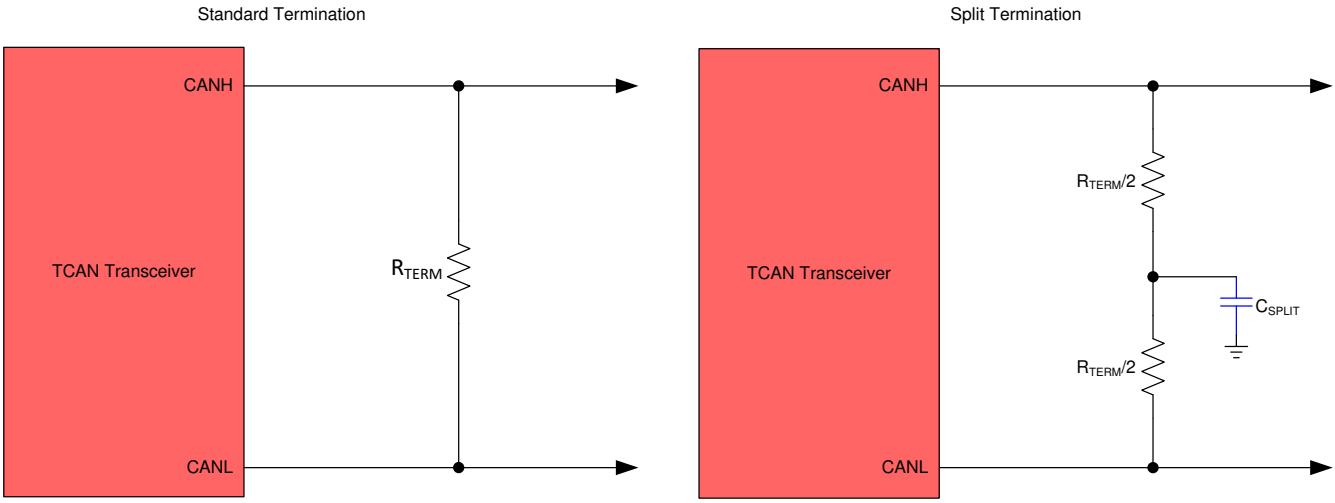



**Figure 9-2. CAN Bus Termination Concepts**

### 9.2.2 Detailed Design Procedures

#### *9.2.2.1 Bus Loading, Length and Number of Nodes*

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1057A(V)-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1057A(V)-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the transceiver is a minimum of 40 kΩ. If 100 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1057A(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

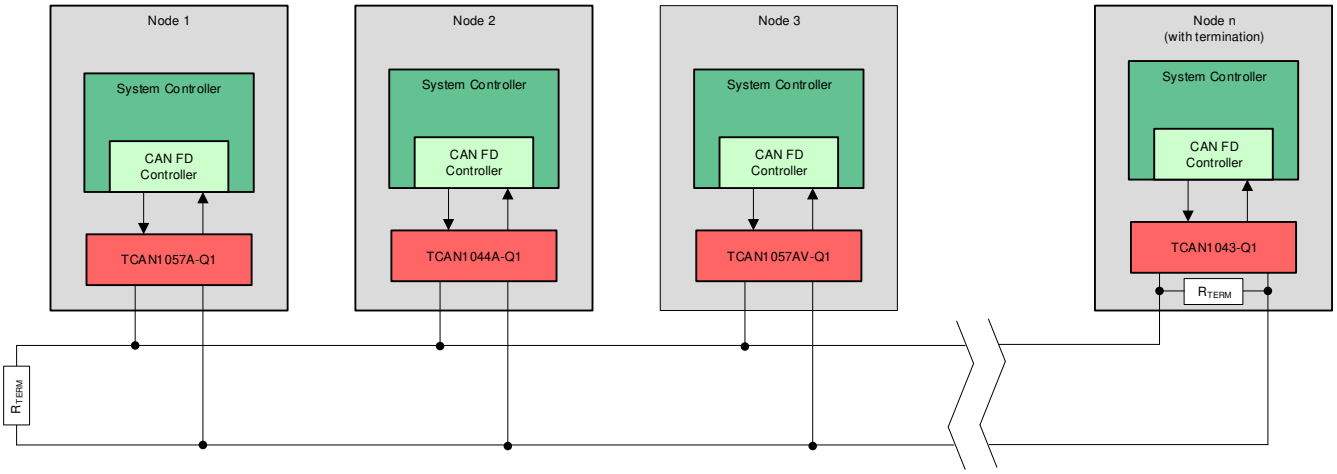
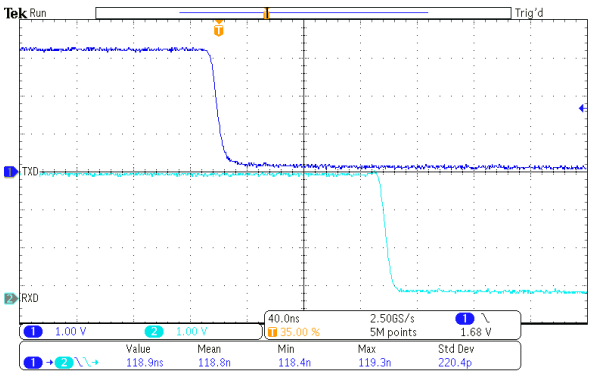


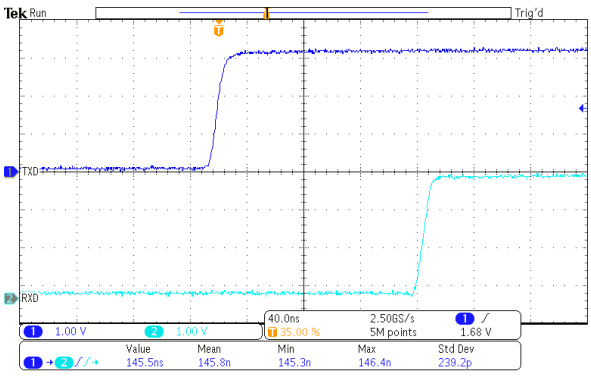

**Figure 9-3. Typical CAN Bus**

### 9.2.3 Application Curves




$V_{CC}$ = 5 V $V_{IO}$ = 3.3 V $R_L$ = 60 Ω

**Figure 9-4. $t_{PROP(LOOP1)}$**




$V_{CC}$ = 5 V $V_{IO}$ = 3.3 V $R_L$ = 60 Ω

**Figure 9-5. $t_{PROP(LOOP2)}$**

### 9.2.4 System Examples

Figure 9-6 shows a typical configuration for 1.8 V, 2.5 V, or 3.3 V systems using the TCAN1057AV. The bus termination is shown for illustrative purposes.

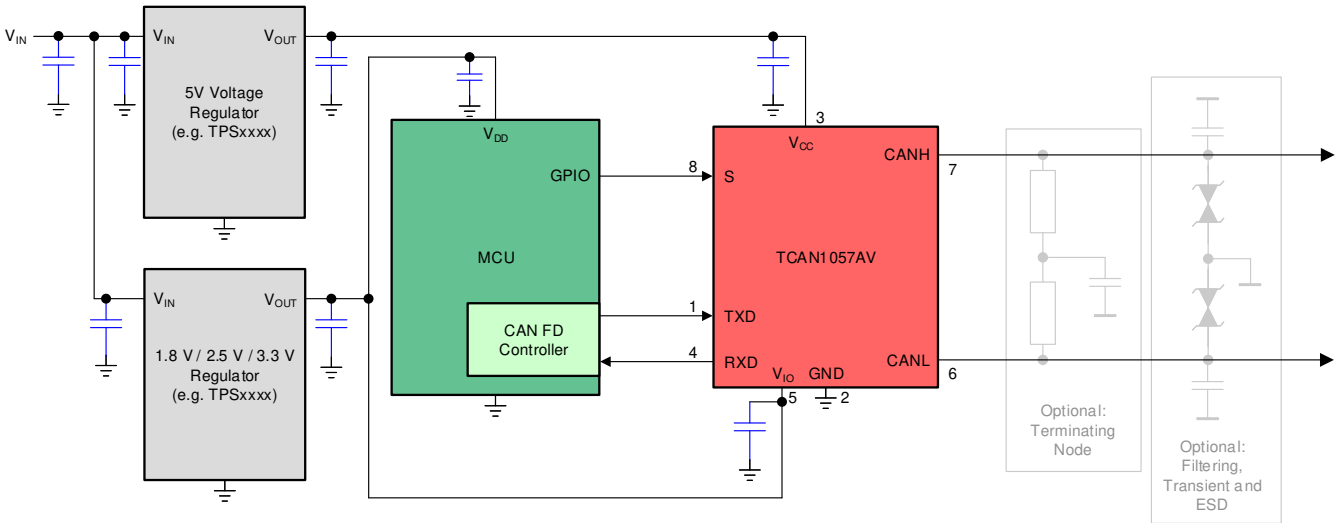



**Figure 9-6. Typical Transceiver Application Using 1.8 V, 2.5 V, 3.3 V IO Connections**

## 10 Power Supply Recommendations

The TCAN1057A transceiver is designed to operate with a main $V_{CC}$ input voltage supply range between 4.5 V and 5.5 V. The TCAN1057AV implements an I/O level shifting supply input, $V_{IO}$, designed for a range between 1.7 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main $V_{CC}$ supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's $V_{IO}$ supply pin in addition to bypass capacitors.

# Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

## 11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins $V_{CC}$ and $V_{IO}$ of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

**Note**

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

## 11.2 Layout Example

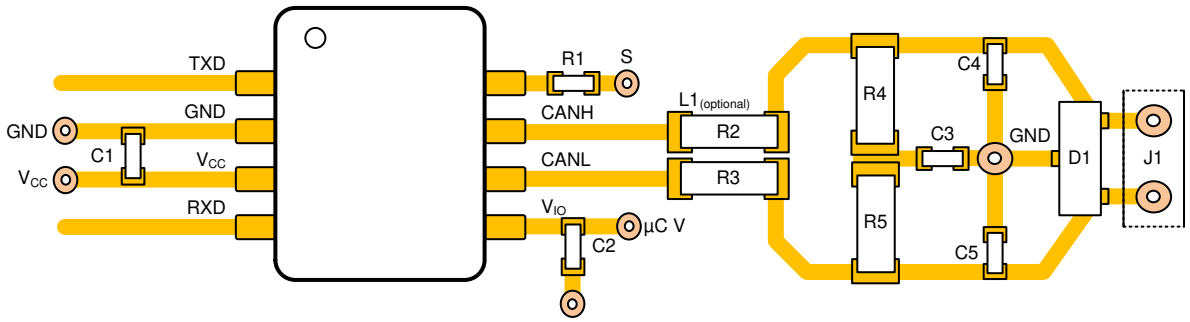



**Figure 11-1. Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAN1057ADDFRQ1 | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 2HEF | Samples |
| TCAN1057ADRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1057A | Samples |
| TCAN1057ADRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 1057A | Samples |
| TCAN1057AVDDFRQ1 | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 2HFF | Samples |
| TCAN1057AVDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1057AV | Samples |
| TCAN1057AVDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 1057AV | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

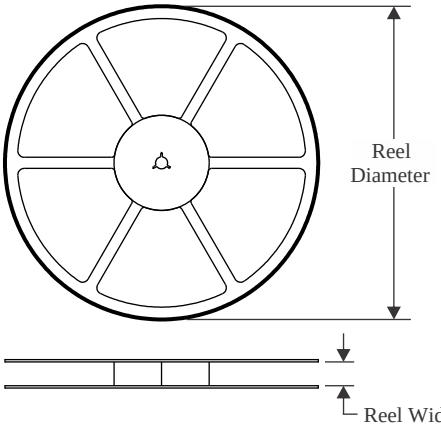
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

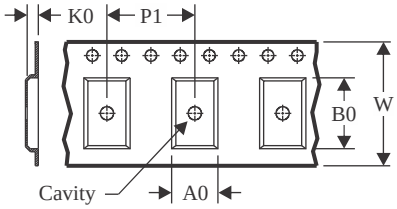
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

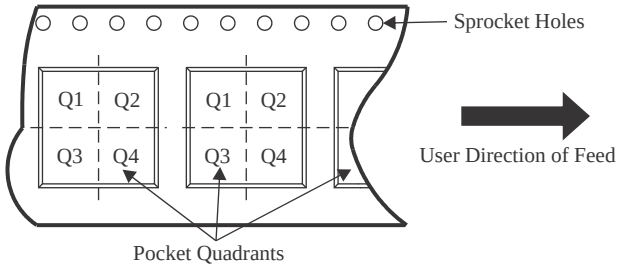



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

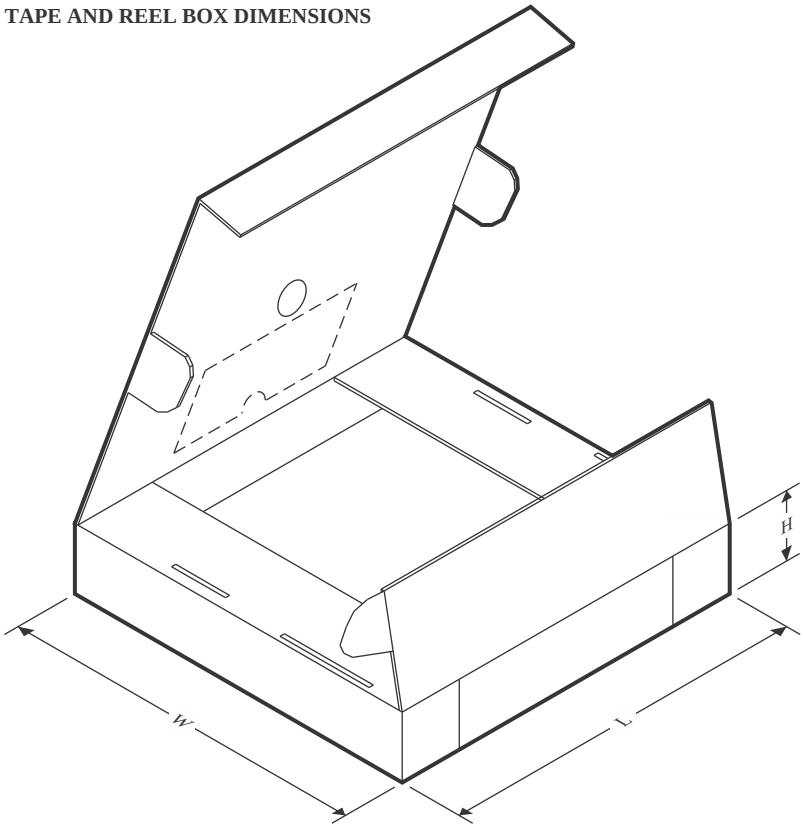
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAN1057ADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TCAN1057ADRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TCAN1057ADRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TCAN1057AVDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TCAN1057AVDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TCAN1057AVDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

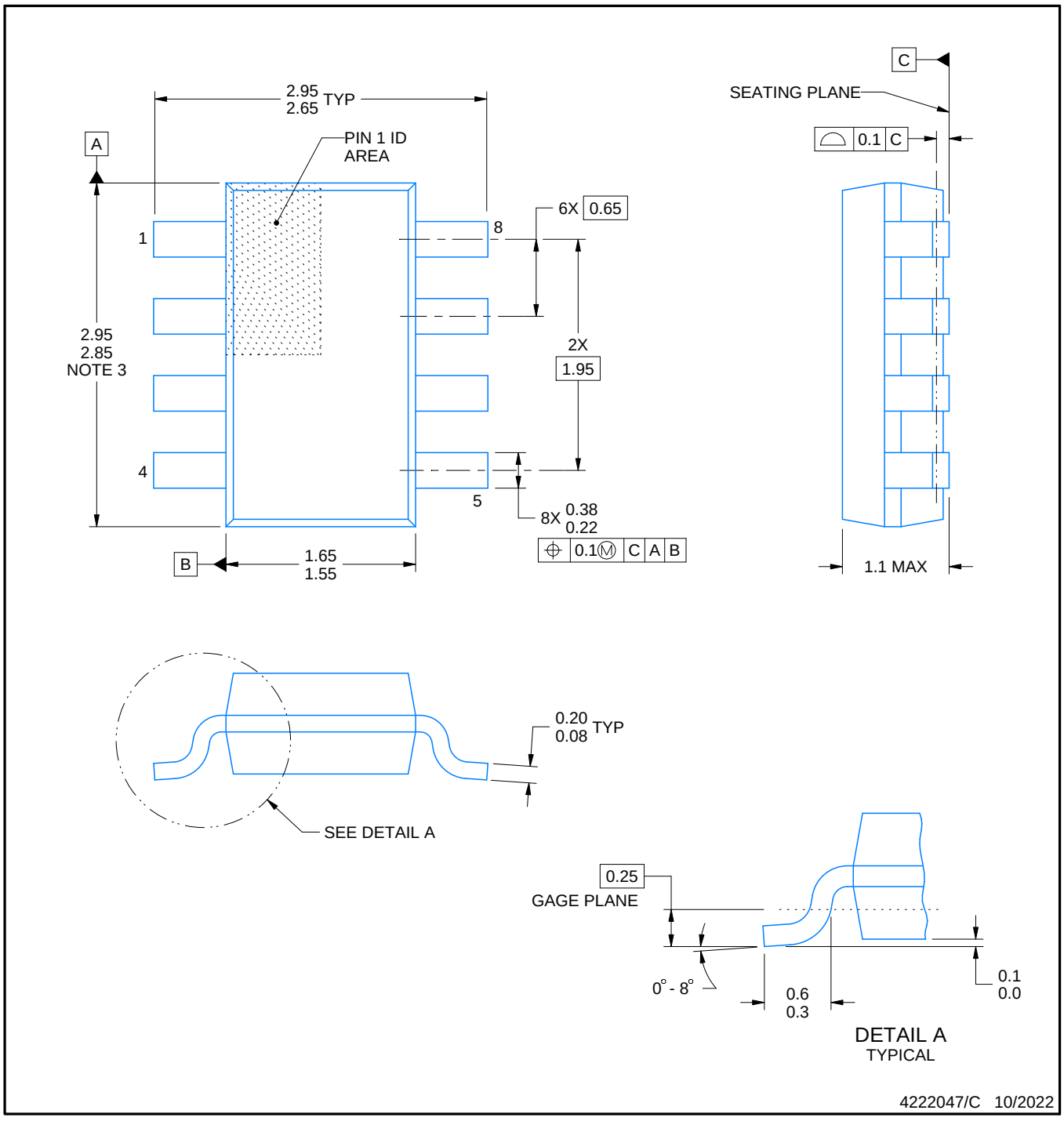
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCAN1057ADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TCAN1057ADRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TCAN1057ADRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TCAN1057AVDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TCAN1057AVDRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TCAN1057AVDRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## DDF0008A

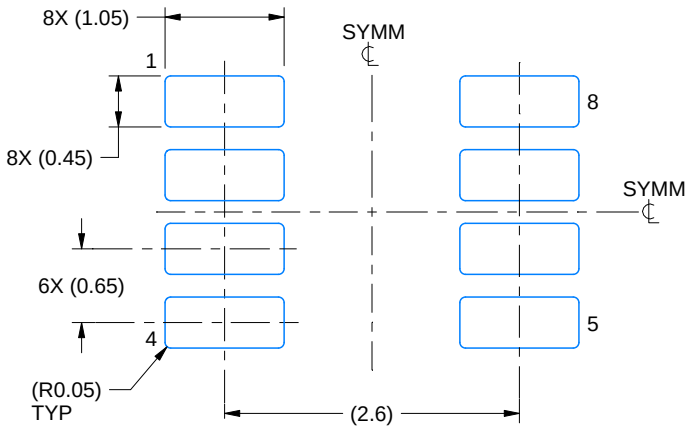
## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
SCALE:15X


NON SOLDER MASK
DEFINED

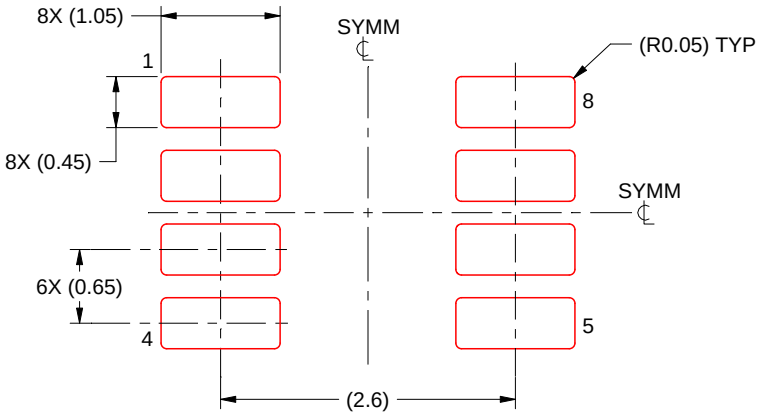
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

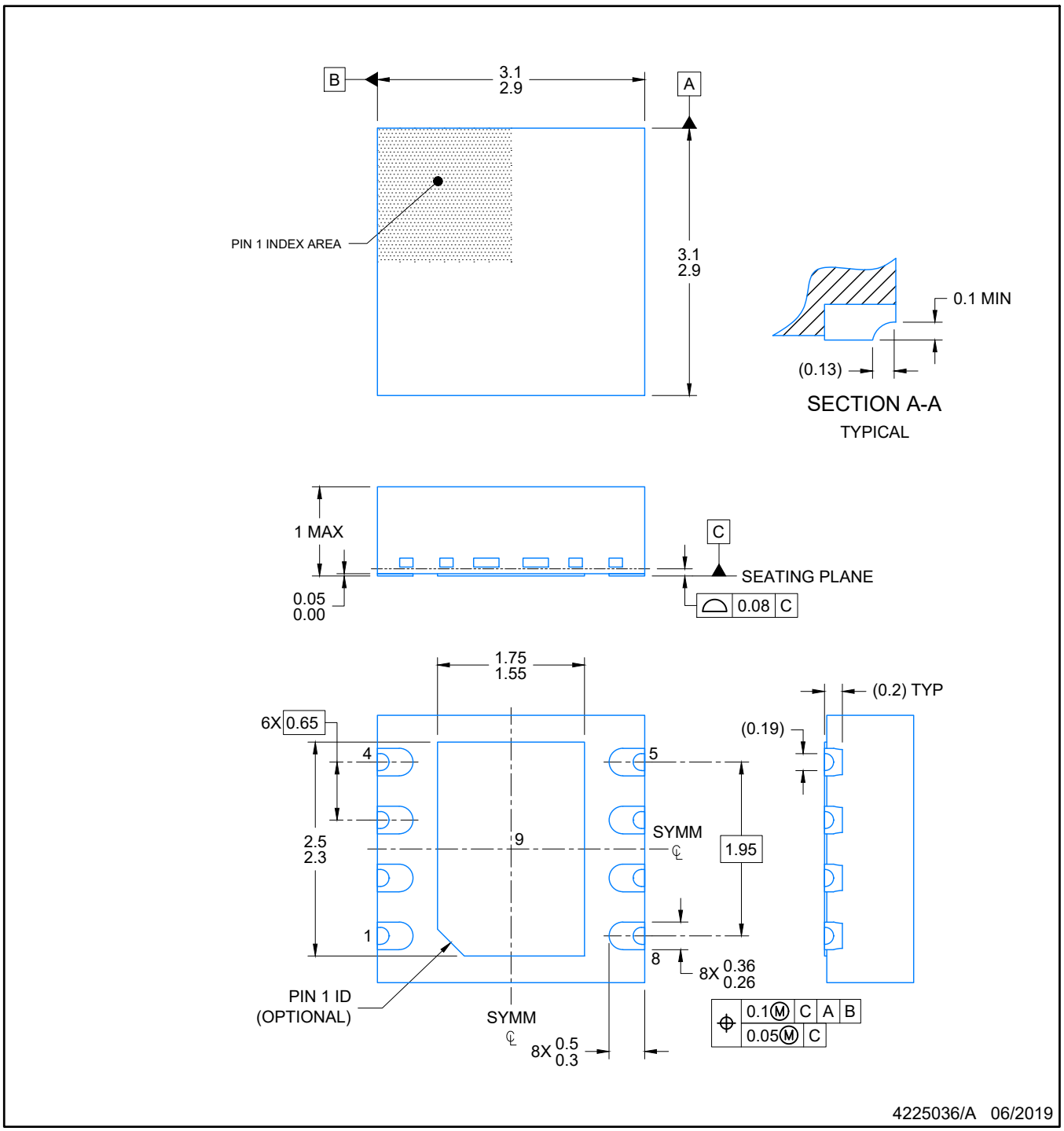
4203482/L

# PACKAGE OUTLINE

## DRB0008J

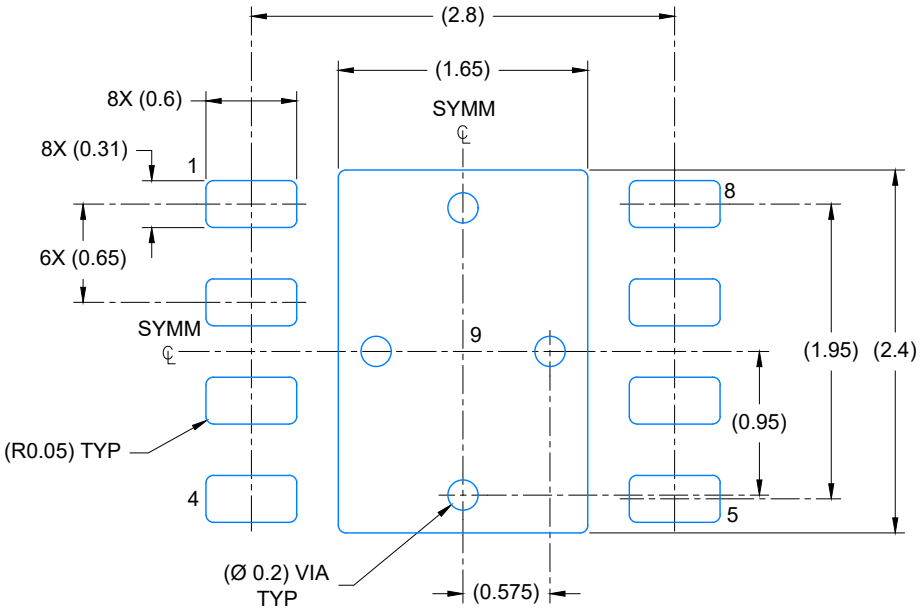
## VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

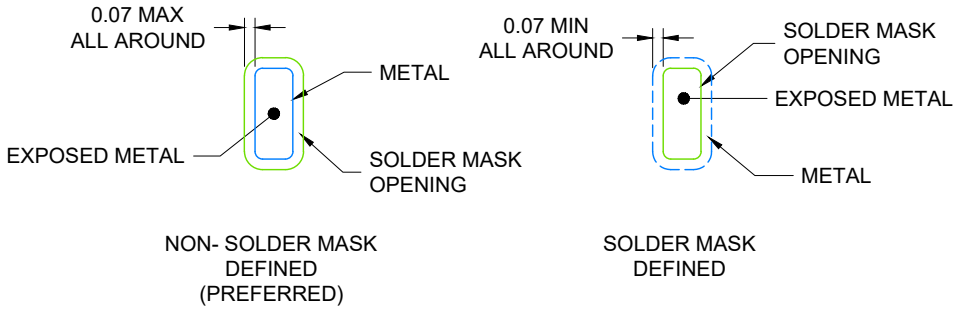



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

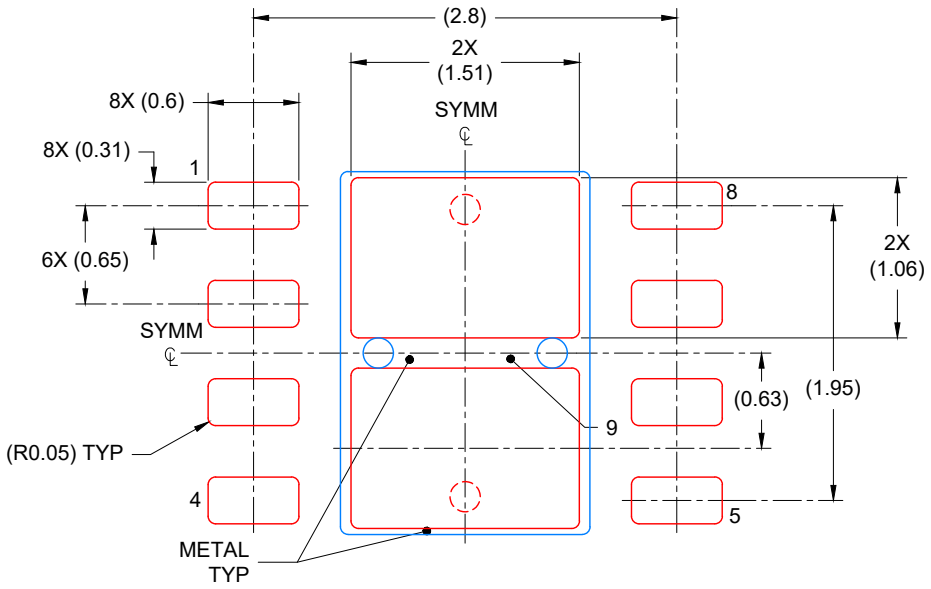



SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

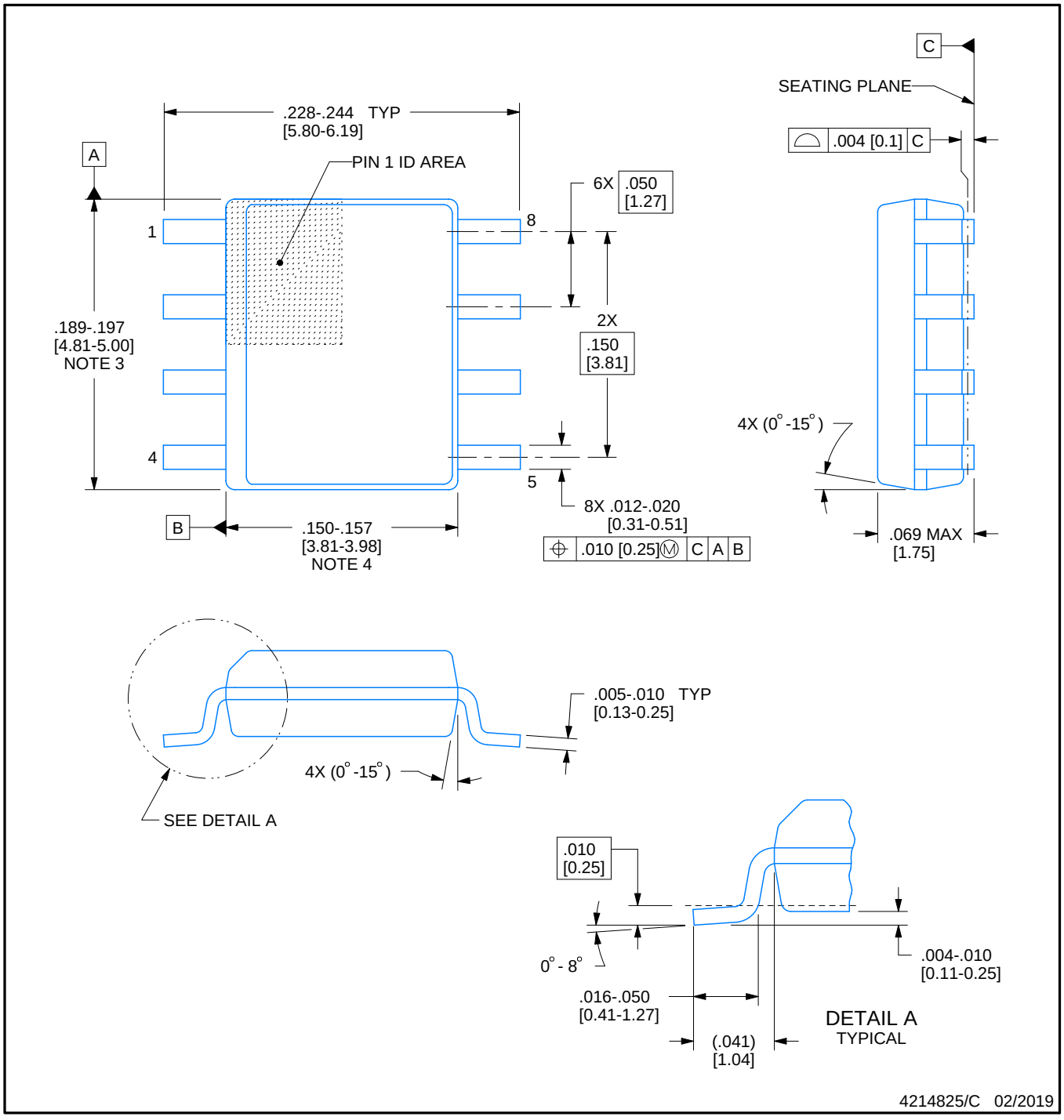
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

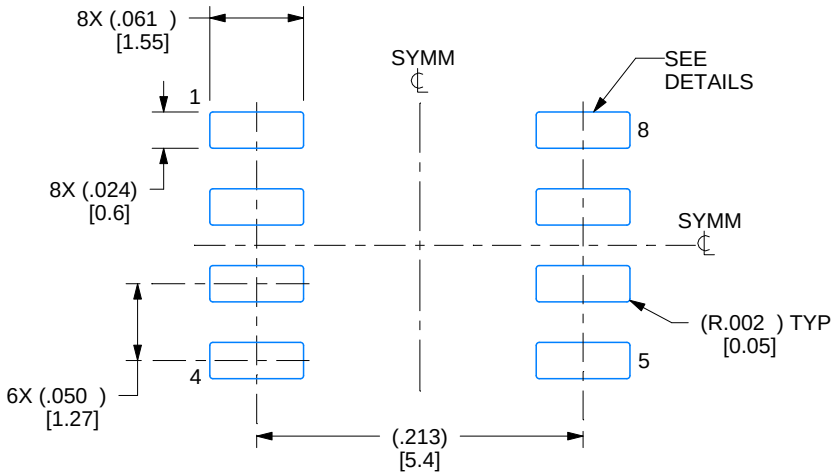
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

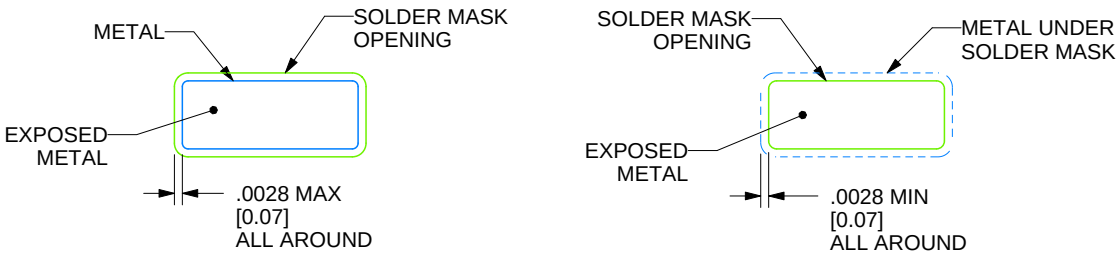
## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

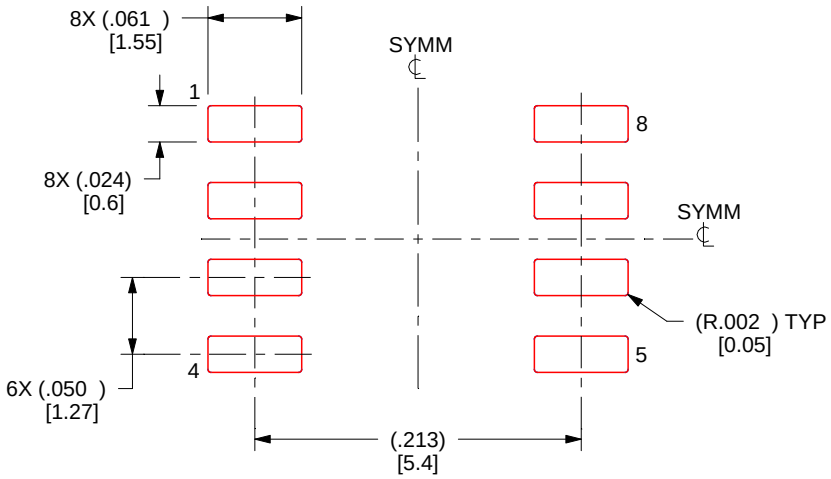
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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