

PJE138K

50V N-Channel Enhancement Mode MOSFET – ESD Protected

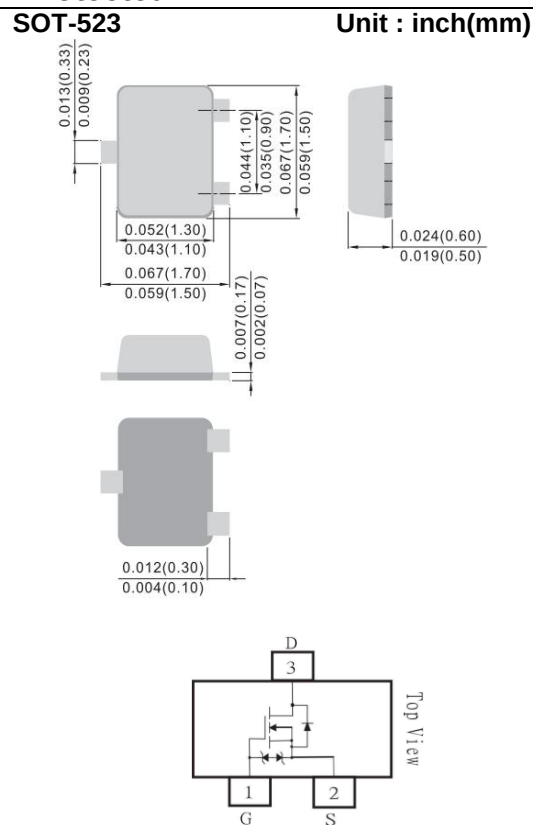
Voltage	50 V	Current	350mA
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Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@500mA < 1.6\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@200mA < 2.5\Omega$
- $R_{DS(ON)}$, $V_{GS}@2.5V$, $I_D@100mA < 4.5\Omega$
- Advanced Trench Process Technology
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOT-523 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00007 ounces, 0.002 grams



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	50	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current		I _D	350	mA
Pulsed Drain Current		I _{DM}	1200	mA
Power Dissipation	T _A =25°C	P _D	223	mW
	Derate above 25°C		1.8	mW/°C
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150	°C
Typical Thermal resistance		R _{θJA}	560	°C/W
- Junction to Ambient ^(Note 3)				



PJE138K

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	50	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.8	1.0	1.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =500mA	-	0.96	1.6	Ω
		V _{GS} =4.5V, I _D =200mA	-	1.25	2.5	
		V _{GS} =2.5V, I _D =100mA	-	2.73	4.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =50V, V _{GS} =0V	-	0.01	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =+20V, V _{DS} =0V	-	+3.0	+10	uA
Dynamic						
Total Gate Charge	Q _g	V _{DS} =25V, I _D =250mA, V _{GS} =4.5V (Note 1,2)	-	0.63	1	nC
Gate-Source Charge	Q _{gs}		-	0.2	-	
Gate-Drain Charge	Q _{gd}		-	0.23	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	-	25	50	pF
Output Capacitance	C _{oss}		-	9.5	20	
Reverse Transfer Capacitance	C _{rss}		-	2.1	5	
Switching						
Turn-On Delay Time	td _(on)	V _{DD} =25V, I _D =500mA, V _{GS} =10V, R _G =6Ω (Note 1,2)	-	2.2	5	ns
Turn-On Rise Time	tr		-	19.2	38	
Turn-Off Delay Time	td _(off)		-	6.2	12	
Turn-Off Fall Time	tf		-	23	50	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	500	mA
Diode Forward Voltage	V _{SD}	I _S =500mA, V _{GS} =0V	-	0.86	1.5	V

NOTES:

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper

PJE138K

TYPICAL CHARACTERISTIC CURVES

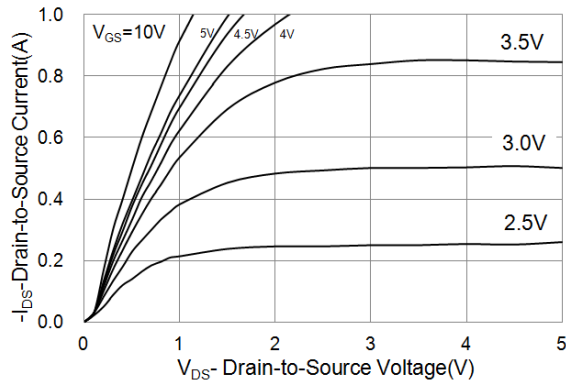


Fig.1 On-Region Characteristics

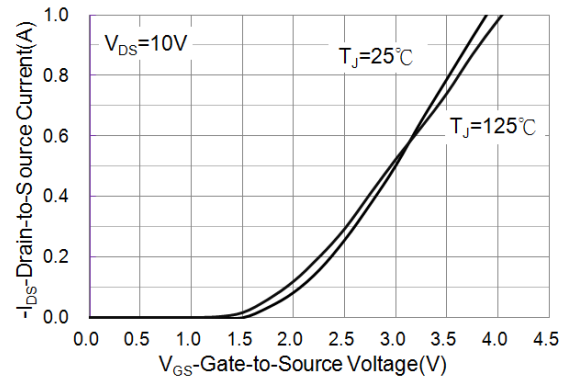


Fig.2 Transfer Characteristics

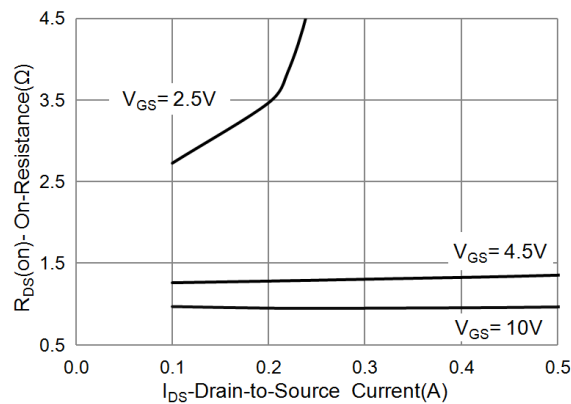


Fig.3 On-Resistance vs. Drain Current

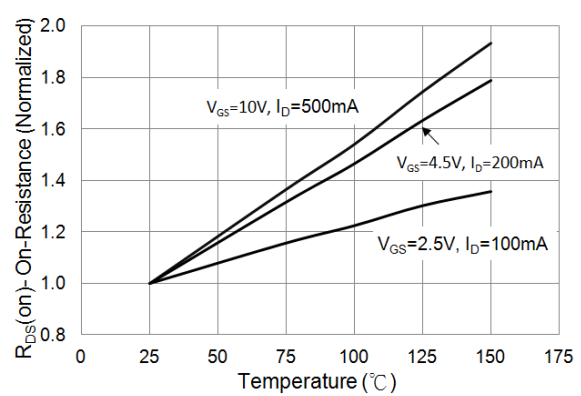


Fig.4 On-Resistance vs. Junction temperature

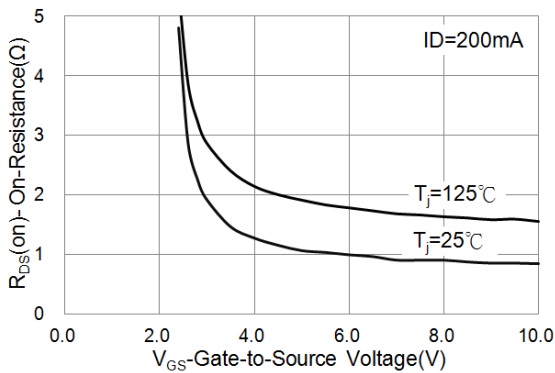


Fig.5 On-Resistance Variation with VGS.

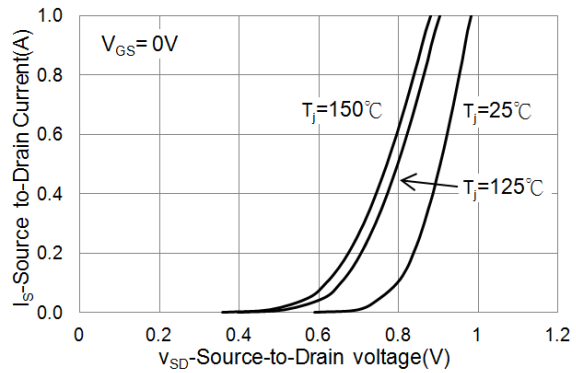


Fig.6 Body Diode Characteristics



PJE138K

TYPICAL CHARACTERISTIC CURVES

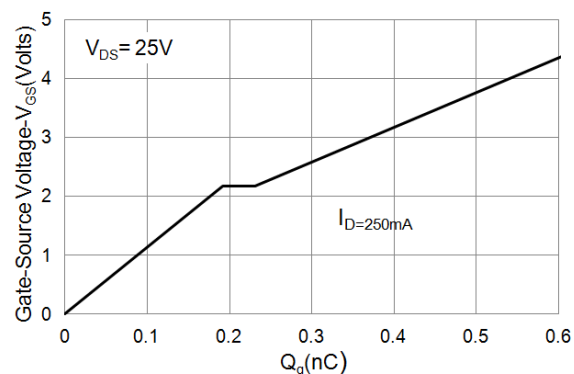


Fig.7 Gate-Charge Characteristics

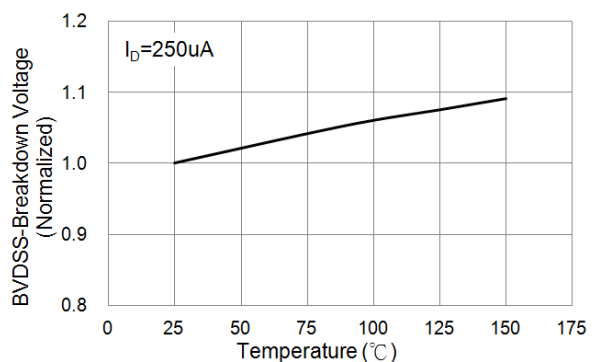


Fig.8 Breakdown Voltage Variation vs. Temperature

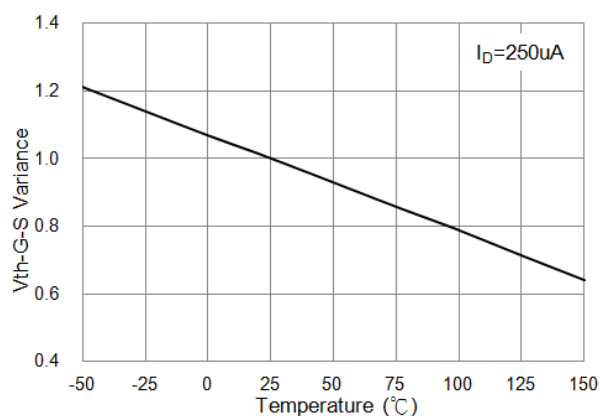


Fig.9 Threshold Voltage Variation with Temperature.

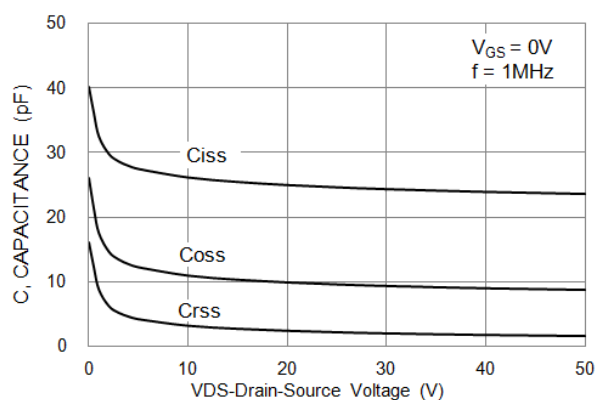


Fig.10 Capacitance vs. Drain-Source Voltage.



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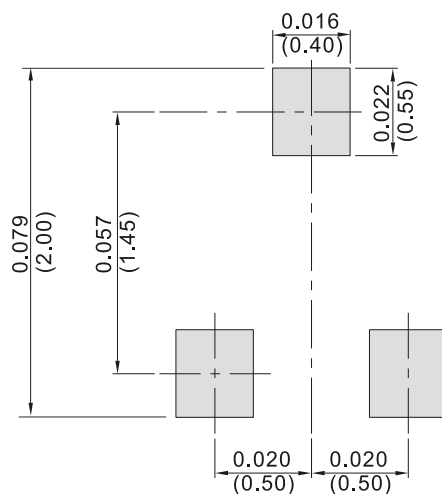
PART NO PACKING CODE VERSION

PART NO PACKING CODE VERSION	Package Type	Packing type	Marking	Version
PJE138K_R1_00001	SOT-523	4K pcs / 7" reel	8KT	Halogen free

MOUNTING PAD LAYOUT

SOT-523

Unit : inch(mm)





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