BelaSigna R281

Always-Listening, Voice Trigger Solution

ON Semiconductor®

www.onsemi.com

Introduction

BelaSigna® R281 is an ultra−low−power voice trigger solution for a wide range of consumer electronic devices. In a typical application BelaSigna R281 is "always listening" and will detect a single, user−trained trigger phrase, asserting a wake−up signal when this trigger phrase is detected.

"Always−listening" key phrase detection with an average power consumption of less than 300 μW (not including the power consumption of the microphone) preserves Standby battery life.

BelaSigna R281 is an ultra−miniature solution that is available in a 2.45 mm x 2.77 mm WLCSP package. It can be designed onto a single layer PCB with 5 mil routing and with a minimal amount of external components.

An external, I^2C host controller is required to configure the device for operation.

Key Features

Proven Ultra−Low−Power Digital Signal Processing (DSP) Technology

- Audio DSP Technology Originally Developed for Hearing Aids Offers the Required Computational Power at Extremely Low Current Consumption
- < 300 μW Average Current Consumption (not including microphone)

Mixed−Signal System−on−Chip (SoC)

- Audio−grade, Analog Input with Onboard Pre−amplifier
- Built−in, Regulated Voltages Including Onboard Microphone Bias for Power Efficient Operation
- Supports Analog or Digital Microphone Input

Interfaces and Peripherals

- I^2C−based Device Configuration and Control
- GPIO Wake Signal
- Internal Oscillator

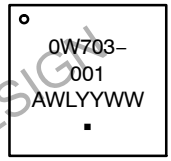
Applications

- Mobile Phones
- Tablets
- Portable Electronic Devices
- Wearables
- Toys

MARKING DIAGRAM



WLCSP31
CASE 567NB



0W689−001 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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Figures and Data

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Input Voltage on any Digital Pin		−0.3	3.8	V
Input Voltage on any Analog Pin		−0.3	3.8	V
Input Voltage on any Supply Pin		−0.3	3.8	V
Current on any Digital Pin			± 5	mA
Current on any Analog Pin			± 10	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Applied to VBAT	VBAT	1.75	1.8	1.98	V
Power Supply Applied to VDDO	VDDO	1.62	1.8	3.63	V
Internal Oscillator Clock Frequency		1	2.56	20	MHz
Ambient Operating Temperature Range	Ta	−40		85	°C

Table 3. ESD AND LATCH−UP CHARACTERISTICS

Parameter	Conditions	Max	Units
ESD − Human Body Model	JEDEC JS − 001 − 2010, all pins	2000	V
ESD − Charged Device Model	JESD22 − C101 − E, all pins	750	V
ESD − Machine Model	JESE22 − A115 − C, all pins	250	V
Latch − Up	JEDEC STD − 78, all pins	± 100	mA

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Electrical Performance Specifications

Typical Values

Unless otherwise noted, Typ values specify the typical values based on design and characterization data under normal operating conditions. Normal operating conditions include a supply voltage (VBAT) of 1.8 V and an operating temperature of 25°C. For specific blocks, the details of the normal operation conditions are described in their respective sections.

Minimum and Maximum Values

Unless otherwise noted, Min and Max values specify the designed range or measurement range and are guaranteed by design and/or characterization.

Min and Max values specified may be based on factory production test limits, design, or characterization data.

Normal Operating Conditions

Unless otherwise noted, normal operating conditions indicate an ambient temperature Ta = 25°C and a supply voltage VBAT = 1.8 V. VDDD and VDDA are calibrated to their preset factory calibration settings and correspond to their respective Typ values. VDDO is powered externally at 1.8 V. No external loads are applied to digital I/O or analog pins.

Table 4. SYSTEM DC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C, VBAT=VDDO=1.8 V, VDDD=1.4 V) unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Average Run Mode Current	IDD	VBAT=VDDA=1.8 V, charge pump disabled Assumes a ratio of speech present versus quiet environment of 20/80		170		μA

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Table 5. DIGITAL I/O PINS (I2C, WAKE_UP, DMIC) DC ELECTRICAL CHARACTERISTICS
Typical operating conditions (Ta = 25°C, VDDO = 1.8 V, Pull − up/Pull − down Enabled) unless otherwise noted

Parameter	Symbol	Conditions		Min	Typ	Max	Units
VDDO Supply Voltage Range	VDDO			1.25	1.8	3.63	V
Output Low Level	V_{ol}	I_{ol} = 4 mA			0	0.2 x VDDO	V
Output High Level	V_{oh}	I_{ol} = −4 mA		0.8 x VDDO	VDDO		V
Input Low Level	V_{il}				0	0.2 x VDDO	V
Input High Level	V_{ih}			0.8 x VDDO	VDDO		V
Pull−Up Resistance	R_{pu}	Non−I^2C	VDDO = 1.8 V	80	122	160	kΩ
			VDDO = 3.3 V	30	48	60	
		I^2C (strong/weak)	VDDO = 1.8 V	0.8 / 8	1 / 10	1.2 / 12	
			VDDO = 3.3 V	0.8 / 8	1 / 10	1.2 / 12	
Pull−Down Resistance	R_{pd}	VDDO = 1.8 V		120	168	210	kΩ
		VDDO = 3.3 V		30	60	80	
Pin Capacitance	C_{pd}				5		pF
Maximum Output Current	I_{ol}, I_{oh}					±4	mA
Input Leakage Current	I_I					±1	μA

Table 6. VDDA REGULATOR DC & AC ELECTRICAL CHARACTERISTICS
Typical operating conditions (Ta = 25°C), charge pump in use, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VDDA	CL = 1 μF	1.8	1.98	2.0	V
Load Current					4	mA
Load Regulation				5		mV/mA
Line Regulation				20		mV/V
PSRR		@ 1 kHz unloaded	20			dB

Table 7. VREG REGULATOR DC & AC ELECTRICAL CHARACTERISTICS
Typical operating conditions (Ta = 25°C), unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VREG	CL = 1 μF	0.89	0.92	0.95	V
Load Current					2	mA
Load Regulation					20	mV/mA
Line Regulation					5	mV/V
PSRR		@ 1 kHz unloaded	40			dB

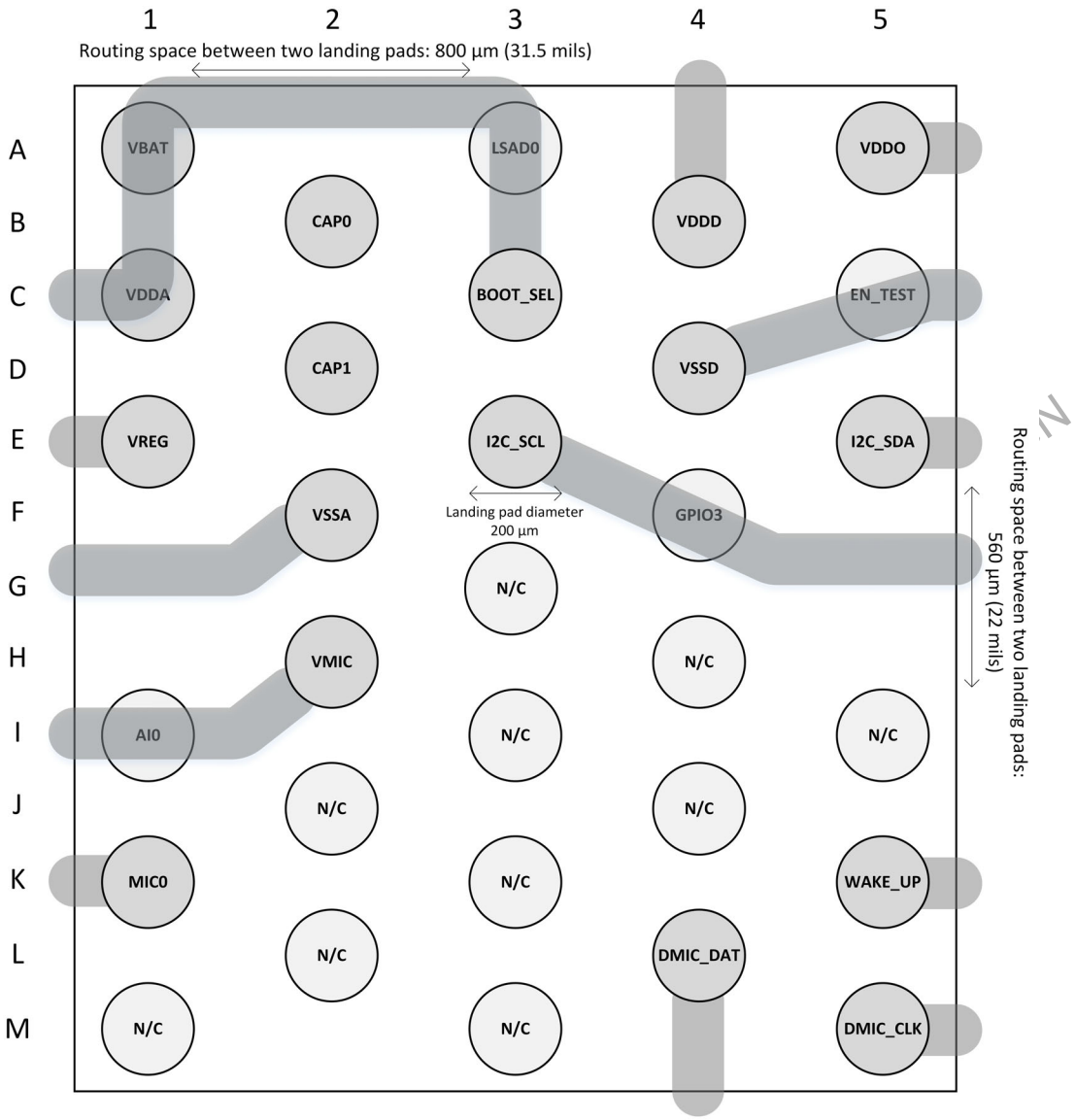
Table 8. VDDD REGULATOR DC & AC ELECTRICAL CHARACTERISTICS
Typical operating conditions (Ta = 25°C), unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VDDD	CL = 1 μF	1.2	1.4	1.7	V
Load Current					15	mA
Load Regulation					10	mV/mA
Line Regulation					20	mV/V
PSRR		@ 1 kHz unloaded	20			dB

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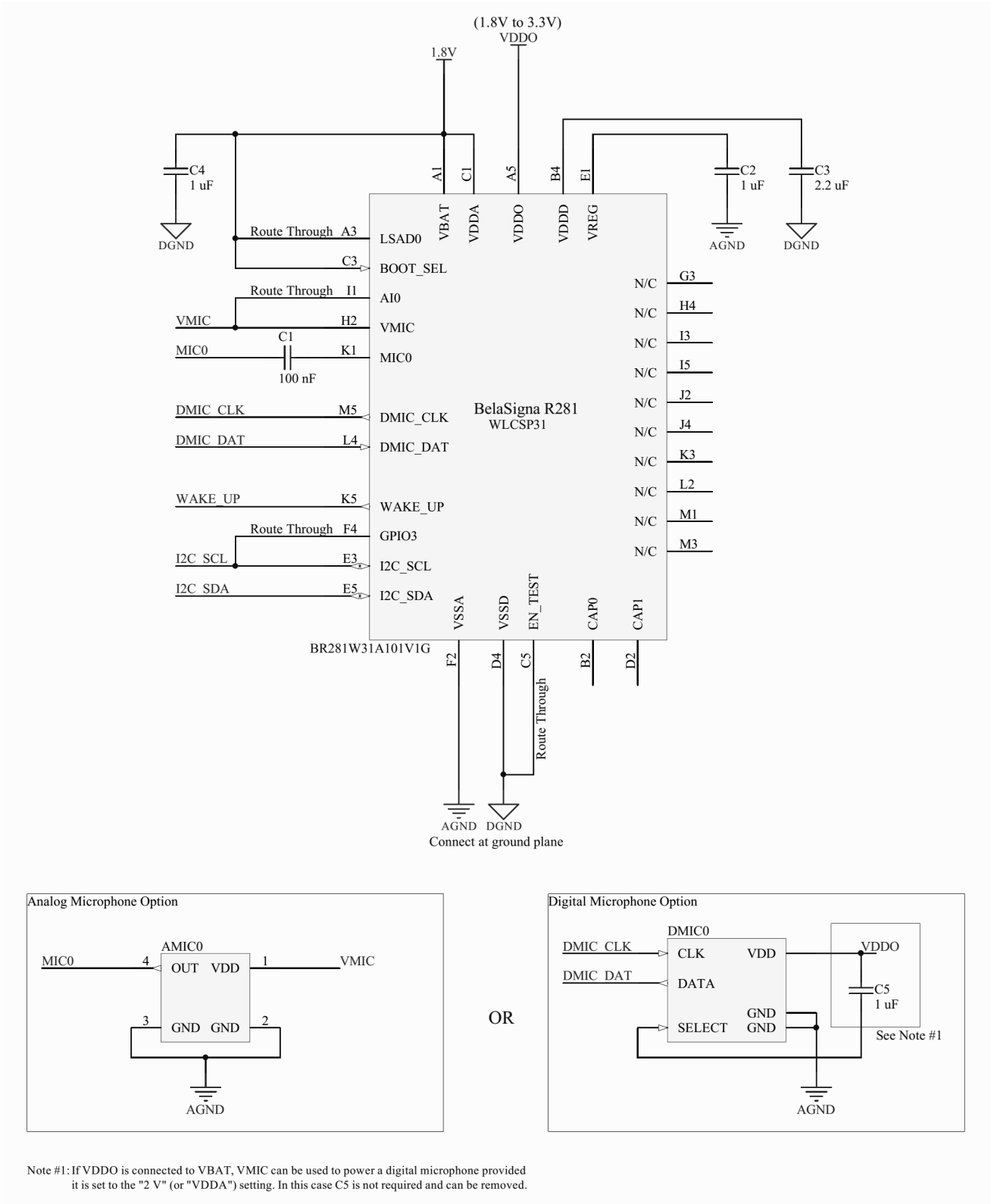
System Diagrams



BelaSigna R281 WLCSP 5 mil routing - top and soldering footprint view
(balls facing down)

Figure 1. BelaSigna R281 WLCSP Suggested PCB Routing

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Note #1: If VDDO is connected to VBAT, VMIC can be used to power a digital microphone provided it is set to the "2 V" (or "VDDA") setting. In this case C5 is not required and can be removed.

Figure 2. BelaSigna R281 System Diagram (WLCSP Package)

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Description of Operation

Efficient implementation of the trigger phrase recognition algorithm is accomplished through the use of three processing units running concurrently. In addition to the main DSP core performing system configuration and signal processing, an input/output processor continuously collects frames of input speech signals which are analyzed by a highly optimized frequency domain co−processor.

There are two main modes of operation: Recognition Mode and Training Mode.

Recognition Mode

When in Recognition Mode, the entire system remains in an extremely low−power, “always−on” state continuously listening for speech. When speech is detected, the algorithm proceeds to extract features from the collected audio data, comparing these features to a known set of data computed during the training process. If the features appear to be similar enough to the trained feature data, a match is indicated on the WAKE_UP pin.

Once the feature extraction and comparison is complete, the system returns to its original low−power state, once again waiting until speech is detected.

Training Mode

Before BelaSigna R281 can be placed into Recognition Mode, it must be trained. Training involves recording and analyzing three utterances of a *trigger phrase*. A trigger phrase can be any collection of words or sounds, in any language, up to a maximum length of approximately 1.5 seconds.

When speaking a given phrase, a human will naturally say the same phrase subtly different each time. Having multiple instances of the same phrase, each slightly different, helps to make the matching algorithm more robust.

Training must be performed in a quiet environment, or the trigger phrase match results in Recognition Mode will be unpredictable. BelaSigna R281 is placed into Training Mode by issuing an appropriate SetMode command via I^2C. The algorithm stores relevant feature data from the three separate utterances of the trigger phrase, also known as *training templates*.

Once training is complete, the training templates can be read from memory and stored offline. This template data can then be loaded into memory in the event of a power cycle and the device can be placed directly into Recognition Mode, thus avoiding the need to re−train the device. This same procedure can be used to recognize multiple trigger phrases, provided they have each been individually trained and stored offline. Only one trigger phrase can be active at any one time.

Refer to AND9267/D for more information on the different modes, as well as a description of the I^2C host control protocol.

Initial Power−On State

When BelaSigna R281 is powered on, the device will perform a brief initialization procedure and then wait for a connection to be made from an external host via I^2C. At this point, the host controller must connect to BelaSigna R281 and load its memory with the algorithm binary image, as well as the training template data. Once this has been completed, the device can be put into Recognition Mode. If no training template data is available (e.g. the training procedure has never been performed), then BelaSigna R281 must be placed into Training Mode and the training procedure performed before entering Recognition Mode.

Whenever power is removed from the device, the contents of memory are lost and must be re−loaded.

For more information refer to AND9267/D.

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System Performance

Recognition Rate

Performance has been measured in various noise conditions and is shown in Figure 3. Tests were performed in a sound isolation booth with a series of pre−recorded trigger and non−trigger phrases playing continuously, mixed with varying levels of noise. Recognition rate is 100% in a quiet environment (no noise playing). The system was trained in a quiet environment. In all cases, the false trigger rate (the number of times the system triggered on a non−trigger phrase) was 0%.

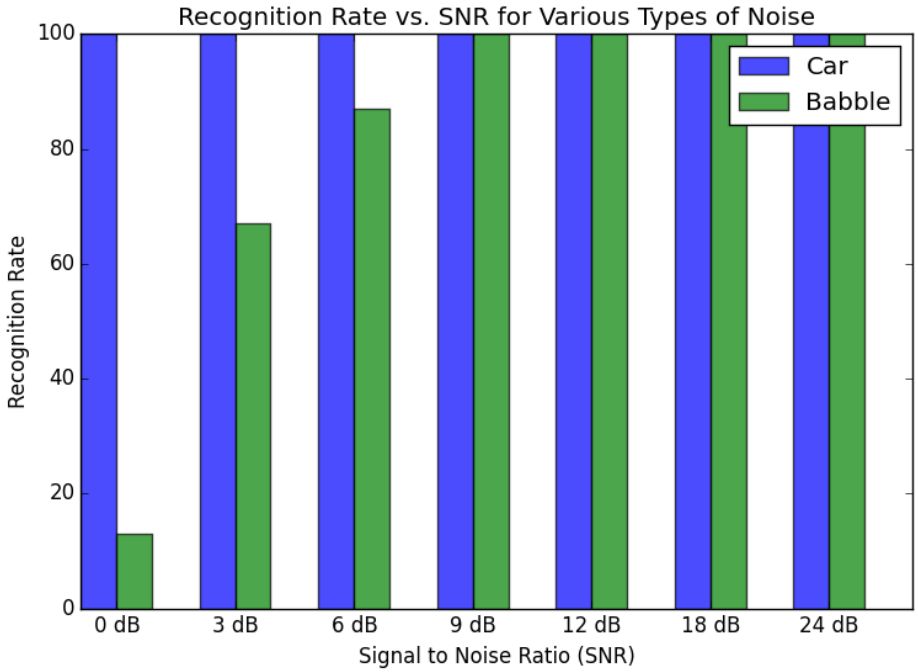


Figure 3. Recognition Rate Versus SNR

Current Consumption

Average current consumption was also measured with the device operating in a pure noise environment with no speech present. The results are presented in Table 9.

Table 9. AVERAGE CURRENT CONSUMPTION

Condition	Average Current Consumption (uA), VBAT = 1.8 V
Quiet Environment	160
Babble Noise	170

*Not including microphone current consumption

Single User Operation

Because BelaSigna R281 performs recognition based on a training procedure performed by a specific individual, recognition of the trigger phrase is effectively “single−user”. Only the person who trained the system (or an individual with an extremely similar voice print) will be able to reliably trigger the device.

Digital Interfaces

Wake Up Pin

The Wake Up pin is a digital output (referenced to VDDO) which is used to indicate that the trigger phrase was detected. It is intended to be connected to a digital input of an external host, and its behavior (active high versus active low and duration) is configurable via I^2C.

For more information refer to AND9267/D.

Boot Select Pin

This pin is reserved for future purpose and must be connected to VDDA.

Inter−IC Communication (I^2C) Interface

The I^2C interface is an industry−standard interface that can be used for high−speed transmission of data between BelaSigna R281 and an external device. The interface operates at speeds up to 100 Kbit/sec, and always operates in slave mode at an address of 0x62.

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Digital Microphone (DMIC) Interface

The digital microphone interface provides a means of interfacing a digital microphone to the system instead of an analog microphone. When the device is configured to use a digital microphone input instead of an analog microphone input (the default), an appropriate clock is output on the DMIC_CLK pin and device accepts PDM signals from a digital microphone on the DMIC_DAT input pin. A separate algorithm binary image is available supporting a digital microphone input.

Figure 4 shows the timing of the DMIC interface. For more information refer to AND9267/D.

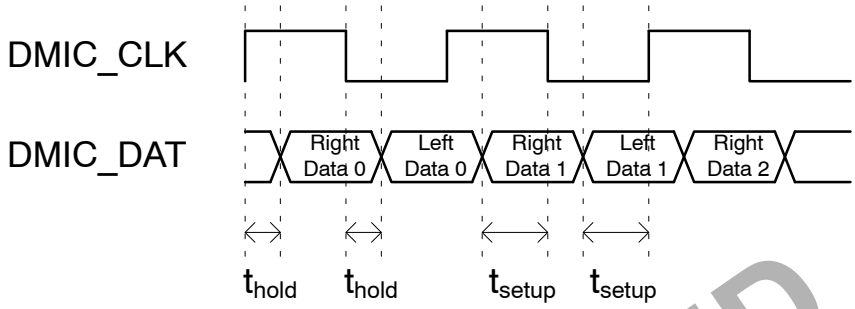


Figure 4. DMIC Timing Diagram

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Mechanical Information and Circuit Design Guidelines

Table 10. PIN DESCRIPTION

WLCSP Ball Index	Name	Description	Pad Type	Pull
A1	VBAT	Main power supply	P	
A3	LSAD0	Low−speed Analog to Digital Input	I	
A5	VDDO	Digital I/O supply, capacitor to VSSD, typically connected to VBAT	P	
B2	CAP0	Charge pump capacitor to CAP1	A	
B4	VDDD	Digital supply, capacitor to VSSD	P	
C1	VDDA	Analog supply voltage (output), capacitor to VSSA, or connected to VBAT (max. 1.98 V)	P	
C3	BOOT_SEL	Boot selection (always connect to VDDA)	AI	
C5	EN_TEST	Test enable	DIO	
D2	CAP1	Charge pump capacitor to CAP0	A	
D4	VSSD	Digital core and I/O ground, connect to VSSA on PCB	P	
E1	VREG	Analog supply voltage (output), capacitor to VSSA	A	
E3	I2C_SCL	I^2C clock	DIO	PU
E5	I2C_SDA	I^2C data	DIO	PU (Note 1)
F2	VSSA	Analog ground	P	
F4	GPIO3	General purpose digital input/output	DIO	
G3	N/A	No connection	NC	
H2	VMIC	Analog microphone supply output	A	
H4	N/A	No connection	NC	
I1	AI0	Analog input (unused)	AI	
I3	N/A	No connection	NC	
I5	N/A	No connection	NC	
J2	N/A	No connection	NC	
J4	N/A	No connection	NC	
K1	MIC0	Analog microphone input	AI	
K3	N/A	No connection	NC	
K5	WAKE_UP	Wake up signal (output)	DIO	
L2	N/A	No connection	NC	
L4	DMIC_DAT	Digital microphone data input (optional)	DIO	
M1	N/A	No connection	NC	
M3	N/A	No connection	NC	
M5	DMIC_CLK	Digital microphone clock (optional)	DIO	PU (Note 2)

1. The value of the I^2C pull−ups is 10 K
2. Pull−up is disabled when the DMIC interface is enabled.

Legend:

Type: A = analog; D = digital; I = input; O = output; P = power; NC = not connected
Pull: PU = pull up; PD = pull down
All digital pads have a Schmitt trigger input

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Reflow Information

The reflow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Information from JEDEC Standard 22−A113D and J−STD−020D.01 can be used as a guideline.

Electrostatic Discharge (ESD) Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Ordering Information

To order BelaSigna R281, please contact your account manager.

Chip Identification

Chip identification information can be retrieved using the GetChipID I^2C command.

Refer to AND9267/D for more details regarding supported I^2C commands.

Company or Product Inquiries

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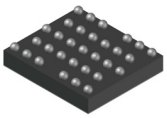
ORDERING INFORMATION

Part Number	Chip ID	Package Option	Shipping†
BR281W31A101V1G	0x5000	WLCSP31 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

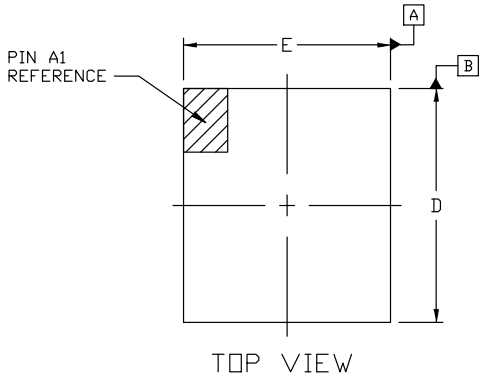
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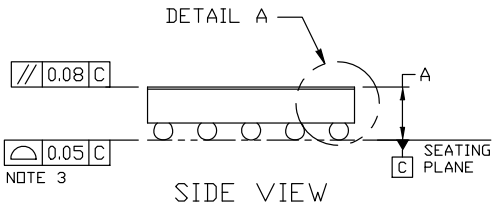
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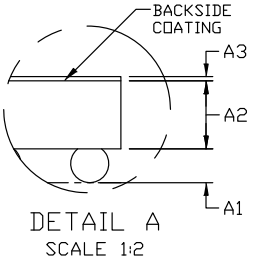


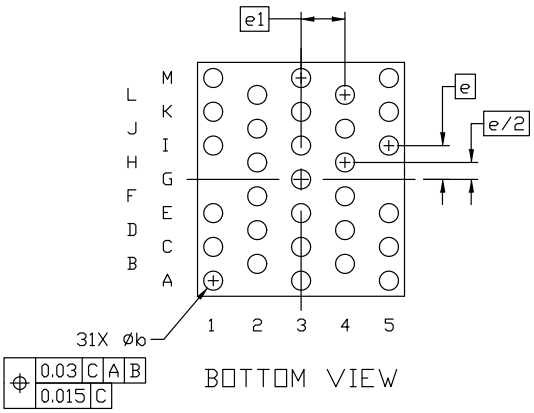
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CASE 567NB
ISSUE B

DATE 13 MAR 2023





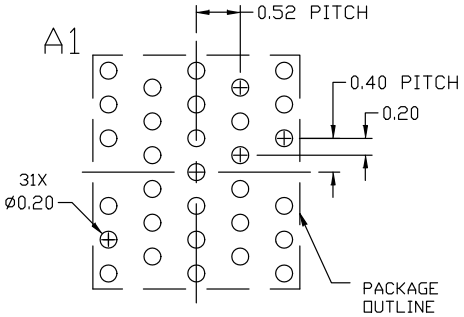




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.569	0.627	0.685
A1	0.192	0.222	0.252
A2	0.355	0.380	0.405
A3	0.022	0.025	0.028
b	0.224	0.254	0.284
D	2.74	2.77	2.80
E	2.42	2.45	2.48
e	0.40 BSC		
e1	0.52 BSC		



RECOMMENDED
SOLDERING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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