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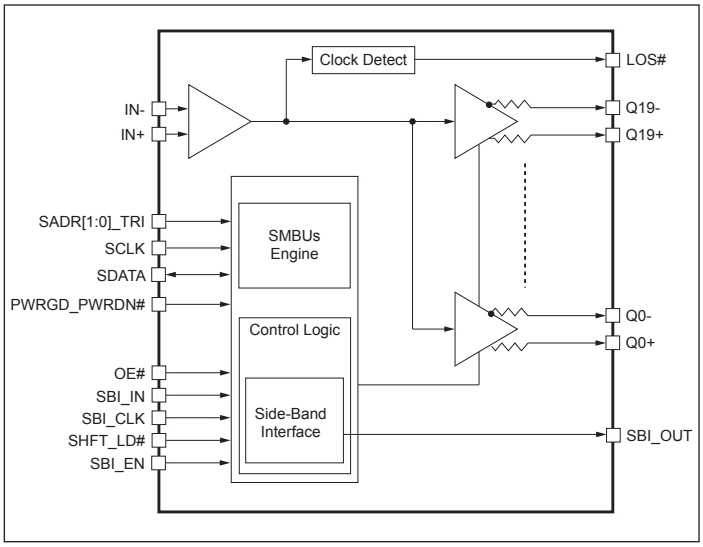
PI6CB332020B

20-Output Low-Power Fanout Clock Buffer for PCIe 6.0/7.0 Application

Description

The PI6CB332020B is a low-power PCIe® 5.0/6.0 and PCIe 7.0 compatible clock buffer. It takes a reference input to fanout 20 low-power differential HCSL outputs up to 400MHz, with on-chip terminations for 85Ω output impedance. An individual OE pin for each output provides easier power management. The device also supports Power Down Tolerant (PDT), automatic output clock parking upon loss of input clock, and Flexible Startup Sequencing features.

Block Diagram



Features

- **3.3V Tolerant Clock Output in HiZ Mode, Supporting Flex-IO System**
- **Outputs in HiZ Mode when Disabled**
- 20 Low-Power HCSL Outputs with On-Chip Termination
- 85Ω Output Impedance
- Individual Output Enable
- Supports I/O Power Down Tolerant
- Flexible Startup Power Sequencing
- Automatic Output Clock Parking Upon Loss of Input Clock
- Up to 9 Selectable SMBus Addresses
- Supports SBI OE# Interface
- Differential Output-to-output Skew <50ps
- Additive Phase Jitter
  - PCIe 5.0: Typical 5fs RMS
  - PCIe 6.0: Typical 3fs RMS
  - DB2000QL: Typical 10fs RMS
- 3.3V Supply Voltage
- Temperature Range: –40°C to 105°C
- Packaging (Pb-free & Green):
  - 80-QFN, 6mm × 6mm (20 outputs)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
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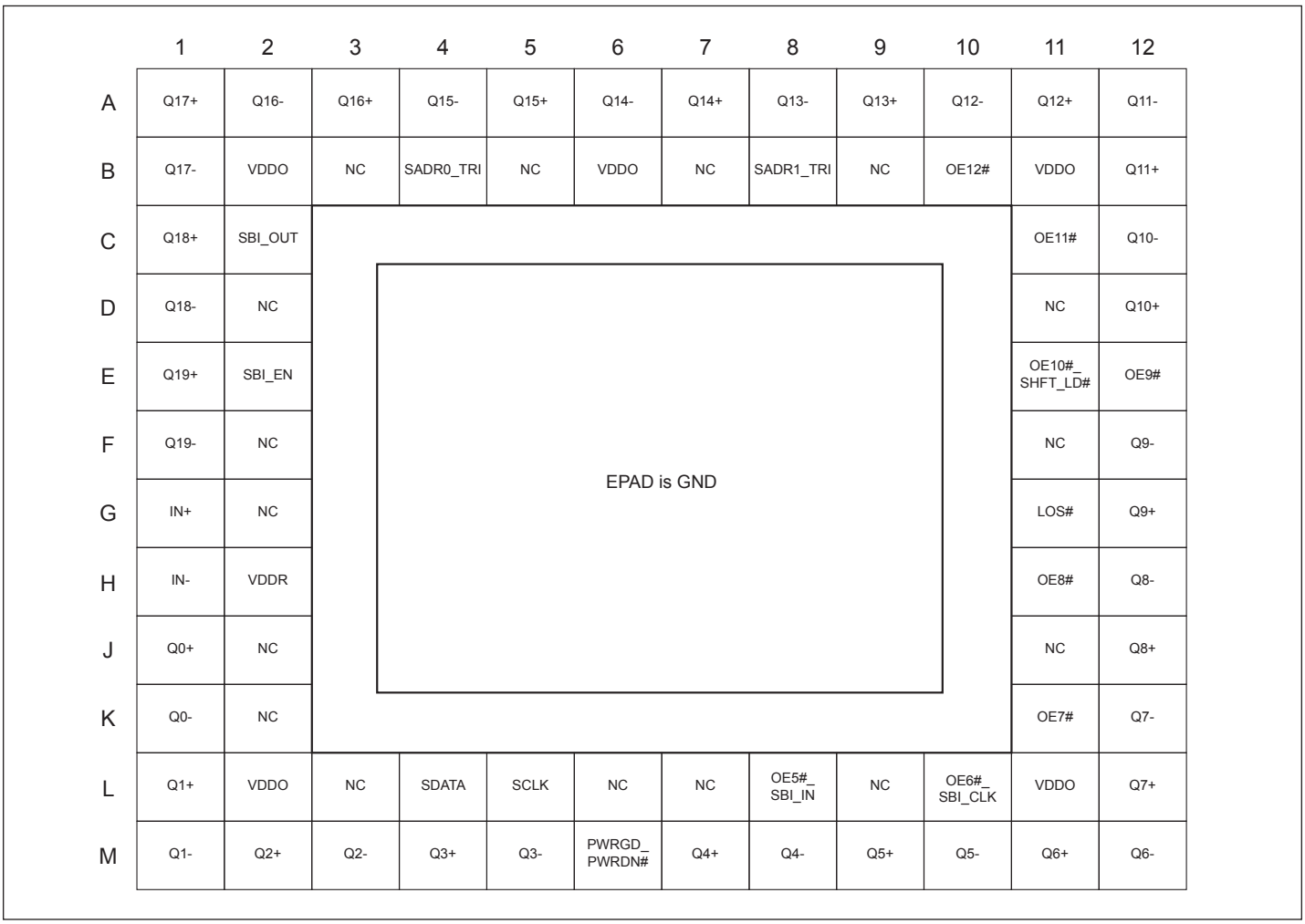
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Description
A1	Q17+	Output	Diff.	Differential true clock output.
A2	Q16-	Output	Diff.	Differential complementary clock output.
A3	Q16+	Output	Diff.	Differential true clock output.
A4	Q15-	Output	Diff.	Differential complementary clock output.
A5	Q15+	Output	Diff.	Differential true clock output.
A6	Q14-	Output	Diff.	Differential complementary clock output.
A7	Q14+	Output	Diff.	Differential true clock output.
A8	Q13-	Output	Diff.	Differential complementary clock output.
A9	Q13+	Output	Diff.	Differential true clock output.
A10	Q12-	Output	Diff.	Differential complementary clock output.

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Pin Number	Pin Name	Type		Description
A11	Q12+	Output	Diff.	Differential true clock output.
A12	Q11-	Output	Diff.	Differential complementary clock output.
B1	Q17-	Output	Diff.	Differential complementary clock output.
B2	VDDO	Power		Power supply for differential clock outputs.
B3	NC	NC		Not connected.
B4	SADR0_TRI	Input	Tri-level	SMBus address bit. This is a tri-level input that works in conjunction with SADR1_TRI pin, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
B5	NC	NC		Not connected.
B6	VDDO	Power		Power supply for differential clock outputs.
B7	NC	NC		Not connected.
B8	SADR1_TRI	Input	Tri-level	SMBus address bit. This is a tri-level input that works in conjunction with SADR0_TRI pin, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
B9	NC	NC		Not connected.
B10	OE12#	Input	CMOS	Active low input for enabling output 12. 0 = enable output, 1 = disable output. Output in HiZ mode, Internal pull down, PDT.
B11	VDDO	Power		Power supply for clock outputs.
B12	Q11+	Output	Diff.	Differential true clock output.
C1	Q18+	Output	Diff.	Differential true clock output.
C2	SBI_OUT	Output	CMOS	Side-Band Interface data output.
C11	OE11#	Input	CMOS	Active low input for enabling output 11. 0 = enable output, 1 = disable output. Output in HiZ mode, Internal pull down, PDT.
C12	Q10-	Output	Diff.	Differential complementary clock output.
D1	Q18-	Output	Diff.	Differential complementary clock output.
D2	NC	NC		Not connected.
D11	NC	NC		Not connected.
D12	Q10+	Output	Diff.	Differential true clock output.
E1	Q19+	Output	Diff.	Differential true clock output.
E2	SBI_EN	Input	CMOS	0 = SBI is disabled. 1 = SBI is enabled. Internal pull down, PDT.
E11	OE10#_ SHFTLD#	Input	CMOS	SBI_EN=0: OE mode. 0 = Enable output 10, 1 = Disable output 10 (HiZ mode) SBI_EN=1: SBI mode. This pin becomes SHFT_LD pin. For both OE mode and SBI mode, Internal pull down, PDT.

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Pin Number	Pin Name	Type		Description
E12	OE9#	Input	CMOS	Active low input for enabling Q9 pair. 0 = Enable output, 1 = Disable output (HiZ mode). The pin has internal pull down.
F1	Q19-	Output	Diff.	Differential complementary clock output.
F2	NC	NC		Not connected.
F11	NC	NC		Not connected.
F12	Q9-	Output	Diff.	Differential complementary clock output.
G1	IN+	Input	Diff.	Differential true clock input, PDT. Internal pull up
G2	NC	NC		Not connected.
G11	LOS#	Output	Open Drain	Open drain output, needs external pull up, Low output indicates loss of input clock signal, PDT.
G12	Q9+	Output	Diff.	Differential true clock output.
H1	IN-	Input		Differential complementary clock input, PDT. Internal pull down
H2	VDDR	Power		Power supply for clock input (receiver).
H11	OE8#	Input	CMOS	Active low input for enabling output 8. 0 = Enable output, 1 = Disable output (HiZ mode). Internal pull down, PDT.
H12	Q8-	Output	Diff.	Differential complementary clock output.
J1	Q0+	Output	Diff.	Differential true clock output.
J2	NC	NC		Not connected.
J11	NC	NC		Not connected.
J12	Q8+	Output	Diff.	Differential true clock output.
K1	Q0-	Output	Diff.	Differential complementary clock output.
K2	NC	NC		Not connected.
K11	OE7#	Input	CMOS	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output (HiZ mode). Internal pull down, PDT.
K12	Q7-	Output	Diff.	Differential complementary clock output.
L1	Q1+	Output	Diff.	Differential true clock output.
L2	VDDO	Power		Power supply for differential clock outputs.
L3	NC	NC		Not connected.
L4	SDATA	I/O	CMOS	SMBUS Data line, 3.3V tolerant .
L5	SCLK	Input	CMOS	SMBUS Clock input, 3.3V tolerant .
L6	NC	NC		Not connected.
L7	NC	NC		Not connected.
L8	OE5#_SBI_IN	Input	CMOS	SBI_EN=0: OE mode. 0 = Enable output 5, 1 = Disable output 5 (HiZ mode). SBI_EN=1: SBI mode. This pin becomes SBI_IN pin. For both OE mode and SBI mode, Internal pull down, PDT.
L9	NC	NC		Not connected.

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Pin Number	Pin Name	Type		Description
L10	OE6#_SBI_CLK	Input	CMOS	SBI_EN=0: OE mode. 0 = Enable output 6, 1 = Disable output 6 (HiZ mode). SBI_EN=1: SBI mode. This pin becomes SBI_CLK pin. For both OE mode and SBI mode, Internal pull down, PDT.
L11	VDDO	Power		Power supply for differential clock outputs.
L12	Q7+	Output	Diff.	Differential true clock output.
M1	Q1-	Output	Diff.	Differential complementary clock output.
M2	Q2+	Output	Diff.	Differential true clock output.
M3	Q2-	Output	Diff.	Differential complementary clock output.
M4	Q3+	Output	Diff.	Differential true clock output.
M5	Q3-	Output	Diff.	Differential complementary clock output.
M6	PWRGD_PWRDN#	Input	CMOS	1 = power good mode, I2C address is latched. 0 = power down mode. Internal pull-down, PDT.
M7	Q4+	Output	Diff.	Differential true clock output.
M8	Q4-	Output	Diff.	Differential complementary clock output.
M9	Q5+	Output	Diff.	Differential true clock output.
M10	Q5-	Output	Diff.	Differential complementary clock output.
M11	Q6+	Output	Diff.	Differential true clock output.
M12	Q6-	Output	Diff.	Differential complementary clock output.
EPAD	EPAD	Power		Connect to Ground.

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx}..... –0.5V to +3.9V
Input Voltage .....–0.5V to V_{DD} +0.3V, not exceed 3.9V
Input Voltage (PDT Pin) ..... –0.5V to +3.9V
ESD Protection (HBM) 2000V
Iout (Output Current Continuous) 30mA
Iout (Output Current Surge).....60mA
Junction Temperature ..... 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}, V_{DDR}	Power Supply Voltage		2.97	3.3	3.63	V
V_{DDO}	Output Power Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current	V_{DDO} + V_{DDR}, All outputs active @100MHz		200	240	mA
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DDO} + V_{DDR}, All outputs in HiZ mode		6	7.5	mA
I_{DDO_PD}	Power Supply Current Power Down(1) for Outputs	V_{DDO}, All outputs in HiZ mode		1.76	2.05	mA
T_A	Ambient Temperature	Industrial grade	–40		105	°C

Note:
1. Input clock is not running.
2. Outputs drive 10 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pull up Resistance			120		KΩ
R_{dn}	Internal Pull down Resistance			120		KΩ
L_{PIN}	Pin Inductance				7	nH

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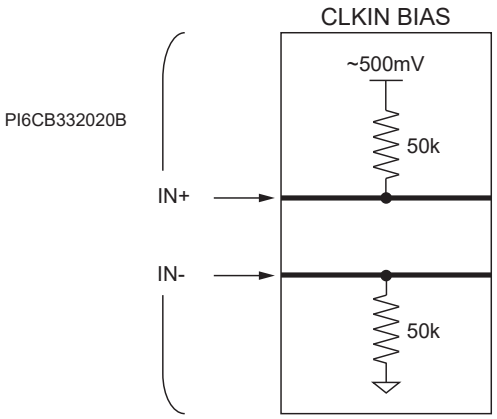


Figure 1. Input Clock Bias Network

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal Bus Voltage		2.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.8	V
		SMBus, V_{DDSMB} < 3.3V			0.8	
$I_{SMBSINK}$	SMBus Sink Current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus Operating Frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus Rise Time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			300	ns
t_{FMSB}	SMBus Fall Time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

Side-Band Interface Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{PERIOD}	Clock Period	Clock period	40			ns
t_{SETUP}	SHFT Setup Time to Clock	SHFT_LDB high to SBI_CLK rising edge	10			ns
t_{DSU}	SBI_IN Setup Time	SBI_IN setup to SBI_CLK rising edge	5			ns
t_{DHOLD}	SBI_IN Hold Time	SBI_IN hold after SBI_CLK rising edge	2			ns

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Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{CO}	SBI_CLK to SBI_OUT	SBI_CLK rising edge to SBI_OUT valid	2			ns
t_{SHOLD}	SHFT Hold Time	SHFT_LDB hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LDB falling edge)	10			ns
$t_{EN/DIS}$	Enable/Disable Time	Delay from SHFT_LDB falling edge to next output configuration taking effect	4		12	clocks
t_{SLEW}	Slew Rate	SBI_CLK (between 20% and 80%)	0.7		4	V/ns
		SBI_OUT impedance		50		Ω

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	2.4			V
V_{IM}	Input Mid Voltage	SADR0_TRI, SADR1_TRI, BW_SEL_TRI	1.2		1.7	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus			0.55	V
I_{IH}	Input High Current	Single-ended inputs with pullup/pulldown resistor, $V_{IN} = V_{DD}$			50	uA
I_{IL}	Input Low Current	Single-ended inputs with pullup/pulldown resistor, $V_{IN} = 0$	–50			µA
C_{IN}	Input Capacitance		1.5		5	pF

HCSL Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
fIN	Input Frequency	V_{DD} = 3.3V	1	100	400	MHz
	Autoparking On		25			MHz
	Autoparking Off		1			MHz
V_{IHDIF}	Diff. Input High Voltage (3)	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage (3)	IN+, IN-, single-end measurement	–300	0	300	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	200			mV
V_{COM}	Common mode voltage		100		1200	mV
t_{RF}	Diff. Input Slew Rate (2)		0.7			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN+} = V_{DD}$, V_{IN-} = 0.8V	–40		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%

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Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is $(V_{IH}-V_{IL})/2$

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output voltage high		660	780	900	mV
V_{OL}	Output voltage low		–150	20	150	mV
Vcross absolute	Absolute crossing point voltage		250		550	mV
Vcross_var	Cross point voltage variation				140	mV
f_{OUT}	Output Frequency			100	400	MHz
t_{RF}	Slew rate [1,2,3]	Scope averaging on, 10 inch trace	1.5	3.0	4	V/ns
Dt_{RF}	Slew rate matching [1,2,4]	Scope averaging on, 10 inch trace			20	%
t_{SKEW}	Output Skew [1,2]	Averaging on, V_T = 50%			50	ps
t_{DC}	Diff. Output Duty Cycle	Measured differentially	45		55	%
T_{pd}	Propagation Delay			2.0	3	ns
t_{OELAT}	Output Enable Latency	Q start after OE# assertion Q stop after OE# deassertion	4	5	10	clocks
t_{PDLAT}	PD# De-assertion	Differential outputs enable after PD# de-assertion		20	300	µs
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of input clock to LOS assert		200	300	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of input clock to LOS de-assert		6	9	clocks
I_{Leak}	LPHCSL Qx± leakage current		–10		10	uA

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. Duty cycle distortion is the difference in duty cycle between the out and input clock

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HCSL Output AC Characteristics - Phase Jitter

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Typ.	Max.	Specification Limit	Units
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen 1 (2.5 GT/s)	1300		86,000	fs p-p
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Hi Band (5.0 GT/s)	58		3,100	fs RMS
		PCIe Gen 2 Lo Band (5.0 GT/s)	4		3,000	
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (8.0 GT/s)	19		1,000	
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (16.0 GT/s)	19		500	
$t_{jphPCIeG5-CC}$		PCIe Gen 5 (32.0 GT/s)	5	11.5	150	
$t_{jphPCIeG6-CC}$		PCIe Gen 6 (64.0 GT/s)	4	6.6	100	
$t_{jphPCIeG1-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS)SSC ≤ -0.3%	PCIe Gen 1 (2.5 GT/s)	111			fs RMS
$t_{jphPCIeG2-IR}$		PCIe Gen 2 (5.0 GT/s)	51			
$t_{jphPCIeG3-IR}$		PCIe Gen 3 (8.0 GT/s)	23			
$t_{jphPCIeG4-IR}$		PCIe Gen 4 (16.0 GT/s)	22			
$t_{jphPCIeG5-IR}$		PCIe Gen 5 (32.0 GT/s)	6	8.1		
$t_{jphPCIeG6-IR}$		PCIe Gen 6 (64.0 GT/s)	4	7		

Note: The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 6.0, Revision 1.0. For the exact measurements

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SMBus Serial Data Interface

After power-up and PWRGD's first edge changes from 0 to 1, then the SMBus starts working. The PI6CB332020B is a slave only device that supports block and byte protocol using a single 7-bit address and read/write bit as shown below. The highest bit of register address is to distinguish block write/read and byte write/read. When the highest bit is "1", it's the byte operation, the highest bit is "0", it's the block operation.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	See SMBus Address Selection Table				1/0

Note: SMBus address is latched on SADR pin

Byte Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	data	Ack	Stop bit

Byte Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	data	NAck	Stop bit

Block Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Data Byte count = X	Ack	Beginning Date Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

Block Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Date Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop bit

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SMBus Address Decode

Address Selection		Binary Value								Hex Value
SADR_tri1	SADR_tri0	7	6	5	4	3	2	1	Read/Write	
0	0	1	1	0	1	1	0	0	0	D8
	M	1	1	0	1	1	0	1	0	DA
	1	1	1	0	1	1	1	1	0	DE
M	0	1	1	0	0	0	0	1	0	C2
	M	1	1	0	0	0	1	0	0	C4
	1	1	1	0	0	0	1	1	0	C6
1	0	1	1	0	0	1	0	1	0	CA
	M	1	1	0	0	1	1	0	0	CC
	1	1	1	0	0	1	1	1	0	CE

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Side-Band Interface

This interface consists of DATA, CLK and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the Output register.

When the SBI is enabled, DATA, CLK, and SHFT_LD# are enabled on OE5#, OE6# and OE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled.' This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled, and power has been applied, the SBI is active, even if the PWRGD/PWRDN# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of PWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. Figure 2 provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift bits to disable their respective output. See Figure 2.

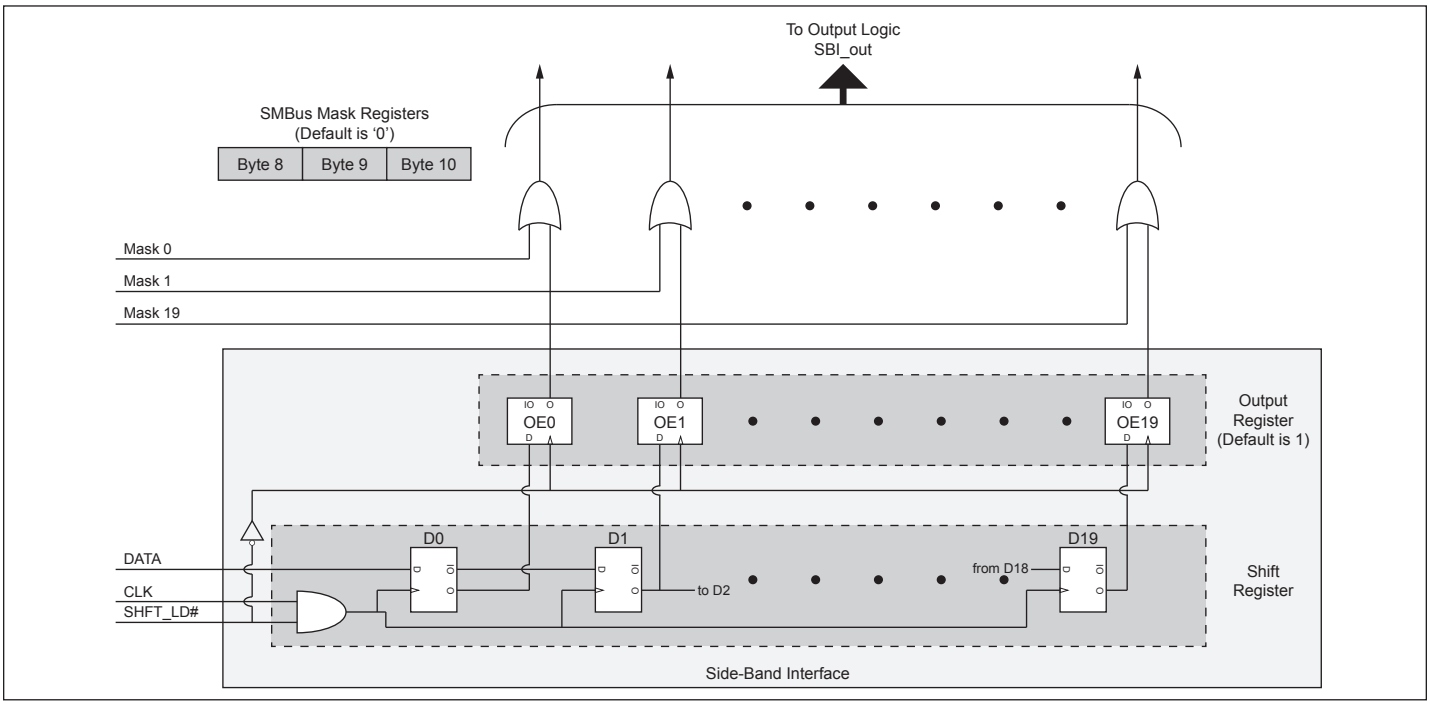


Figure 2. Side Band Interface Control Logic Description

Figures 3 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock for output 19, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

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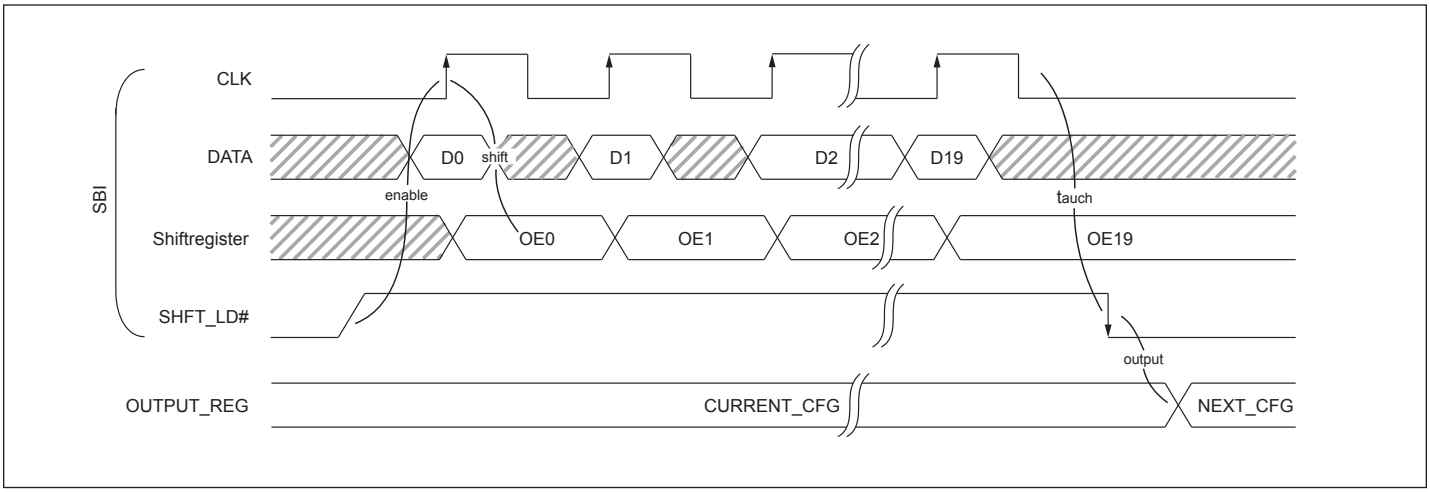


Figure 3. Side Band Interface Functional Timing

The SBI interface supports clock rates up to 10MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LD# pin to each devices allows its use as a chip-select pin. When the SHFT_LD# pin is low, the PI6CB332020B ignores any activity on the CLK and DATA pins.

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SMBus Registers

Byte 0: OUTPUT_ENABLE_2					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0	0 = output is disabled (HiZ mode) 1 = output is enabled
6	Q19_EN	Output Enable for Q19	RW	1	
5	Q18_EN	Output Enable for Q18	RW	1	
4	Q17_EN	Output Enable for Q17	RW	1	
3	Q16_EN	Output Enable for Q16	RW	1	
2	Reserved		RW	0	
1	Reserved		RW	0	
0	Reserved		RW	0	

Byte 1: OUTPUT_ENABLE_0					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Q7_EN	Output Enable for Q7	RW	1	0 = output is disabled (HiZ mode) 1 = output is enabled
6	Q6_EN	Output Enable for Q6	RW	1	
5	Q5_EN	Output Enable for Q5	RW	1	
4	Q4_EN	Output Enable for Q4	RW	1	
3	Q3_EN	Output Enable for Q3	RW	1	
2	Q2_EN	Output Enable for Q2	RW	1	
1	Q1_EN	Output Enable for Q1	RW	1	
0	Q0_EN	Output Enable for Q0	RW	1	

Byte 2: OUTPUT_ENABLE_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Q15_EN	Output Enable for Q15	RW	1	0 = output is disabled (HiZ mode) 1 = output is enabled
6	Q14_EN	Output Enable for Q14	RW	1	
5	Q13_EN	Output Enable for Q13	RW	1	
4	Q12_EN	Output Enable for Q12	RW	1	
3	Q11_EN	Output Enable for Q11	RW	1	
2	Q10_EN	Output Enable for Q10	RW	1	
1	Q9_EN	Output Enable for Q9	RW	1	
0	Q8_EN	Output Enable for Q8	RW	1	

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Byte 3: OE#_PIN_READBACK					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	RB_OE#_12	Status of OE#12	RO	1'bX	0 = pin low 1 = pin high
6	RB_OE#_11	Status of OE#11	RO	1'bX	
5	RB_OE#_10	Status of OE#10	RO	1'bX	
4	RB_OE#_9	Status of OE#9	RO	1'bX	
3	RB_OE#_8	Status of OE#8	RO	1'bX	
2	RB_OE#_7	Status of OE#7	RO	1'bX	
1	RB_OE#_6	Status of OE#6	RO	1'bX	
0	RB_OE#_5	Status of OE#5	RO	1'bX	

Byte 4: SBEN_RDBK_ ACP_CONFIG					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	1'b111	
6			RW		
5			RW		
4	ACP_ENABLE	Enable Automatic Clock Parking to HiZ mode when LOS event is detected	RW	1	0 = disable ACP 1 = enable ACP
3	Reserved		RW	1'b110	
2			RW		
1			RW		
0	RB_SBI_ENQ	Status of SBI_ENQ	RO	1'bX	0 = pin low 1 = pin high

Byte 5: VENDOR_REVISION_ID					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	RID	REVISION ID, A rev is 0000	RO	0x0	
6			RO		
5			RO		
4			RO		
3	VID	VENDOR ID, Diodes	RO	0011	
2			RO		
1			RO		
0			RO		

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Byte 6: DEVICE_ID					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	DEVICE_ID	Device ID	RO	0H54	
6			RO		
5			RO		
4			RO		
3			RO		
2			RO		
1			RO		
0			RO		

Byte 7: BYTE_COUNT					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0x0	
6			RW		
5			RW		
4	BC	Writing to this register configures how many bytes will be read back in a block read.	RW	0x7	
3			RW		
2			RW		
1			RW		
0			RW		

Byte 8: SBI_MASK_0					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	MASK7	Masks off Side-band Disable for CLK7	RW	0	0 = SBI may disable the output 1 = SBI cannot disable the output
6	MASK6	Masks off Side-band Disable for CLK6	RW	0	
5	MASK5	Masks off Side-band Disable for CLK5	RW	0	
4	MASK4	Masks off Side-band Disable for CLK4	RW	0	
3	MASK3	Masks off Side-band Disable for CLK3	RW	0	
2	MASK2	Masks off Side-band Disable for CLK2	RW	0	
1	MASK1	Masks off Side-band Disable for CLK1	RW	0	
0	MASK0	Masks off Side-band Disable for CLK0	RW	0	

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Byte 9: SBI_MASK_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	MASK15	Masks off Side-band Disable for CLK15	RW	0	0 = SBI may disable the output 1 = SBI cannot disable the output
6	MASK14	Masks off Side-band Disable for CLK14	RW	0	
5	MASK13	Masks off Side-band Disable for CLK13	RW	0	
4	MASK12	Masks off Side-band Disable for CLK12	RW	0	
3	MASK11	Masks off Side-band Disable for CLK11	RW	0	
2	MASK10	Masks off Side-band Disable for CLK10	RW	0	
1	MASK9	Masks off Side-band Disable for CLK9	RW	0	
0	MASK8	Masks off Side-band Disable for CLK8	RW	0	

Byte 10: SBI_MASK_2					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0	
6			RW		
5			RW		
4			RW		
3	MASK19	Masks off Side-band Disable for CLK19	RW	0	0 = SBI may disable the output 1 = SBI cannot disable the output
2	MASK18	Masks off Side-band Disable for CLK18	RW	0	
1	MASK17	Masks off Side-band Disable for CLK17	RW	0	
0	MASK16	Masks off Side-band Disable for CLK16	RW	0	

Byte 11: OUTPUT_SLEW_ RATE_0					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Q7_SLEWRATE	Q7 Slew Rate Control	RW	1	0 = low slew rate 1 = high slew rate
6	Q6_SLEWRATE	Q6 Slew Rate Control	RW	1	
5	Q5_SLEWRATE	Q5 Slew Rate Control	RW	1	
4	Q4_SLEWRATE	Q4 Slew Rate Control	RW	1	
3	Q3_SLEWRATE	Q3 Slew Rate Control	RW	1	
2	Q2_SLEWRATE	Q2 Slew Rate Control	RW	1	
1	Q1_SLEWRATE	Q1 Slew Rate Control	RW	1	
0	Q0_SLEWRATE	Q0 Slew Rate Control	RW	1	

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Byte 12: OUTPUT_SLEW_ RATE_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Q15_SLEWRATE	Q15 Slew Rate Control	RW	1	
6	Q14_SLEWRATE	Q14 Slew Rate Control	RW	1	
5	Q13_SLEWRATE	Q13 Slew Rate Control	RW	1	
4	Q12_SLEWRATE	Q12 Slew Rate Control	RW	1	0 = low slew rate
3	Q11_SLEWRATE	Q11 Slew Rate Control	RW	1	1 = high slew rate
2	Q10_SLEWRATE	Q10 Slew Rate Control	RW	1	
1	Q9_SLEWRATE	Q9 Slew Rate Control	RW	1	
0	Q8_SLEWRATE	Q8 Slew Rate Control	RW	1	

Byte 13: OUTPUT_SLEW_ RATE_2					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0	
6			RW		
5			RW		
4			RW		
3	Q19_SLEWRATE	Q19 Slew Rate Control	RW	1	
2	Q18_SLEWRATE	Q18 Slew Rate Control	RW	1	0 = low slew rate
1	Q17_SLEWRATE	Q17 Slew Rate Control	RW	1	1 = high slew rate
0	Q16_SLEWRATE	Q16 Slew Rate Control	RW	1	

Byte 14-19 : RESERVED

Byte 20: LPHCSL_AMP_CTRL					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	AMP	Global Differential output Control 0.625V~1V 25mV/step Default = 0.8V	RW	0x70	
6			RW		
5			RW		
4			RW		
3	Reserved		RW	0x0	
2			RW		
1	Stop 1	Output disable	RW	0	00: HiZ/HiZ 01: Low/Low
0	Stop 0	Output disable	RW	0	10: Low/High 11: High/Low

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Byte 21: D_RESTORE_LOS#					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	AC_IN	Enable receiver bias when IN is AC coupled	RW	0	0 = DC coupled input 1 = AC coupled input
6	Rx_TERM	Enable termination resistors on IN	RW	0	0 = input termination R is disabled 1 = input termination R is enabled
5	Reserved			2'b00	
4					
3	PD_RESTORE#	Save Configuration in Power Down	RW	1	0 = Config Cleared 1 = Config Saved
2	SDATA_TIMEOUT_EN	Enable SMB SDATA time out monitoring	RW	1	0 = disable SDATA time out 1 = enable SDATA time out
1	Reserved		RO	0	
0	LOS#_RB	Real time read back of loss detect block output	RO	X	0 = LOS event detected 1 = NO LOS event detected.

Byte 22-32 : RESERVED (Default: 0xXX)

Byte 33: SBI_READBACK_0(1)					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	SBI_Q7	Readback of Side-band Disable for Q7	RO	1'bX	0 = bit low 1 = bit high
6	SBI_Q6	Readback of Side-band Disable for Q6	RO	1'bX	
5	SBI_Q5	Readback of Side-band Disable for Q5	RO	1'bX	
4	SBI_Q4	Readback of Side-band Disable for Q4	RO	1'bX	
3	SBI_Q3	Readback of Side-band Disable for Q3	RO	1'bX	
2	SBI_Q2	Readback of Side-band Disable for Q2	RO	1'bX	
1	SBI_Q1	Readback of Side-band Disable for Q1	RO	1'bX	
0	SBI_Q0	Readback of Side-band Disable for Q0	RO	1'bX	

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Byte 34: SBI_READBACK_1(1)					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	SBI_Q15	Readback of Side-band Disable for Q15	RO	1'bX	
6	SBI_Q14	Readback of Side-band Disable for Q14	RO	1'bX	
5	SBI_Q13	Readback of Side-band Disable for Q13	RO	1'bX	
4	SBI_Q12	Readback of Side-band Disable for Q12	RO	1'bX	0 = bit low
3	SBI_Q11	Readback of Side-band Disable for Q11	RO	1'bX	1 = bit high
2	SBI_Q10	Readback of Side-band Disable for Q10	RO	1'bX	
1	SBI_Q9	Readback of Side-band Disable for Q9	RO	1'bX	
0	SBI_Q8	Readback of Side-band Disable for Q8	RO	1'bX	

Byte 35: SBI_READBACK_2(1)					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RO	1'bXXX	
6			RO		
5			RO		
4			RO		
3	SBI_Q19	Readback of Side-band Disable for Q19	RO	1'bX	
2	SBI_Q18	Readback of Side-band Disable for Q18	RO	1'bX	0 = bit low
1	SBI_Q17	Readback of Side-band Disable for Q17	RO	1'bX	1 = bit high
0	SBI_Q16	Readback of Side-band Disable for Q16	RO	1'bX	

Byte 36-37 : RESERVED (Default: 0xXX)

Byte 38: WRITE_LOCK_NCLEAR					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0x0	
6			RW		
5			RW		
4			RW		
3			RW		
2			RW		
1			RW		
0	WRITE_LOCK	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by cycling power.	RW	0	0 = SMBus not locked for writing by this bit. See WRITE_LOCK_R W1C bit. 1 = SMBus locked for writing

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Byte 39: WRITE_LOCK_CLEAR_ LOS_EVENT					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW1C	1'b000000	
6			RW1C		
5			RW1C		
4			RW1C		
3			RW1C		
2			RW1C		
1	LOS_EVT	LOS Event Status When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it.	RW1C	0	0 = No LOS event detected 1 = LOS event detected.
0	WRITE_LOCK_ RW1C	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to it.	RW1C	0	0 = SMBus not locked for writing by this bit. See WRITE_ LOCK bit. 1 = SMBus locked for writing

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Applications Information

Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the PI6CB332020B may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the PI6CB332020B before it has received power.

Flexible Startup Sequencing

PI6CB332020B devices support Flexible Startup Sequencing (FSS), IN+/- pins are PDT. FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table shows the supported sequences; that is, the PI6CB332020B devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Loss of Signal and Automatic Clock Parking

The PI6CB332020B buffers have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOS# pin (the "#" suffix indicates "bar", or active-low) and sets the LOS_EVT bit in the SMBus register space. There are two slightly different LOS# pin behaviors at power up. Figure 4 and Figure 5 show the LOS# de-assertion timing for the 4, 8, 13, 16 and 20-output buffers. CLKIN is represented differentially in Figure 4 and Figure 5.

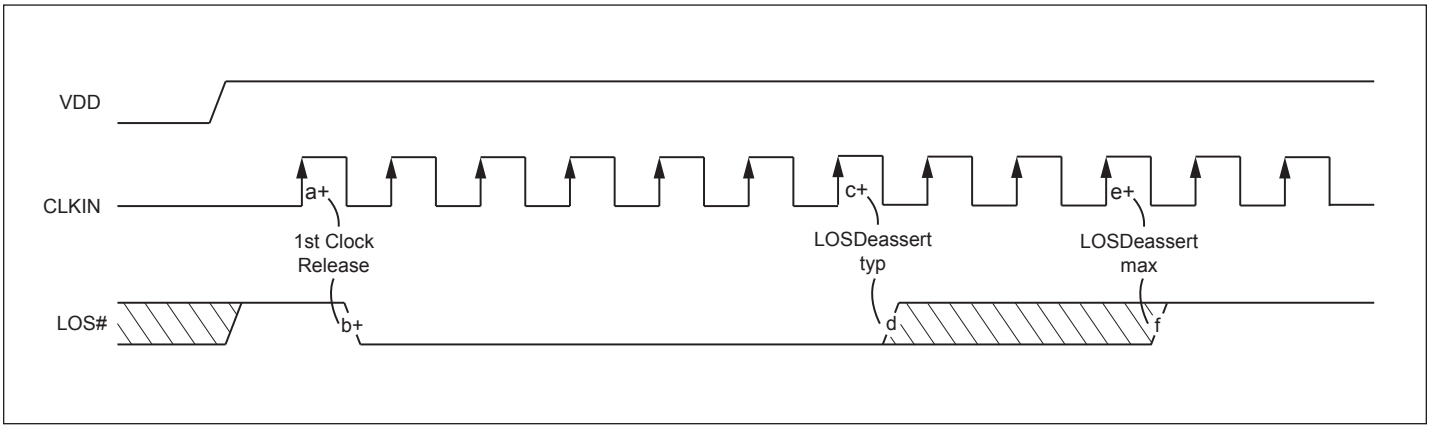


Figure 4. LOS# De-assert Timing for 4/8/13/16 Outputs

Figure 5 shows the LOS# de-assertion timing for the 20-output buffers. LOS# on the 20-output buffers defaults to low at power up.

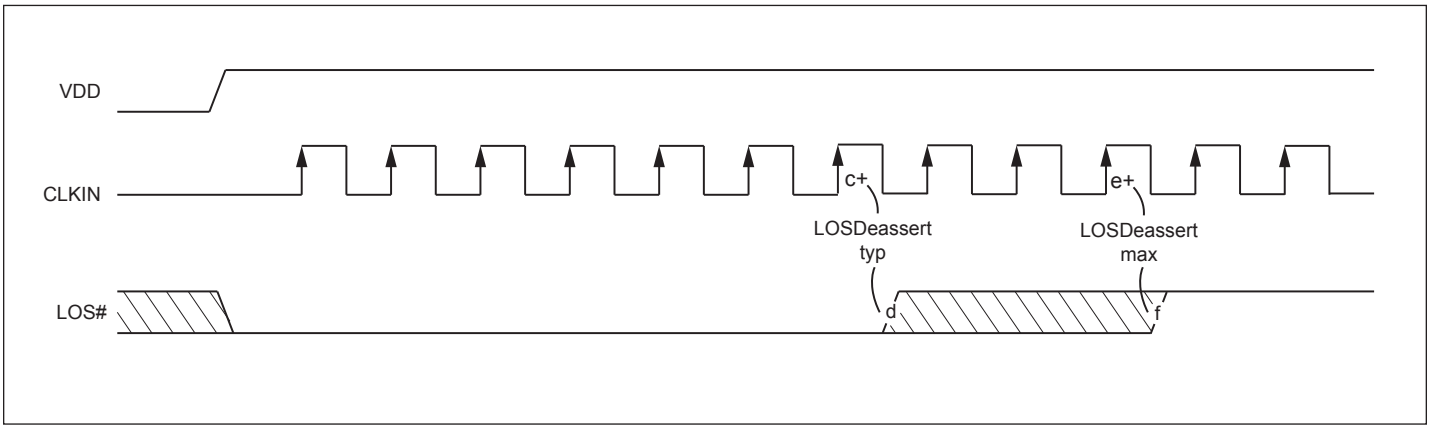


Figure 5. LOS# De-assert Timing for 20 Outputs

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The following diagram shows the LOS# assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the outputs to a HiZ mode state after an LOS event. For exact timing, see Electrical Characteristics.

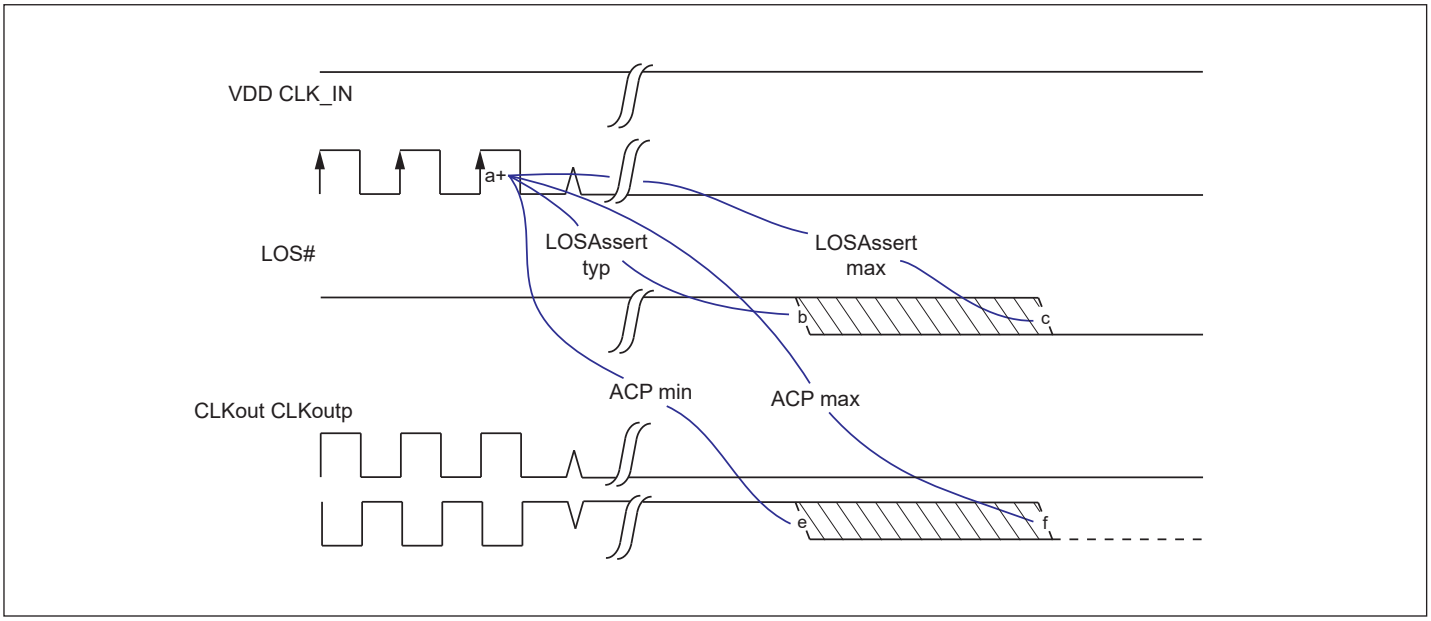


Figure 6. LOS# Assert Timing

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Test Load

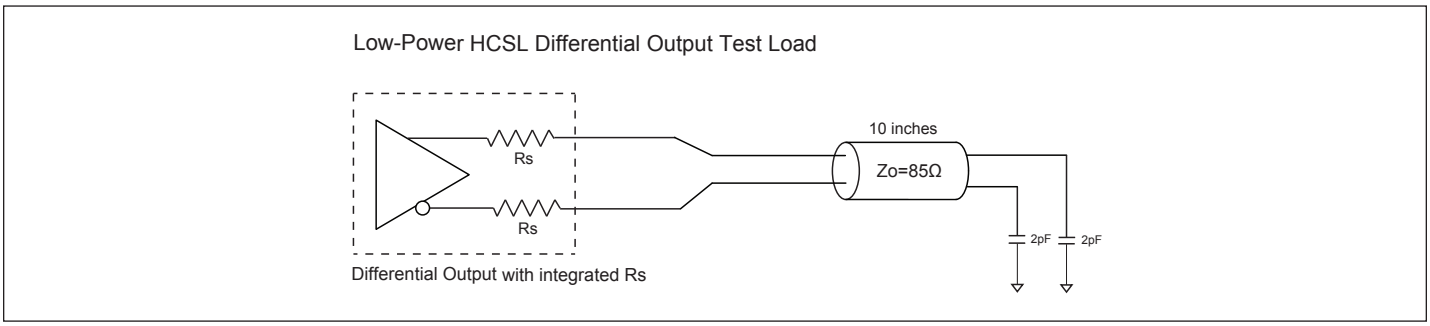


Figure 7. Low Power HCSL Test Circuit

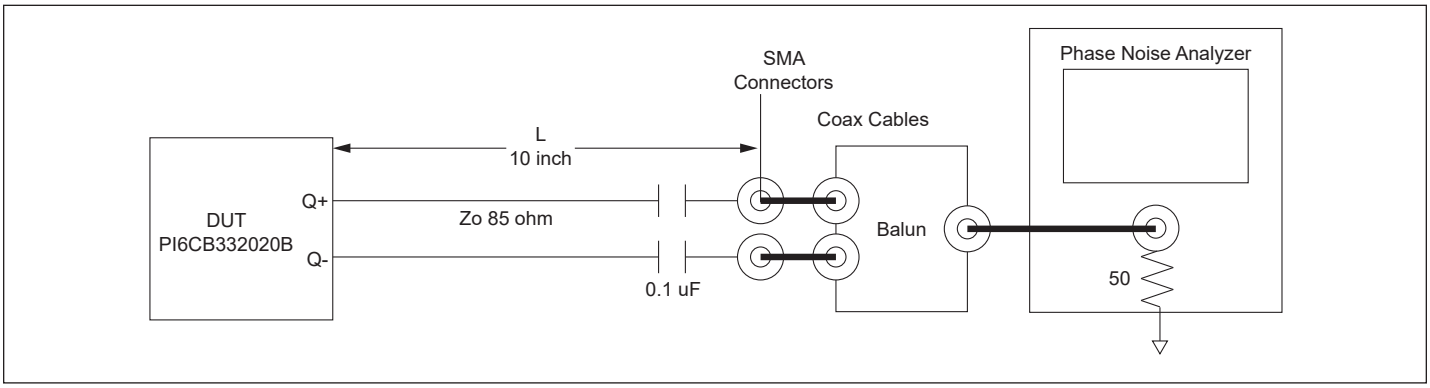


Figure 8. Test Set Up for Phase Jitter Measurement

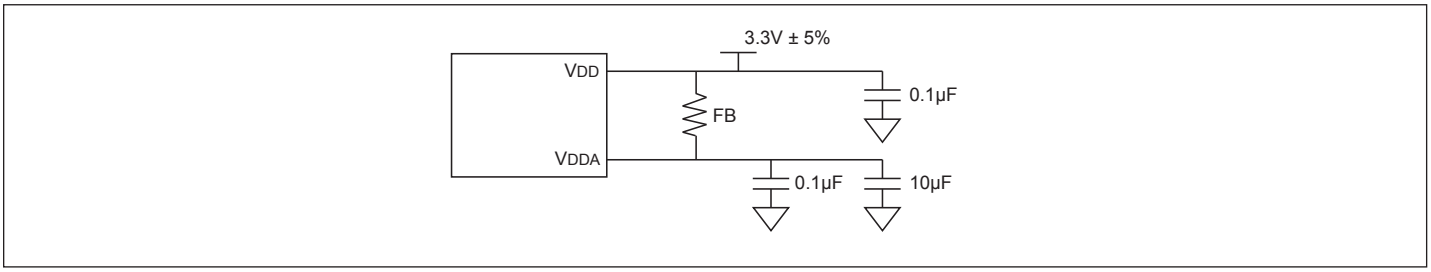
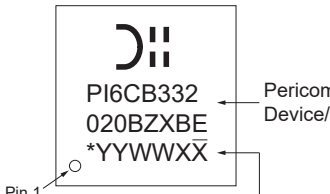


Figure 9. Power Supply Filter

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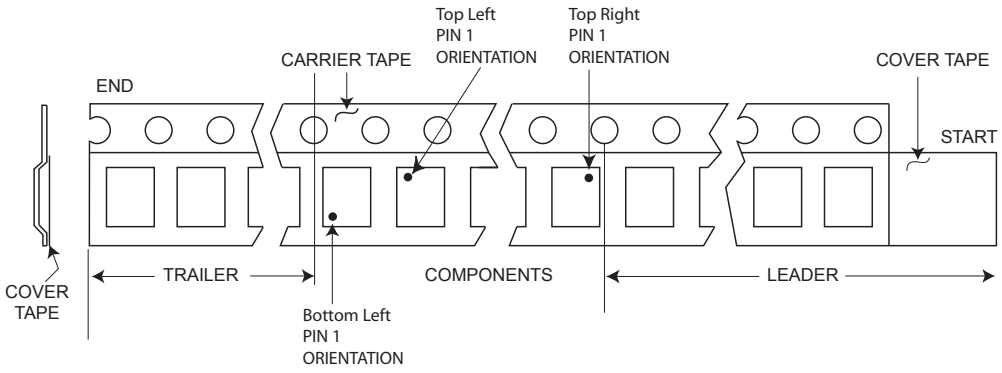
Part Marking



Pericom Product Family
Device/Pkg Type

*: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Note: Date Code per MA-1251

Package Information

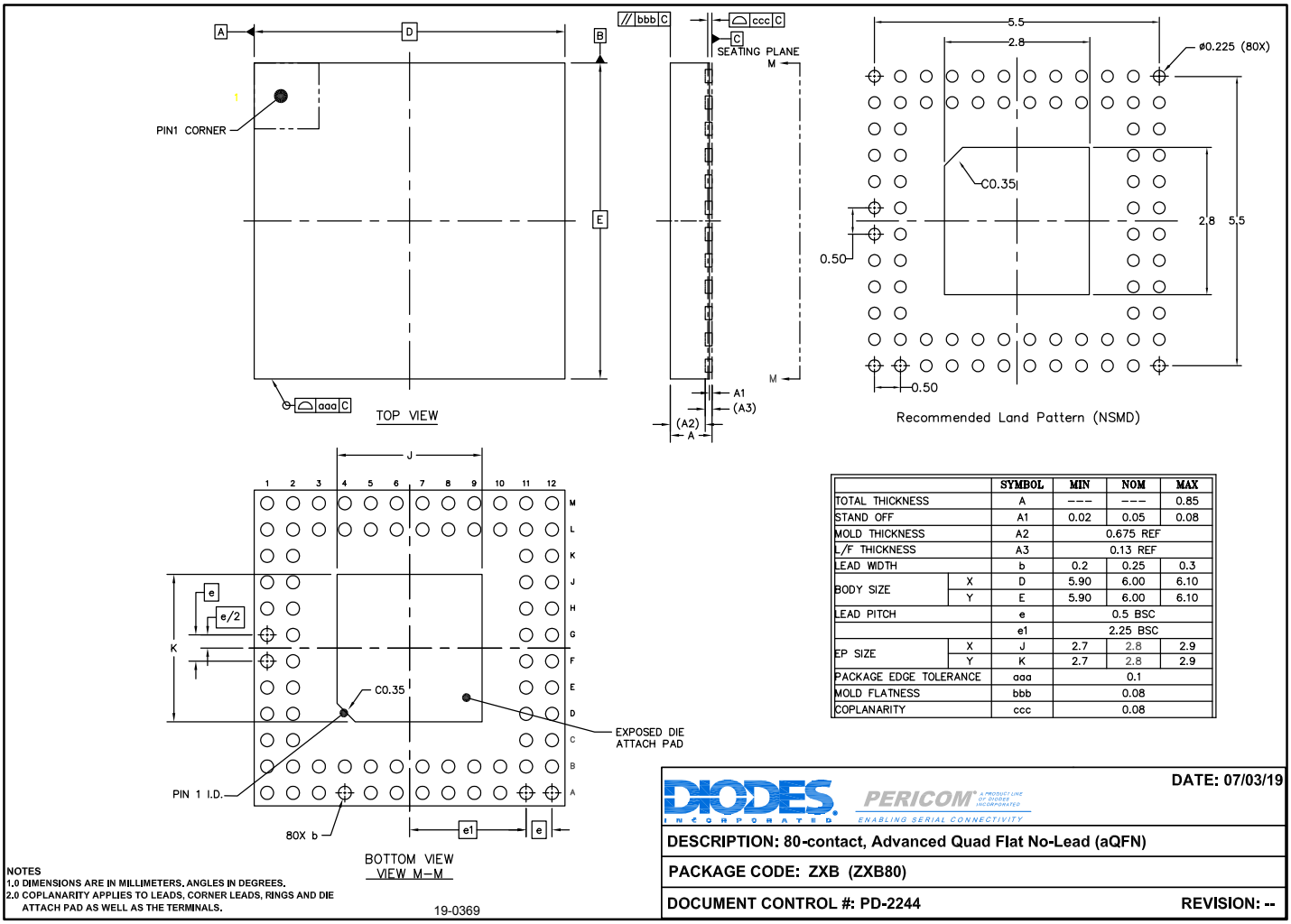


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Packaging Mechanical

80-aQFN (ZXB)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.85
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2		0.675 REF	
L/F THICKNESS		A3		0.13 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
LEAD PITCH		e		0.5 BSC	
		e1		2.25 BSC	
EP SIZE	X	J	2.7	2.8	2.9
	Y	K	2.7	2.8	2.9
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.08	
COPLANARITY		ccc		0.08	

NOTES
1.0 DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS, RINGS AND DIE ATTACH PAD AS WELL AS THE TERMINALS.

DATE: 07/03/19

DESCRIPTION: 80-contact, Advanced Quad Flat No-Lead (aQFN)

PACKAGE CODE: ZXB (ZXB80)

DOCUMENT CONTROL #: PD-2244 REVISION: --

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Ni/Pd/Au Plated Leads, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0653 grams (Approximate)

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Ordering Information

Orderable Part Number	Package Code	Package Description	Pin 1 Orientation	Temperature	Tape Pitch
PI6CB332020BZXBEX	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN) 6x6mm	Top Right Corner	–40~105°C	12mm
PI6CB332020BZXBEX-13	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN) 6x6mm	Top Right Corner	–40~105°C	8mm
PI6CB332020BZXBEX-13R	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN) 6x6mm	Top Left Corner	–40~105°C	12mm

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. A = For 85Ω output impedance
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

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