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December 2015

# FDB0170N607L

# N-Channel PowerTrench® MOSFET **60 V, 300 A, 1.4 m** $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 1.4 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 39 A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low
- High Power and Current Handling Capability
- RoHS Compliant



### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been especially tailored to minimize the on-state resistance while maintaining superior ruggedness and switching performance for industrial applications.

#### **Applications**

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



2. Source/Kelvin Sense

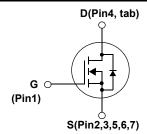
3. Source/Kelvin Sense

4. Drain

5. Source

6. Source 7. Source

D2-PAK (TO263)



#### **MOSFET Maximum Ratings** T<sub>C</sub> = 25 °C unless otherwise noted.

Symbol	Param	eter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			60	V
$V_{GS}$	Gate to Source Voltage			±20	V
I <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25°C	(Note 5)	300	
	-Continuous	T <sub>C</sub> = 100°C	(Note 5)	210	Α
	-Pulsed		(Note 4)	1620	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	1109	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C		250	W
	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	3.8	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 to +175	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB0170N607L	FDB0170N607L	D2-PAK-7L	330mm	24mm	800 units

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# **Electrical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions		Тур.	Max.	Units
Off Chara	octeristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		13		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-13		mV/°C
r	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 39 \text{ A}$		1.1	1.4	mΩ
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS}$ = 10 V, $I_{D}$ = 39 A, $T_{J}$ = 150°C		1.9	3.5	1115.2
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 39 A		159		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	.,	13750	19250	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	3235	4530	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	T = 1 MHZ	240	340	pF
$R_g$	Gate Resistance		2.5		Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				61	97	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 39	$V_{DD}$ = 30 V, $I_{D}$ = 39 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$		64	103	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> =			83	133	ns
t <sub>f</sub>	Fall Time				37	60	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V			173	243	nC
Qg	Total Gate Charge		V <sub>DD</sub> = 30 V,		89	125	
Q <sub>gs</sub>	Gate to Source Gate Charge		I <sub>D</sub> = 39 A		61		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				26		nC

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current				300	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			1620	Α	
$V_{SD}$	Source to Drain Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>S</sub> = 39 A (Note 2)			0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 39 A, di/dt = 100 A/μs		90	144	ns
Q <sub>rr</sub>	Reverse Recovery Charge			95	152	nC

Notes:
1. R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

a) 40 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper.

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0 %.

<sup>3.</sup>  $E_{AS}$  of 1109 is based on starting  $T_J$  = 25 °C, L = 0.3 mH,  $I_{AS}$  = 86 A,  $V_{DD}$  = 10V,  $V_{GS}$  = 54 V. 100% test at L =0.1 mH,  $I_{AS}$  = 124 A.

<sup>4.</sup> Pulsed Id please refer to Figure "Forward Bias Safe Operating Area" for more details.

<sup>5.</sup> Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

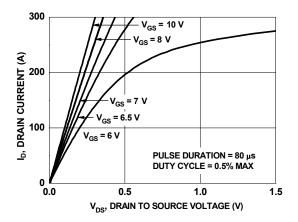


Figure 1. On Region Characteristics

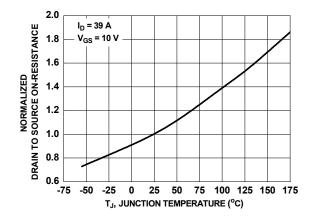


Figure 3. Normalized On Resistance vs. Junction Temperature

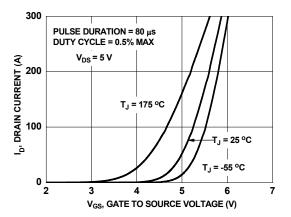


Figure 5. Transfer Characteristics

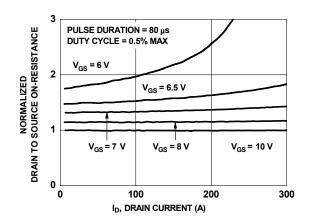


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

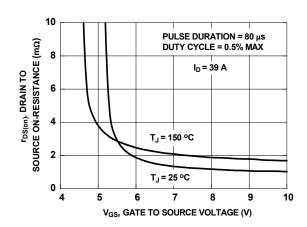


Figure 4. On-Resistance vs. Gate to Source Voltage

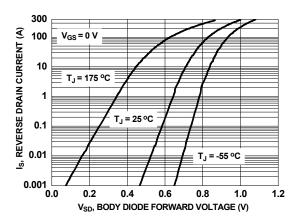
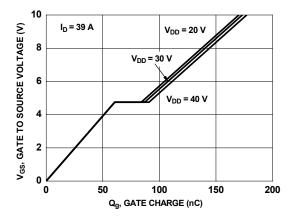
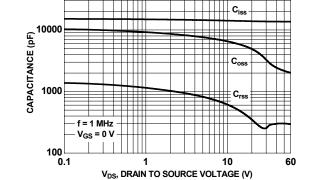


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

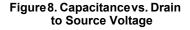
# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

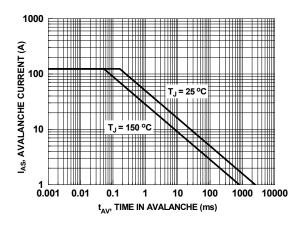




50000

Figure 7. Gate Charge Characteristics





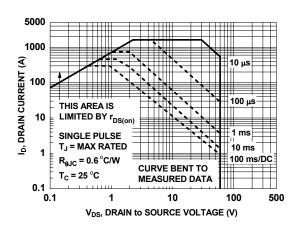


Figure 9. Unclamped Inductive Switching Capability

Figure 10. Forward Bias Safe Operating Area

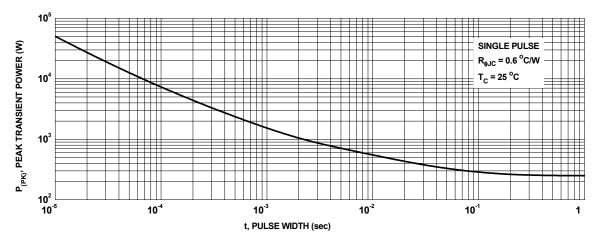


Figure 11. Single Pulse Maximum Power Dissipation

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

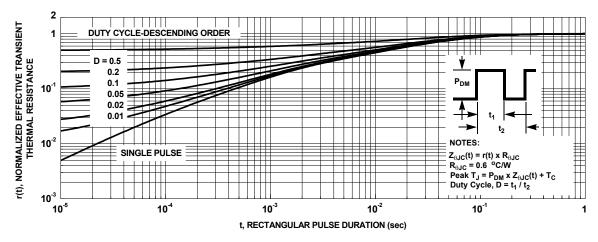
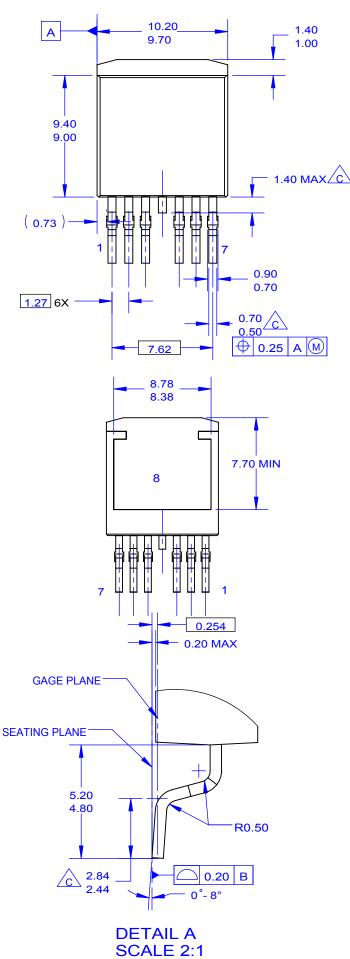
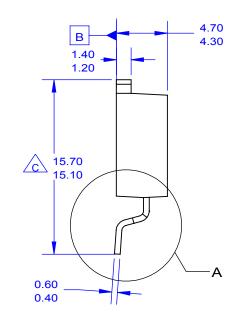


Figure 12. Junction-to-Case Transient Thermal Response Curve



(10.50) (8.40) (10,20) (3.45) (0.95) (1.27) 6X (7.62)

#### LAND PATTERN RECOMMENDATION



#### NOTES:

1.40

1.00

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED. B. ALL DIMENSIONS ARE IN MILLIMETERS.
- OUT OF JEDEC STANDARD VALUE.
  D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC. TO127P1524X465-8N.
- G. DRAWING FILE NAME: TO263A07REV5.

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