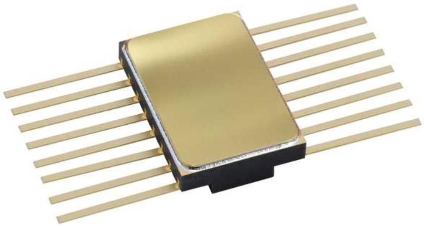
RHFLVDS32A

Rad-hard quad LVDS receivers

Datasheet - production data



Ceramic Flat-16

The upper metallic lid is electrically connected to ground

Features

- LVDS input
- CMOS output
- ANSI TIA/EIA-644 compliant
- 400 Mbps (200 MHz)
- Cold spare on all pins
- Fail-safe function
- 3.3 V operating power supply
- 4.8 V absolute rating
- Power consumption: 43 mW at 3.3 V
- Hermetic package
- Large input common mode: -4 V to +5 V
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm²/mg
- SET/SEU immune up to 32 MeV.cm²/mg
- SMD pin: 5962F98652
- Mass: 0.65 g

Description

The RHFLVDS32A is a quad, low-voltage differential signaling (LVDS) receiver specifically designed, packaged and qualified for use in aerospace environments in a low-power and fast data transmission standard.

The circuit features an internal fail-safe function to ensure a known state in case of an input short circuit or a floating input.

All pins have cold spare buffers to ensure they are in high impedance when V_{CC} is tied to GND.

Designed on ST's proprietary CMOS process with specific mitigation techniques, the RHFLVDS32A achieves “best in the class” for hardness to total ionization dose and heavy ions.

The RHFLVDS32A can operate over a large temperature range of -55 °C to +125 °C and it is housed in an hermetic Ceramic Flat-16 package.

Contents

1 Functional description

Figure 1. Logic diagram and logic symbol

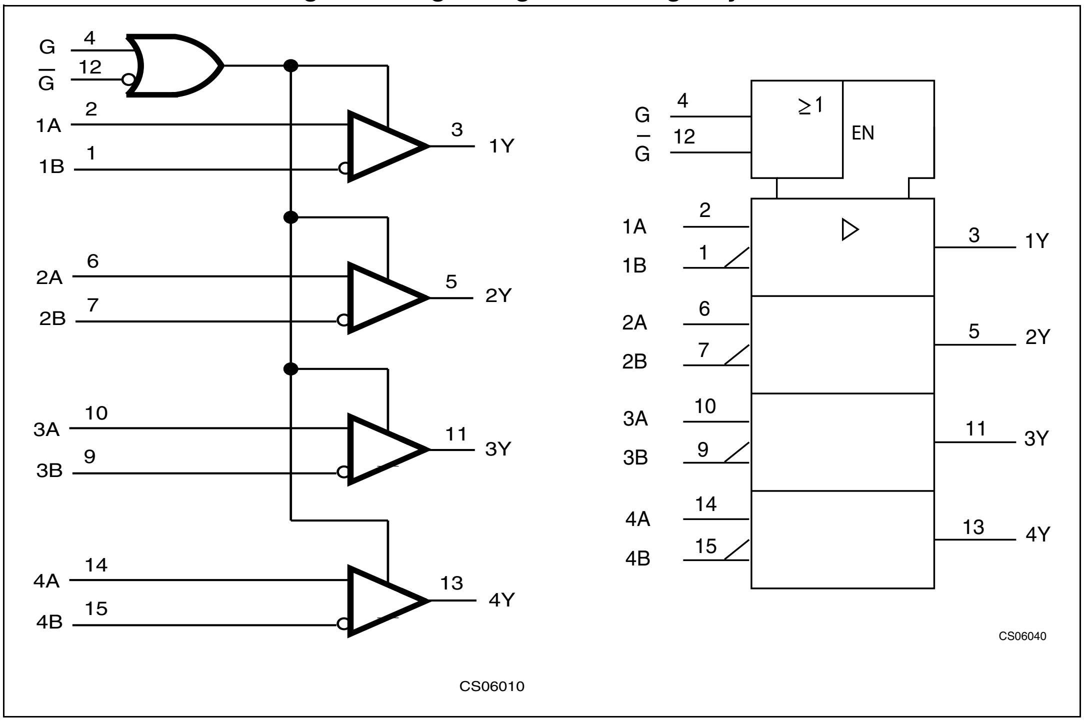


Table 1. Truth table

Differential inputs	Enables		Output
A, B	**G**	**$\overline{G}$**	**Y**
V_{ID} ≥100 mV	H	X	H
	X	L	H
-100 mV < V_{ID} < 100 mV	H	X	?
	X	L	?
V_{ID} ≤-100 mV	H	X	L
	X	L	L
X	L	H	Z
Open/Short or terminated	H	X	H
	X	L	H

Note: 1 *The G input features an internal pull-up network. The $\overline{G}$ input features an internal pull-down network. If they are floating the circuit is enabled.*

2 *Vid = V_{IA}-V_{IB}*

3 *L = low level, H = high Level, X = irrelevant, Z = high impedance (off). ? = intermediate*

2 Pin configuration

Figure 2. Pin connections (top view)

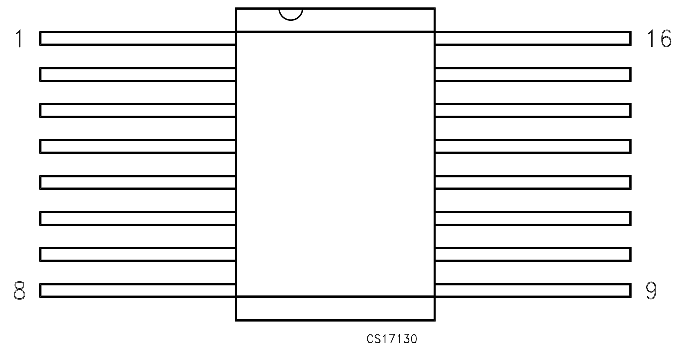


Table 2. Pin description

Pin number	Symbol	Name and function
2, 6, 10, 14	1A to 4A	Receiver inputs
1, 7, 9, 15	1B to 4B	Negated receiver inputs
3, 5, 11, 13	1Y to 4Y	Receiver outputs
4	G	Enable
12	$\overline{G}$	
8	GND	Ground
16	V_{CC}	Supply voltage

3 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Absolute maximum ratings

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Value</th><th>Unit</th></tr>
<tr><td>V_{CC}</td><td>Supply voltage [1]</td><td>4.8</td><td rowspan="3">V</td></tr>
<tr><td>V_i</td><td>TTL inputs (operating or cold-spare)</td><td>-0.3 to 4.8</td></tr>
<tr><td>V_{IN}</td><td>LVDS inputs (operating or cold-spare)</td><td>-5 to +6</td></tr>
<tr><td>V_{ID}</td><td>Differential amplitude on LVDS input (operating or cold-spare)</td><td>5</td><td>Vpp</td></tr>
<tr><td>V_{OUT}</td><td>TTL outputs (operating or cold-spare)</td><td>-0.3 to 4.8</td><td>V</td></tr>
<tr><td>T_{stg}</td><td>Storage temperature range</td><td>-65 to +150</td><td rowspan="2">°C</td></tr>
<tr><td>T_j</td><td>Maximum junction temperature</td><td>+150</td></tr>
<tr><td>R_{thjc}</td><td>Thermal resistance junction to case [2]</td><td>22</td><td>°C/W</td></tr>
<tr><td rowspan="2">ESD</td><td>HBM: Human body model
– All pins
– LVDS inputs vs. GND</td><td>
2
8</td><td>kV</td></tr>
<tr><td>CDM: Machine model</td><td>500</td><td>V</td></tr>
</table>

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 4. Operating conditions

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>V_{CC}</td><td>Supply voltage</td><td>3</td><td>3.3</td><td>3.6</td><td rowspan="2">V</td></tr>
<tr><td>V_{CM}</td><td>Static common mode on the receiver</td><td>- 4</td><td></td><td>+ 5</td></tr>
<tr><td>T_A</td><td>Ambient temperature range</td><td>-55</td><td></td><td>+125</td><td>°C</td></tr>
</table>

4 Radiation

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS32A is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in *Table 6: Electrical characteristics* apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 5. Radiations

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec) up to:	300	krad
Heavy ions	SEL immune up to: (with a particle angle of 60 ° at 125 °C)	135	MeV.cm²/mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C)	67	
	SET/SEU immune up to: (at 25 °C)	32	

5 Electrical characteristics

In *Table 6* below, V_{CC} = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at T_{amb} = +25 °C, min. and max values are at T_{amb} = - 55 °C and + 125 °C unless otherwise specified

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Total enabled supply current, receivers enabled, not switching	V_{ID} = 400 mV		13	15	mA
I_{CCZ}	Total disabled supply current, receivers disabled	V_{ID} = 400 mV G = GND and $\overline{G}$ = V_{CC}			4	
I_{OFF}	LVDS input power-off leakage current(1)	V_{CC} = 0 V, V_{IN} = -4 V to 5 V	-60		60	µA
	TTL I/O power-off leakage current(1)	V_{CC} = 0 V, V_{IN}, G and $\overline{G}$ = 3.6 V, V_{OUT} = 3.6 V	-10		10	
V_{IH}	Enable threshold high level	G and $\overline{G}$ inputs	2		V_{CC}	V
V_{IL}	Enable threshold low level		GND		0.8	
I_{IH}	High level input current	G and $\overline{G}$ inputs V_{CC} = 3.6 V, V_{IN} = V_{CC}	-10		10	µA
I_{IL}	Low level input current	G and $\overline{G}$ inputs V_{CC} = 3.6 V, V_{IN} = 0	-10		10	
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V			-100	mV
		-4 V < V_{CM} < +5 V			-130	
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V	100			
		-4 V < V_{CM} < +5 V	130			
V_{CL}	TTL input clamp voltage	I_{CL} = 18 mA			1.5	V
V_{CMR}	Common mode voltage range	V_{ID} = 200 mVp-p	- 4		+5	
V_{CMREJ}	Common mode rejection(2)	F = 10 MHz		300		mVp-p
I_{ID}	Differential input current	V_{ID} = 400 mVp-p	-10		10	µA
I_{ICM}	Common mode input current	V_{IC} = - 4 V to + 5 V	-70		70	
V_{OH}	Output voltage high	I_{OH} = -0.4 mA, V_{CC} = 3 V	2.7			V
V_{OL}	Output voltage low	I_{OL} = 2 mA, V_{CC} = 3 V			0.25	
I_{OS}	Output short-circuit current	V_{OUT} = 0 V	-90		-30	mA
I_{OZ}	Output tri-state current	Disabled, V_{OUT} = 0 V or V_{CC}	-10		10	µA
C_{IN}	Input capacitance	On each LVDS input vs. GND		3		pF
R_{out}	Output resistance			45		Ω

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PHLD}	Propagation delay time, high to low output	V_{ID} = 200 mVp-p, input pulse from 1.1 V to 1.3 V, V_{CM} = 1.2 V Load: refer to *Figure 3*	1		2.5	ns
t_{PLHD}	Propagation delay time, low to high output		1		2.5	
t_{SK1}	Channel to channel skew(3)	V_{ID} = 200 mVp-p Load: refer to *Figure 3*			0.25	ns
t_{SK2}	Chip to chip skew(4)(5)				0.7	
t_{SKD}	Differential skew(6) (t_{PHLD}-t_{PLHD})				0.3	
t_r	Output signal rise time	Load: refer to *Figure 3*		0.9		
t_f	Output signal fall time			0.9		
t_{PLZ}	Propagation delay time, low level to high impedance output	Load: refer to *Figure 4*			3.8	
t_{PHZ}	Propagation delay time, high level to high impedance output				3.8	
t_{PZH}	Propagation delay time, high impedance to high level output				3.8	
t_{PZL}	Propagation delay time, high impedance to low level output				3.8	
t_{D1}	Fail-safe to active time			1		µs
t_{D2}	Active to fail-safe time			1		

1. All pins except pin under test and V_{CC} are floating.
2. Guaranteed by characterization on the bench.
3. t_{SK1} is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
4. t_{SK2} is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
5. Guaranteed by design. t_{SKD} is the maximum delay time difference between t_{PHLD}-t_{PLHD}
6. t_{SKD} is the maximum delay time difference between t_{PHLD} and t_{PLHD}, see *Figure 3*.

Cold sparing

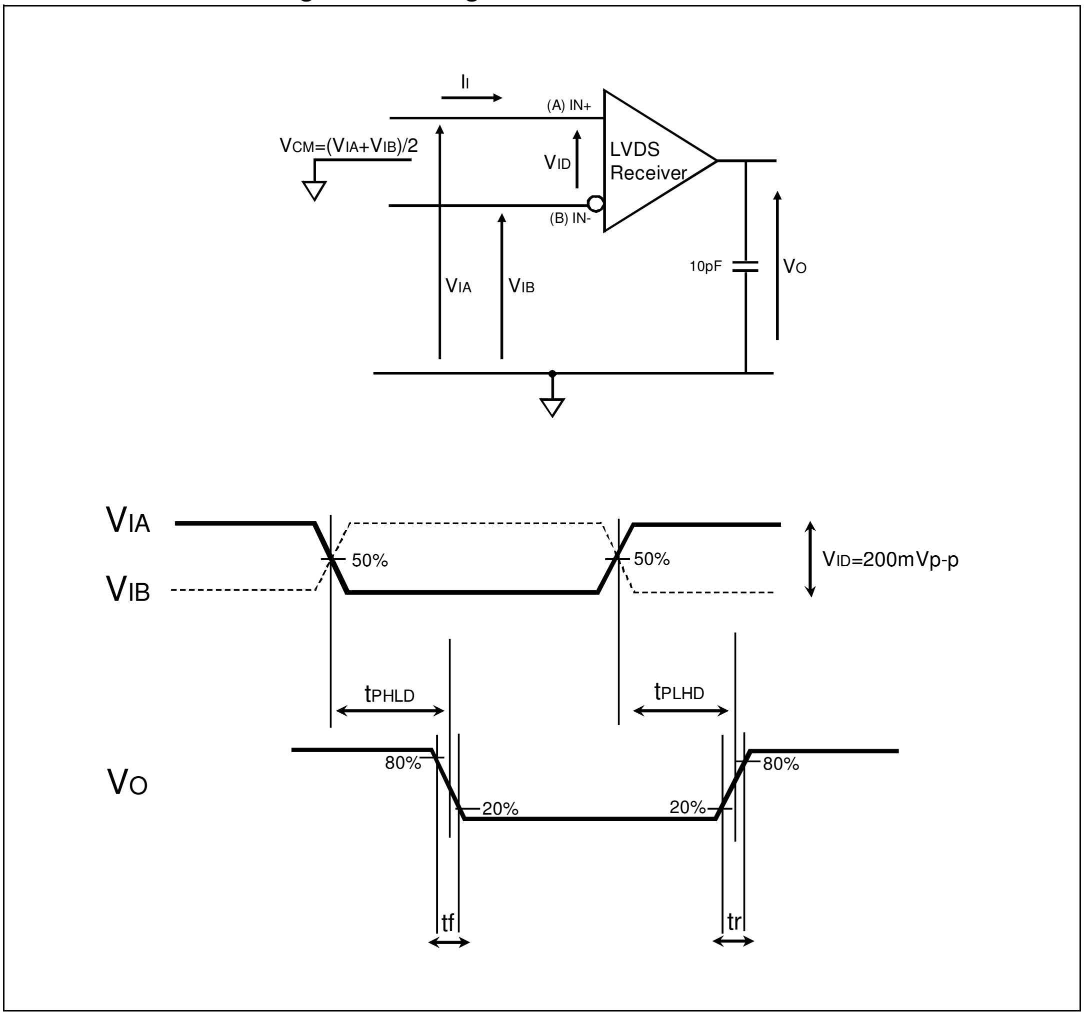
The RHFLVDS32A features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. The ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short circuit or floating inputs, the TTL outputs remain in stable logic-high state.

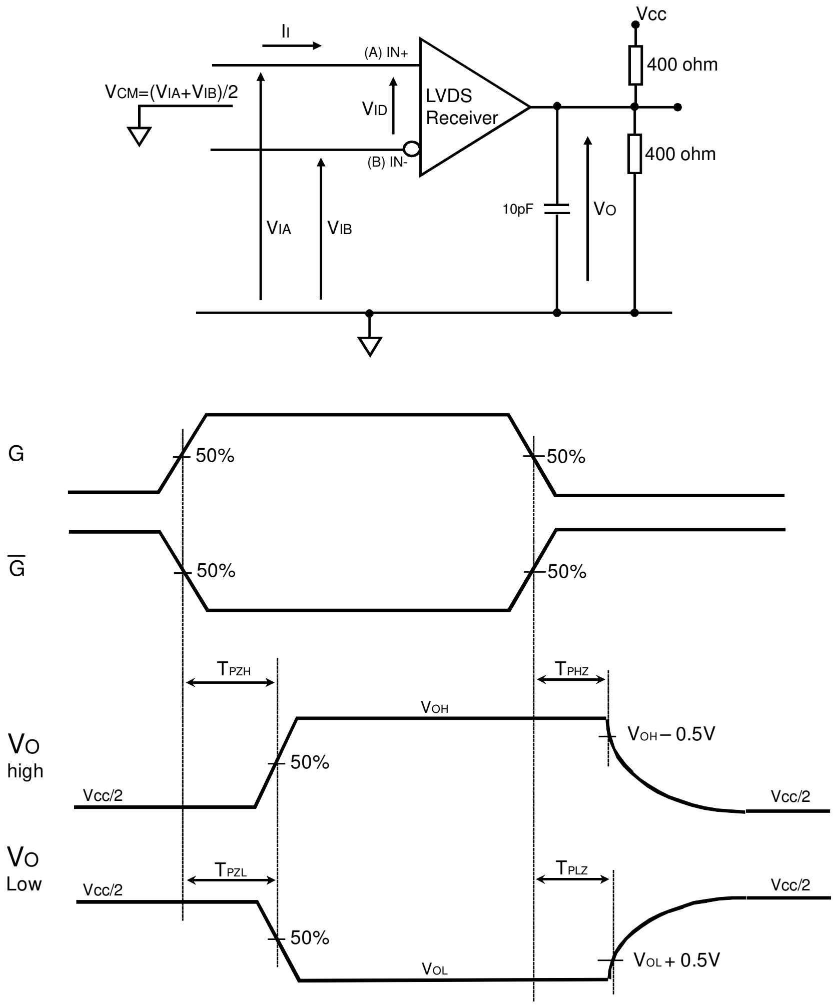
6 Test circuit

Figure 3. Timing test circuit and waveform



1. All input pulses are supplied by a generator with the following characteristics: t_r or t_f ≤ 1 ns, f = 1 MHz, Z_O = 50 Ω, and duty cycle = 50%.
2. The product is guaranteed in test with CL = 10 pF

Figure 4. Enable and disable time test circuit and waveform



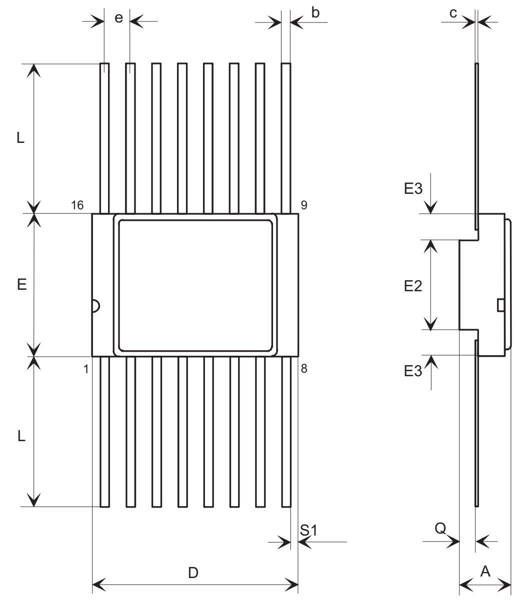
1. All input pulses (including G and $\overline{G}$) are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f_G or $f_{\overline{G}}$ = 500 kHz, and pulse width G or $\overline{G}$ = 500 ns.
2. *The product is guaranteed in test with CL = 10 pF*

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Ceramic Flat-16 package information

Figure 5. Ceramic Flat 16 package mechanical drawing



1. The upper metallic lid is electrically connected to ground.

Table 7. Ceramic Flat 16 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.75		10.13	0.384		0.399
E	6.75		7.06	0.266		0.278
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

8 Ordering information

Table 8. Order codes

Order code	SMD (1)	Quality level	Mass	Package	Lead finish	Marking (2)	Packing
RHFLVDS32AK1	-	Engineering model	0.65 g	Flat-16 with grounded lid	Gold	RHFLVDS32AK1	Conductive Strip pack
RHFLVDS32AK01V	5962F98652	QML-V Flight				5962F9865207VZC	
RHFLVDS32AK02V					Solder Dip	5962F9865207VZA	

1. Standard microcircuit drawing.
2. Specific marking only. Complete marking includes the following:

- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- Country of origin (FR = France)

Note: Contact your ST sales office for information about the specific conditions for products in die form.

9 Shipping information

Date code

The date code (date the package was sealed) is structured as follows

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in table 9 below.

The Certificate of Conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the Certificate of Conformance, is provided on a CDROM.

Note: Contact ST for details on the documentation of other quality levels.

Table 9. Product documentation

Quality level	Item
Engineering Model	Certificate of Conformance including: Customer name Customer Purchase Order number ST Sales Order number & Item ST Part Number Quantity delivered Date Code Reference to ST datasheet Reference to TN1181 on Engineering Models ST Rennes assembly lot ID
QML-V Flight	Certificate of Conformance including: Customer name Customer Purchase Order number ST Sales Order number & Item ST Part Number Quantity delivered Date Code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality Control Inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND test (1)
	SEM inspection report (2)
	X-Ray plates

1. PIND: Particle Impact Noise Detection.
2. SEM: Scanning Electronic Microscope.

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Oct-2013	1	Initial release
30-Oct-2014	2	– Updated production status and marking information relative to order code RHFLVDS32AK01V in Table 1: Device summary and Table 9: Order codes. – Removed row regarding CL parameter from Table 5: Operating conditions. – Changed title of Section 4 to “Radiation” and moved Electrical characteristics to Section 5.
04-Mar-2015	3	– Added V_{OUT} to Table 4: Absolute maximum ratings. – Added V_{CL} to Table 7: Electrical characteristics.
28-Apr-2017	4	– Table 1: Device summary: added mass value.
10-Nov-2023	5	– Added VIN and VID in Table 4: Absolute maximum ratings.
09-Dec-2024	6	– Added features on the cover page. – Updated figure on the cover page, *Table 4*, *Section 8* and *Section 9*.