

# USB Type-C port controller for power sinks

## General description

EZ-PD™ BCR-LITE is highly-integrated pre-programmed USB Type-C sink port controller and a part of the barrel connector replacement (BCR) family. It has the ability to support ports with or without USB data capability. It mainly targets electronic devices that have legacy barrel connectors or USB micro-B connectors for power such as drones, smart speakers, power tools, and other rechargeable devices.

EZ-PD™ BCR-LITE complies with the latest USB Type-C standard and enables users to quickly convert their devices from being powered through a barrel connector to being powered via the USB-C connector with few external components and no additional firmware development. EZ-PD™ BCR-LITE integrates a complete USB Type-C transceiver, a load switch controller with a soft start, all termination resistors required for a USB Type-C port, and system-level ESD protection. It is available in a 24-pin QFN package.

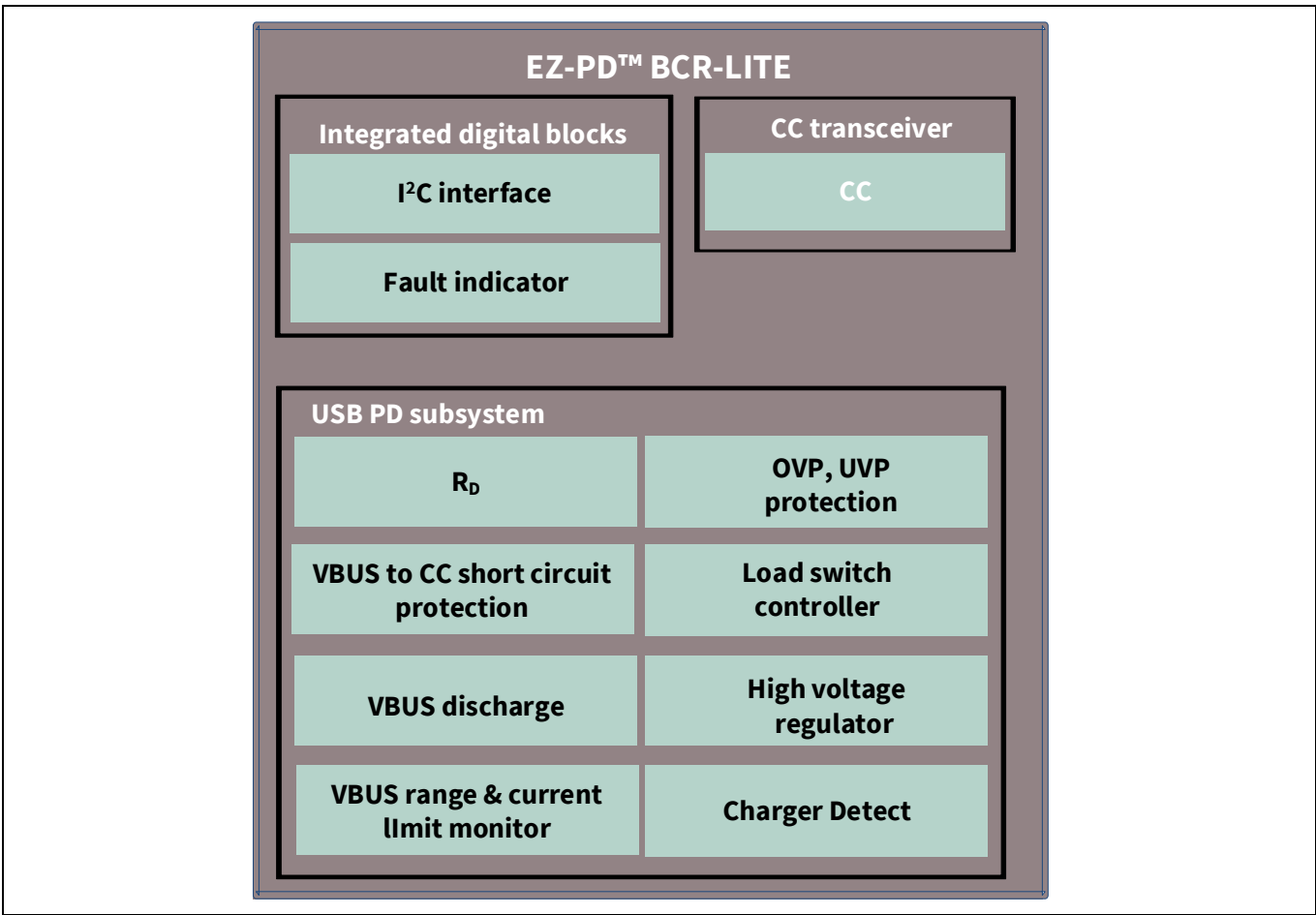
## Features

- USB Type-C support
  - Supports one USB Type-C port with the capability of sinking 5 V @ 3 A
- Legacy charging
  - Support for legacy charging or Type-C 5 V operation when connected to USB Type-A ports
  - Support for legacy charging protocols like BC1.2, Apple, AFC, QC 2.0<sup>[1]</sup>
  - Enables negotiation of VBUS > 5 V (total power > 15 W) using D+/D-
- System-level fault protection
  - VBUS to CC short protection
  - On-chip over-voltage protection (OVP)
- Power
  - 3.0 V to 24.5 V operation (30 V tolerant)
  - Integrated VBUS load switch gate drivers with in-rush current control
- Configurability
  - I<sup>2</sup>C based host processor interface (HPI) for dynamic configuration and reporting
- System-level ESD protection
  - On CC, VBUS\_IN\_DIS, DC\_OUT\_DIS, D+, D-, HPI\_SDA, and HPI\_SCL pins
  - ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C
- Packages
  - 24-pin QFN package
  - Supports extended industrial temperature range (–40°C to +105°C)

### Note

1. Customers need to acquire their own licensing for AFC and QC2.0.

Logic block diagram



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# 1 Functional overview

## 1.1 USB PD subsystem

The USB PD subsystem provides the interface to the USB Type-C USB port. This subsystem comprises a high-voltage regulator, OVP, and supply switch blocks. This subsystem also includes all ESD protection required and supported on the USB Type-C port.

### 1.1.1 USB Type-C physical layer

The USB Type-C block includes the termination resistor  $R_D$  which is required to implement connection detection, plug orientation detection, and for establishing USB UFP role.

According to the USB Type-C spec, a USB Type-C controller such as the EZ-PD™ BCR-LITE device must present certain termination resistors depending on its role in its unpowered state. The Sink role requires  $R_D$  resistor to be present on the CC pins even in an unpowered state. To implement this function, EZ-PD™ BCR-LITE has a dead battery  $R_D$  resistor bonded to both the CC pins.

### 1.1.2 VBUS overvoltage, undervoltage protection

The EZ-PD™ BCR-LITE device has an integrated hardware block for VBUS OVP and UVP with thresholds and response times that are configurable over HPI.

In an event of OVP, the BCR-LITE device informs the external master about the event.

### 1.1.3 VBUS short protection

The EZ-PD™ BCR-LITE device provides VBUS short protection on CC1 and CC2 pins. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A USB-PD controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, the EZ-PD™ BCR-LITE device can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the CC1 and CC2 pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without the EZ-PD™ BCR-LITE device connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when the EZ-PD™ BCR-LITE device is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

### 1.1.4 Sink load switch controller on VBUS path

The EZ-PD™ BCR-LITE device has an integrated load switch controller to drive external PFETs on the VBUS sink path. This load switch controller has a soft start feature that limits the in-rush current flowing through the sink power path when the system is connected to an external load and powered on.

### 1.1.5 SAFE\_PWR\_EN gate driver

The EZ-PD™ BCR-LITE device has a SAFE\_PWR\_EN gate driver that can be used to drive an alternate load switch/FET. It is enabled whenever the EZ-PD™ BCR-LITE device is unable to negotiate the requested power contract. In such a scenario, the EZ-PD™ BCR-LITE device negotiates a 5 V contract which can be delivered through the SAFE\_PWR\_EN FET to an alternate power rail in the system. This allows the system to operate in a limited mode when the requested power is unavailable through the USB Type-C port. Note that the SAFE\_PWR output is available only when CHARGING\_MODE pin is set to enable all legacy charging protocols.

### 1.1.6 VBUS discharge FETs

The EZ-PD™ BCR-LITE device also has an integrated VBUS discharge FET used to discharge VBUS upon disconnection of the source.

## 1.2 Integrated digital blocks

### 1.2.1 Serial communication block (SCB)

The integrated SCB is configured to act as an I<sup>2</sup>C block for the EZ-PD™ BCR-LITE device. The EZ-PD™ BCR-LITE device has an I<sup>2</sup>C slave interface that can be connected to an I<sup>2</sup>C host. The slave address is 0x08. Contact Technical Support for further details related with EZ-PD™ BCR-PLUS/BCR-LITE host processor interface specification.

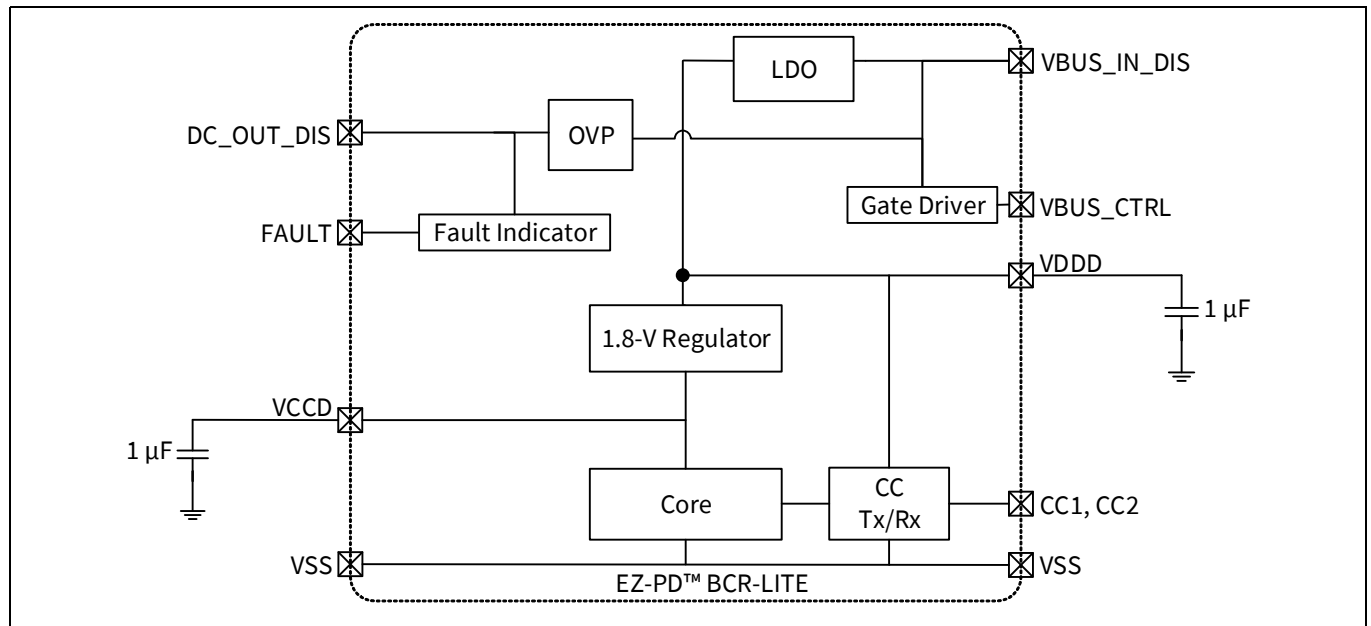
The I<sup>2</sup>C interface is capable of operating at speeds of up to 1 Mbps (fast-mode plus). The I<sup>2</sup>C interface is also compatible with the I<sup>2</sup>C standard-mode, fast-mode, and fast-mode plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual ([UM10204](#)). The I<sup>2</sup>C bus I/Os are implemented with GPIO in open-drain modes.

The I<sup>2</sup>C interface is not completely compliant with the I<sup>2</sup>C spec in the following aspects:

- Fast-mode plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8-mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and fast-mode plus specify minimum fall times, which are not met with the GPIO cell; slow strong mode can help meet this spec depending on the bus load.

## 2 Power systems overview

The EZ-PD™ BCR-LITE device can operate from two possible external supply sources: VBUS\_IN\_DIS (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS\_IN\_DIS, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. Refer to the application diagram (see [Figure 3](#)) for capacitor connections.



**Figure 1** Power system requirement block diagram

## 3 Pinouts

**Table 1** EZ-PD™ BCR-LITE pin descriptions

24-pin QFN	Pin name	Description
1	VBUS_MIN	Connect a resistor divider to this pin that is connected to 3.3 V (from the VDDD pin) to indicate the minimum voltage needed by the system from the attached power adapter. See <a href="#">Table 2</a> in <a href="#">Application overview</a> section for details. VBUS_MIN must be set to 5 V if the application needs to inter-operate with USB Type-C or USB Type-A power sources that provide only 5 V supply.
2	VBUS_MAX	Connect a resistor divider to this pin that is connected to 3.3 V (from the VDDD pin) to indicate the maximum voltage needed by the system from the attached power adapter. See <a href="#">Table 2</a> in <a href="#">Application overview</a> section for details.
3	VBUS_CTRL	Connect this pin to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver that is slew-rate controlled. This signal is enabled when the EZ-PD™ BCR-LITE device successfully negotiates a power contract within the requested range set by VBUS_MIN and VBUS_MAX voltage settings.
4	SAFE_PWR_EN	Connect this signal to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver. This signal is enabled when the EZ-PD™ BCR-LITE device fails to negotiate for higher power and defaults to 5 V.
5	D+	USB D+. Connect this pin to the D+ line of the Type-C connector for support for legacy and proprietary charging.
6	D-	USB D-. Connect this pin to the D- line of the Type-C connector for support for legacy and proprietary charging.
7	HPI_INT/SWD_DAT	Active low HPI Interrupt pin.
8	FAULT/SWD_CLK	The EZ-PD™ BCR-LITE device pulls this pin high if the power adapter cannot supply the required voltage or current or if an OVP/UVF event is detected. The pin is low otherwise.
9	CHARGING_MODE	This pin can be configured in 2 different ways to support the legacy charging protocols: <ul style="list-style-type: none"> <li>Option 1: BC1.2 support only. Connect pin to a 5 kΩ resistor pulled up to VDDD</li> <li>Option 2: All legacy charging protocols supported: Leave this pin floating.</li> </ul>

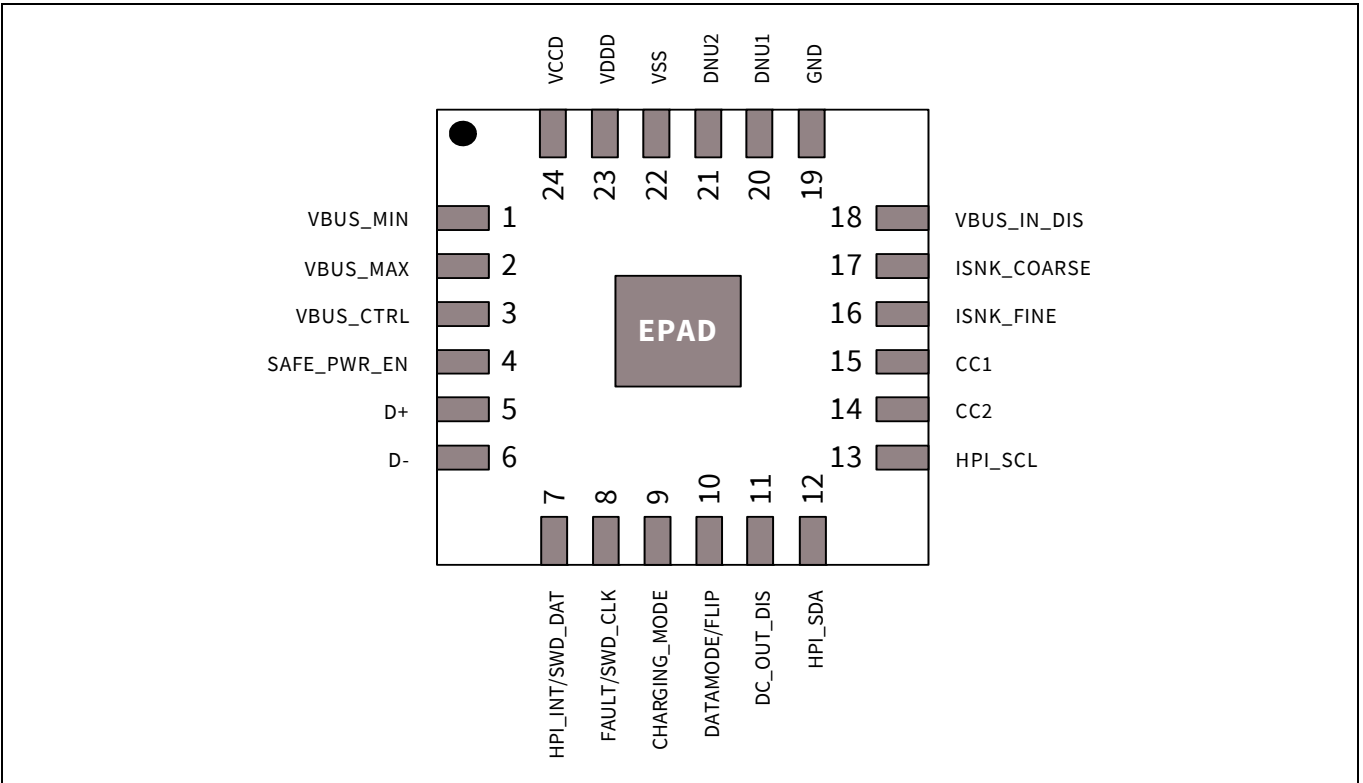
## Pinouts

**Table 1** EZ-PD™ BCR-LITE pin descriptions (continued)

24-pin QFN	Pin name	Description
10	DATAMODE/FLIP	Connect this pin to a 1 kΩ pull-up resistor for applications that do not require data communication. Leave this pin unconnected for applications that need to sink power as well as support USB communication. Once the BCR-LITE device is powered up, this pin will be sampled to determine the data mode of the device. When this pin is left unconnected, it will also be reconfigured to indicate the orientation of the type-C cable connection after sampling this pin. In the output mode (FLIP functionality), the EZ-PD™ BCR-LITE device drives this line low if no device is attached or if CC polarity is unflipped (CC1 connected). If a device is attached on CC2 (polarity is flipped), the EZ-PD™ BCR-LITE device drives this line high. While reporting FLIP status, this is a strong drive output pin.
11	DC_OUT_DIS	Connect this pin to the output of the PFETs controlled by the VBUS_FET_EN pin. This is used for monitoring the VBUS output. This is the power output of the system.
12	HPI_SDA	This is the I <sup>2</sup> C slave interface provided for a host processor to control and monitor the EZ-PD™ BCR-LITE device. For more details, refer to the EZ-PD™ BCR-PLUS/BCR-LITE host processor interface specification.
13	HPI_SCL	
14	CC2	Communication Channel 2 pin used to negotiate a voltage/current with the attached adapter.
15	CC1	Communication Channel 1 pin used to negotiate a voltage/current with the attached adapter.
16	ISNK_FINE	Connect resistor divider networks to these pins that are to 3.3 V (from the VDDD pin) to set the operating current requested from the power adapter. See <a href="#">Table 3</a> and <a href="#">Table 4</a> in <a href="#">Application overview</a> section for details. The settings on these pins will be considered only for legacy charging protocols that support a sink current request (for e.g.: AFC).
17	ISNK_COARSE	
18	VBUS_IN_DIS	Connect to VBUS of USB Type-C connector. Used to supply power to the EZ-PD™ BCR-LITE device and monitor incoming voltage.
19	GND	System ground pin
20	DNU1	Leave this pin unconnected
21	DNU2	Leave this pin unconnected
22	VSS	Ground pin, connect to USB Type-C connector GND.
23	VDDD	Output of internal 3.3 V regulator. Connect 1 μF and 2x 100 nF capacitors to this pin.
24	VCCD	Output of internal 1.8 V regulator. Connect a 1 μF decoupling capacitor to this pin.
–	EPAD	Ground. Connect to same ground as VSS.

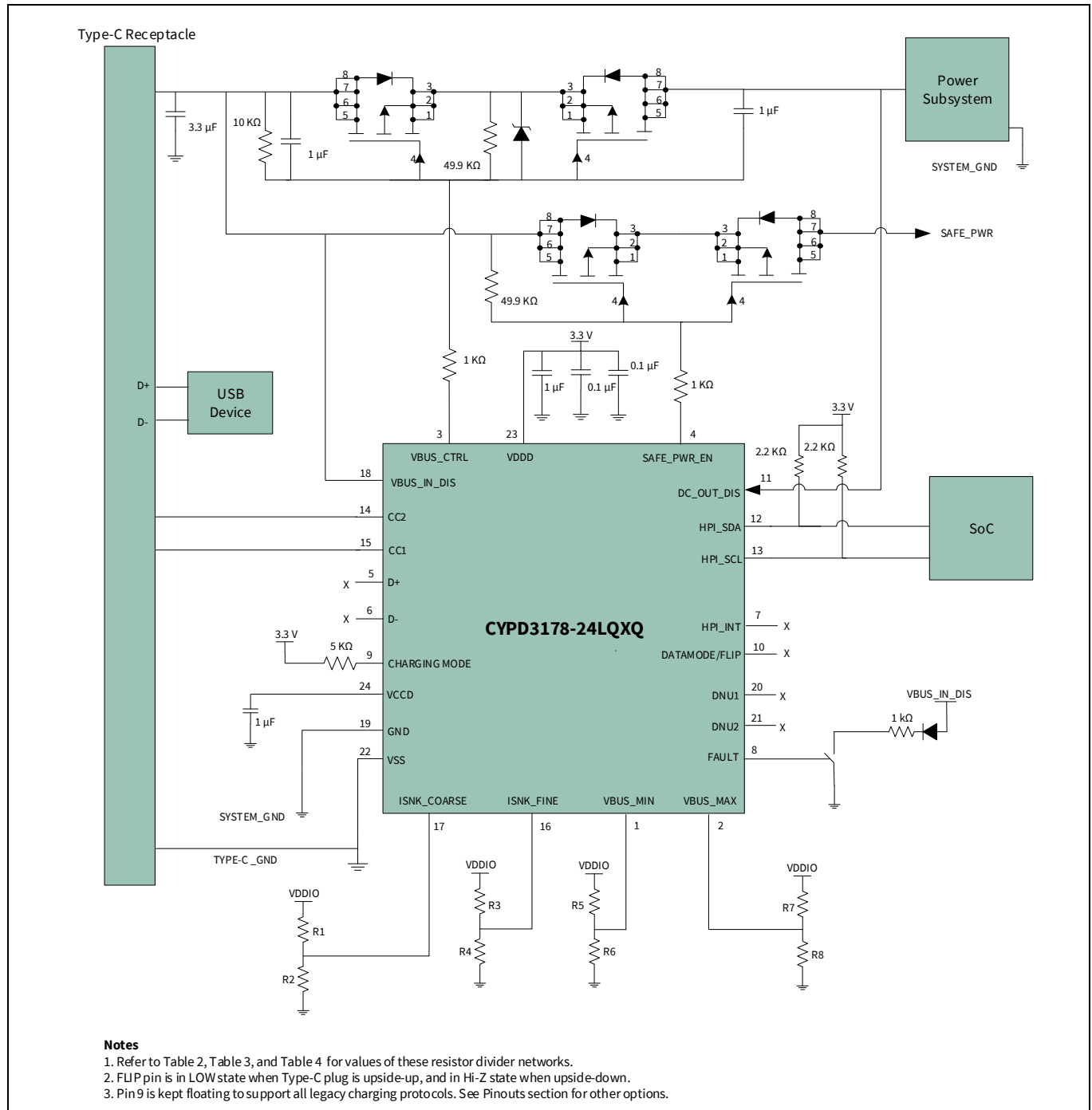


## Pinouts



**Figure 2** Pinout of 24-QFN package (top view)





**Figure 4** EZ-PD™ BCR-LITE based application diagram for power sinks plus data peripherals

The four sets of resistor divider networks are used to determine the voltage and current range that the EZ-PD™ BCR-LITE device will negotiate with the USB Type-C power adapter. [Table 2](#), [Table 3](#), and [Table 4](#) show the values of pull-up and pull-down resistors on each pin applicable for a desired VBUS\_MIN, VBUS\_MAX, ISNK\_COARSE or ISNK\_FINE value.

### Notes

- VBUS\_MAX should be set to select a voltage that is higher than or equal to that set by VBUS\_MIN.
- EZ-PD™ BCR-LITE device does not monitor the current on VBUS\_IN\_DIS and enforce it within ISNK limits. It is the responsibility of the system to not consume more current than what the power adapter can provide.
- VBUS\_MIN and VBUS\_MAX can be set to the same value to select one specific voltage level from the Type-C power adapter.
- Ensure that the board layout design does not inject any noise into the VBUS\_MIN, VBUS\_MAX, ISNK\_COARSE, ISNK\_FINE pins.
- To be able to negotiate a power contract with USB Type-C only power adapters, the VBUS\_MIN must be set to 5 V.
- ISNK\_COARSE and ISNK\_FINE values are only considered for a power contract that is made using the AFC protocol. All other protocols supported by the CYPD3178 device do not support sink current requests.

**Table 2 Resistor divider values for minimum or maximum voltage requested on VBUS**

Voltage requested (V)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
5	0/6	Open	0	0–248
9	1/6	5.1	1	249–786
12	2/6	5.1	2.4	787–1347
15	3/6	5.1	5.1	1348–1920
19	4/6	5.1	10	1921–2778
20	≥ 5/6	0	Open	≥ 2779

**Table 3 Resistor divider values for coarse setting on operating current (for VDDD = 3.3 V)**

Operating current requested for coarse setting (A)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
0	0/6	Open	0	0–248
1	1/6	5.1	1	249–786
2	2/6	5.1	2.4	787–1347
3	3/6	5.1	5.1	1348–1920
4	4/6	5.1	10	1921–2778
5	≥ 5/6	0	Open	≥ 2779

**Table 4 Resistor divider values for fine setting on operating current (for VDDD = 3.3 V)**

Operating current requested for fine setting (A)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
+0	0/6	Open	0	0–248
+250	1/6	5.1	1	249–786
+500	2/6	5.1	2.4	787–1347
+750	3/6	5.1	5.1	1348–1920
+900	≥ 4/6	0	Open	≥ 1921

## 4.1 FAULT pin behavior

The FAULT pin is driven low by default, and is driven high under the following conditions:

- A power contract was negotiated but none of the voltages offered are within VBUS\_MIN and VBUS\_MAX ranges.
- Voltages offered by the power adapter are within VBUS\_MIN, VBUS\_MAX range but the current is below the ILIM limit (applicable to AFC protocol only).
- VBUS voltage supplied by power adapter is outside expected limits.

## 4.2 SAFE\_PWR\_EN pin behavior

This gate driver is enabled when the power contract defaults to 5 V due to mismatching capabilities. This driver is not enabled when the device is configured so that 5 V input is accepted by the system. This driver is also not enabled when there is an overvoltage condition on the 5 V VBUS input at the USB-C connector.

The system can use this power to run any digital logic (on embedded controller) that notifies the user about an incompatible power adapter.

## 4.3 VBUS\_FET\_EN pin behavior

This gate driver is enabled when a power adapter with matching power capabilities is detected, as determined by the VBUS\_MIN, VBUS\_MAX, ISNK\_COARSE, and ISNK\_FINE pins. When enabling the gate driver, the current sink inside the driver is used to ensure that the gate voltage rises slowly (rate of rise can be externally controlled) which in turn controls the inrush current of the system.

When VBUS is out of range (i.e. in an event of OVP or UVP), the gate driver is quickly disabled. This gate driver can be turned on or off independently over HPI interface.

## 4.4 Legacy charging support

BCR-LITE device supports BC 1.2, QC 2.0 sink (Class B), AFC and Apple charging protocols. When a non-PD charger is connected, the BCR-LITE device is able to negotiate any of the legacy charging protocols supported by the sink device. Customers can select support for all legacy charging protocols or BC1.2 protocol based on the hardware setup for the CHARGING\_MODE pin (see [Pinouts](#) for more details). If the connected Type-C charger supports multiple charging protocols, then the order of priority of negotiation is as follows:

**Negotiation sequence:** (BC1.2 → AFC → QC2.0 (Class B) → Apple → Type-C only)

When negotiating legacy protocols, the BCR-LITE device negotiates voltage and current based on the VBUS\_MIN/MAX and ISNK\_COARSE/ISNK\_FINE settings. Note that when VBUS\_MIN and VBUS\_MAX are set to 5 V, the BCR-LITE device is capable of accepting VBUS voltages between 4.75 V to 5.5 V when negotiating legacy charging protocols. If the power adapter is not able to support the voltage/current requirements, then the BCR-LITE device negotiates a 5V contract and turns on the SAFE\_PWR path.

### 5 Electrical specifications

#### 5.1 Absolute maximum ratings

**Table 5 Absolute maximum ratings**

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
$V_{BUS\_MAX}$	Max supply voltage relative to $V_{SS}$ on $VBUS\_IN\_DIS$ and $DC\_OUT\_DIS$ pins	–	–	30	V	Absolute max.
$V_{DDD\_MAX}$	Max supply voltage relative to $V_{SS}$	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins	–	–	22 <sup>[2]</sup>	V	
$V_{GPIO\_ABS}$	GPIO voltage	–0.5	–	$V_{DDD} + 0.5$	V	
$I_{GPIO\_ABS}$	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$ , and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to pins HPI_INT and GPIO_1
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, $VBUS\_IN\_DIS$ , HPI_SDA and HPI_SCL pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for D+, D-, CC1, CC2, $VBUS\_IN\_DIS$ , HPI_SDA and HPI_SCL pins

**Note**

2. As per USB PD specification, maximum allowed  $VBUS = 21.5$  V.

## Electrical specifications

### 5.2 Device-level specifications

All specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$  and  $T_J \leq 120^{\circ}\text{C}$ , except where noted.

**Table 6 DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#2	$V_{\text{DDD}}$	Power supply input voltage	2.7	–	5.5	V	Sink mode, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID.PWR#3	$V_{\text{BUS\_IN}}$	Power supply input voltage	3.0	–	24.5	V	$-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID.PWR#5	$V_{\text{CCD}}$	Output voltage for core Logic	–	1.8	–	V	–
SID.PWR#13	$C_{\text{exc}}$	Power supply decoupling capacitor for $V_{\text{DDD}}$	0.8	1	–	$\mu\text{F}$	X5R ceramic or better
SID.PWR#14	$C_{\text{exv}}$	Power supply decoupling capacitor for $V_{\text{BUS\_IN\_DIS}}$	–	0.1	–	$\mu\text{F}$	X5R ceramic or better
<b>Active mode. Typical values measured at <math>V_{\text{DDD}} = 5.0\text{ V}</math> or <math>V_{\text{BUS}} = 5.0\text{ V}</math> and <math>T_A = 25^{\circ}\text{C}</math>.</b>							
SID.PWR#8	$I_{\text{DD\_A}}$	Supply current from $V_{\text{BUS}}$ or $V_{\text{DDD}}$	–	10	–	mA	$V_{\text{DDD}} = 5\text{ V}$ OR $V_{\text{BUS}} = 5\text{ V}$ , $T_A = 25^{\circ}\text{C}$ . CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz.
<b>Sleep mode. Typical values measured at <math>V_{\text{DD}} = 3.3\text{ V}</math> and <math>T_A = 25^{\circ}\text{C}</math>.</b>							
SID25A	$I_{\text{DD\_S}}$	CC, I <sup>2</sup> C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	$V_{\text{DDD}} = 3.3\text{ V}$ , $T_A = 25^{\circ}\text{C}$ , All blocks except CPU are on, CC IO on, EA/ADC/CSA/UVOV on.
<b>Deep Sleep mode. Typical values measured at <math>T_A = 25^{\circ}\text{C}</math>.</b>							
SID_PB_DS_A_SNK	$I_{\text{DD\_PB\_DS\_A\_SNK}}$	$V_{\text{BUS}}$ 4.0 to 24.5 V. CC, I <sup>2</sup> C, WDT Wakeup on	–	500	–	$\mu\text{A}$	For sink applications, $V_{\text{BUS}} = 24.5\text{ V}$ , $T_A = 25^{\circ}\text{C}$ , Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV on.

**Table 7 AC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#17	$T_{\text{SLEEP}}$	Wakeup from Sleep mode	–	0	–	$\mu\text{s}$	–
SID.PWR#18	$T_{\text{DEEPSLEEP}}$	Wakeup from Deep Sleep mode	–	–	35	$\mu\text{s}$	–
SYS.FES#1	$T_{\text{PWR\_RDY}}$	Power-up to “Ready to accept I <sup>2</sup> C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{\text{POR\_HIZ\_T}}$	Power-on I/O initialization time	–	3	–	ms	–

## Electrical specifications

### 5.2.1 I/O

**Table 8 I/O DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#37	$V_{IH\_CMOS}$	Input voltage HIGH threshold	$0.7 \times V_{DD}$	–	–	V	CMOS input
SID.GIO#38	$V_{IL\_CMOS}$	Input voltage LOW threshold	–	–	$0.3 \times V_{DD}$	V	CMOS input
SID.GIO#33	$V_{OH\_3V}$	Output voltage HIGH level	$V_{DD} - 0.6$	–	–	V	$I_{OH} = 4 \text{ mA}$ at $3\text{-}V_{DD}$
SID.GIO#36	$V_{OL\_3V}$	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 10 \text{ mA}$ at $3\text{-}V_{DD}$
SID.GIO#16	$I_{IL}$	Input leakage current (absolute value)	–	–	2	nA	$+25^{\circ}\text{C } T_A$ , $3\text{-}V_{DD}$
SID.GIO#17	$C_{PIN\_A}$	Max pin capacitance	–	–	22	pF	Capacitance on D+, D– pins. Guaranteed by characterization.
SID.GIO#17A	$C_{PIN}$	Max pin capacitance	–	3	7	pF	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C } T_A$ , All $V_{DD}$ , all other I/Os. Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	mV	$V_{DD} < 4.5 \text{ V}$ . Guaranteed by characterization.
SID69	$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	–	–	100	$\mu\text{A}$	Guaranteed by design.
SID.GIO#45	$I_{TOT\_GPIO}$	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
OVT							
SID.GIO#46	$I_{IHS}$	Input current when Pad $> V_{DD}$ for OVT inputs	–	–	10.00	$\mu\text{A}$	Per $I^2C$ specification

**Table 9 I/O AC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	$3.3\text{-}V_{DD}$ , $C_{load} = 25 \text{ pF}$
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	–	12	ns	$3.3\text{-}V_{DD}$ , $C_{load} = 25 \text{ pF}$



## Electrical specifications

**Table 10 HPI pins DC specifications (applicable to pins HPI\_SDA and HPI\_SCL only)**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	-140	-	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	1	-	25	kΩ	+25°C T <sub>A</sub> , 1.4 V to GPIO_20VT_Voh (min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value	2.5	-	20	kΩ	+25°C T <sub>A</sub> , 1.4-V to V <sub>DD</sub>
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	-	-	2	nA	+25°C T <sub>A</sub> , 3-V V <sub>DD</sub>
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	-	25	pF	-40°C to +85°C T <sub>A</sub> , All V <sub>DD</sub> , F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT output Voltage low level	-	-	0.4	V	I <sub>OL</sub> = 2 mA
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	-	-	100	μA	-

**Table 11 HPI pins AC specifications (applicable to pins HPI\_SDA and HPI\_SCL only)**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT#70	GPIO_20VT_TriseF	GPIO_20VT rise time in fast strong mode	1	-	45	ns	All V <sub>DD</sub> , C <sub>load</sub> = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_TfallF	GPIO_20VT fall time in fast strong mode	2	-	15	ns	All V <sub>DD</sub> , C <sub>load</sub> = 25 pF

### 5.3 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the timer mode.

#### 5.3.1 I<sup>2</sup>C

**Table 12 Fixed I<sup>2</sup>C DC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	100	μA	–
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	135	μA	–
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	–	1.4	–	μA	–

**Table 13 Fixed I<sup>2</sup>C AC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F <sub>I2C1</sub>	Bit rate	–	–	400	kbps	–

### 5.4 System resources

#### 5.4.1 Power-on reset (POR) with brown-out SWD interface

**Table 14 Imprecise POR (PRES)**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	V <sub>RISEIPOR</sub>	POR rising trip voltage	0.80	–	1.50	V	–
SID186	V <sub>FALLIPOR</sub>	POR falling trip voltage	0.70	–	1.4	V	–

**Table 15 Precise POR**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	V <sub>FALLPPOR</sub>	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

**Table 16 USB PD DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) dead battery CC termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 1.32 V applied at CC1 or CC2
SID.PD.6	Vgndoffset	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter

### 5.4.2 Gate driver specifications

**Table 17 Gate driver DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	R <sub>PD</sub>	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_CTRL and SAFE_PWR_EN to turn ON external PFET.
SID.GD.2	R <sub>PU</sub>	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_CTRL to turn OFF external PFET.
SID.GD.3	I <sub>PD0</sub>	Pull-down current sink at drive strength of 1	25	–	75	μA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_CTRL and SAFE_PWR_EN to turn ON external PFET.
SID.GD.4	I <sub>PD1</sub>	Pull-down current sink at drive strength of 2	50	–	150	μA	
SID.GD.5	I <sub>PD2</sub>	Pull-down current sink at drive strength of 4	140	–	300	μA	
SID.GD.6	I <sub>PD3</sub>	Pull-down current sink at drive strength of 8	280	–	580	μA	
SID.GD.7	I <sub>PD4</sub>	Pull-down current sink at drive strength of 16	560	–	1200	μA	
SID.GD.8	I <sub>PD5</sub>	Pull-down current sink at drive strength of 32	1120	–	2300	μA	
SID.GD.9	I <sub>leak_p1</sub>	Pin leakage on VBUS_CTRL	–	0.00 3	–	μA	+25°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>
SID.GD.10	I <sub>leak_c1</sub>	Pin leakage on SAFE_PWR_EN	–	0.00 3	–	μA	+25°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>
SID.GD.11	I <sub>leak_p2</sub>	Pin leakage on VBUS_CTRL	–	–	2	μA	+85°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>
SID.GD.12	I <sub>leak_c2</sub>	Pin leakage on SAFE_PWR_EN	–	–	2	μA	+85°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>
SID.GD.13	I <sub>leak_p3</sub>	Pin leakage on VBUS_CTRL	–	–	7	μA	+125°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>
SID.GD.14	I <sub>leak_c3</sub>	Pin leakage on SAFE_PWR_EN	–	–	7	μA	+125°C T <sub>J</sub> , 5-V V <sub>DDD</sub> , 20-V V <sub>BU</sub>

## Electrical specifications

**Table 18 Gate driver AC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.15	$T_{PD1}$	Pull down delay on SAFE_PWR_EN	–	–	2	$\mu\text{s}$	Clload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 k $\Omega$ tied between SAFE_PWR_EN and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on SAFE_PWR_EN	–	–	5	V/ $\mu\text{s}$	80% to 20%, 50 k $\Omega$ tied between SAFE_PWR_EN and VBUS, Clload = 2 nF, Vinitial = 24 V
SID.GD.17	$T_{PD2}$	Pull down delay on VBUS_CTRL	–	–	2	$\mu\text{s}$	Clload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 k $\Omega$ tied between SAFE_PWR_EN and VBUS
SID.GD.18	$T_{PU}$	Pull up delay on VBUS_CTRL	–	–	18	$\mu\text{s}$	Clload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 k $\Omega$ tied between SAFE_PWR_EN and VBUS
SID.GD.19	$SR_{PU}$	Output slew rate on VBUS_CTRL	–	–	5	V/ $\mu\text{s}$	Clload = 2 nF, 20% to 80% of VBUS_CTRL range
SID.GD.20	$SR_{PD}$	Output slew rate on VBUS_CTRL	–	–	5	V/ $\mu\text{s}$	Clload = 2 nF, 80% to 20% of VBUS_CTRL range

**Table 19 VBUS discharge specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V <sub>BUS</sub> value from setting	–	–	10	%	When V <sub>BUS</sub> is discharged to 5 V. Guaranteed by characterization.

## Electrical specifications

**Table 20 Voltage (VBUS) regulation DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	V <sub>IN_3</sub>	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	V <sub>IN_5</sub>	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	V <sub>IN_9</sub>	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	V <sub>IN_15</sub>	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	V <sub>IN_20</sub>	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	V <sub>IN_3_DS</sub>	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	V <sub>IN_5_DS</sub>	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	V <sub>IN_9_DS</sub>	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	V <sub>IN_15_DS</sub>	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	V <sub>IN_20_DS</sub>	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I <sub>KA_OFF</sub>	Off-state cathode current	–	–	10	μA	–
SID.DC.VR.12	I <sub>KA_ON</sub>	Current through cathode pin	–	–	10	mA	–

**Table 21 VBUS short protection specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VSP.1	V <sub>SHORT_TRIGGER</sub>	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by characterization.

**Table 22 VBUS DC regulator specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.2	VBUS_DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

**Table 23 VBUS AC regulator specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.3	T <sub>start</sub>	Total startup time for the regulator supply outputs	–	–	200	μs	Guaranteed by characterization

### 5.4.3 Analog to digital converter (used for determining VBUS\_MIN, VBUS\_MAX, ISNK\_COARSE, ISNK\_FINE values)

**Table 24 ADC DC specifications**

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V <sub>REF_ADC2</sub>	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

**Table 25 ADC AC specifications**

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

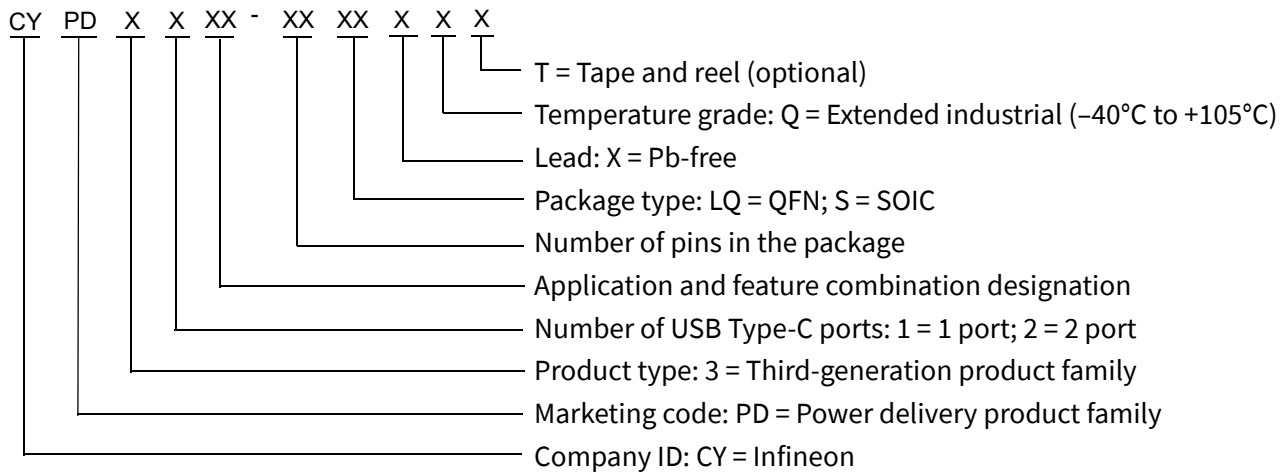
## 6 Ordering information

**Table 26** lists the EZ-PD™ BCR-LITE part numbers and features.

**Table 26 EZ-PD™ BCR-LITE ordering information**

MPN	Application	Termination resistor	Role	Package type	Si ID
CYPD3178-24LQXQ	Barrel connector replacement or generic UFP sink	$R_D$ , $R_{D-DB}$	UFP	24-Pin QFN	20A2

### 6.1 Ordering code definitions





## 7 Packaging

**Table 27** Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T <sub>A</sub>	Operating ambient temperature	Extended industrial	−40	25	105	°C
T <sub>J</sub>	Operating junction temperature	Extended industrial	−40	25	120	°C
T <sub>JA</sub>	Package $\theta_{JA}$ (24-pin QFN)	–	–	–	19.98	°C/W
T <sub>JC</sub>	Package $\theta_{JC}$ (24-pin QFN)	–	–	–	4.78	°C/W

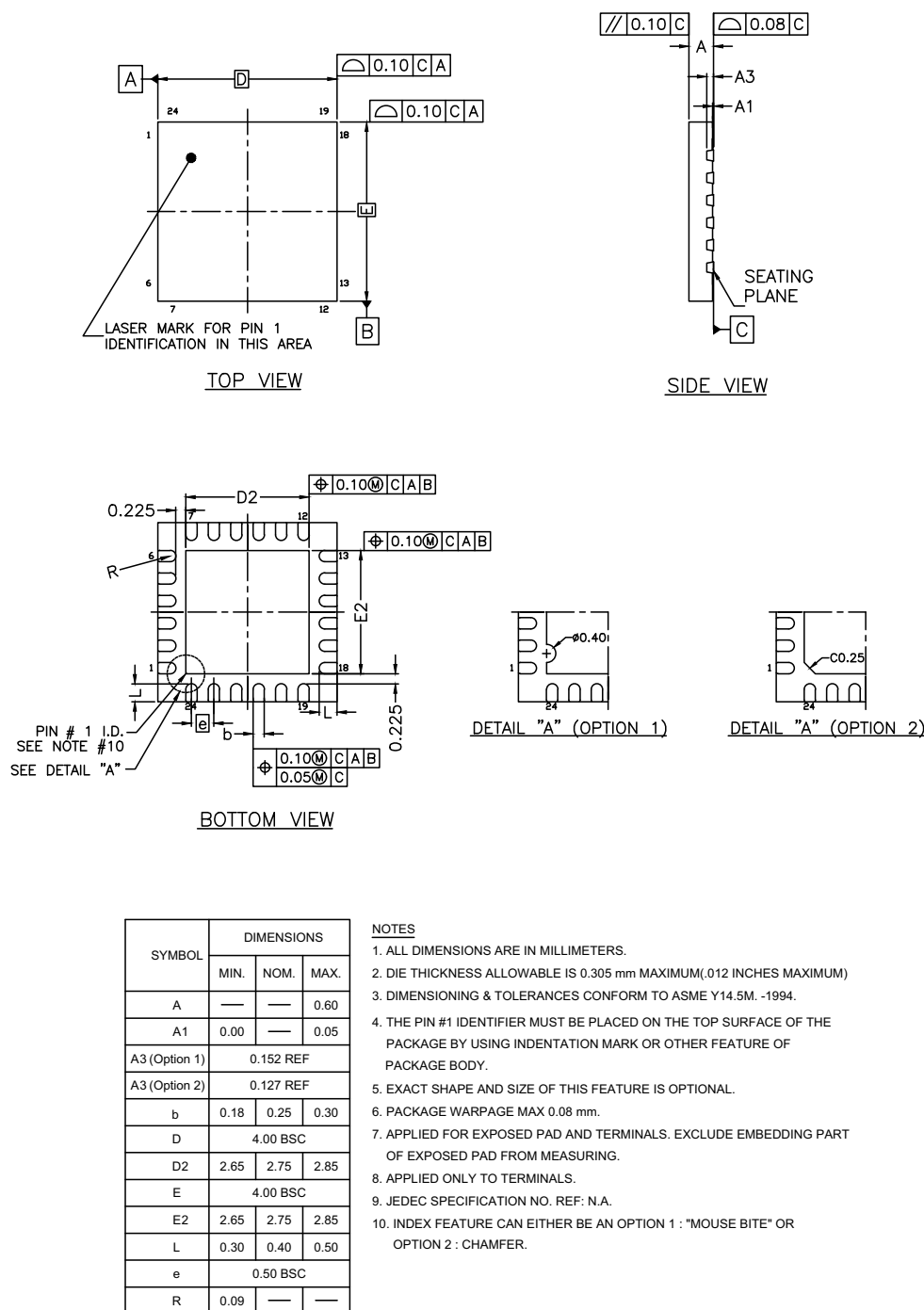
**Table 28** Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
24-pin QFN	260°C	30 seconds

**Table 29** Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3

## Packaging



002-16934 \*E

**Figure 5** 24-pin QFN ((4.0 × 4.0 × 0.6 mm), 2.75 × 2.75 mm E-Pad (Sawn)) package outline, 002-16934

## 8 Acronyms

**Table 30** Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
BCR	barrel connector replacement
BOD	brown-out detect
BMC	Biphase Mark Code
CC	configuration channel
CPU	central processing unit
CS	current sense
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
ESD	electrostatic discharge
GPIO	general-purpose input/output
HPI	host processor interface
IC	integrated circuit
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
I/O	input/output, see also GPIO
LDO	low-dropout regulator
MCU	microcontroller unit
NC	no connect
OCP	overcurrent protection
OTP	over-temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant
PD	power delivery
PHY	physical layer
POR	power-on reset
PMOS	P-channel MOSFET (metal oxide semiconductor field effect transistor)
PPS	programmable power supply
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RISC	reduced-instruction-set computing
RX	receive
SCB	serial communication block
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
SDK	software development kit

## Acronyms

**Table 30**      **Acronyms used in this document** *(continued)*

Acronym	Description
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UFP	upstream facing port
USB	Universal Serial Bus

## 9 Document conventions

### 9.1 Units of measure

**Table 31** Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	mega samples per second
μA	microampere
μF	microfarad
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document version	Date of release	Description of changes
**	2021-09-24	Initial release.
*A	2022-05-20	Changed status from Preliminary to Final. Updated <b>Packaging</b> : spec 002-16934 – Changed revision from *C to *E.
*B	2022-06-24	Removed “Restricted” status.

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