OBSOLETE - PART DISCONTINUED

Features

- Real time AEQ 4-channel Video/Audio decoder for WD1(960H) and D1 cameras
- Built-in Adaptive Equalizer(AEQ) for the best picture image in the several hundred meter coax cable condition
- Proprietary Pericom AEQ technology recover weak, noisy, or unstable analog input signals
- Resilient SYNC TIP detection to lock video signal in a noisy environment
- Programmable sharpness, CTI, hue, saturation, contrast and brightness
- Support time multiplexed format of ITU-R BT.656 output with 54/108MHz or72/144MHz
- Provides a programmable mapping from four or eight (non-real-time) analog video inputs to four BT.656 digital outputs
- NTSC(M), NTSC 4.43, PAL (B, D, G, H, I, M, Nc, 60) standard support
- High performance 5H comb filter for all NTSC/PAL standards
- Built-in 10-bit audio Codec to allow 5analog audio inputs and 1 audio output
- Mixed audio analog output for multiple audio channels
- Two serial audio formats (I2S and DSP) are supported for recording/mixing output and playback input
- Selectable Master and Slave serial audio interface
- Multiple audio sample rates for 8, 16, 32, 44.1, 48KHz audio frequency
- Integrated video PLL for 108MHz,144MHz clock output
- Two-wire serial interface(I^2C) for register access
- Provide system interrupt request for video
- Packages: 128-pin LQFP

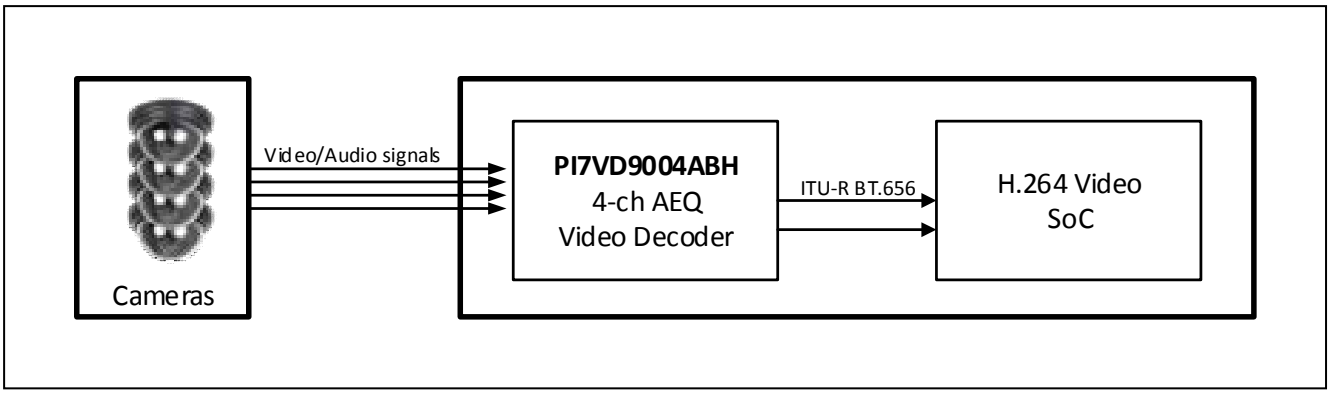
Description

PI7VD9004ABH is AEQ 4-Channel Video Decoders and Audio Codec. Built-in Adaptive equalizer (AEQ)recover the noisy signals caused by long or small wire gauge Coax cables and display the best picture image view quality. The video decoder converts NTSC, PAL analog composite video broadcasting signal (CVBS) into digital components YCbCr for video controller or processor to perform pre-view, compression and storage etc. The converted digital video streams complying with ITU-R BT.656 are transported in time multiplexed format, which contains one, two or four video channels.

Single 27MHz reference crystal clock support NTSC, PAL and 960H standard resolution. Each video channel contains 10-bit ADC, proprietary clamp, automatic gain controller and 5H comb filter for separating luminance & chrominance to reduce artificial noise.

Application

- Video Security DVRs, PC-DVR, Video Capture cards
- Automotive Camera Driver Assistant Systems
- Video Broadcasting Equipment



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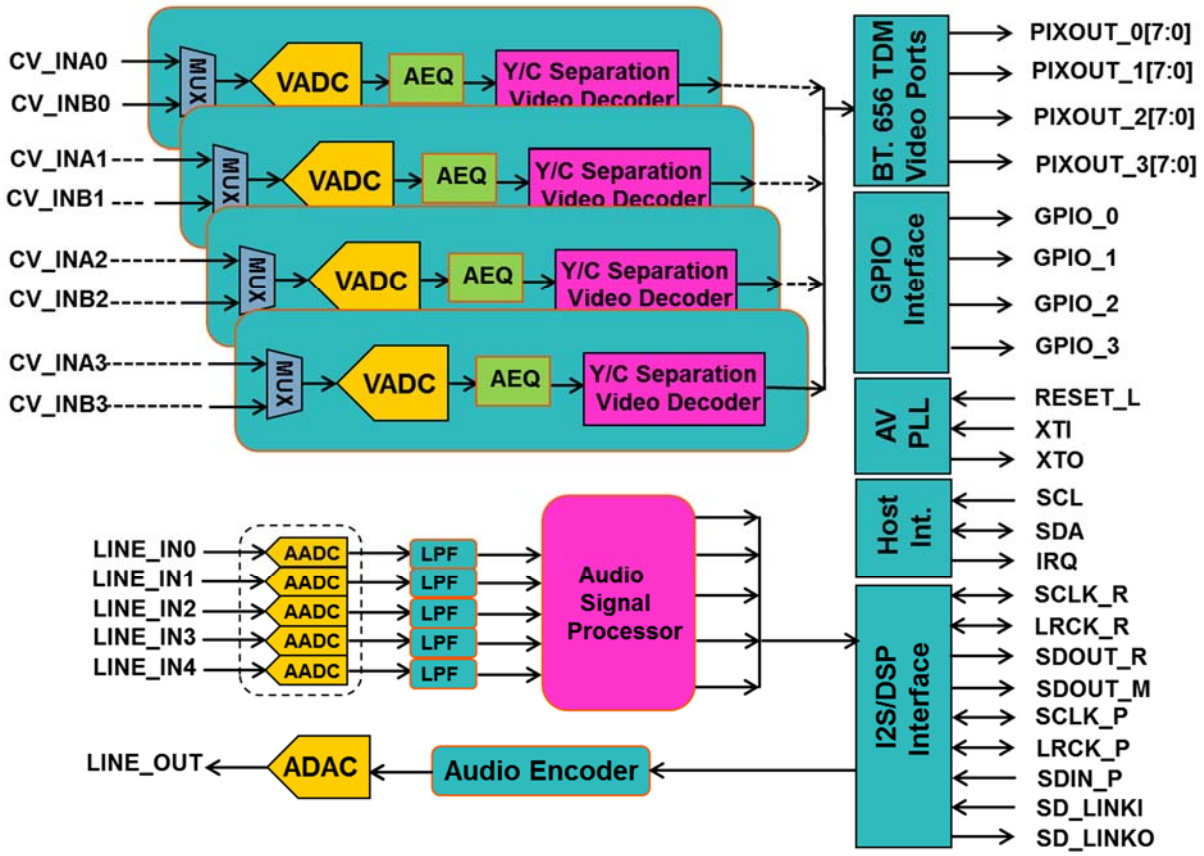
1 PI7VD9004ABH Block Diagram



Video input sources:	CV_INA0, CV_INB0, CV_INA1, CV_INB1, CV_INA2, CV_INB2, CV_INA3 and CV_INB3
BT.656 TDM ports:	PIXOUT_0, PIXOUT_1, PIXOUT_2 and PIXOUT_3
Audio input sources:	LINE_IN0, LINE_IN1, LINE_IN2, LINE_IN3, and LINE_IN4
I2S/DSP Audio Interface	(SCLK_R, LRCK_R, SDOUT_R and SDOUT_M), (SCLK_P, LRCK_P and SDIN_P), (SD_LINKI, SD_LINKO)

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2 Pin Configuration(128-LQFP)

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Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	33	PIXOUT_2[4]	65	PIXOUT_0[5]	97	ADAC_VDD
2	VSS	34	VSS	66	PIXOUT_0[4]	98	ADAC_VDD
3	VSS	35	VDDC	67	VSS	99	LINE_OUT
4	VDDC	36	PIXOUT_2[3]	68	PIXOUT_0[3]	100	VSS
5	TM1	37	PIXOUT_2[2]	69	PIXOUT_0[2]	101	VSS
6	SA0	38	PIXOUT_2[1]	70	PIXOUT_0[1]	102	VCM
7	SA1	39	PIXOUT_2[0]	71	PIXOUT_0[0]	103	LINE_IN0
8	VSS	40	VSS	72	VD33	104	LINE_IN1
9	VDDC	41	VD33	73	SCLK_R	105	LINE_IN2
10	RESET_L	42	PIXCLK_PO	74	LRCK_R	106	LINE_IN3
11	SCL	43	PIXCLK_NO	75	SDOUT_R	107	LINE_IN4
12	SDA	44	VSS	76	SDOUT_M	108	ADC_VDD
13	VSS	45	VDDC	77	VSS	109	ADC_VDD
14	SD_LINKI	46	XIN	78	SCLK_P	110	CV_INA0
15	VD33	47	XOUT	79	LRCK_P	111	CV_INB0
16	PIXOUT_3[7]	48	VSS	80	SDIN_P	112	VSS
17	PIXOUT_3[6]	49	VD33	81	SD_LINKO	113	CV_INA1
18	PIXOUT_3[5]	50	PIXOUT_1[7]	82	VD33	114	CV_INB1
19	PIXOUT_3[4]	51	PIXOUT_1[6]	83	GPIO_0	115	ADC_VDD
20	VSS	52	PIXOUT_1[5]	84	GPIO_1	116	CV_INA2
21	VDDC	53	PIXOUT_1[4]	85	GPIO_2	117	CV_INB2
22	PIXOUT_3[3]	54	VSS	86	GPIO_3	118	VSS
23	PIXOUT_3[2]	55	VDDC	87	VDDC	119	CV_INA3
24	PIXOUT_3[1]	56	PIXOUT_1[3]	88	INT	120	CV_INB3
25	PIXOUT_3[0]	57	PIXOUT_1[2]	89	VSS	121	ADC_VDD
26	VSS	58	PIXOUT_1[1]	90	VSS	122	ADC_VDD
27	VDDC	59	PIXOUT_1[0]	91	NC	123	VSS
28	VSS	60	VD33	92	NC	124	ADC_VDD
29	VD33	61	VSS	93	NC	125	VSS
30	PIXOUT_2[7]	62	VDDC	94	NC	126	ADC_VDD
31	PIXOUT_2[6]	63	PIXOUT_0[7]	95	NC	127	VDDPLL
32	PIXOUT_2[5]	64	PIXOUT_0[6]	96	NC	128	VDDPLL

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3 Pin-out Information

Analog Video/Audio Interface

Pin Name	Pin Number	Type	Description
CV_INA0, CV_INB0, CV_INA1, CV_INB1, CV_INA2, CV_INB2, CV_INA3, CV_INB3	110, 111, 113, 114, 116, 117, 119, 120	Analog	CVBS input A of Video channel 0 CVBS input B of Video channel 0 CVBS input A of Video channel 1 CVBS input B of Video channel 1 CVBS input A of Video channel 2 CVBS input B of Video channel 2 CVBS input A of Video channel 3 CVBS input B of Video channel 3
VCM	102	Analog	Connect to an external capacitor
LINE_IN0, LINE_IN1, LINE_IN2, LINE_IN3, LINE_IN4	103, 104, 105, 106, 107	Analog	Line input of Audio channel 0 Line input of Audio channel 1 Line input of Audio channel 2 Line input of Audio channel 3 Line input of Audio channel 4
LINE_OUT	99	Analog	Mixed Analog Audio Output

Digital Video/Audio Interface

Pin Name	Pin Number	Type	Description
PIXOUT_0[7:0]	63, 64, 65, 66,68,69, 70,71	Output	Bt.656 Time Multiplex Division output of port 0
PIXOUT_1[7:0]	50, 51, 52, 53, 56,57,58,59	Output	Bt.656 Time Multiplex Division output of port 1
PIXOUT_2[7:0]	30, 31, 32, 33, 36, 37, 38, 39	Output	Bt.656 Time Multiplex Division output of port 2
PIXOUT_3[7:0]	16, 17, 18, 19, 22, 23, 24, 25	Output	Bt.656 Time Multiplex Division output of port 3
GPIO_0	83	Output	According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 0
GPIO_1	84	Output	According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 1
GPIO_2	85	Output	According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 2
GPIO_3	86	Output	According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 3
SCLK_R	73	Input/ Output	Record audio serial clock. It is an input pin under slave mode, while output pin under master mode.
LRCK_R	74	Input/ Output	Record audio serial sync pulse. It is an input pin under slave mode, while output pin under master mode.
SDOUT_R	75	Output	Record audio serial data output.
SDOUT_M	76	Output	Mixing audio serial data output.
SCLK_P	78	Input/ Output	Playback audio serial clock. It is an input pin under slave mode, while output pin under master mode

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LRCK_P	79	Input/ Output	Playback audio serial sync pulse. It is an input pin under slave mode, while output pin under master mode.
SDIN_P	80	Input	Playback audio serial data input.
SD_LINKI	14	Input	Chip-to-Chip audio serial data input.
SD_LINKO	81	Output	Chip-to-Chip audio serial data output.

System Control Interface

Pin Name	Pin Number	Type	Description
RESET_L	10	Input	Chip Reset. Active Low.
XIN	46	Input	27MHz or 54MHz crystal input or 27MHz/54MHz/108MHz oscillator input
XOUT	47	Output	27MHz or 54MHz crystal output
PIXCLK_P0	42	Output	Positive Output clock signal running at 27/54/108MHz (720H mode) or 36/72/144MHz (960H mode) for bus PIXOUT_0.
PIXCLK_N0	43	Output	Negative Output clock signal running at 27/54/108MHz (720H mode) or 36/72/144MHz (960H mode) for bus PIXOUT_0
TM1	5	Input	Test pin. Tied to VSS.
SA1	7	Input	Device Address 1 of I2C slave interface
SA0	6	Input	Device Address 0 of I2C slave interface
SCL	11	Input	Input clock signal of I2C slave interface
SDA	12	Input/ Output	Data signal of I2C slave interface
INT	88	Output	Interrupt signal to system. Active High.

Power and Ground

Pin Name	Pin Number	Type	Description
VDDC	4, 9, 21, 27, 35, 45, 55, 62, 87	Power	1.0V Power for core logic
VD33	15, 29, 41, 49, 60, 72, 82	Power	3.3V Power for IO pads
VSS	1, 2, 3, 13, 20, 26, 28, 34, 40, 44, 48, 54, 61, 67, 77, 89, 90, 100, 101, 112, 118, 123, 125	Ground	Ground for video ADC, audio ADC, audio DAC, PLL, core logic and IO pads
ADC_VDD	108, 109, 115, 121, 122, 124, 126	Power	3.3V Power for video ADC and audio ADC.
ADAC_VDD	97, 98	Power	3.3V Power for audio DAC
VDDPLL	127, 128	Power	3.3V Power for AV PLL

No Connection Pins

Pin Name	Pin	Type	Description
NC	91, 92, 93, 94, 95, 96	N/A	Not Connected Pin. Please let these pins floating.

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4 Functional Description

4.1 Video/Audio Analog Input

PI7VD9004ABH offers4 channels NTSC, PAL (720H or 960H) format composite (CVBS) inputs(CV_INAx and CV_INBx, x= 0,1,2,3). When the input signal is weak and the color burst is not able to be recognized, the video is automatically switched to Black and White mode to enhance the picture image quality.

Format	Lines	Field	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan	525	60	3.579545 MHz	Japan *
NTSC (4.43)	525	60	4.433619 MHz	Transcoding
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-I /H /D	625	50	4.433619 MHz	Belgium ,China Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
PAL-60	525	60	4.433619 MHz	China

* NTSC-Japan has 0 IRE setup

4.2 Clamping and Automatic Gain Control

Each analog input channel has built-in clamping circuits to restore signal DC level. Automatic Gain Control (AGC) circuits in the internal video processor can compensate average input video signal level for each analog input channel. The AGC and clamping circuits prevent signal level saturation and allow the video decoder to deliver the best signal-to-noise performance. On the other hand, the AGC cooperates with the digital multiplier of video decoder to boost the weak signals. The circuits perform Automatic Gain Control through internal feedback look. Manual gain control is also available through configuring the Video Decoder Control and Status Registers

4.3 Video Decoder

The video decoder in the chip converts NTSC and PAL video signals to 8-bit ITU-R BT.656 format. The chip includes four high speed and low power 10-bit analog-to-digital converters (ADC) with 2x sampling rate to support 4-channel video decoding. When the incoming video is in the 720H format, the sampling rate is 27MHz or 54MHz by 2x factor. For 960H format, the sampling rate is 36MHz or 72MHz by 2x factor. The chip implements proprietary circuit design that is optimized for locking in weak, noisy, or unstable signals. The minimal signal voltage that can be locked in is at 160/80 mV

4.4 Adaptive Equalization

The CVBS is suffered from channel loss by an extended transmission distance (greater than 500m) and a small diameter (less than 0.5mm) of CCTV cable. The distortion on CVBS after the energy reduction effect of cable length is illustrated as below. For example, a Multi-Burst test signal is respectively measured at 0.5m and 500m of cable.It appears that color burst and sync tip have sever degration after 500m transmission distance. Adaptive equalization on the distorted CVBS recovers the signal back to close to the original level. Since the different cable conditions present various effects on CVBS picture image, the adaptive equalization provides to compensate the signal loss on some frequency components pertinent to the Coax cable.

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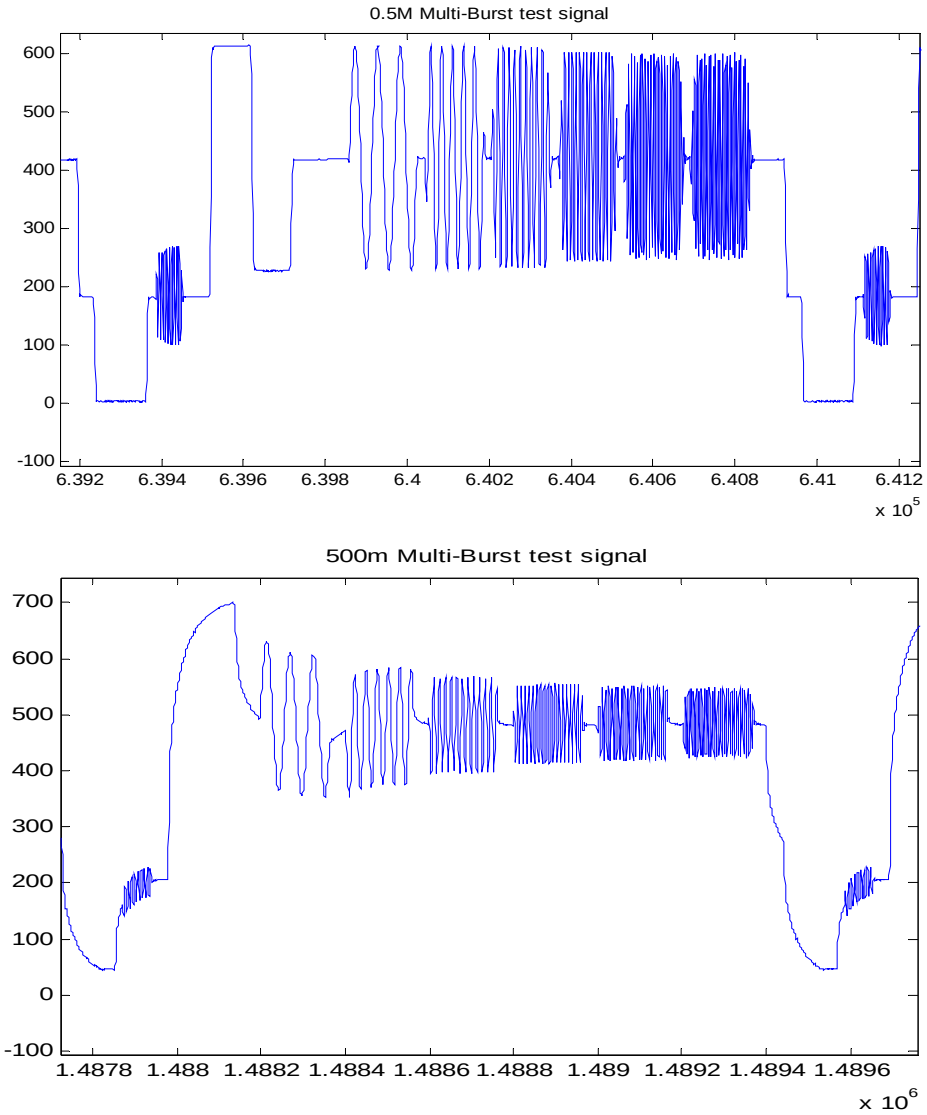

4.5 Comb filter and Y/C Separation

Thevideo decoder is capable of separating luma (Y) and chroma (C) of NTSC or PAL video signals using 5-line adaptive comb filter or notch/band-pass filter. The comb filter searches for correlation between 5 lines of input video stored in the internal buffer. The lines are averaged based on the degree of correlation to produce the output video line. If no correlation is found between the 5 lines of video, notch/band-pass filter is used. This process is very effective at reducing cross-luma and cross-chroma noise. The noise appears as artifacts that degrade the image quality. Reduction of the noise improves the image quality significantly.

4.6 Video Signal Processing

The chip is capable of processing digital video signal to fulfill better detection in a noisy environment and achieve good image quality for viewing as well. For video signal detection, a resilient SYNC TIP detection mechanism is implemented to locate VSYNC and HSYNC correctly in order to lock the video frame or video line.

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In general, the poor power adaptor or camera would introduce high frequency ripples coupling with sync tip to cause the misjudgment on the beginning of a video frame or line. The built-in video processing circuit is able to decouple the noise from sync tip to prevent from video loss.
A sharpness filter is implemented to offer programmable 16 level gains to increase the high frequency and edge information of luma for better viewing on the contour of each object. Through the I2C serial interface, hue, contrast, brightness and saturation can be programmed in the configuration registers. Hue can be controlled in 256 steps from -180 degrees to +180 degrees. Saturation can be programmed in 256 grades. Brightness can be adjusted in 256 levels.

4.7 Video Output Port

The four CVBS analog video channels are converted into four individual digital video data streams. There are four video output ports (PIXOUT_0, PIXOUT_1, PIXOUT_2 and PIXOUT_3) in the chip and each video output port can carry several converted digital video data stream following ITU-R BT.656 compatible data format. The video data of each port is synchronous with the corresponding clock signals of PIXCLK_PO or PIXCLK_NO. The frequency of PIXCLK_*O can be operated at 1x, 2x or 4x of 27MHz (720H mode) or 36MHz (960H mode). When the clock frequency is 2x or 4x rate, the video port outputs 2-channel or 4-channel video data stream in time-multiplexed format. The clock phase of PIXCLK_POor PIXCLK_NOcan be programmed by delay cells through writing delay value into the registers of PIXCLK_P_DEL or PIXCLK_N_DEL. Also, the clock polarity can be controlled through inverter by setting or resetting the register of PIXCLK_P_POL or PIXCLK_N_POL. The flexibility on changing clock phase or polarity facilitates the timing design for video data stream on PCB.

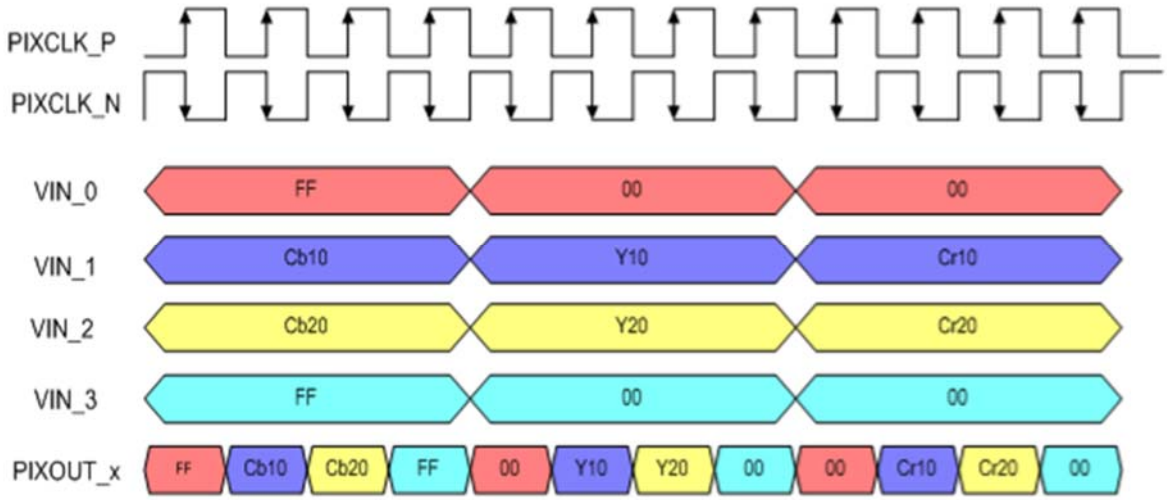

Figure 4-1Time-multiplexed format with 108/144MHz

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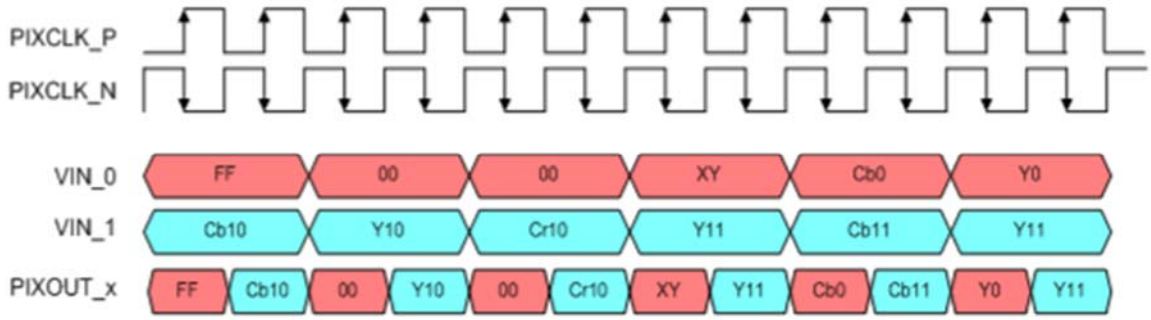

Figure 4-2Time-multiplexed format with 54/72MHz

4.8 ANALOG AUDIO INPUT

The audio ADC offers 5 channels of analog inputs (LINE_INx, x= 0, 1, 2, 3, 4) with a peak-to-peak voltage range from 0.5V to 2V. Each input channel contains 4-bit programmable gain amplifier and an ADC with maximum over-sampling speed of 3.6M Sample/s. A pseudo differential input is used to minimize board level noise problems. The converted audio data stream is fed into a low pass filter to decimate audio sample at an appropriate audio sampling rate such as 8 KHz, 16 KHz, 32 KHz, 44.1 KHz and 48 KHz etc.

4.9 AUDIO PROCESSING

The audio processor accepts 5 digital audio streams from audio ADC. It also receives 2 additional digital serial audio data from pins. One digital serial audio data is SDIN_P coming from AV compression processor, while the other one is SD_LINKI coming from companion device.

SDIN_P represents the decompressed audio data for playback purpose. SD_LINKI is used to cascade with as many as 12 or 15 digital audio outputs from three other PI7VD9004ABH chips for forming one timing multiplexed I2S digital serial audio data containing 16 or 20 digital audio channels. This device processes these 5 digital audio streams and 2 digital serial audio data, then generates one mixing analog audio signal and three digital serial audio data to fulfill the functions of mixing, recording and cascading etc.

For audio mixing, this device has both analog and digital format. The built-in mixer selects among all audio input data to generate the mixing digital audio data (SDOUT_M), which connects to audio DAC for converting to mixing analog audio signal output (LINE_OUT).

For audio recording, the audio processor performs multiplexing over 12 or 15 digital audio streams in timing division way to generate record digital audio output data (SDOUT_R). For the digital serial audio data SDOUT_R and SDOUT_M, they are both synchronized with SCLK_R and LRCK_R. As to SDIN_P, it is synchronized with SCLK_P and LRCK_P. These digital serial audio data support two formats of I2S and DSP that can be selected by control bits RM_SYNC in the register at offset 0xD2 and PB_SYNC in the register at offset 0xDB. Meanwhile, the record and playback digital serial audio interfaces of PI7VD9004A(A/B/C)H can be acted as Master or Slave mode based upon the setting of ACLKRMASTER and PB_MASTER bits in the register at offset 0xDB

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This device supports audio system clock with 256fs or 320fs mode, which is controlled by AIN5MD register. The record output pin contains several channel inputs that can be defined by the registers at offset of 0xD2~ 0xDA describing the number and sequence of recorded audio streams. It supports 8bit and 16bit record data width for trading off between higher audio qualities and saving disk storage space. By controlling bit2 of register at offset 0xDB, the chip allows to select the output record data width to be either 8-bit or 16-bit mode.

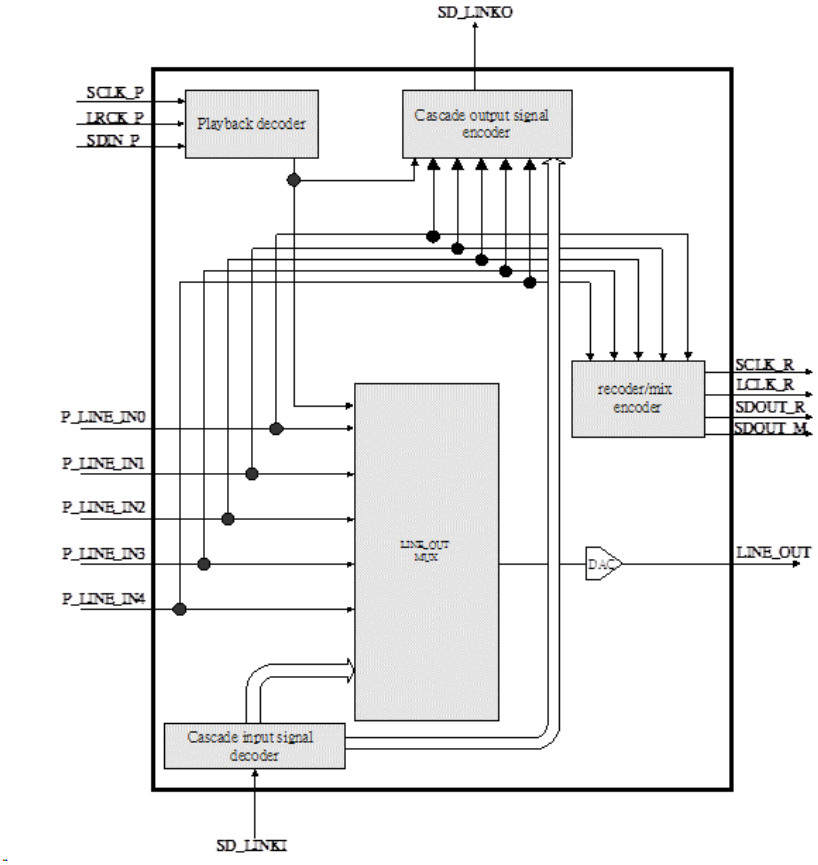

Figure 4-3 Audio Processing Block

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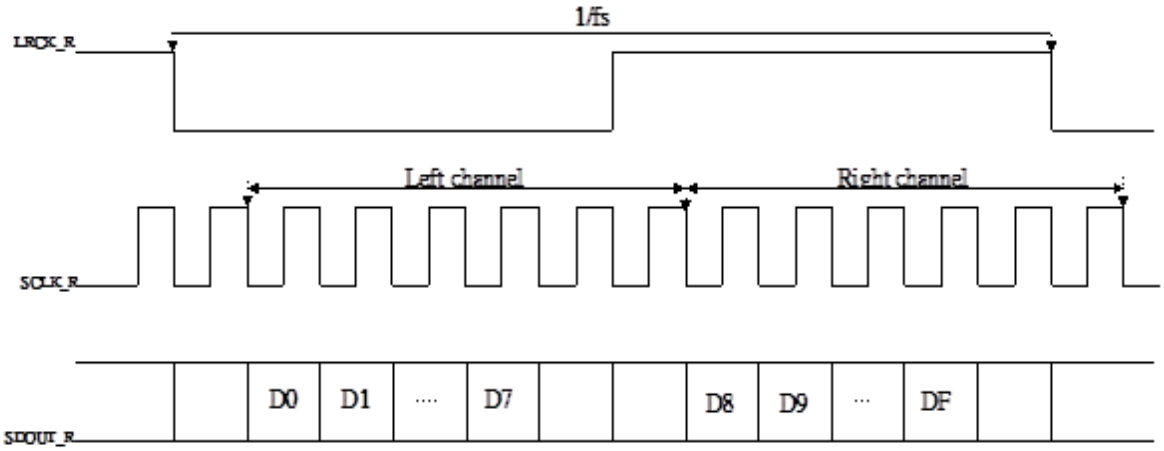
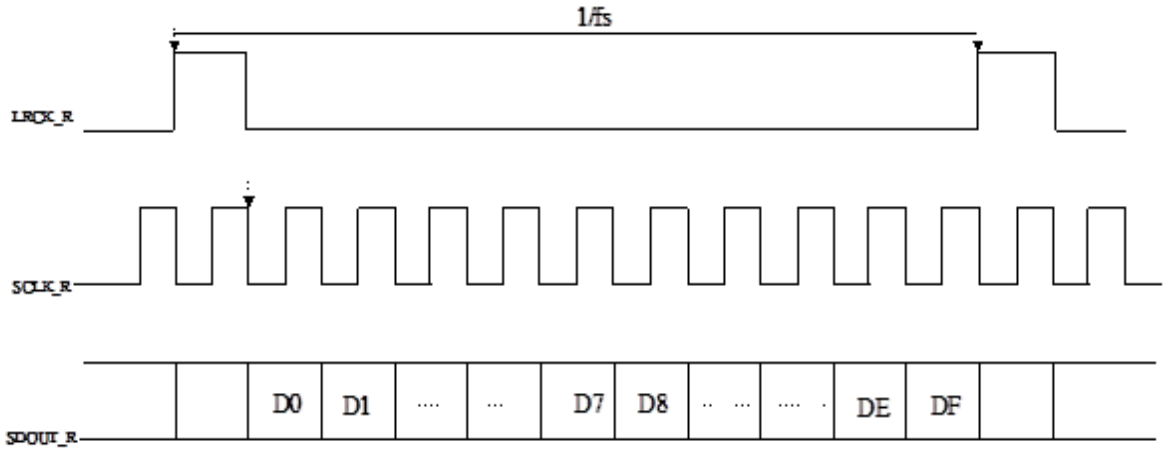


I2S mode



DSP mode

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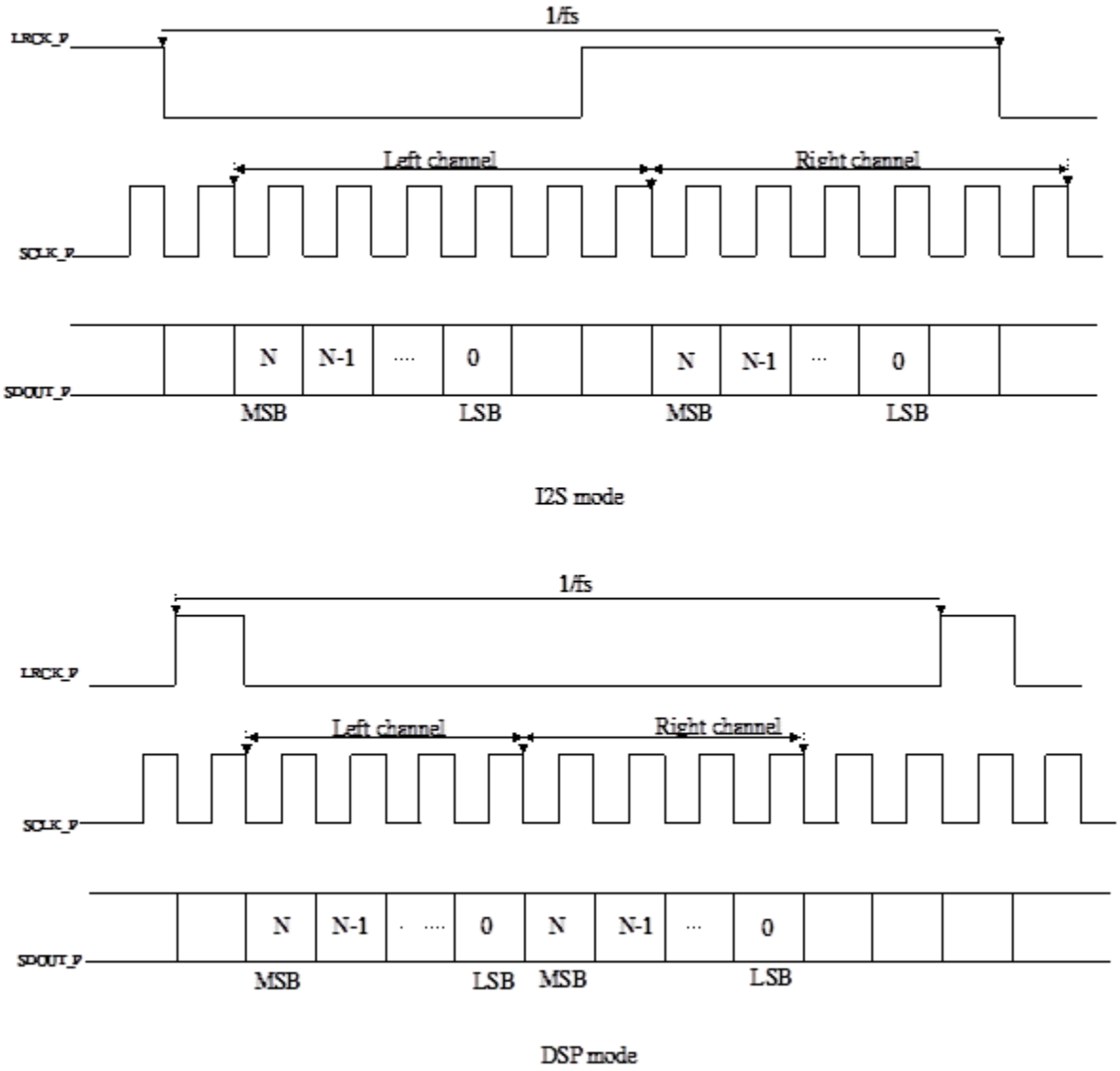

Figure 4-4 Playback input format

4.10 PI7VD9004ABH Cascade Mode

For audio cascading, the chip redirects SDOUT_R as SD_LINKO to connect with SD_LINKI of another PI7VD9004AB product, which cascades its original SDOUT_R and SD_LINKI to create a new SDOUT_R. PI7VD9004AB can support 16 channel data output on first level chip record output pin for saving pin layout on PCB board. The cascade chips have to use same crystal clock source and same reset signal.

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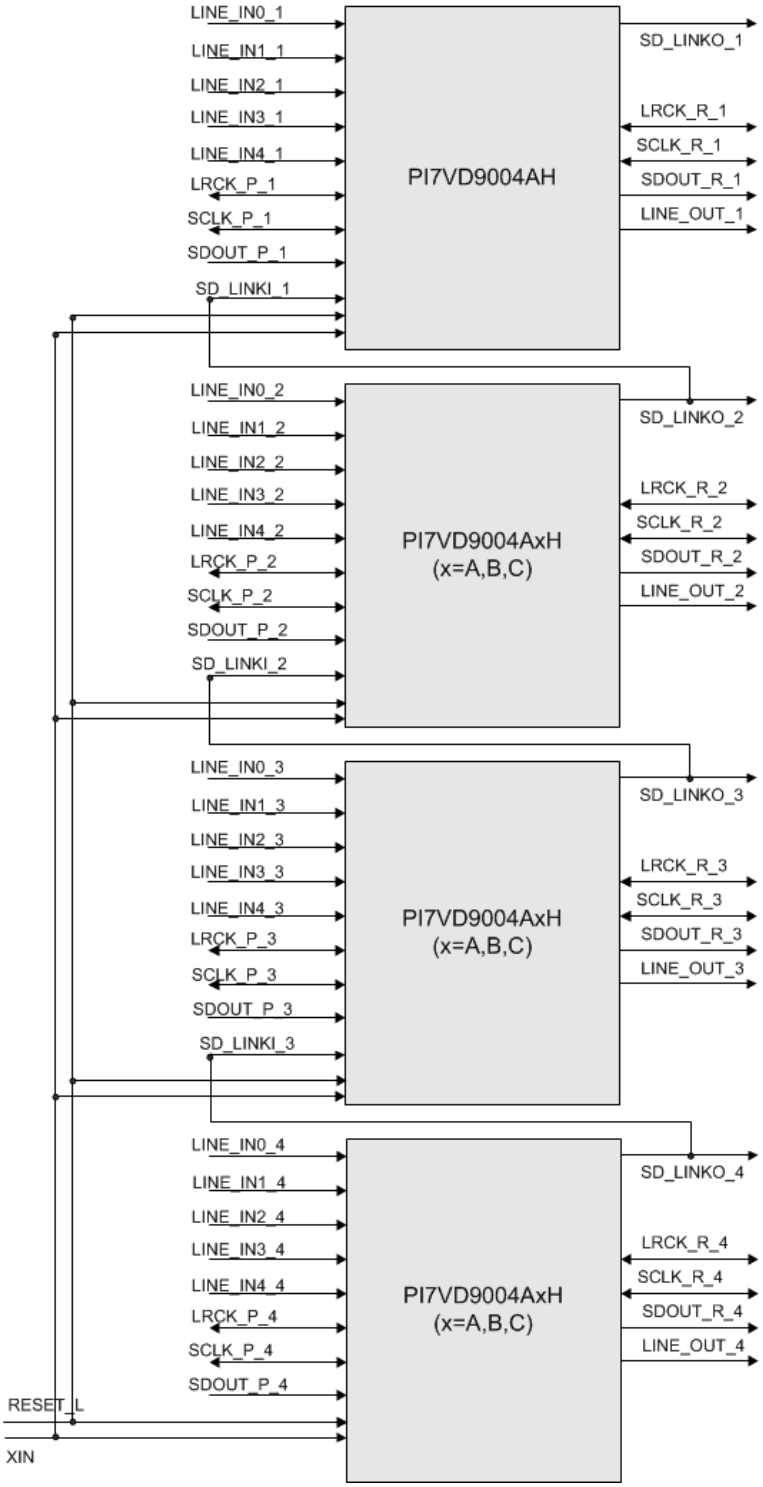

Figure 4-5 Audio Cascading Example

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4.11 I²C Host Interface

The processor can access the internal register by executing read or write command to the indexed locations to implement the function of detecting audio and video signal and reveals the detection status through the configuration registers. If any audio or video channel is present or absent, interrupt pin (INT) can notify the status to the processor to manage CPU resource effectively by polling the status. The chip supports flexibilities to select various detection modes and enable individual audio/video channel for generating interrupt.
These control bits to interrupt pin are defined in the registers of AVDET_MODE, AVDET1_ENA, AVDET2_ENA, A51DET_ENA and A52DET_ENA.

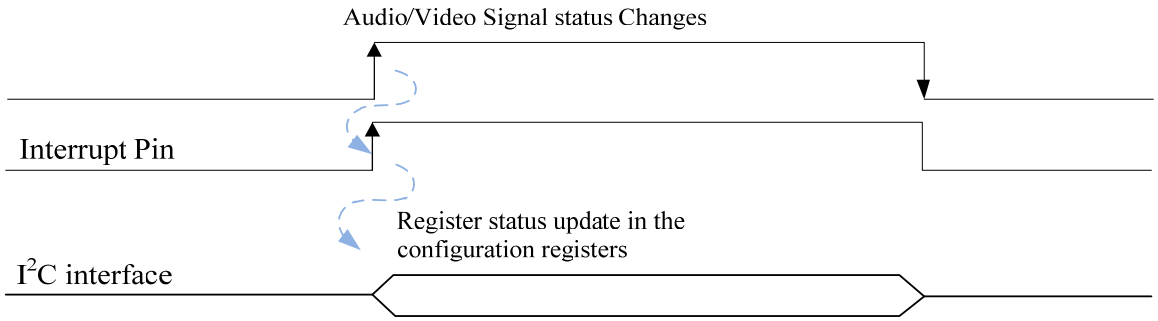

Figure 4-6 Interrupt timing diagram of Audio/Video detection

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5 Configuration, Control, and Status Register Map

Address	Function
00h/10h/20h/30h (00h)	Video Status
01h/11h/21h/31h (00h)	Brightness Control
02h/12h/22h/32h (64h)	Contrast Control
03h/13h/23h/33h (00h)	Sharpness Control
04h/14h/24h/34h (80h)	Chroma (U) Gain
05h/15h/25h/35h (80h)	Chroma (V) Gain
06h/16h/26h/36h (00h)	Hue Control
07h/17h/27h/37h	Reserved
08h/18h/28h/38h	Reserved
09h/19h/29h/39h	Reserved
0Ah/1Ah/2Ah/3Ah	Reserved
0Bh/1Bh/2Bh/3Bh	Reserved
0Ch/1Ch/2Ch/3Ch	Reserved
0Dh/1Dh/2Dh/3Dh	Reserved
0Eh/1Eh/2Eh/3Eh (77h)	Standard Selection
0Fh/1Fh/2Fh/3Fh	Reserved
40h-50h	Reserved
51h (00h)	F-Bit of SAV/EAV Inverted
52h-56h	Reserved
57h/58h/59h/5Ah (90h)	Blanking Length of Horizontal Line
5Bh	Reserved
5Ch (00h)	Video Fast Switch
5Dh-60h	Reserved
61h (03h)	Crystal Clock Select
62h (00h)	36M & GPIO Output Enable
63h (10h)	ID for Video Channel 0 & 1
64h (32h)	ID for Video Channel 2&3
65h (00h)	Clock Output Control
66h-6Fh	Reserved
70h (08h)	Audio Clock Control
71h (00h)	I2S Audio Input Control
72h-7Ah	Reserved
7Bh (00h)	SDOUT_M Select (R)
7Ch (00h)	SDOUT_M Select (L)
7Dh (E4h)	Extended Line Select
7Eh	Reserved
7Fh (08h)	Mix Ratio 4
80h (00h)	Software Reset
81h-84h	Reserved
85h (00h)	Video Source Selection
86h-88h	Reserved
89h (00h)	Audio FS Mode
8Ah-9Eh	Reserved
9Fh (00h)	PIXCLK 0Delay
A0h-B0h	Reserved
B1h (00h)	Channel ID for 8 Video Sources
B2h-C7h	Reserved
C8h (00h)	GPIO_0_1 Mode

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Address	Function
C9h (00h)	GPIO_2_3 Mode
CAh (55h)	Video Output Mode
CBh (00h)	GPIO Polarity
CCh (E4h)	PIXOUT Output CH2 Select
CDh (00h)	PIXOUT Output CH1 Select
CEh	Reserved
CFh (00h)	Serial Mode Control
D0h-D1h	Reserved
D2h (03h)	SDOUT_RM Output
D3h (10h)	SDOUT_R_SEQ_1_0
D4h(32h)	SDOUT_R_SEQ_3_2
D5h (54h)	SDOUT_R_SEQ_5_4
D6h (76h)	SDOUT_R_SEQ_7_6
D7h (98h)	SDOUT_R_SEQ_9_8
D8h (BAh)	SDOUT_R_SEQ_B_A
D9h (DCh)	SDOUT_R_SEQ_D_C
DAh (FEh)	SDOUT_R_SEQ_F_E
DBh (C2h)	I2S Master Control
DCh	Reserved
DDh (88h)	Mix Ratio 0 & 1
DEh (88h)	Mix Ratio 2 & 3
DFh (08h)	PB Ratio
E0h (14h)	Mixing Output Control
E1h (00h)	Audio Detect Threshold 1
E2h (88h)	Audio Detect Threshold 2
E3h (88h)	Audio Detect Threshold 3
E4h-F8h	Reserved
F9h (00h)	PIXCLK Output Mode
FAh (00h)	CCIR656 Control
FBh (0Fh)	Clock Polarity
FCh (FFh)	AV Detection Enable
FDh (00h)	AV Detection Status
FEh (00h)	Device ID_H
FFh (C8h)	Device ID_L

6 Control Register

6.1 REGISTERS

Register Type	Descriptions
R	Read Only
RW	Read/Write

6.1.1 VIDEO STATUS REGISTER – OFFSET 00H/10H/20H/30H (Default: 00H)

BIT	FUNCTION	TYPE	DESCRIPTION

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BIT	FUNCTION	TYPE	DESCRIPTION
0	DET50	R	0: 60Hz source detected 1: 50Hz source detected
1	MONO	R	0:Color burst signal detected 1: No color burst signal detected
2	Reserved	R	Reset to 0b
3	VLOCK	R	0: Vertical logic is not locked 1: Vertical logic is locked to incoming video
4	Reserved	R	Reset to 0b
5	SLOCK	R	0: Sub-carrier sync is not detected 1: Sub-carrier sync is detected
6	HLOCK	R	0:Horizontal sync is not detected 1: Horizontal sync is detected
7	VDLOSS	R	0: Video is detected 1: Video not present

6.1.2 BRIGHTNESS CONTROL REGISTER – OFFSET 01H/11H/21H/31H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	Brightness	RW	These Signed bits control the brightness.Value range from -128 to 127 8'h7F: brightest; 8'h80: darkest ;8'h00 : no effect

6.1.3 CONTRASTCONTROL REGISTER – OFFSET 02H/12H/22H/32H(Default=64H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	Contrast	RW	These unsigned bits control the luminance gain. 8'h7F: maximum contrast 8'h00: minimum contrast

6.1.4 SHARPNESS CONTROL REGISTER – OFFSET 03H/13H/23H/33H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Sharpness	RW	These bits control the amount of sharpness enhancement on the luminance signals "0" has no effect on the output image "1" through "15" provides sharpness enhancement with "15" being the strongest
[7:4]	Reserved	R	Reset to 0h

6.1.5 CHROMA(U) GAIN REGISTER – OFFSET 04H/14H/24H/34H(Default=80H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	Chroma (U) Gain	RW	Chroma gain value of controlling the color saturation

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6.1.6 CHROMA(V) GAIN REGISTER – OFFSET 05H/15H/25H/35H(Default=80H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	Chroma (V) Gain	RW	Chroma gain value of controlling the color saturation

6.1.7 HUECONTROL REGISTER – OFFSET 06H/16H/26H/36H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	Hue	RW	These signed bits control color hue. +90C(7Fh) to -90C(80h)

6.1.8 RESERVED REGISTER– OFFSET07H/17H/27H/37H

6.1.9 RESERVED REGISTER – OFFSET 08H/18H/28H/38H

6.1.10 RESERVED REGISTER – OFFSET09H/19H/29H/39H

6.1.11 RESERVED REGISTER – OFFSET 0AH/1AH/2AH/3AH

6.1.12 RESERVED REGISTER – OFFSET 0BH/1BH/2BH/3BH

6.1.13 RESERVED REGISTER – OFFSET 0CH/1CH/2CH/3CH

6.1.14 RESERVED REGISTER – OFFSET 0DH/1DH/2DH/3DH

6.1.15 STANDARD SELECTION REGISTER – OFFSET 0EH/1EH/2EH/3EH(Default=77H)

BIT	FUNCTION	TYPE	DESCRIPTION
[2:0]	Standard Selection	RW	0: NTSC(M) 1: PAL(B,D,G,H,I) 2:Not valid 3: NTSC4.43 4: PAL(M) 5: PAL(CN) 6: PAL60 7: Auto detection
[3]	Reserved	R	Reset to 0b
[6:4]	Current Standard Detected	R	0: NTSC(M) 1: PAL(B,D,G,H,I) 2:Not valid 3: NTSC4.43 4: PAL(M) 5: PAL(CN) 6: PAL60 7:Not valid
[7]	Reserved	R	Reset to 0b

6.1.16 RESERVEDREGISTER – OFFSET 0FH/1FH/2FH/3FH

6.1.17 RESERVED REGISTER – OFFSET 40H-50H

6.1.18 FBITINV REGISTER – OFFSET 51H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	FBITINV0	R/W	0: F-bit in the 4th byte of 656 EAV/SAV for channel 1 is not inverted.

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BIT	FUNCTION	TYPE	DESCRIPTION
			1: F-bit in the 4th byte for channel 0 is inverted.
[1]	FBITINV1	R/W	0: F-bit in the 4th byte of 656 EAV/SAV for channel 2 is not inverted. 1: F-bit in the 4th byte for channel 1is inverted.
[2]	FBITINV2	R/W	0: F-bit in the 4th byte of 656 EAV/SAV for channel 3 is not inverted. 1: F-bit in the 4th byte for channel 2is inverted.
[3]	FBITINV3	R/W	0: F-bit in the 4th byte of 656 EAV/SAV for channel 4 is not inverted. 1: F-bit in the 4th byte for channel 3is inverted.
[7:4]	Reserved	R	Reset to 0b

6.1.19 RESERVED REGISTER – OFFSET 52H-56H

6.1.20 HBLEN REGISTER – OFFSET 57H/58H/59H/5AH(Default=90H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	HBLENn[7:0] n=1,2,3,4	R	Display the blanking length starting from EAV to SAV code. (1) In 27MHz D1 Mode: 90H for PAL while 8AH for NTSC (2) In 36MHz WD1 Mode: C0H for PAL while B8H for NTSC

6.1.21 RESERVED REGISTER – OFFSET 5BH

6.1.22 BGCTL-REGISTER – OFFSET 5CH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Reserved	RW	Reset to 0h
[4]	Reserved	R	Reset to 0h
[5]	Reserved	R	Reset to 0b
[7:6]	Reserved	R	Reset to 0b

6.1.23 RESERVED REGISTER – OFFSET 5DH-5FH

6.1.24 RESERVED REGISTER – OFFSET 60H

6.1.25 CRYSTAL CLOCK SELECT REGISTER – OFFSET 61H(Default=03H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	XINMD	RW	XIN input frequency 0:27Mhz 1:54Mhz 2:108Mhz 3: 54/27Mhz
[7:2]	Reserved	RW	Reset to 00h

6.1.26 36M/GPIO_OE REGISTER – OFFSET 62H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION

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BIT	FUNCTION	TYPE	DESCRIPTION
[0]	GPIO_0OE	RW	0: GPIO_0 pin is input. 1: GPIO_0 pin is output.
[1]	GPIO_1OE	RW	0: GPIO_1 pin is input. 1: GPIO_1 pin is output.
[2]	GPIO_2OE	RW	0: GPIO_2 pin is input. 1: GPIO_2 pin is output.
[3]	GPIO_3OE	RW	0: GPIO_3 pin is input. 1: GPIO_3 pin is output.
[4]	O36M0	RW	0: Channel 0 generates 27MHz video data 1: Channel 0 generates 36MHz video data
[5]	O36M1	RW	0: Channel 1 generates 27MHz video data 1: Channel 1 generates 36MHz video data
[6]	O36M2	RW	0: Channel 2 generates 27MHz video data 1: Channel 2 generates 36MHz video data
[7]	O36M3	RW	0: Channel 3 generates 27MHz video data 1: Channel 3 generates 36MHz video data

6.1.27 CHANNEL ID01 REGISTER – OFFSET 63H(Default=10H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	CH0NUM	RW	Assign channel ID number in CV_IN0A/CV_IN0B video data output
[7:4]	CH1NUM	RW	Assign channel ID number in CV_IN1A/CV_IN1B video data output

6.1.28 CHANNEL ID23 REGISTER – OFFSET 64H(Default=32H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	CH2NUM	RW	Assign channel ID number in CV_IN2A/CV_IN2B video data output
[7:4]	CH3NUM	RW	Assign channel ID number in CV_IN3A/CV_IN3B video data output

6.1.29 PIXEL OUTPUT BUS TRI-STATE CONTROL REGISTER – OFFSET 65H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	PIXOUT_0 OEB	RW	PIXOUT_0 [7:0] output tri-state control. 0: Put the bus in tri-state mode. 1: Put the bus in output mode
[1]	PIXOUT_1 OEB	RW	PIXOUT_1 [7:0] output tri-state control. 0: Put the bus in tri-state mode. 1: Put the bus in output mode
[2]	PIXOUT_2 OEB	RW	PIXOUT_2 [7:0] output tri-state control. 0: Put the bus in tri-state mode. 1: Put the bus in output mode
[3]	PIXOUT_3 OEB	RW	PIXOUT_3 [7:0] output tri-state control. 0: Put the bus in tri-state mode. 1: Put the bus in output mode
[7:4]	Reserved	R	Reset to 0h

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6.1.30 RESERVED REGISTER – OFFSET 66-6FH

6.1.31 AUDIO CLOCK CONTROL REGISTER – OFFSET 70H(Default=08H)

BIT	FUNCTION	TYPE	DESCRIPTION
[2:0]	AFMD	RW	0: 8KHz 1: 16KHz 2: 32KHz 3: 44.1KHz 4: 48KHz
[3]	Reserved	R	Reset to 1b
[5:4]	Reserved	R	Reset to 0b
[6]	S2I_8BIT	RW	0:SCLK_P/LRCK_P/SDOUT_P pin input 16-bit control 1: SCLK_P/LRCK_P/SDOUT_P pin input 8-bit control
[7]	Reserved	R	Reset to 0b

6.1.32 I2S AUDIO INPUT CONTROL REGISTER – OFFSET 71H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	Reserved	R	Reset to 00b
[2]	SDINPDLY	RW	SDIN_P input data delay by one SCLK_P clock 0:No delay; 1T delay for I2S interface 1:Add 1 SCLK_P clock delay in SDIN_P input.; 0T delay for left-justified interface.
[7:3]	Reserved	R	Reset to 00h

6.1.33 RESERVED REGISTER – OFFSET72H-7AH

6.1.34 SDOUT_M SELECT (R) REGISTER – OFFSET 7BH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	Reserved	R	Reset to 00b
[4:0]	I2SO_RSEL	RW	Select R channel output on SDOUT_M pin when SDOUTM_I2SOEN=1 0:Select record audio channel LINE_IN0_1 1:Select record audio channel LINE_IN1_1 2:Select record audio channel LINE_IN2_1 3:Select record audio channel LINE_IN3_1 4:Select record audio channel LINE_IN0_2 5:Select record audio channel LINE_IN1_2 6:Select record audio channelLINE_IN2_2 7:Select record audio channel LINE_IN3_2 8:Select record audio channel LINE_IN0_3 9:Select record audio channel LINE_IN1_3 A:Select record audio channel LINE_IN2_3 B:Select record audio channel LINE_IN3_3 C:Select record audio channel LINE_IN0_4 D:Select record audio channel LINE_IN1_4 E:Select record audio channel LINE_IN2_4 F:Select record audio channel LINE_IN3_4 10h:Select playback audio of the master chip

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BIT	FUNCTION	TYPE	DESCRIPTION
			11h:Reserved 12h:Select playback audio of the slave chip 13h:Reserved 14h:Playback data output and playback data can adjust volume by DF[3:0] 15h:Select record audio of channel LINE_IN4_1 16h:Select record audio of channel LINE_IN4_2 17h:Select record audio of channel LINE_IN4_3 18h:Select record audio of channel LINE_IN4_4 Others:No audio output
[7:5]	Reserved	R	Reset to 0h

6.1.35 SDOUT_M SELECT (L) REGISTER – OFFSET 7CH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	Reserved	R	Reset to 00b
[4:0]	I2SO_RSEL	RW	Select L channel output on SDOUT_M pin when SDOUTM_I2SOEN=1: 0:Select record audio channel LINE_IN0_1 1:Select record audio channel LINE_IN1_2 2:Select record audio channel LINE_IN2_3 3:Select record audio channel LINE_IN3_4 4:Select record audio channel LINE_IN0_1 5:Select record audio channel LINE_IN1_2 6:Select record audio channel LINE_IN2_3 7:Select record audio channel LINE_IN3_4 8:Select record audio channel LINE_IN0_1 9:Select record audio channel LINE_IN1_2 A:Select record audio channel LINE_IN2_3 B:Select record audio channel LINE_IN3_4 C:Select record audio channel LINE_IN0_1 D:Select record audio channelLINE_IN1_2 E:Select record audio channel LINE_IN2_3 F:Select record audio channel LINE_IN3_4 10h:Select playback audio of the master chip 11h:Reserved 12h:Select playback audio of the slave chip 13h:Reserved 14h:Playback data output and playback data can adjust volume by DF[3:0] 15h:Select record audio of channel LINE_IN4_1 16h:Select record audio of channel LINE_IN4_2 17h:Select record audio of channel LINE_IN4_3 18h:Select record audio of channel LINE_IN4_4 Others:No audio output
[7:5]	Reserved	R	Reset to 000b

6.1.36 EXTENDED LINE SELECT REGISTER – OFFSET 7DH(Default=E4H)

BIT	FUNCTION	TYPE	DESCRIPTION

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BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	Select Output Data In Data51 Position	RW	0: LINE_IN4_1 1: LINE_IN4_2 2: LINE_IN4_3 3: LINE_IN4_4
[3:2]	Select Output Data In Data52 Position	RW	0: LINE_IN4_1 1: LINE_IN4_2 2: LINE_IN4_3 3: LINE_IN4_4
[5:4]	Select Output Data In Data53 Position	RW	0: LINE_IN4_1 1: LINE_IN4_2 2: LINE_IN4_3 3: LINE_IN4_4
[7:6]	Select Output Data In Data54 Position	RW	0: LINE_IN4_1 1: LINE_IN4_2 2: LINE_IN4_3 3: LINE_IN4_4 Note: If I2S mode is set: L data: dat0-dat1-dat2-dat3-dat4-dat5-dat6-dat7-dat51-dat52 Rdata: dat8-dat9-datA-datB-datC-datD-datE-datF-dat53-dat54 If DSP mode is set: dat0-dat1-dat2-dat3-dat4-dat5-dat6-dat7-dat8-dat9-datA-datB-datC-datD-datE-datF- dat51-dat52-dat53-dat54

6.1.37 SDOUT_M REGISTER– OFFSET 7EH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[5:0]	Reserved	R	Reset to 00b
[6]	SDOUT_M I2S OEN	R/W	Define SDOUT_M pin output 2 word data to make standard I2S output 0: Mixing Data or Playback input data are only output on SDOUT_M 1:L/R data on SDOUT_M pin is selected by 0x7B and 0x7C
[7]	A5OUTOFF	R/W	0:LINE_IN4_1/LINE_IN4_2/LINE_IN4_3 /LINE_IN4_4 output on SDOUT_R 1:LINE_IN4_1/LINE_IN4_2/LINE_IN4_3 /LINE_IN4_4 not output on SDOUT_R

6.1.38 MIX RATIO VALUE FOR LINE_IN4 REGISTER – OFFSET 7FH(Default=08H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Mix_Ratio4	RW	LINE_IN4 ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25%

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			5 : 12.5% 6 : 25% 7 : 50% other : 100%
[7:4]	Reserved	R	Reset to 00b

6.1.39 SOFTWARE RESET REGISTER– OFFSET 80H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	ADEC0RST	W	Writing one reset the video decoder 0 to its default state but all registercontent remain unchanged. This bit is self-resetting
[1]	ADEC1RST	W	Writing one reset the video decoder 1 to its default state but all register content remain unchanged. This bit is self-resetting
[2]	ADEC2RST	W	Writing one reset the video decoder 2 to its default state but all register content remain unchanged. This bit is self-resetting
[3]	ADEC3RST	W	Writing one reset the video decoder 3 to its default state but all register content remain unchanged. This bit is self-resetting
[4]	Reserved	R	Reset to 00b
[5]	AUDIORST	W	Writing one reset the audio portion to its default state but all register content remain unchanged. This bit is self-resetting
[7:6]	Reserved	R	Reset to 00b

6.1.40 RESERVED REGISTER – OFFSET 81H-84H

6.1.41 VIDEO SOURCE SELECTION REGISTER – OFFSET 85H (Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	CV_INA0/CV_INB0 Selection	RW	0: CV_INA0 1: CV_INB0
[1]	CV_INA1/CV_INB1 Selection	RW	0: CV_INA1 1: CV_INB1
[2]	CV_INA2/CV_IN_B2 Selection	RW	0: CV_INA2 1: CV_INB2
[3]	CV_INA3/CV_INB3 Selection	RW	0: CV_INA3 1: CV_INB3
[7:4]	Reserved	R	Reset to 0h

6.1.42 RESERVED REGISTER – OFFSET 86H-88H

6.1.43 AUDIO FS MODE REGISTER– OFFSET 89H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	Reserved	R	Reset to 00b
[2]	Audio FS Mode Select	RW	0: 256fs 1: 320fs
[7:3]	Reserved	R	Reset to 00h

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6.1.44 RESERVED REGISTER – OFFSET 8AH-9EH

6.1.45 PIXCLK 0 DELAY REGISTER– OFFSET 9FH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Control Clock Delay Of PIXCLK_P0 Pin	RW	0h/1h/3h/7h/Fh values are effective 0h: No clock delay 1h: About 2ns more delay, 3h: About 4ns more delay, 7h: About 6ns more delay, Fh: About 7ns more delay
[7:4]	Control Clock Delay Of PIXCLK_N0 Pin	RW	0h/1h/3h/7h/Fh values are effective. 0h: No clock delay 1h: About 2ns more delay, 3h: About 4ns more delay, 7h: About 6ns more delay, Fh: About 7ns more delay

6.1.46 RESERVED REGISTER – OFFSET A0H-B0H

6.1.47 CH8IDEN REGISTER – OFFSET B1H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[6:0]	Reserved	R	Reset to 00b
[7]	CH8IDEN	R/W	Video Channel ID number for 8 channels when fast switching is enabled. 0: 4-channel ID only. Please refer to channel ID01 and ID34 registers for defining 4 channels' ID numbers. 1: 8-channel ID. The ID for each channel is defined as follows. CV_IN0A: {1'b0, CH0NUM[2:0]} CV_IN1A: {1'b0, CH1NUM[2:0]} CV_IN2A: {1'b0, CH2NUM[2:0]} CV_IN3A: {1'b0, CH3NUM[2:0]} CV_IN0B: {1'b1, CH0NUM[2:0]} CV_IN1B: {1'b1, CH1NUM[2:0]} CV_IN2B: {1'b1, CH2NUM[2:0]} CV_IN3B: {1'b1, CH3NUM[2:0]}

6.1.48 RESERVED REGISTER – OFFSET B2H-C7H

6.1.49 GPIO_0_1 MODE REGISTER– OFFSET C8H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[2:0]	Output Mode For GPIO_0Pin	RW	Select output mode for GPIO_0 pin 0: Output HSYNC 1: Output VSYNC 2: Field 3: H-active 4: VH-active 5: 27MHz clock output 6: VH-sync 7: GPP_VA1
[3]	General Purpose Value	RW	Set general purpose value in GPIO_0 pin

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BIT	FUNCTION	TYPE	DESCRIPTION
	In GPIO_0 Pin		
[6:4]	Output Mode For GPIO_1 Pin	RW	Select output mode for GPIO_1 pin 0: Output HSYNC 1: Output VSYNC 2: Field 3: H-active 4: VH-active 5: 27MHz clock output 6: VH-sync 7: GPP_VA2
[7]	General Purpose Value In GPIO_1 Pin	RW	Set general purpose value in GPIO_1 pin

6.1.50 GPIO_2_3 MODE REGISTER– OFFSET C9H(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[2:0]	Output Mode For GPIO_2 Pin	RW	Select output mode for GPIO_2 pin 0: Output HSYNC 1: Output VSYNC 2: Field 3: H-active 4: VH-active 5: 27MHz clock output 6: VH-sync 7: GPP_VA1
[3]	General Purpose Value In GPIO_2 Pin	RW	Set general purpose value in GPIO_2 pin
[6:4]	Output Mode For GPIO_3 Pin	RW	Select output mode for GPIO_3 pin 0: Output HSYNC 1: Output VSYNC 2: Field 3: H-active 4: VH-active 5: 27MHz clock output 6: VH-sync 7: GPP_VA2
[7]	General Purpose Value In GPIO_3 Pin	RW	Set general purpose value in GPIO_3 pin

6.1.51 VIDEO OUTPUT MODE REGISTER – OFFSET CAH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	PIXOUT_0 Pin Output Mode	RW	0: Single output 1: dual channel video output 2:quad channel video output 3: Reserved
[3:2]	PIXOUT_1 Pin Output Mode	RW	0: Single output 1: dual channel video output 2:quad channel video output 3: Reserved

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BIT	FUNCTION	TYPE	DESCRIPTION
[5:4]	PIXOUT_2 Pin Output Mode	RW	0: Single output 1: dual channel video output 2:quad channel video output 3: Reserved
[7:6]	PIXOUT_3 Pin Output Mode	RW	0: Single output 1: dual channel video output 2:quad channel video output 3: Reserved

6.1.52 GPIO POLARITY REGISTER – OFFSET CBH (Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Reserved	R	Reset to 0h
[4]	Select GPIO_0 Pin Output Polarity.	RW	0: Normal 1: Inverse polarity
[5]	Select GPIO_1 Pin Output Polarity.	RW	0: Normal 1: Inverse polarity
[6]	Select GPIO_2 Pin Output Polarity.	RW	0: Normal 1: Inverse polarity
[7]	Select GPIO_3 Pin Output Polarity.	RW	0: Normal 1: Inverse polarity

6.1.53 PIXOUT OUTPUT CH2 SELECT REGISTER – OFFSET CCH (Default=39H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	CH2 Data Selection In PIXOUT_0	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 00b
[3:2]	CH2 Data Selection In PIXOUT_1	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 01b
[5:4]	CH2 Data Selection In PIXOUT_2	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 10b
[7:6]	CH2 Data Selection In PIXOUT_3	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 11b

6.1.54 PIXOUT OUTPUT CH1 SELECT REGISTER – OFFSET CDH (Default=E4H)

BIT	FUNCTION	TYPE	DESCRIPTION

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BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	CH1 Data Selection In PIXOUT_0	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 00b
[3:2]	CH1 Data Selection In PIXOUT_1	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 01b
[5:4]	CH1 Data Selection In PIXOUT_2	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 10b
[7:6]	CH1 Data Selection In PIXOUT_3	RW	0: CV_IN0 Video Decoder data 1: CV_IN1 Video Decoder data 2: CV_IN2 Video Decoder data 3: CV_IN3 Video Decoder data Reset to 11b

6.1.55 RESERVED REGISTER– OFFSET CEH

6.1.56 SERIAL MODE CONTROL REGISTER– OFFSET CFH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[6:0]	Reserved	R	Reset to 00h
[7]	SMD	RW	Cascade Audio Serial mode. 0: SD_LINKO is tri stated 1: SD_LINKO is enabled

6.1.57 RESERVED REGISTER– OFFSET D0H-D1H

6.1.58 SDOUT_RM OUTPUT REGISTER– OFFSET D2H(Default=03H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	16 Audios Recorded On The SDOUT_R Pin	R	Reset to 11b
[3:2]	R_SDOUTM	RW	Select the output mode for SDOUT_M pin 0:The output is controlled by SDOUTM_I2SOE 1: Record audio in SDOUT_R format 2: Record audio in SDOUT_M format
[5:4]	Reserved	R	Reset to 00b
[6]	RM_SYNC	RW	Record and mixing audio data format 0: I2S mode 1: DSP mode
[7]	Data Position	RW	I2S MODE 0: Mix data on position 0, Playback data on position 8 1: Mix data on position 8, Playback data on position 0 DSP MODE

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			0: Mix data on position 0, Playback data on position 1 1: Mix data on position 1, Playback data on position 0

6.1.59 SDOUT_R_SEQ_1_0 REGISTER– OFFSET D3H(Default=10H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQ0	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQ1	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.60 SDOUT_R_SEQ_3_2 REGISTER– OFFSET D4H(Default=32H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQ2	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2

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			5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQ3	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.61 SDOUT_R_SEQ_5_4 REGISTER– OFFSET D5H(Default=54H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQ4	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQ5	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1

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BIT	FUNCTION	TYPE	DESCRIPTION
			2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.62 SDOUT_R_SEQ_7_6REGISTER– OFFSETD6H(Default=76H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQ6	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQ7	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4

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			F: LINE_IN3_4

6.1.63 SDOUT_R_SEQ_9_8 REGISTER– OFFSET D7H(Default=98H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQ8	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQ9	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.64 SDOUT_R_SEQ_B_A REGISTER– OFFSET D8H(Default= BAH)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQA	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2

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			7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQB	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.65 SDOUT_R_SEQ_D_C REGISTER– OFFSET D9H(Default= DCH)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQC	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQD	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1

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			4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

6.1.66 SDOUT_R_SEQ_F_E REGISTER– OFFSET DAH(Default= FEH)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	R_SEQE	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4
[7:4]	R_SEQF	RW	The sequence on the SDOUT_R 0: LINE_IN0_1 1: LINE_IN1_1 2: LINE_IN2_1 3: LINE_IN3_1 4: LINE_IN0_2 5: LINE_IN1_2 6: LINE_IN2_2 7: LINE_IN3_2 8: LINE_IN0_3 9: LINE_IN1_3 A: LINE_IN2_3 B: LINE_IN3_3 C: LINE_IN0_4 D: LINE_IN1_4 E: LINE_IN2_4 F: LINE_IN3_4

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6.1.67 I2S MASTER CONTROL REGISTER– OFFSET DBH(Default= C2H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	ACLKRMASTER	RW	0: SCLK_R pin is slave mode 1: SCLK_R pin is master mode
[1]	Reserved	R	Reset to 1b
[2]	SDOUT_RPin Data Format	RW	Per word unit on SDOUT_R Pin 0: 16bit 1: 8bit
[3]	PB_SYNC	RW	The audio data format for audio playback mode 0: I2S mode for playback 1: DSP mode for playback
[4]	PB_LRSEL	RW	Select the audio data position in playback input I2S mode: 0: 1st Left channel audio data 1: 1st Right channel audio data DSP mode: 0: 1st channel audio data 1: 2nd channel audio data
[5]	PB_MASTER	RW	The operation mode for playback mode. 0: SCLK_P pin is slave mode 1: SCLK_P pin is master mode
[7:6]	Reserved	R	Reset to 11b

6.1.68 MIX_MUTE REGISTER– OFFSET DCH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[4:0]	MIX_MUTE	R	Mute function Enable 0 : disable 1: mute Bit[0] : LINE_0_1; Bit[1] : LINE_1_1; Bit[2] : LINE_2_1; Bit[3] : LINE_3_1; Bit[4] : Playback audio input;
[7:5]	Reserved	R	Reset to 00b

6.1.69 MIX RATIO VALUE FOR LINE_IN0 & LINE_IN1 REGISTER – OFFSET DDH (Default=88H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Mix_Ratio0	RW	LINE_IN0 ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25% 5 : 12.5% 6 : 25% 7 : 50%

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			other : 100%
[7:4]	Mix_Ratio1	R/W	LINE_IN1 ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25% 5 : 12.5% 6 : 25% 7 : 50% other : 100%

6.1.70 MIX RATIO VALUE FOR LINE_IN2 & LINE_IN3 REGISTER – OFFSET DEH (Default=88H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Mix_Ratio2	RW	LINE_IN2 ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25% 5 : 12.5% 6 : 25% 7 : 50% other : 100%
[7:4]	Mix_Ratio3	R/W	LINE_IN3 ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25% 5 : 12.5% 6 : 25% 7 : 50% other : 100%

6.1.71 PB RATIO REGISTER – OFFSET DFH (Default=08H)

BIT	FUNCTION	TYPE	DESCRIPTION
[3:0]	Ratio Value For Audio Mixing	RW	Playback input ratio value for audio mixing function 0 : 0.39% 1 : 0.78% 2 : 1.56% 3 : 3.12% 4 : 6.25% 5 : 12.5% 6 : 25%

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			7 : 50% other : 100%
[7:4]	Reserved	R	Reset to 0h

6.1.72 MIXING OUTPUT CONTROL REGISTER– OFFSET E0H(Default=14H)

BIT	FUNCTION	TYPE	DESCRIPTION
[4:0]	MIX_OUTSEL	RW	Define the final audio output for analog and digital mixing out: 0h: LINE_IN0_1 1h: LINE_IN1_1 2h: LINE_IN2_1 3h: LINE_IN3_1 4h: LINE_IN0_2 5h: LINE_IN1_2 6h: LINE_IN2_2 7h: LINE_IN3_2 8h: LINE_IN0_3 9h: LINE_IN1_3 Ah: LINE_IN2_3 Bh: LINE_IN3_3 Ch: LINE_IN0_4 Dh: LINE_IN1_4 Eh: LINE_IN2_4 Fh: LINE_IN3_4 10h: Playback audio of the master chip 11h: Reserved 12h: Playback audio of the slave chip 13h: Reserved 14h: Playback data output and playback data can adjust volume by DFh[3:0] 15h: LINE_IN4_1 16h" LINE_IN4_2 17h: LINE_IN4_3 18h: LINE_IN4_4 Others: No audio output
[7:5]	Reserved	R	Reset to 000b

6.1.73 RESERVED REGISTER– OFFSET E1H-F8H

6.1.74 PIXCLK OUTPUT MODE REGISTER– OFFSET F9H (Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[0]	PIXCLK_PF	RW	Output frequency mode of PIXCLK_PO pin. 0: Output one of 27MHz, 54MHz or 180MHz frequency. 1: Output one of 36MHz, 72MHz or 144MHz frequency.
[1]	PIXCLK_NF	RW	Output frequency mode of PIXCLK_NO pin. 0: Output one of 27MHz, 54MHz or 180MHz frequency. 1: Output one of 36MHz, 72MHz or 144MHz frequency.
[7:2]	Reserved	R	Reset to 0h

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6.1.75 CCIR656 CONTROL REGISTER– OFFSET FAH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	PIXOUT format Control	W	Control the data frequency of PIXOUT pins 0: 27M/36MHz data output 1: 54M/72MHz data output 2: 108M/144MHz data output Reset to 00b
[3:2]	Reserved	W	Reset to 00b
[4]	Reserved	R	Reset to 0b
[5]	Reserved	R	Reset to 0b
[6]	CCIR656 Output Enable	RW	0: All outputs are tri-stated 1:All outputs(PIXOUT_n/PIXCLK_PO/PIXCLK_NO) are enabled
[7]	Reserved	R	Reset to 0b

6.1.76 CLOCK POLARITY REGISTER– OFFSET FBH(Default=0FH)

BIT	FUNCTION	TYPE	DESCRIPTION
[1:0]	VDET_MODE	RW	Define the polarity of state register and interrupt request for video detection. 0: No interrupt request by the video detection 1: Make the interrupt request rising only when the video comes in 2: Make the interrupt request falling only when the video goes out 3: Make the interrupt request rising and falling whenthe video comes in and goes out
[3:2]	ADET_MODE	RW	Define the polarity of state register and interrupt request for audio detection. 0: No interrupt request by the audio detection 1: Make the interrupt request rising only when the audio comes in 2: Make the interrupt request falling only when the audio goes out 3: Make the interrupt request rising and falling whenthe audio comes in and goes out
[4]	IRQPOL	RW	Select the polarity of interrupt request through theIRQ pin. 0: Falling edge requests the interrupt and keeps itsstate until cleared 1: Rising edge requests the interrupt and keeps itsstate until cleared
[5]	IRQENA R/W	RW	Enable/Disable the interrupt request through the IRQ pin 0: Disable 1: Enable
[6]	PIXCLK_P_POL	RW	0:The polarity of PIXCLK_Pis not inversed

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			1: The polarity of PIXCLK_P is inversed
[7]	PIXCLK_N_POL	RW	0:The polarity of PIXCLK_N is not inversed 1: The polarity of PIXCLK_N is inversed

6.1.77 VIDEO/AUDIO DETECTION ENABLE REGISTER–OFFSET FCH (Default=FFH)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	AVDET_EN	RW	Enable the status register updated and interrupt request if the following video or audio source is detected. The mapping of video/audio input to each bit of the register is defined as below. Bit0: Video input CV_IN0. Bit1: Video input CV_IN1. Bit2: Video input CV_IN2. Bit3: Video input CV_IN3. Bit4: Audio input LINE_IN0. Bit5: Audio input LINE_IN1. Bit6: Audio input LINE_IN2. Bit7: Audio input LINE_IN3. 0: Disable status register updated and interrupt request 1: Enable status register updated and interrupt request

6.1.78 VIDEO/AUDIO DETECTION STATUS REGISTER–OFFSET FDH (Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[7:0]	AVDET_STATUS	R	Display the detection status of each video or audio source according to AVDET_EN, VDET_MODE and ADET_MODE. The mapping of video/audio input to each bit of the register is defined as below. The bits will be cleared once the register is read by software except VDET_MODE =3 or ADET_MODE=3. Bit0: Video input CV_IN0. Bit1: Video input CV_IN1. Bit2: Video input CV_IN2. Bit3: Video input CV_IN3. Bit4: Audio input LINE_IN0. Bit5: Audio input LINE_IN1. Bit6: Audio input LINE_IN2. Bit7: Audio input LINE_IN3. 0: Inactive. No event detected after the last access to this bit. 1: Active. An event is detected.

6.1.79 DEVICE ID_H REGISTER– OFFSET FEH(Default=00H)

BIT	FUNCTION	TYPE	DESCRIPTION
[5:0]	Reserved	R	Reset to 00h

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[7:6]	Dev_ID[6:5]	R	Reset to 00b

6.1.80 DEVICE ID - L REGISTER– OFFSET FFH(Default=E8H)

BIT	FUNCTION	TYPE	DESCRIPTION
[2:0]	REV_ID	R	Reset to 000b
[7:3]	Dev_ID[4:0]	R	Reset to 1dh

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Parameters		Value
Supply Voltage Range	3.3V Power Supply	-0.3V to 4.5V
	Core Power 1.0V Supply	-0.3V to 1.8V
T_A Operating free-air temperature range		-45 °C to 85 °C
T_{stg} Storage Temperature		-65 °C to 150 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7.2 Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
VD33,ADC_VDD, ADAC_VDD, VDDPLL	3.3V Power supply voltage	3.0	3.3	3.6	V
VDDC	Core Power supply voltage	0.9	1.0	1.1	V
$V_{I(P-P)}$	Analog input voltage (ac-coupling necessary)	0		1.6	V
T_A	Ambient free-air temperature	0		70	°C

7.3 DC Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Digital input high voltage		2.0		3.6	V
V_{IL}	Digital input low voltage		-0.3		0.8	V
V_{OH}	Digital Output high voltage		2.4			V

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V_{OL}	Digital Output low voltage				0.4	V
I_L	Input Leakage Current				+/- 1	uA
I_{OZ}	Tri-state output leakage current				+/- 1	uA
I_{OH}	High level output current	V_{OH}=2.4V	11	17	24	mA
I_{OL}	Low level output current	V_{OL}=0.4V	8	13	16	mA
R_{pu}	Input pull-up resistance	Vin=0	61	75	105	KΩ
R_{pd}	Input pull-down resistance	Vin=DVDD33	101	199	330	KΩ
T_j	Junction temperature		-40	25	125	°C

7.3.1 Power Dissipation

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Unit
$3.3V_{TOTAL}$	Total 3.3V Power Voltage	Connect all Video/Audio PINS		218		mA
$1.0V_{TOTAL}$	Core Supply Voltage (VDDC)	Connect all Video/Audio PINS		158		mA
P_{TOT}	Total Power Consumption	Connect all Video/Audio PINS		741		mW

7.3.2 Power-On Sequence of 3.3V and 1.0V Power

Symbol	Parameters	Min	Typ	Max	Unit
T1	Interval Delay between IO and Core Power Supply	0	10	500	ms

7.3.3 Crystal Specifications

Parameters	Min	Typ	Max	Unit
Frequency		27		MHz
Frequency tolerance		±50		ppm

7.4 AC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Zi	Input impedance	Analog video inputs by design		40		kΩ
Ci	Input Capacitance	Analog video inputs by design		10		pF
DNL	Differential Non Linearity				±2	LSB
INL	Integral Non Linearity				±3	LSB
Vi	Full scale input range	The expected full input range is only 0.5 Vpp to 1.0 Vpp.	0.25		1.6	Vpp
SNR	Signal to Noise Ratio	This is measured with a -1dB full scale input signal and adjusted for full scale amplitude	50			dB
THD	Total Harmonic Distortion			-50		dB
	Analog input bandwidth	This bandwidth does not include		300		MHz

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		limitations due to the source impedance of 37.5 and loading on the board, 30 pF (140 MHz).				

7.4.1 Audio Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Zi	Input impedance	Analog video inputs by design		40		kΩ
Ci	Input Capacitance	Analog video inputs by design		10		pF
Vi	Maximum Input Range		0.25		1.6	V
SNR	Signal to Noise Ratio			85		dB
DNR	Dynamic Range			80		dB
THD	Total Harmonic Distortion			-75		dB

7.4.2 Pixel Clock and Video Data Timing

Symbol	Parameter	Min	Typ	Max	Unit
TS1	Setup from PIXCLK_PO to PIXOUT (144MHz)	2.6	-	4.3	ns
TH1	Hold from PIXCLK_PO to PIXOUT (144MHz)	2.7	-	4.4	ns
TS2	Setup from PIXCLK_PO to PIXOUT (108MHz)	3.8	-	5.4	ns
TH2	Hold from PIXCLK_PO to PIXOUT (108MHz)	3.9	-	5.5	ns
TS3	Setup from PIXCLK_PO to PIXOUT (72MHz)	5.6	-	7.6	ns
TH3	Hold from PIXCLK_PO to PIXOUT (72MHz)	6.3	-	8.3	ns
TS4	Setup from PIXCLK_PO to PIXOUT (54MHz)	8.2	-	10.3	ns
TH4	Hold from PIXCLK_PO to PIXOUT (54MHz)	8.3	-	10.4	ns
TS5	Setup from PIXCLK_PO to PIXOUT (36MHz)	14.1	-	16.1	ns
TH5	Hold from PIXCLK_PO to PIXOUT (36MHz)	11.7	-	13.7	ns
TS6	Setup from PIXCLK_PO to PIXOUT (27MHz)	19	-	20.9	ns
TH6	Hold from PIXCLK_PO to PIXOUT (27MHz)	16.1		18	ns

The timing value is measured by the following conditions: (1) the clock delay control on PIXCLK_PO pin is set to zero; (2) the clock polarity control on PIXCLK_PO pin is not inverted.

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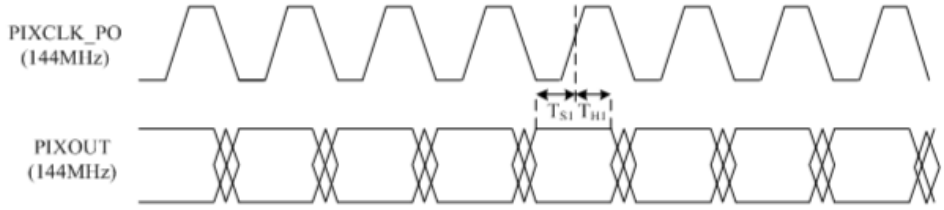

Figure 7-1 OTDM is operated at 144MHz

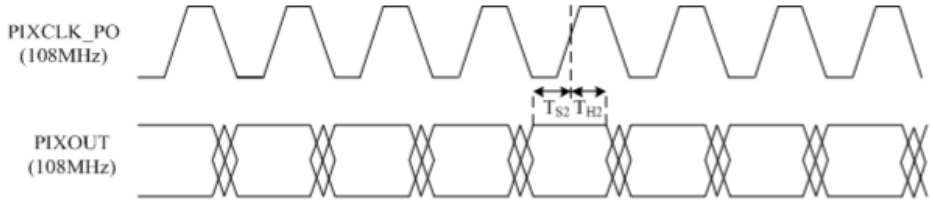

Figure 7-2OTDM is operated at 108MHz

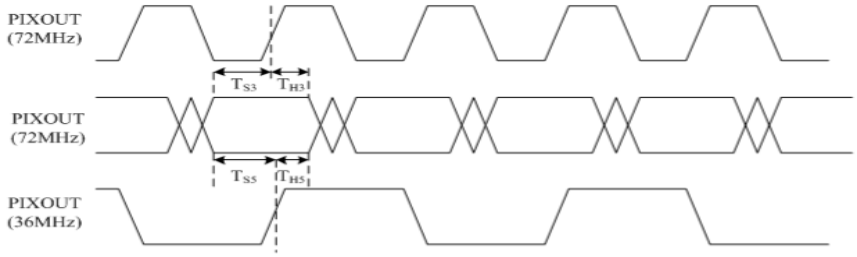

Figure 7-3 OTBM at 72/36MHz

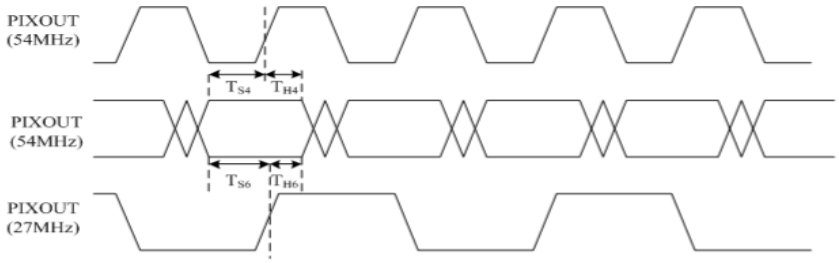

Figure 7-4 OTBM at 54/27MHz

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7.4.3 Audio Interface Timing

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$T_{S_LRCK_R}$	Setup Time for LRCK_R	Slave Mode	0.2	-		ns
$T_{H_LRCK_R}$	Hold Time for LRCK_R		0.4	-		ns
T_{S_PB}	Setup Time for LRCK_P and SDIN_P		0.1	-		ns
T_{H_PB}	Hold Time for LRCK_P and SDIN_P		0.55	-		ns
T_{RM_PD}	Propagation Delay for SDOUT_R/M, LRCK_R	Master Mode	2.6	-	5.9	ns
T_{PB_PD}	Propagation Delay for LRCK_P		2.2	-	4.8	ns

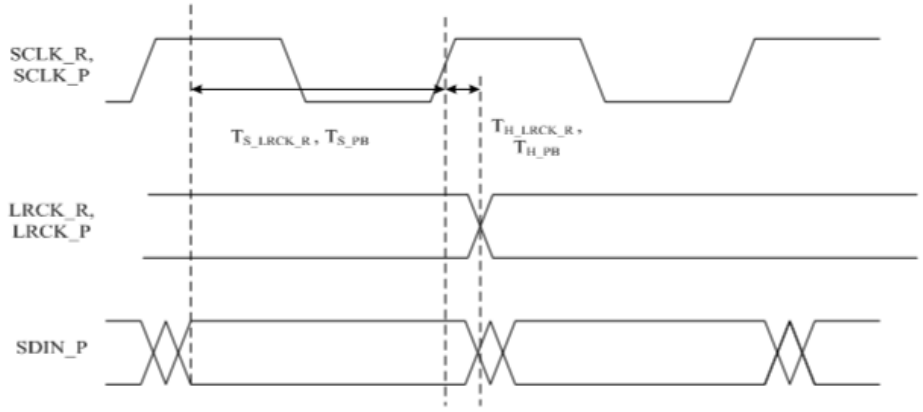

Figure 7-5 Digital Serial Audio Interface Slave Mode Timing Diagram

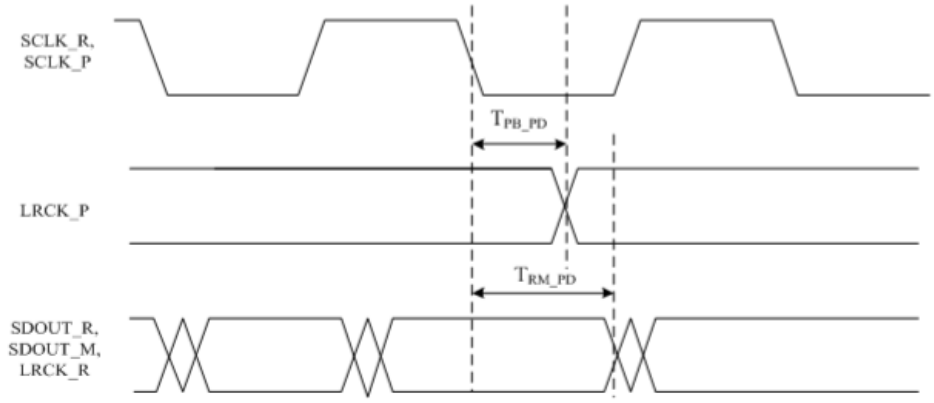

Figure 7-6 Digital Serial Audio Interface Master Mode Timing Diagram

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7.4.5 I2C Host Port Timing

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t1	Bus free time between STOP and START		1.3			µs
t2	Setup time, (repeated) START condition		0.6			µs
t3	Hold time, (repeated) START condition		0.6			µs
t4	Setup time, STOP condition		0.6			ns
t5	Data setup time		100			ns
t6	Data hold time		0		0.9	µs
t7	Rise time, VC1(SDA) and VC0(SCL) signal	Specified by design			250	ns
t8	Fall time, VC1(SDA) and VC0(SCL) signal	Specified by design			250	ns
C_b	Capacitive load for each bus line	Specified by design			400	pF
f_{i2c}	I^2C clock frequency				400	kHz

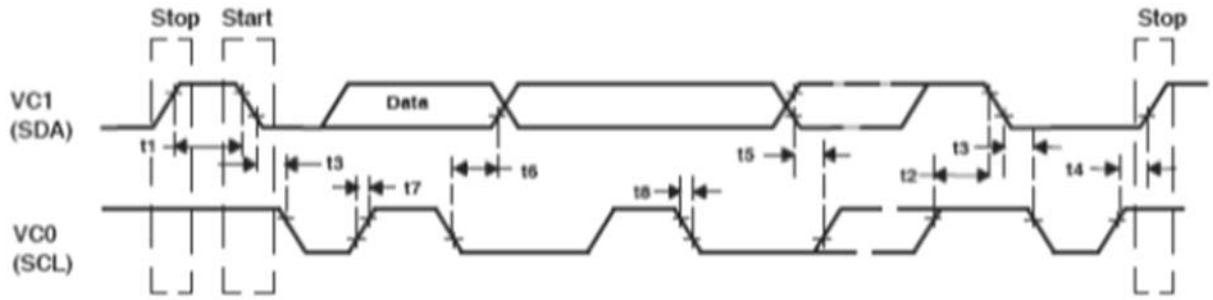

Figure 7-7I2C Host Port Timing

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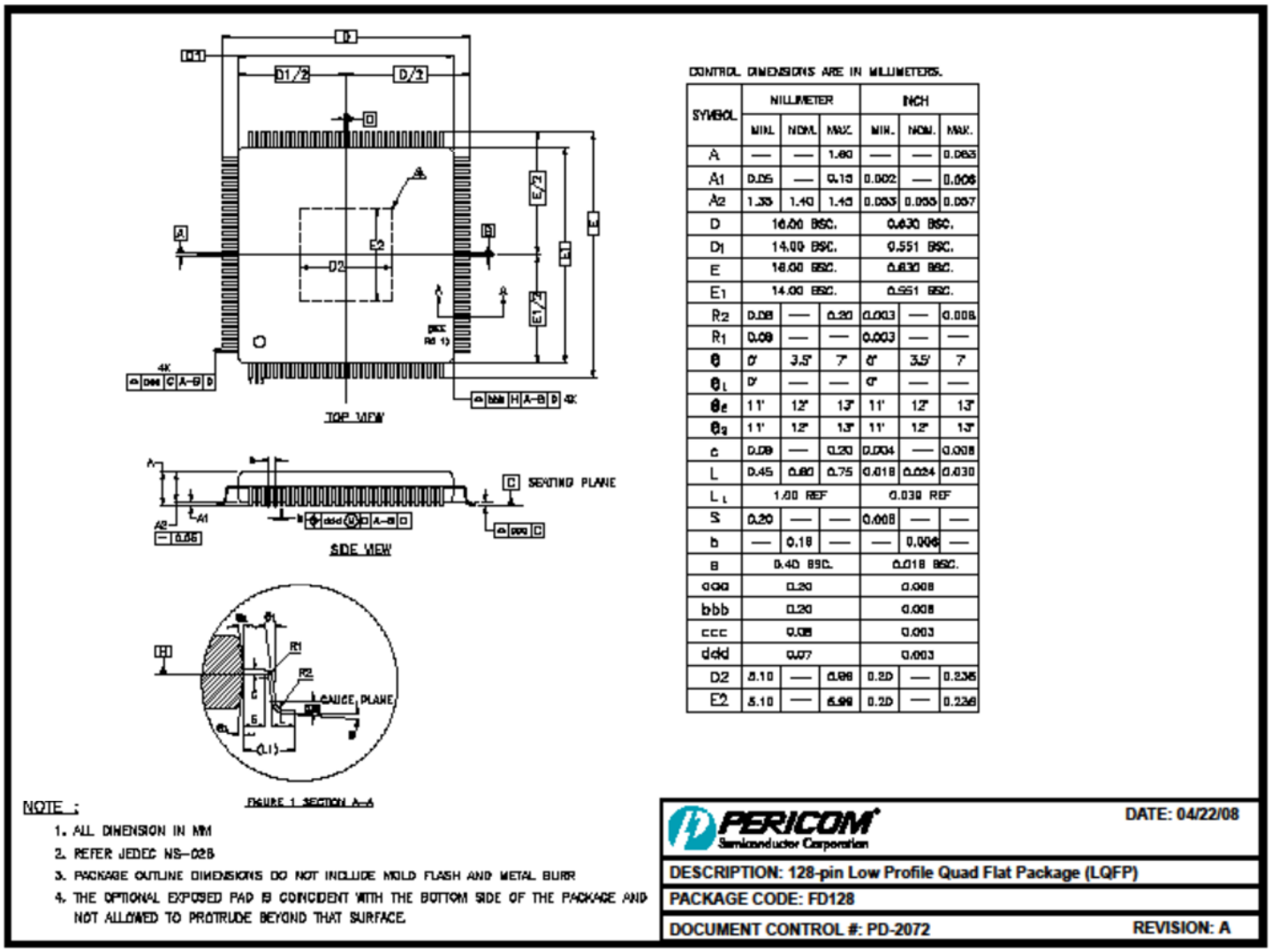
8 Packaging Mechanical



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	—	0.18	—	—	0.006	—
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		
D2	5.10	—	5.66	0.20	—	0.235
E2	5.10	—	5.66	0.20	—	0.236

NOTE :
1. ALL DIMENSION IN MM
2. REFER JEDEC MS-026
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
4. THE OPTIONAL EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE.

PERICOM Semiconductor Corporation — DATE: 04/22/08

DESCRIPTION: 128-pin Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FD128

DOCUMENT CONTROL #: PD-2072 — REVISION: A

07-0353

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

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9 Ordering Information

Ordering Code	Package Code	Package Description
PI7VD9004ABHFD	FD128(No EPAD)	128-LQFP, Pb-free & Green

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. Adding "E" = Pb-free, "I"=Industrial, "FP"=Package code, "X" suffix = Tape/Reel

10 Related Product Information

Part Number	Product Description
PI7VD9008H	8-channel 960H Video Decoder with 10-bit Audio ADC
PI7VD9004H	4-channel 960H Video Decoder with 10-bit Audio ASC
PI7C9X9208	8-channel D1 PCIe Video Decoder with 16-bit Audio ADC
PI7C9X9204S	4-channel D1 PCIe Video Decoder with 16-bit Audio ADC
PI7VD9008HEVB	PI7VD9008 Evaluation Kit
PI7VD9208HEVB	PI7VD9208 Evaluation Kit

11 Reference Document Information

Document	Description
Register Datasheet	PI7VD9004ABH Register Specification
Application Note	Reference schematic and board layout application notes

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