

## Thermally-Enhanced High Power RF LDMOS FET 50 W, 50 V, 1200 – 1400 MHz

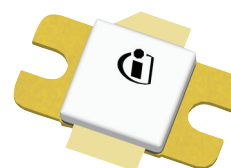
### Description

The PTVA120501EA LDMOS FET is designed for use in power amplifier applications in the 1200 to 1400 MHz frequency band. Features include high gain and thermally-enhanced package with bolt-down flange. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

**Advance Specification Data Sheets** describe products that are being considered by Infineon for development and market introduction. The target performance shown in Advance Specifications is not final and should not be used for any design activity. Please contact Infineon about the future availability of these products.

### Features

- Broadband input matching
- High gain and efficiency
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant
- Capable of withstanding a 10:1 load mismatch (all phase angles) at 50 W peak under RF pulse, 300  $\mu$ S, 10% duty cycle.



PTVA120501EA  
Package H-36265-2

### Target RF Characteristics

#### Typical Pulsed RF Performance

$V_{DD} = 50$  V,  $I_{DQ} = 50$  mA, Input signal ( $t_r = 5$  ns,  $t_f = 5$  ns),  $f_1 = 1200$  MHz,  $f_2 = 1300$  MHz,  $f_3 = 1400$  MHz, 300  $\mu$ s pulse width, 10 % duty cycle, class AB test

Test Signal	IRL (dB)	P <sub>1dB</sub>			P <sub>3dB</sub>			Max P <sub>droop</sub> (pulse) dB @ P <sub>1dB</sub>	t <sub>r</sub> (ns) @ P <sub>1dB</sub>	t <sub>f</sub> (ns) @ P <sub>1dB</sub>	Gain Flatness (dB)
		Gain (dB)	Eff (%)	P <sub>OUT</sub> (W)	Gain (dB)	Eff (%)	P <sub>OUT</sub> (W)				
300 $\mu$ s, 10%	-8.0	16.5	55	54	14.5	57	63	0.2	5	<2	1

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

## DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1	$\mu\text{A}$
	$V_{DS} = 105\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	10	$\mu\text{A}$
On-State Resistance	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.4	—	$\Omega$
Operating Gate Voltage	$V_{DS} = 50\text{ V}$ , $I_{DQ} = 50\text{ mA}$	$V_{GS}$	3.0	3.5	4.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	1	$\mu\text{A}$

## Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	105	V
Gate-Source Voltage	$V_{GS}$	−6 to +12	V
Junction Temperature	$T_J$	200	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	−65 to +150	$^{\circ}\text{C}$
Thermal Resistance	$R_{\theta JC}$	TBD	$^{\circ}\text{C/W}$

## Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTVA120501EA V1	TBD	H-36265-2, bolt-down	Tray
PTVA120501EA V1 R250	TBD	H-36265-2, bolt-down	Tape & Reel, 250 pcs

## Package Outline Specifications

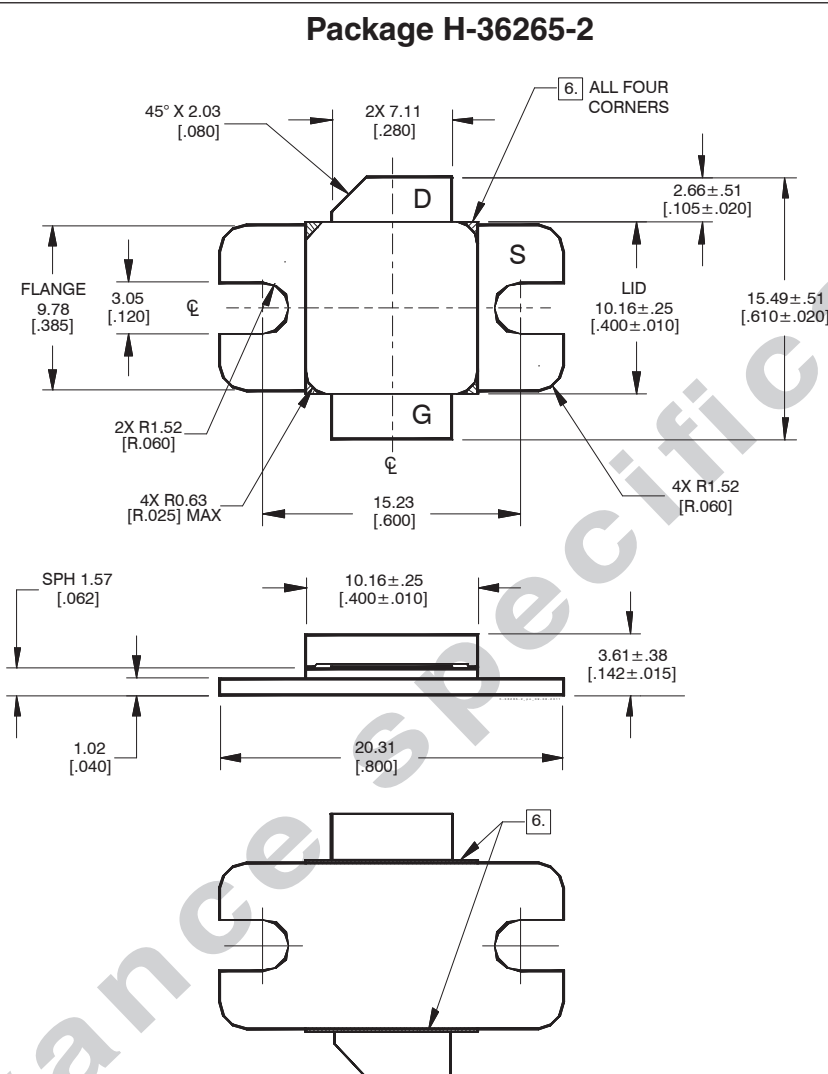


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances  $\pm 0.127$  [0.005] unless specified otherwise.
4. Pins: D – drain; G – gate; S – source
5. Lead thickness:  $0.10 + 0.051/-0.025$  mm [ $0.004 + 0.002/-0.001$  inch].
6. Exposed metal plane on top and bottom of ceramic insulator.
7. Gold plating thickness:  $1.14 \pm 0.38$  micron [ $45 \pm 15$  microinch].

Find the latest and most complete information about products and packaging at the Infineon Internet page <http://www.infineon.com/rfpower>

Page	Subjects (major changes since last revision)

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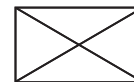
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**Edition 2013-05-29**

**Published by**

**Infineon Technologies AG**

**85579 Neubiberg, Germany**

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