FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13747-4E

*16-bit Microcontroller*

**CMOS**

# F²MC-16LX MB90340E Series

**MB90341E(S)/341CE(S)/342E(S)/342CE(S)/F342E(S)/F342CE(S)/F345E(S)/F345CE(S)/346E(S)/
MB90346CE(S)/F346E(S)/F346CE(S)/347E(S)/347CE(S)/F347E(S)/F347CE(S)/348E(S)/348CE(S)/
MB90349E(S)/349CE(S)/F349E(S)/F349CE(S)/V340E-101/V340E-102**

## ■ DESCRIPTION

The MB90340E series with up to 2 FULL-CAN interfaces is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The power to the MCU core (3 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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## ■ FEATURES

- **CPU**
  - Instruction system best suited to controller
    - Wide choice of data types (bit, byte, word, and long word)
    - Wide choice of addressing modes (23 types)
    - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
    - Enhanced high-precision computing with 32-bit accumulator
  - Instruction system compatible with high-level language (C language) and multitask
    - Employing system stack pointer
    - Various enhanced pointer indirect instructions
    - Barrel shift instructions
  - Increased processing speed
    - 4-byte instruction queue
- **Serial interface**
  - LIN-UART : 4 channels
    - Equipped with full-duplex double buffer
    - Clock-asynchronous or clock-synchronous serial transmission is available
  - $I^2C$ interface : 2 channels (only for devices with a C suffix in the part number)
    - Up to 400 kbps transfer rate
- **Interrupt controller**
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 16 external interrupts are supported
  - Automatic data transfer function independent of CPU
    - Expanded intelligent I/O service function ($EI^2OS$) : up to 16 channels
- **I/O ports**
  - General-purpose input/output port (CMOS output)
    - 80 ports (for devices without an S suffix in the part number - i.e. devices that support the sub clock)
    - 82 ports (for devices with an S suffix in the part number - i.e. devices that do not support the sub clock)
- **8/10-bit A/D converter**
  - 16 channels (only for devices without a C suffix in the part number)
  - 24 channels (only for devices with a C suffix in the part number)
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time : 3 μs (at 24 MHz machine clock, including sampling time)
- **Address match detection (program patch) function**
  - Detects address matches against 6 address pointers
- **Timer**
  - Time-base timer, watch timer, watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 16 channels, or 16-bit × 8 channels
  - 16-bit reload timer : 4 channels
  - 16-bit input/output timer
    - 16-bit free-run timer : 2 channels
    (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
    - 16-bit input capture: (ICU): 8 channels
    - 16-bit output compare: (OCU): 8 channels

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- **Full-CAN controller**
  - Up to 2 channels
  - Compliant with Ver2.0A and Ver2.0B CAN specifications
  - 16 built-in message buffers
  - CAN wake-up function
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
  - Watch mode (a mode that operates sub clock and watch timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU intermittent operation mode
- **Clock modulation circuit**
- **Technology**
  - CMOS technology



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## ■ PRODUCT LINEUP

| Part Number / Parameter | MB90V340E-101, MB90V340E-102 | MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
|---|---|---|---|
| Type | Evaluation products | Flash memory products | MASK ROM products |
| CPU | F²MC-16LX CPU | | |
| System clock | On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6) | | |
| ROM | External | 512 Kbytes :<br>MB90F345E(S), MB90F345CE(S)<br>256 Kbytes :<br>MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S)<br>128 Kbytes :<br>MB90F347E(S), MB90F347CE(S)<br>64 Kbytes :<br>MB90F346E(S), MB90F346CE(S) | 256 Kbytes :<br>MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S)<br>128 Kbytes :<br>MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S)<br>64 Kbytes :<br>MB90346E(S), MB90346CE(S) |
| RAM | 30 Kbytes | 20 Kbytes :<br>MB90F345E(S), MB90F345CE(S)<br>16 Kbytes :<br>MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S)<br>6 Kbytes :<br>MB90F347E(S), MB90F347CE(S)<br>2 Kbytes :<br>MB90F346E(S), MB90F346CE(S) | 16 Kbytes :<br>MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)<br>6 Kbytes :<br>MB90347E(S), MB90347CE(S)<br>2 Kbytes :<br>MB90346E(S), MB90346CE(S) |
| Emulator-specific power supply* | Yes | — | |
| Technology | 0.35 µm CMOS with regulator for built-in power supply | 0.35 µm CMOS with built-in power supply regulator +<br>Flash memory with Charge pump for programming voltage | |
| Operating voltage range | 5 V ± 10% | 3.5 V to 5.5 V : When normal operating (not using A/D converter)<br>4.0 V to 5.5 V : When using the A/D converter/Flash programming<br>4.5 V to 5.5 V : When using the external bus | |
| Temperature range | — | −40 °C to +105 °C | |
| Package | PGA-299 | QFP-100, LQFP-100 | |
| LIN-UART | 5 channels | 4 channels | |
| | Wide range of baud rate settings using a dedicated baud rate generator (reload timer)<br>Special synchronous options for adapting to different synchronous serial protocols<br>LIN functionality working either as master or slave LIN device | | |
| I²C (400 kbps) | 2 channels | Devices with a C suffix in the part number : 2 channels<br>Devices without a C suffix in the part number : — | |

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| Parameter \ Part Number | MB90V340E-101, MB90V340E-102 | MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
|---|---|---|---|
| A/D Converter | 24 input channels | Devices with a C suffix in the part number : 24 channels<br>Devices without a C suffix in the part number : 16 channels | |
| | 10-bit or 8-bit resolution<br>Conversion time : Min 3 µs include sample time (per one channel) | | |
| 16-bit Reload Timer (4 channels) | Operation clock frequency : fsys/$2^1$, fsys/$2^3$, fsys/$2^5$ (fsys = Machine clock frequency)<br>Supports External Event Count function | | |
| 16-bit Free-run Timer (2 channels) | Generates an interrupt signal on overflow<br>Supports Timer Clear when the output compare finds a match<br>Operation clock freq. : fsys, fsys/$2^1$, fsys/$2^2$, fsys/$2^3$, fsys/$2^4$, fsys/$2^5$, fsys/$2^6$, fsys/$2^7$<br>(fsys = Machine clock freq.)<br>Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3<br>Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7 | | |
| 16-bit Output Compare (8 channels) | Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register<br>A pair of compare registers can be used to generate an output signal. | | |
| 16-bit Input Capture (8 channels) | Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges). | | |
| 8/16-bit Programmable Pulse Generator | 8 channels (16-bit) /16 channels (8-bit)<br>Sixteen 8-bit reload counters<br>Sixteen 8-bit reload registers for L pulse width<br>Sixteen 8-bit reload registers for H pulse width | | |
| | Supports 8-bit and 16-bit operation modes<br>A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter<br>Operating clock freq. : fsys, fsys/$2^1$, fsys/$2^2$, fsys/$2^3$, fsys/$2^4$ or 128 µs@fosc = 4 MHz<br>(fsys = Machine clock frequency, fosc = Oscillation clock frequency) | | |
| CAN Interface | 3 channels | 2 channels :<br>MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S)<br>1 channel :<br>MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | 2 channels :<br>MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S)<br>1 channel :<br>MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
| | Conforms to CAN Specification Version 2.0 Part A and B<br>Automatic re-transmission in case of error<br>Automatic transmission in response to Remote Frames<br>Prioritized 16 message buffers for data and ID's<br>Supports multiple messages<br>Flexible configuration of acceptance filtering :<br>Full bit compare/Full bit mask/Two partial bit masks<br>Supports up to 1 Mbps | | |

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| Part Number / Parameter | MB90V340E-101, MB90V340E-102 | MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
|---|---|---|---|
| External Interrupt (16 channels) | Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI$^2$OS) and DMA | | |
| D/A Converter | 2 channels | — | |
| Sub clock (maximum 100 kHz) | Only for MB90V340E-102 | Devices with sub clock : devices without an S suffix in the part number<br>Devices without sub clock : devices with an S suffix in the part number | |
| I/O Ports | Virtually all external pins can be used as general purpose I/O port<br>All ports are push-pull outputs<br>Bit-wise settable as input/output or peripheral signal<br>Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins)<br>TTL input level settable for external bus (32-pin only for external bus) | | |
| Flash Memory | — | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of erase cycles : 10000 cycles<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S) ) | |

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01-E) is used.
Please refer to the Emulator operation manual for details.

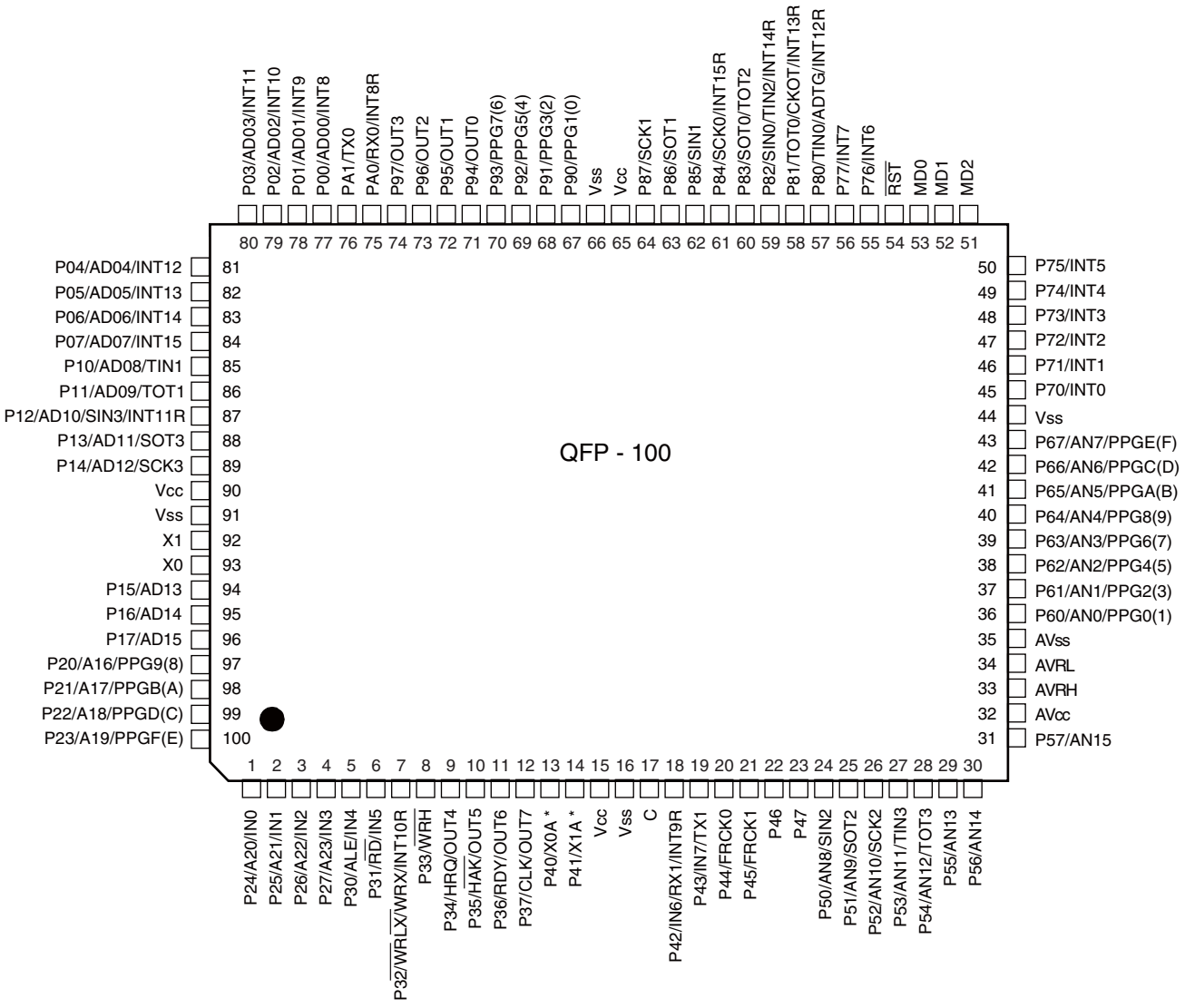


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## ■ PIN ASSIGNMENTS

- MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)

(TOP VIEW)




(FPT-100P-M06)

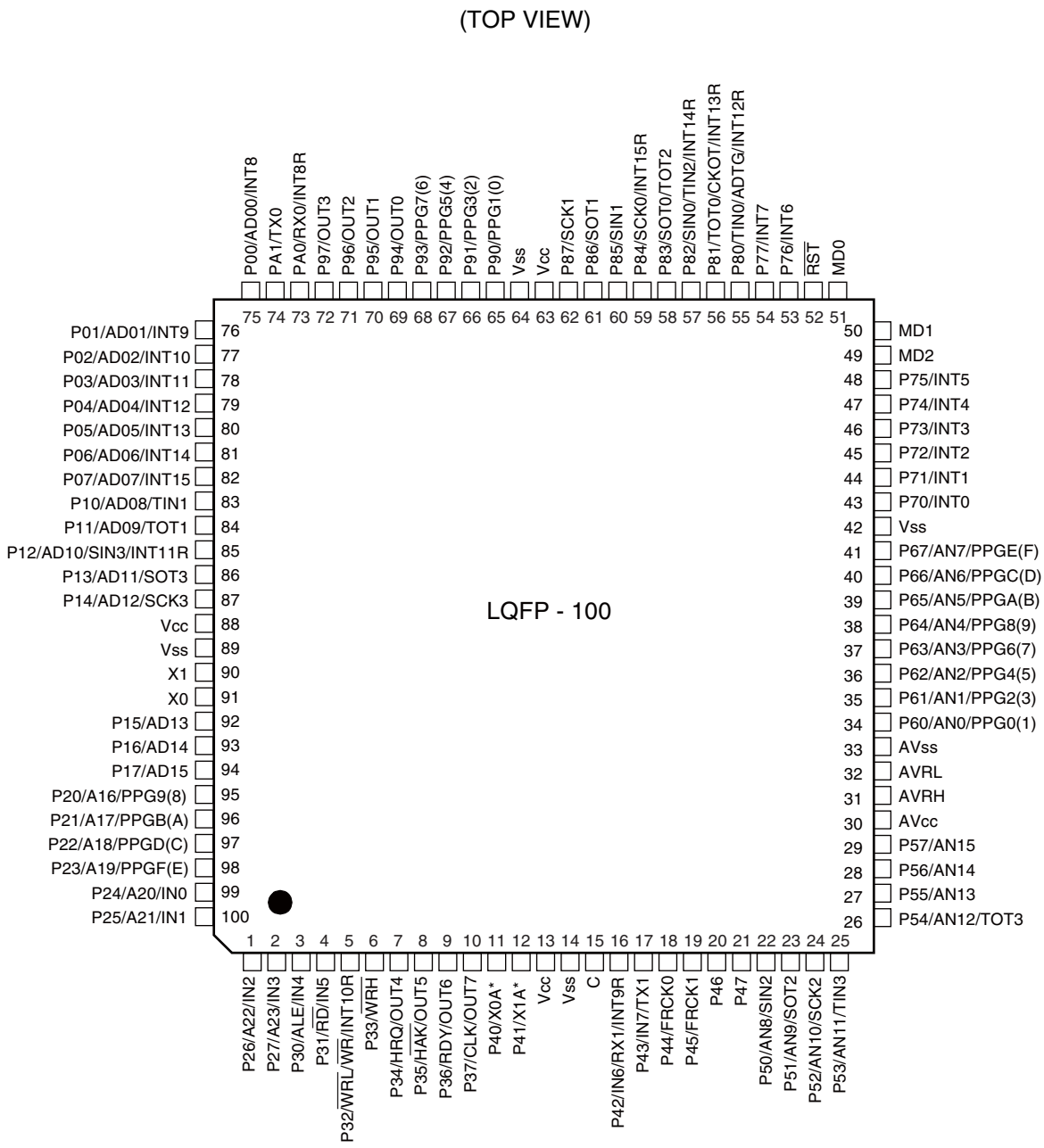
* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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(FPT-100P-M20)

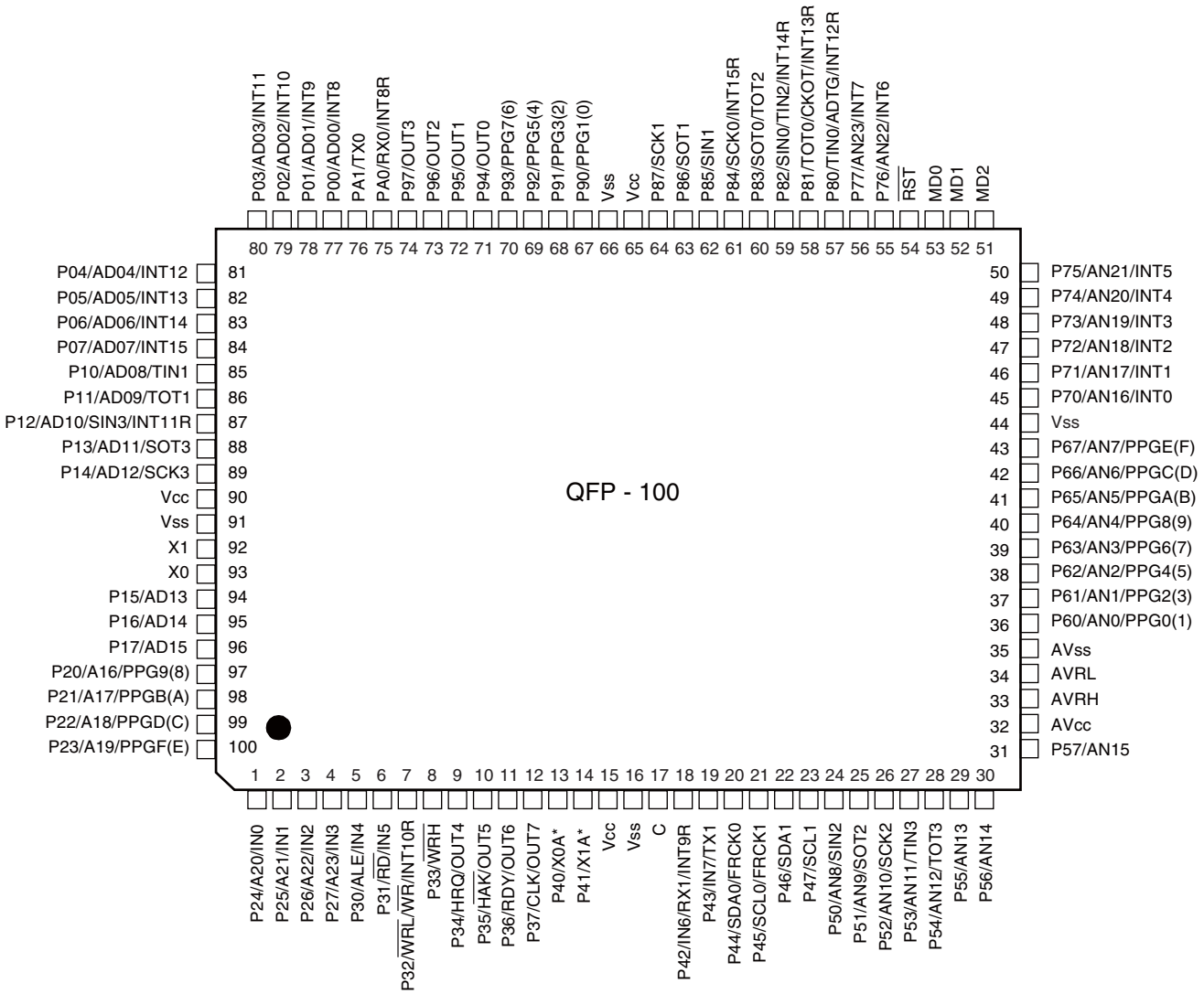
* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number



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- MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

(TOP VIEW)




(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

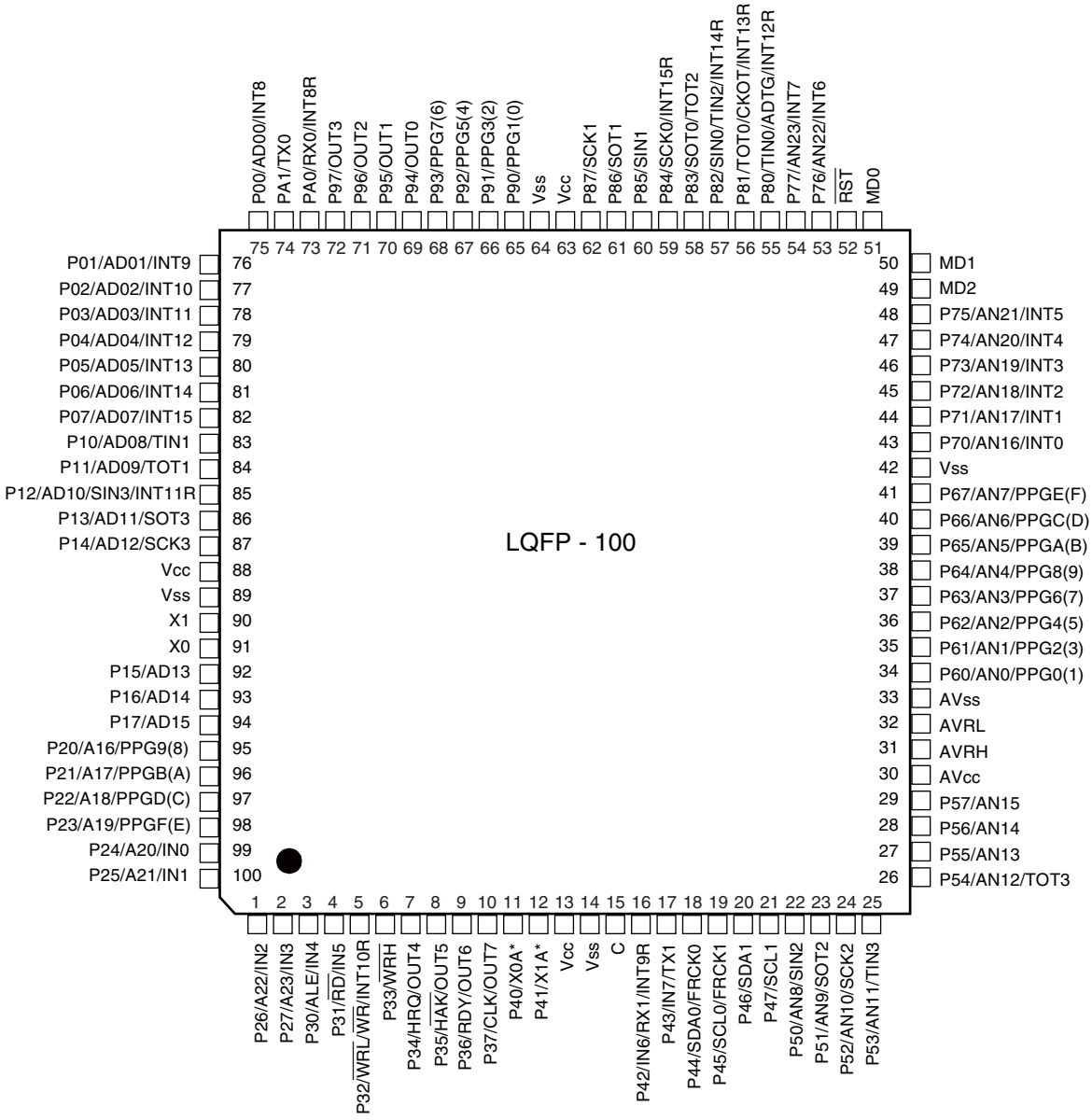
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(TOP VIEW)



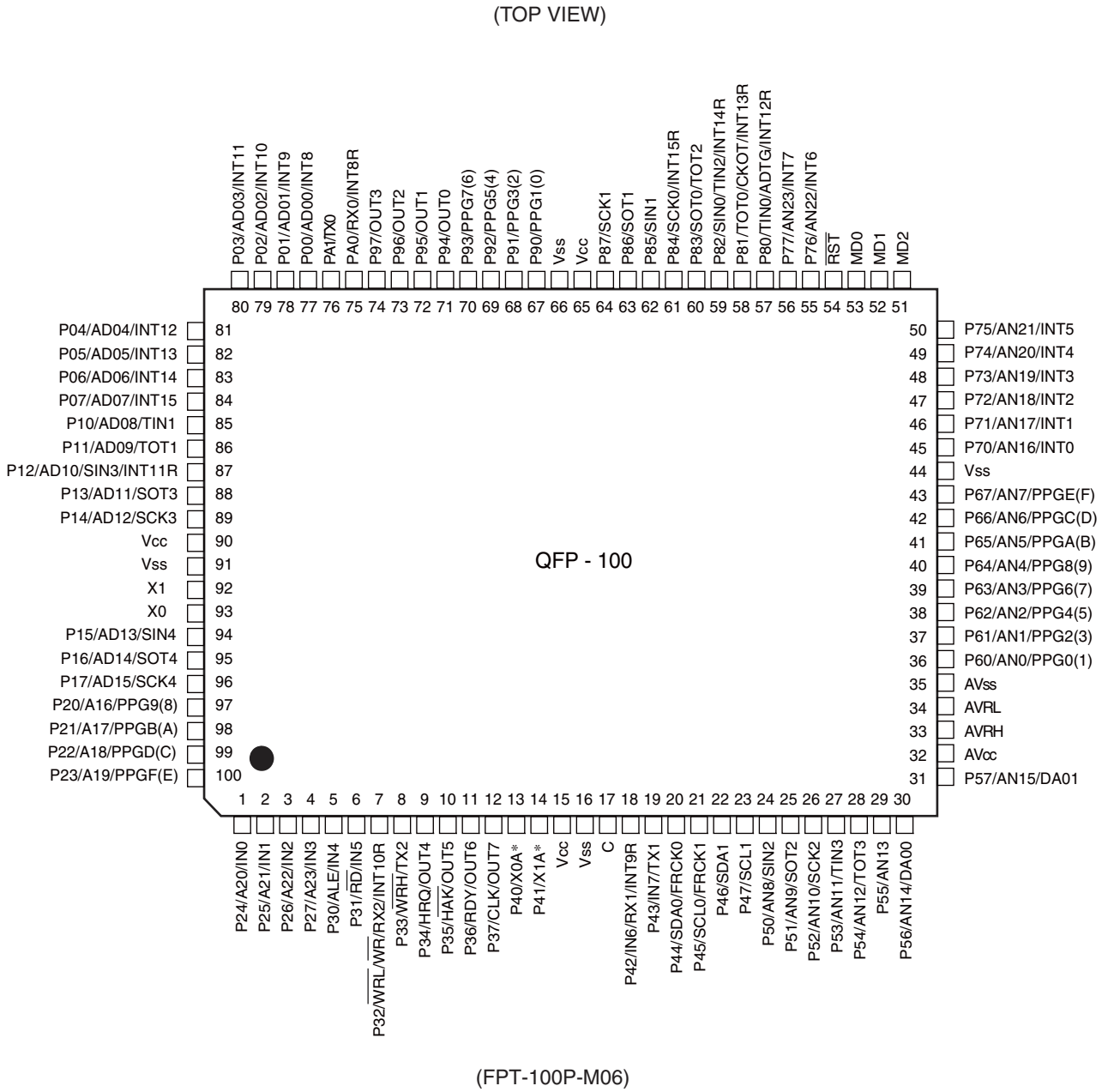

(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number



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• MB90V340E-101/MB90V340E-102




(FPT-100P-M06)

*: X0A, X1A : MB90V340E-102
P40, P41 : MB90V340E-101

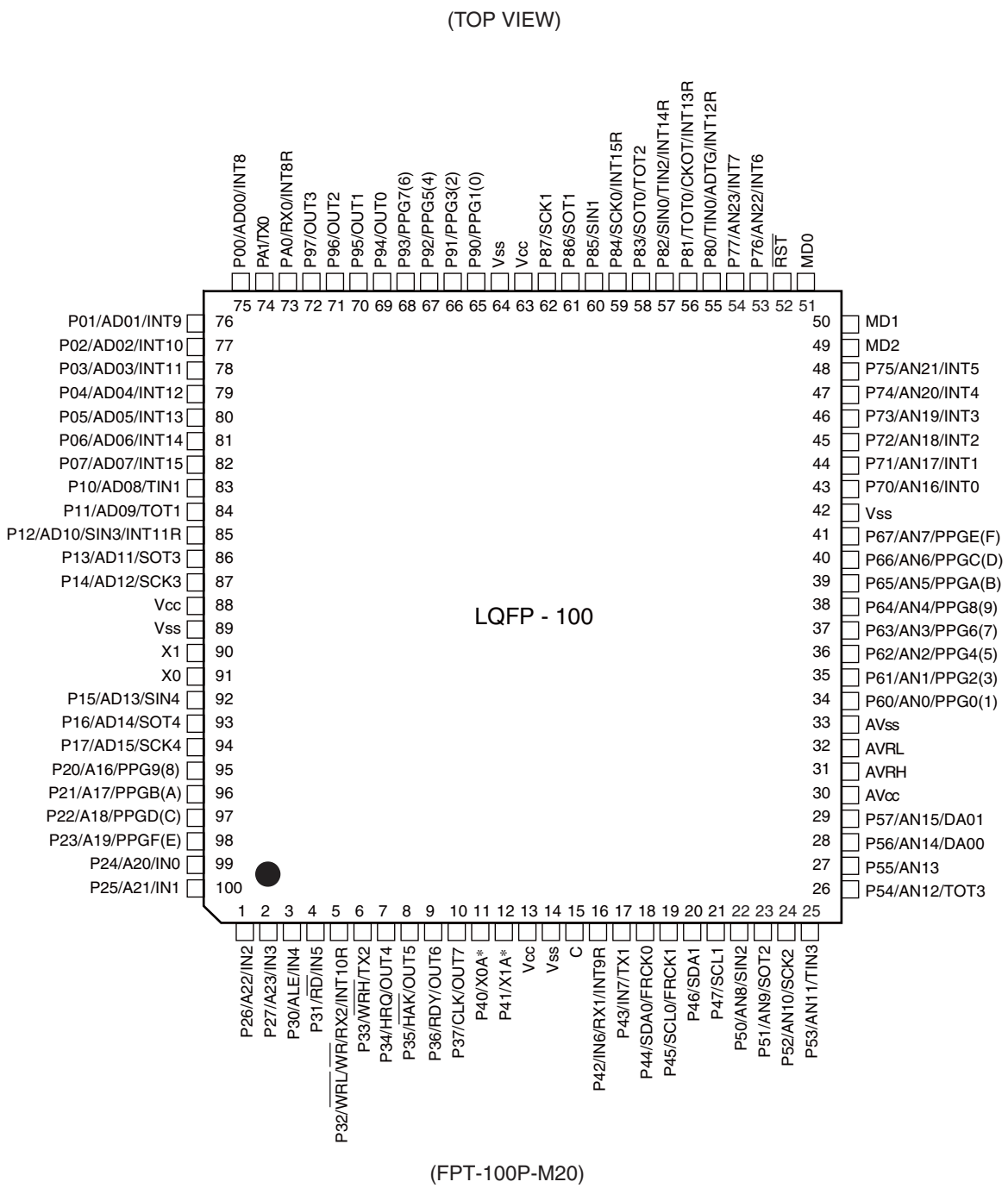
This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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* : X0A, X1A : MB90V340E-102
P40, P41 : MB90V340E-101

This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.



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## ■ PIN DESCRIPTION

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 1 to 4 | 99 to 2 | P24 to P27 | G | General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | | A20 to A23 | | Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23). |
| | | IN0 to IN3 | | Trigger input pins for input captures. |
| 5 | 3 | P30 | G | General purpose I/O pin.The register can be set to select whether to use a pull-up resistor.<br>This function is enabled in single-chip mode. |
| | | ALE | | Address latch enable output pin. This function is enabled when the external bus is enabled. |
| | | IN4 | | Trigger input pin for input capture. |
| 6 | 4 | P31 | G | General purpose I/O pin.The register can be set to select whether to use a pull-up resistor.<br>This function is enabled in single-chip mode. |
| | | $\overline{RD}$ | | External read strobe output pin. This function is enabled when the external bus is enabled. |
| | | IN5 | | Trigger input pin for input capture. |
| 7 | 5 | P32 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR}$/$\overline{WRL}$ pin output is disabled. |
| | | $\overline{WR}$ / $\overline{WRL}$ | | Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access. |
| | | INT10R | | External interrupt request input pin. |
| 8 | 6 | P33 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output is disabled. |
| | | $\overline{WRH}$ | | Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled. |

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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 9 | 7 | P34 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | HRQ | | Hold request input pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT4 | | Waveform output pin for output compare. |
| 10 | 8 | P35 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | $\overline{\text{HAK}}$ | | Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT5 | | Waveform output pin for output compare. |
| 11 | 9 | P36 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled. |
| | | RDY | | External ready input pin. This function is enabled when both the external bus and the external ready function are enabled. |
| | | OUT6 | | Waveform output pin for output compare. |
| 12 | 10 | P37 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled. |
| | | CLK | | Clock output pin. This function is enabled when both the external bus and clock output are enabled. |
| | | OUT7 | | Waveform output pin for output compare |
| 13, 14 | 11, 12 | P40, P41 | F | General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101) |
| | | X0A, X1A | B | Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102) |
| 15 | 13 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 16 | 14 | $V_{SS}$ | — | GND pin |
| 17 | 15 | C | K | This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF. |
| 18 | 16 | P42 | F | General purpose I/O pin. |
| | | IN6 | | Trigger input pin for input capture. |
| | | RX1 | | RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only) |
| | | INT9R | | External interrupt request input pin |

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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 19 | 17 | P43 | F | General purpose I/O pin. |
| | | IN7 | | Trigger input pin for input capture. |
| | | TX1 | | TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only) |
| 20 | 18 | P44 | H | General purpose I/O pin. |
| | | SDA0 | | Serial data I/O pin for I²C (devices with a C suffix in the part number) |
| | | FRCK0 | | Input pin for the 16-bit Free-run Timer 0 |
| 21 | 19 | P45 | H | General purpose I/O pin. |
| | | SCL0 | | Serial clock I/O pin for I²C (devices with a C suffix in the part number) |
| | | FRCK1 | | Input pin for the 16-bit Free-run Timer |
| 22 | 20 | P46 | H | General purpose I/O pin. |
| | | SDA1 | | Serial data I/O pin for I²C (devices with a C suffix in the part number) |
| 23 | 21 | P47 | H | General purpose I/O pin. |
| | | SCL1 | | Serial clock I/O pin for I²C (devices with a C suffix in the part number) |
| 24 | 22 | P50 | O | General purpose I/O pin. |
| | | AN8 | | Analog input pin for the A/D converter |
| | | SIN2 | | Serial data input pin for UART2 |
| 25 | 23 | P51 | I | General purpose I/O pin. |
| | | AN9 | | Analog input pin for the A/D converter |
| | | SOT2 | | Serial data output pin for UART2 |
| 26 | 24 | P52 | I | General purpose I/O pin. |
| | | AN10 | | Analog input pin for the A/D converter |
| | | SCK2 | | Clock I/O pin for UART2 |
| 27 | 25 | P53 | I | General purpose I/O pin. |
| | | AN11 | | Analog input pin for the A/D converter |
| | | TIN3 | | Event input pin for the reload timer |
| 28 | 26 | P54 | I | General purpose I/O pin. |
| | | AN12 | | Analog input pin for the A/D converter |
| | | TOT3 | | Output pin for the reload timer |
| 29 | 27 | P55 | I | General purpose I/O pin. |
| | | AN13 | | Analog input pin for the A/D converter |
| 30, 31 | 28, 29 | P56, P57 | J | General purpose I/O pins. |
| | | AN14, AN15 | | Analog input pins for the A/D converter |
| 32 | 30 | $AV_{CC}$ | K | Analog power input pin for the A/D Converter |

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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 33 | 31 | AVRH | L | Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AVCC. |
| 34 | 32 | AVRL | K | Lower reference voltage input pin for the A/D Converter |
| 35 | 33 | AVSS | K | Analog GND pin for the A/D Converter |
| 36 to 43 | 34 to 41 | P60 to P67 | I | General purpose I/O pins. |
| | | AN0 to AN7 | | Analog input pins for the A/D converter |
| | | PPG0, 2, 4, 6, 8, A, C, E | | Output pins for PPGs |
| 44 | 42 | VSS | — | GND pin |
| 45 to 50 | 43 to 48 | P70 to P75 | I | General purpose I/O pins. |
| | | AN16 to AN21 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT0 to INT5 | | External interrupt request input pins |
| 51 | 49 | MD2 | D | Input pin for specifying the operating mode. |
| 52, 53 | 50, 51 | MD1, MD0 | C | Input pins for specifying the operating mode. |
| 54 | 52 | $\overline{RST}$ | E | Reset input pin |
| 55, 56 | 53, 54 | P76, P77 | I | General purpose I/O pins. |
| | | AN22, AN23 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT6, INT7 | | External interrupt request input pins |
| 57 | 55 | P80 | F | General purpose I/O pin. |
| | | TIN0 | | Event input pin for the reload timer |
| | | ADTG | | Trigger input pin for the A/D converter |
| | | INT12R | | External interrupt request input pin |
| 58 | 56 | P81 | F | General purpose I/O pin. |
| | | TOT0 | | Output pin for the reload timer |
| | | CKOT | | Output pin for the clock monitor |
| | | INT13R | | External interrupt request input pin |
| 59 | 57 | P82 | M | General purpose I/O pin. |
| | | SIN0 | | Serial data input pin for UART0 |
| | | TIN2 | | Event input pin for the reload timer |
| | | INT14R | | External interrupt request input pin |
| 60 | 58 | P83 | F | General purpose I/O pin. |
| | | SOT0 | | Serial data output pin for UART0 |
| | | TOT2 | | Output pin for the reload timer |

*(Continued)*



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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 61 | 59 | P84 | F | General purpose I/O pin. |
| | | SCK0 | | Clock I/O pin for UART0 |
| | | INT15R | | External interrupt request input pin |
| 62 | 60 | P85 | M | General purpose I/O pin. |
| | | SIN1 | | Serial data input pin for UART1 |
| 63 | 61 | P86 | F | General purpose I/O pin. |
| | | SOT1 | | Serial data output pin for UART1 |
| 64 | 62 | P87 | F | General purpose I/O pin. |
| | | SCK1 | | Clock I/O pin for UART1 |
| 65 | 63 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 66 | 64 | $V_{SS}$ | — | GND pin |
| 67 to 70 | 65 to 68 | P90 to P93 | F | General purpose I/O pins |
| | | PPG1, 3, 5, 7 | | Output pins for PPGs |
| 71 to 74 | 69 to 72 | P94 to P97 | F | General purpose I/O pins |
| | | OUT0 to OUT3 | | Waveform output pins for output compares. This function is enabled when the OCU enables waveform output. |
| 75 | 73 | PA0 | F | General purpose I/O pin. |
| | | RX0 | | RX input pin for CAN0 Interface |
| | | INT8R | | External interrupt request input pin |
| 76 | 74 | PA1 | F | General purpose I/O pin. |
| | | TX0 | | TX Output pin for CAN0 |
| 77 to 84 | 75 to 82 | P00 to P07 | G | General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD00 to AD07 | | I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | INT8 to INT15 | | External interrupt request input pins. |
| 85 | 83 | P10 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD08 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | TIN1 | | Event input pin for the reload timer |

*(Continued)*



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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 86 | 84 | P11 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD09 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | TOT1 | | Output pin for the reload timer |
| 87 | 85 | P12 | N | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD10 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SIN3 | | Serial data input pin for UART3 |
| | | INT11R | | External interrupt request input pin |
| 88 | 86 | P13 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD11 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SOT3 | | Serial data output pin for UART3 |
| 89 | 87 | P14 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD12 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SCK3 | | Clock I/O pin for UART3 |
| 90 | 88 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 91 | 89 | $V_{SS}$ | — | GND pin |
| 92 | 90 | X1 | A | Main clock output pin |
| 93 | 91 | X0 | | Main clock input pin |
| 94 | 92 | P15 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD13 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| 95 | 93 | P16 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD14 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |

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| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 96 | 94 | P17 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD15 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| 97 to 100 | 95 to 98 | P20 to P23 | G | General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | | A16 to A19 | | Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19). |
| | | PPG9,PPGB, PPGD,PPGF | | Output pins for PPGs |

*1 : FPT-100P-M06

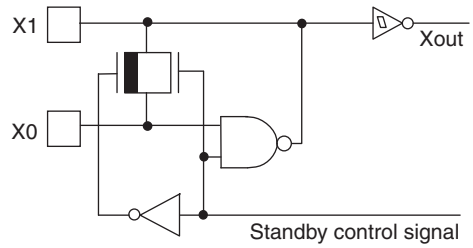
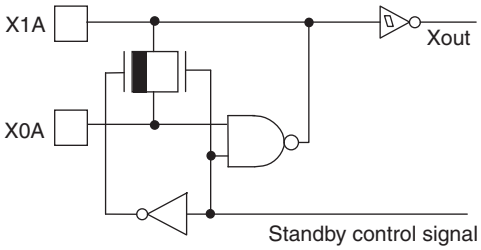
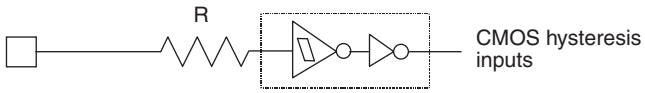
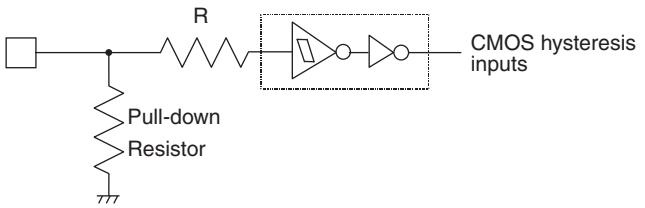
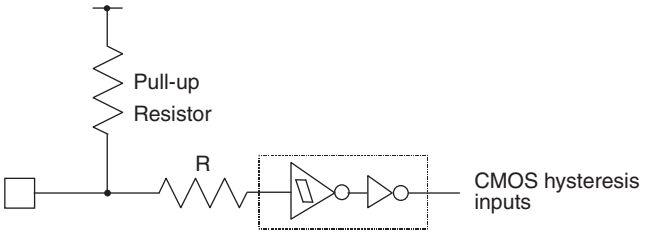
*2 : FPT-100P-M20

*3 : For I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.



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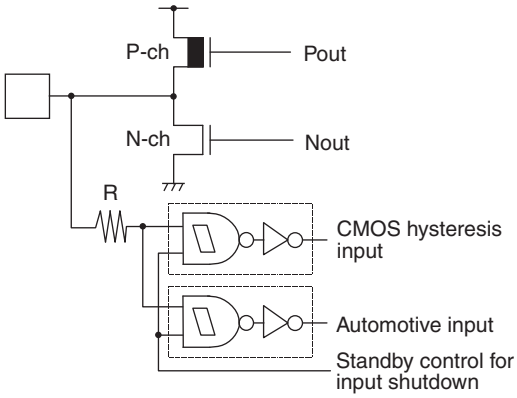
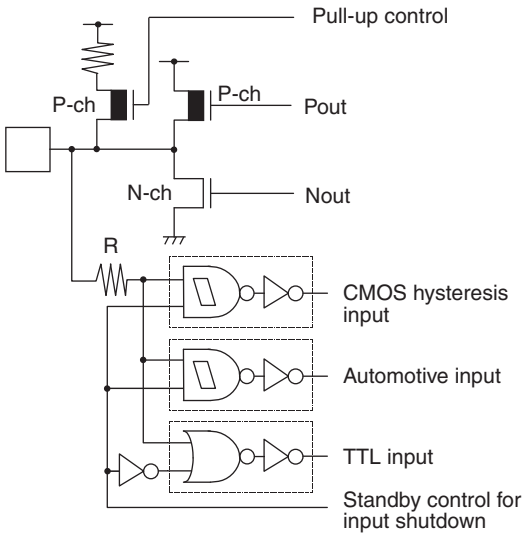
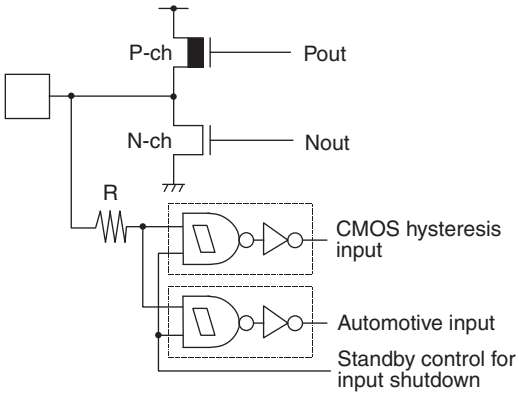
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>High-speed oscillation feedback resistor = approx. 1 MΩ |
| B |  | Oscillation circuit<br>Low-speed oscillation feedback resistor = approx. 10 MΩ |
| C |  | • MASK ROM and evaluation products: CMOS hysteresis input pin<br>• Flash memory products: CMOS input pin |
| D |  | MASK ROM and evaluation products:<br>• CMOS hysteresis input pin<br>• Pull-down resistor value: approx. 50 kΩ<br>Flash memory products:<br>• CMOS input pin<br>• No pull-down |
| E |  | CMOS hysteresis input pin<br>Pull-up resistor value: approx. 50 kΩ |

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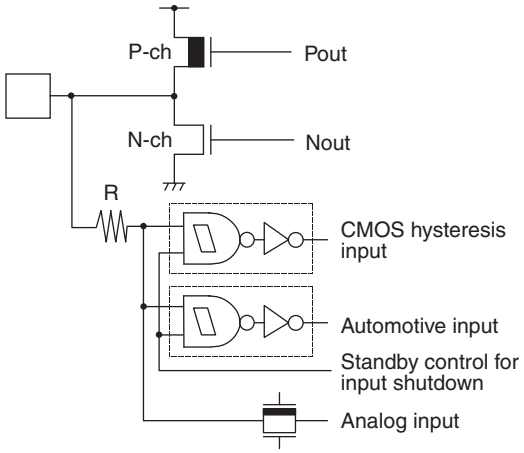
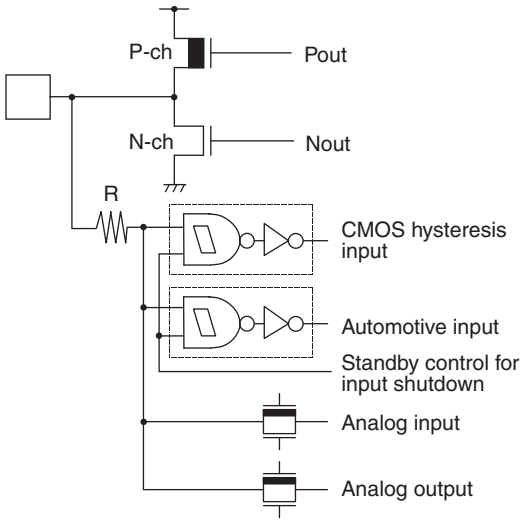
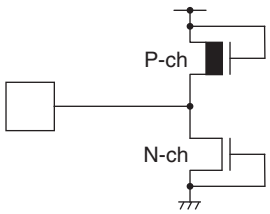
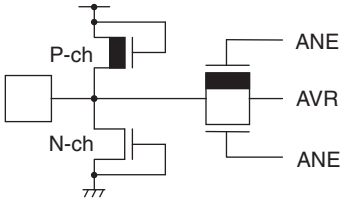
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| Type | Circuit | Remarks |
|---|---|---|
| F |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby) |
| G |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby)<br>• TTL input (with function to disconnect input during standby)<br>• Programmable pull-up resistor: 50 kΩ approx. |
| H |  | • CMOS level output ($I_{OL}$ = 3 mA, $I_{OH}$ = –3 mA)<br>• CMOS hysteresis input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby) |

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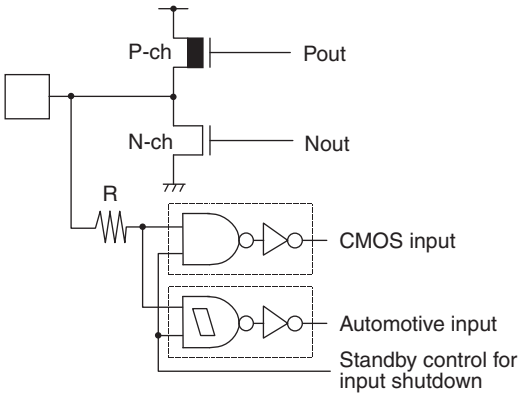
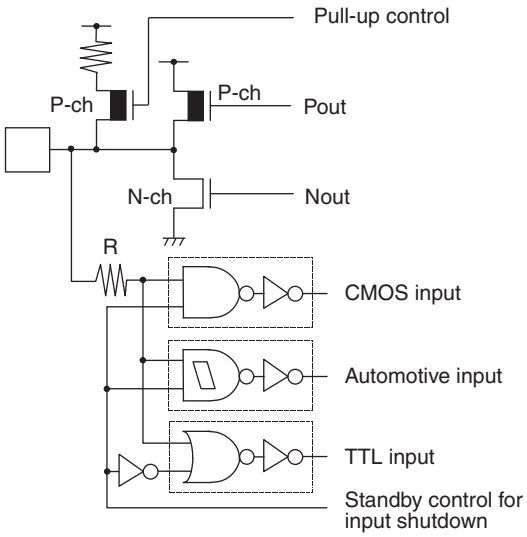
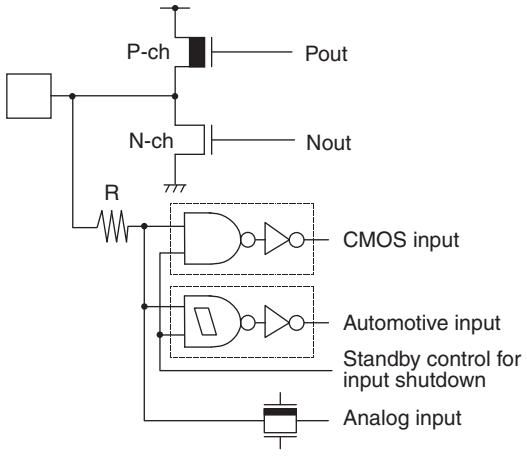
| Type | Circuit | Remarks |
|---|---|---|
| I |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby)<br>• A/D converter analog input |
| J |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• D/A analog output<br>• CMOS hysteresis input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby)<br>• A/D converter analog input |
| K |  | Power supply input protection circuit |
| L |  | • A/D converter reference voltage power supply input pin, with the protection circuit<br>• Flash memory devices do not have a protection circuit against $V_{CC}$ for pin AVRH |

*(Continued)*



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*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| M |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby) |
| N |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby)<br>• TTL input (with function to disconnect input during standby)<br>Programmable pull-up resistor: 50 kΩ approx |
| O |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS input (with function to disconnect input during standby)<br>• Automotive input (with function to disconnect input during standby)<br>• A/D converter analog input |



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## ■ HANDLING DEVICES

### 1. Preventing latch-up

**CMOS IC may suffer latch-up under the following conditions:**

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ and $V_{SS}$ pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

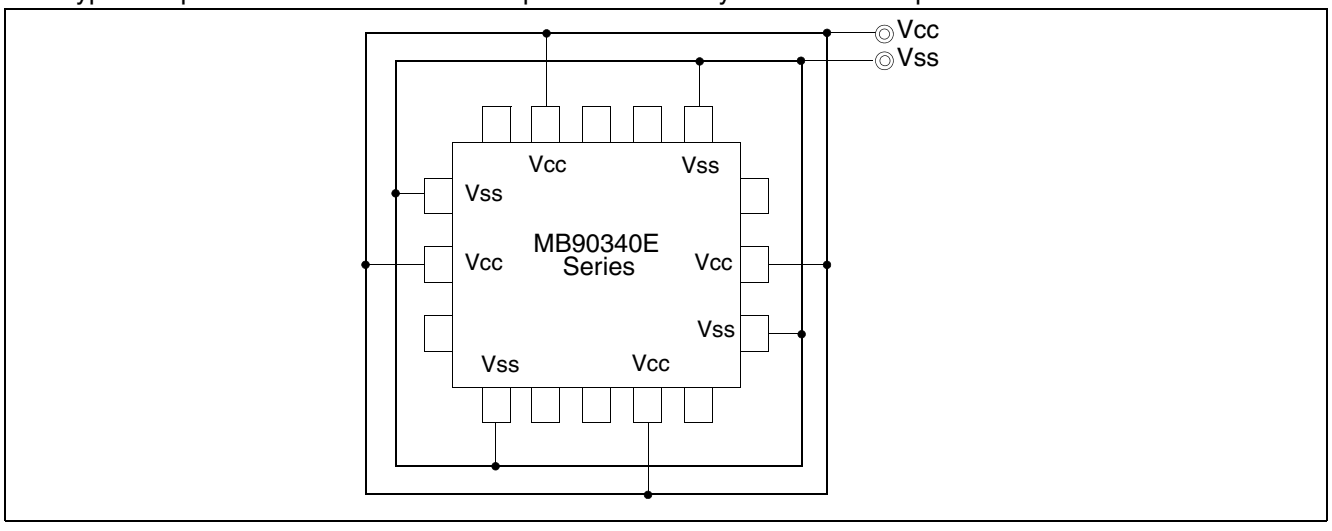
For the same reason, also be careful not to let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

### 2. Handling unused pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

### 3. Power supply pins ($V_{CC}$/$V_{SS}$)

- If there are multiple $V_{CC}$ and $V_{SS}$ pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the $V_{CC}$ and $V_{SS}$ pins to the power supply and ground externally.
  Connect $V_{CC}$ and $V_{SS}$ pins to the device from the current supply source at a possibly low impedance.
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between $V_{CC}$ and $V_{SS}$ pins in the vicinity of $V_{CC}$ and $V_{SS}$ pins of the device.




### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to $V_{CC}$ or $V_{SS}$ pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to $V_{CC}$ or $V_{SS}$ pins and to provide a low-impedance connection.



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## 5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply ($V_{CC}$).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS}$ = AVRH = AVRL = $V_{SS}$.

## 7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

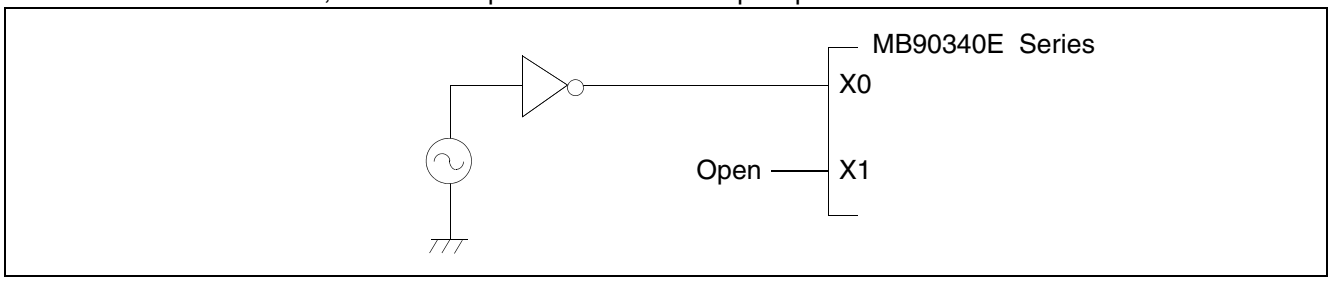
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

## 8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

## 9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.




## 10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

## 11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 µs or more (0.2 V to 2.7 V)



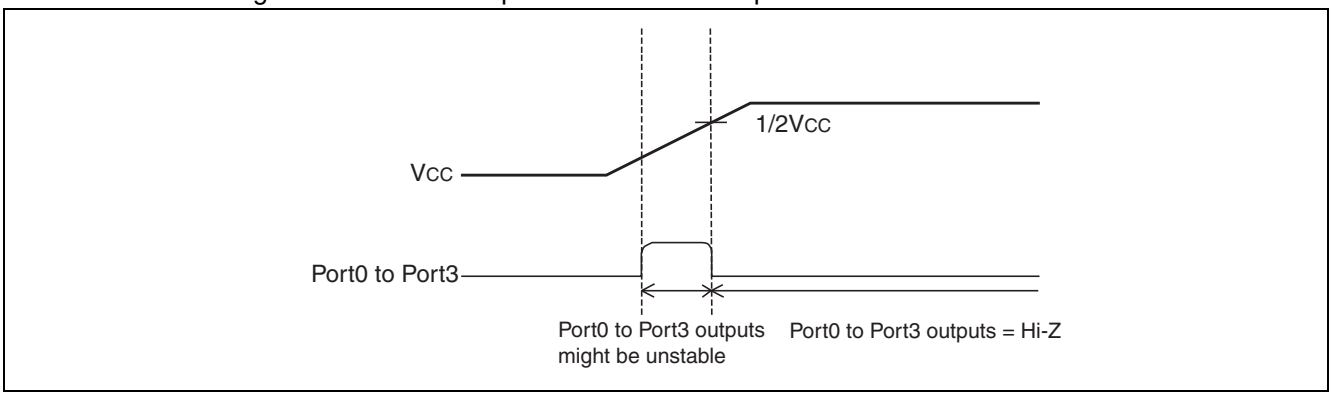
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## 13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the $V_{CC}$ supply voltage operating range. Therefore, the $V_{CC}$ supply voltage should be stabilized. For reference, the supply voltage should be controlled so that $V_{CC}$ ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard $V_{CC}$ supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

## 14. Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.




## 15. Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

## 16. Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.
If protection code $01_H$ is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write $01_H$ in this address if you do not use the security function.
Refer to following table for the address of the security bit.

| | Flash memory size | Address of the security bit |
|---|---|---|
| MB90F347E | Embedded 1 Mbit Flash Memory | $FE0001_H$ |
| MB90F342E<br>MB90F349E | Embedded 2 Mbits Flash Memory | $FC0001_H$ |
| MB90F345E | Embedded 4 Mbits Flash Memory | $F80001_H$ |

## 17. Serial Communication

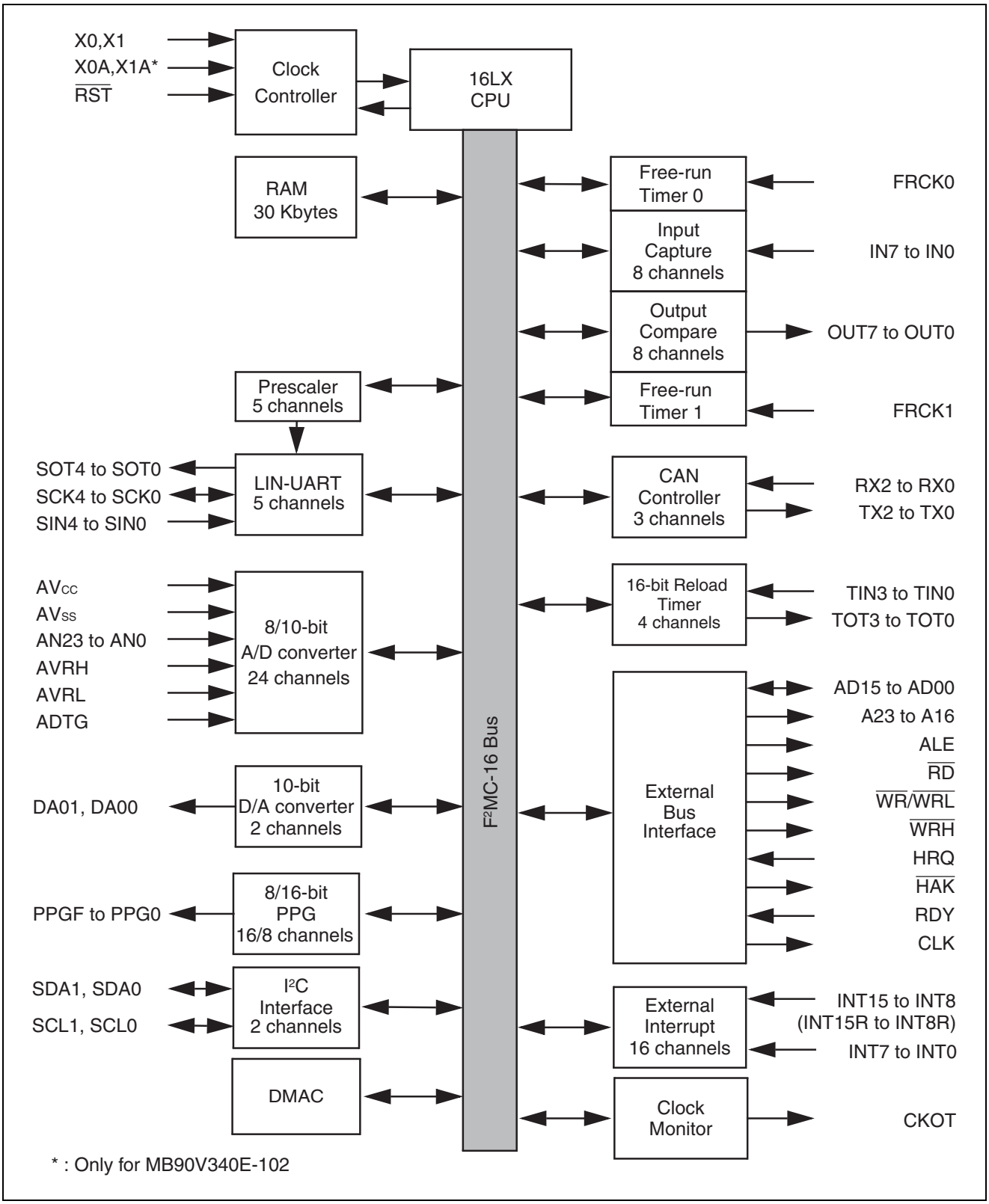
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.



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## ■ BLOCK DIAGRAMS

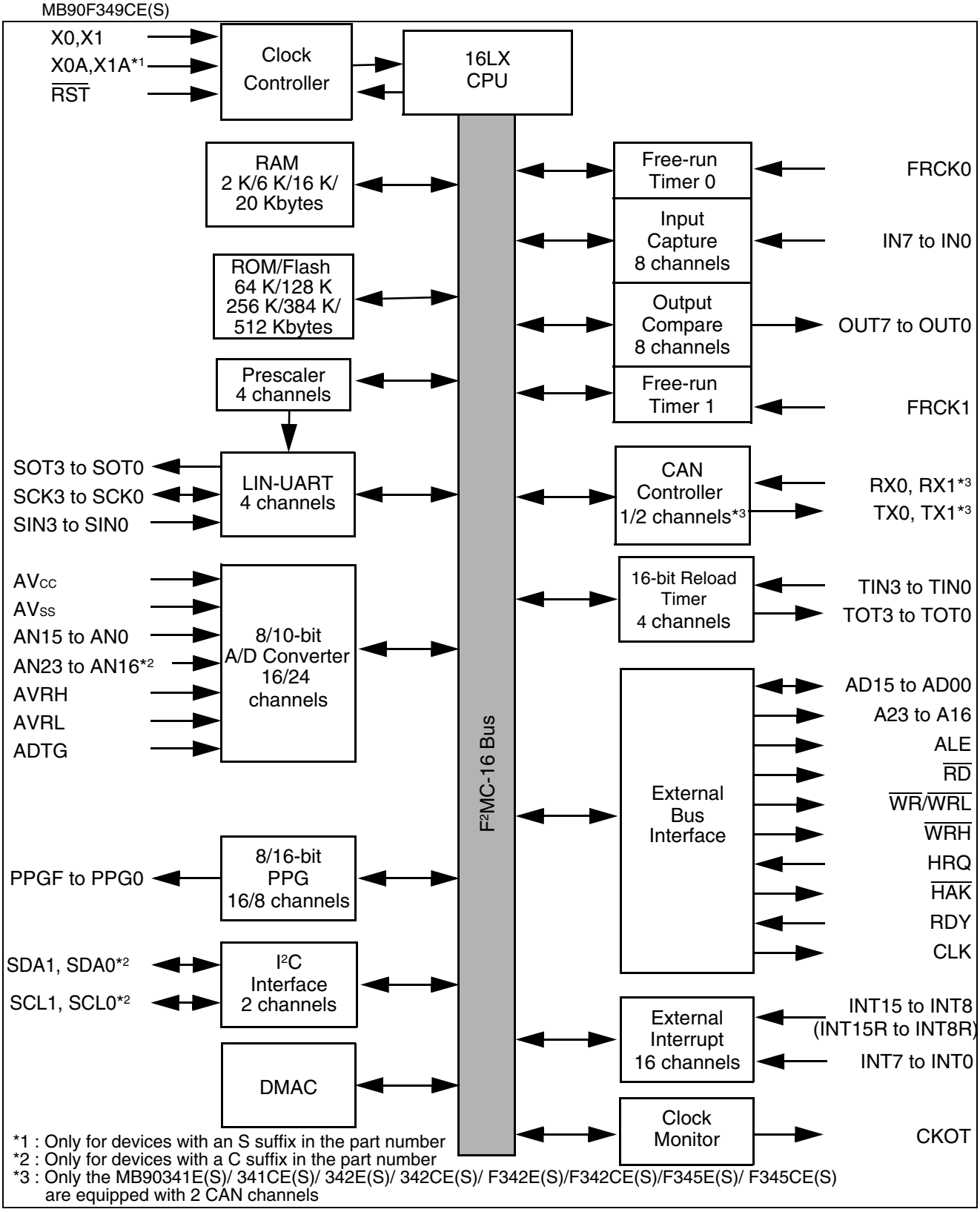
- MB90V340E-101/102






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- MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)

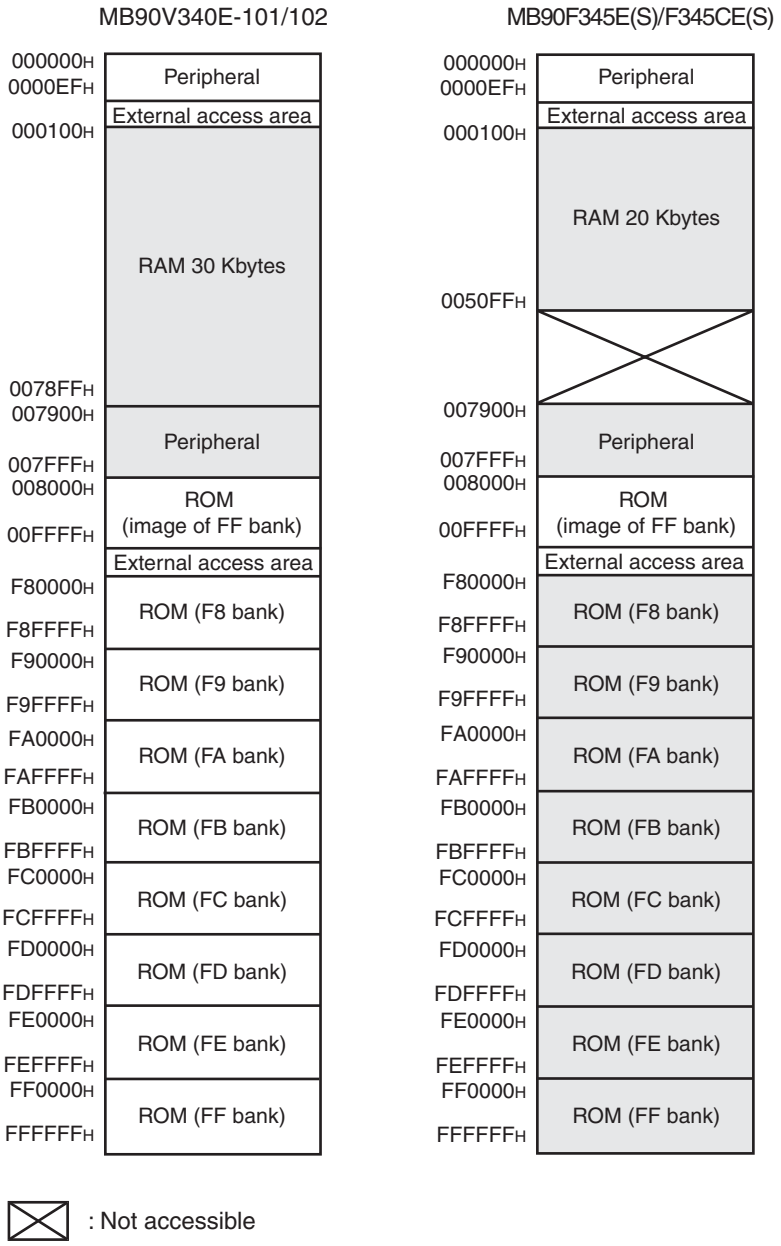



*1 : Only for devices with an S suffix in the part number
*2 : Only for devices with a C suffix in the part number
*3 : Only the MB90341E(S)/ 341CE(S)/ 342E(S)/ 342CE(S)/ F342E(S)/F342CE(S)/F345E(S)/ F345CE(S) are equipped with 2 CAN channels



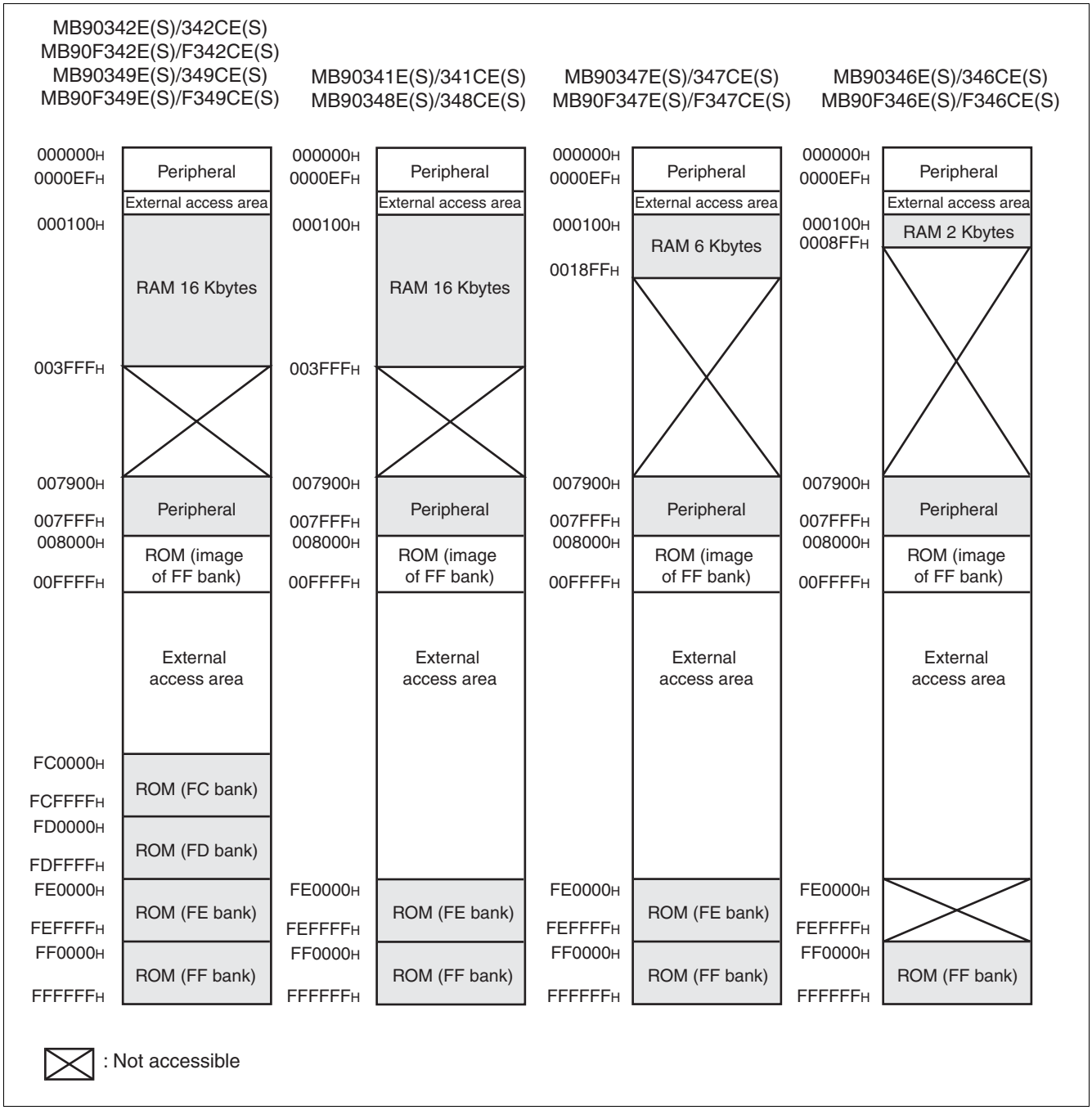
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## ■ MEMORY MAP






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Note: An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address 00C000H is accessed, the data at FFC000H in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.



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## ■ I/O MAP

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000000H | Port 0 Data Register | PDR0 | R/W | Port 0 | XXXXXXXXB |
| 000001H | Port 1 Data Register | PDR1 | R/W | Port 1 | XXXXXXXXB |
| 000002H | Port 2 Data Register | PDR2 | R/W | Port 2 | XXXXXXXXB |
| 000003H | Port 3 Data Register | PDR3 | R/W | Port 3 | XXXXXXXXB |
| 000004H | Port 4 Data Register | PDR4 | R/W | Port 4 | XXXXXXXXB |
| 000005H | Port 5 Data Register | PDR5 | R/W | Port 5 | XXXXXXXXB |
| 000006H | Port 6 Data Register | PDR6 | R/W | Port 6 | XXXXXXXXB |
| 000007H | Port 7 Data Register | PDR7 | R/W | Port 7 | XXXXXXXXB |
| 000008H | Port 8 Data Register | PDR8 | R/W | Port 8 | XXXXXXXXB |
| 000009H | Port 9 Data Register | PDR9 | R/W | Port 9 | XXXXXXXXB |
| 00000AH | Port A Data Register | PDRA | R/W | Port A | XXXXXXXXB |
| 00000BH | Port 5 Analog Input Enable Register | ADER5 | R/W | Port 5, A/D | 11111111B |
| 00000CH | Port 6 Analog Input Enable Register | ADER6 | R/W | Port 6, A/D | 11111111B |
| 00000DH | Port 7 Analog Input Enable Register | ADER7 | R/W | Port 7, A/D | 11111111B |
| 00000EH | Input Level Select Register 0 | ILSR0 | R/W | Ports | XXXXXXXXB |
| 00000FH | Input Level Select Register 1 | ILSR1 | R/W | Ports | XXXX0XXXB |
| 000010H | Port 0 Direction Register | DDR0 | R/W | Port 0 | 00000000B |
| 000011H | Port 1 Direction Register | DDR1 | R/W | Port 1 | 00000000B |
| 000012H | Port 2 Direction Register | DDR2 | R/W | Port 2 | 00000000B |
| 000013H | Port 3 Direction Register | DDR3 | R/W | Port 3 | 00000000B |
| 000014H | Port 4 Direction Register | DDR4 | R/W | Port 4 | 00000000B |
| 000015H | Port 5 Direction Register | DDR5 | R/W | Port 5 | 00000000B |
| 000016H | Port 6 Direction Register | DDR6 | R/W | Port 6 | 00000000B |
| 000017H | Port 7 Direction Register | DDR7 | R/W | Port 7 | 00000000B |
| 000018H | Port 8 Direction Register | DDR8 | R/W | Port 8 | 00000000B |
| 000019H | Port 9 Direction Register | DDR9 | R/W | Port 9 | 00000000B |
| 00001AH | Port A Direction Register | DDRA | R/W | Port A | 00000100B |
| 00001BH | Reserved | | | | |
| 00001CH | Port 0 Pull-up Control Register | PUCR0 | R/W | Port 0 | 00000000B |
| 00001DH | Port 1 Pull-up Control Register | PUCR1 | R/W | Port 1 | 00000000B |
| 00001EH | Port 2 Pull-up Control Register | PUCR2 | R/W | Port 2 | 00000000B |
| 00001FH | Port 3 Pull-up Control Register | PUCR3 | W, R/W | Port 3 | 00000000B |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000020H | Serial Mode Register 0 | SMR0 | W,R/W | UART0 | 00000000B |
| 000021H | Serial Control Register 0 | SCR0 | W,R/W | | 00000000B |
| 000022H | Reception/Transmission Data Register 0 | RDR0/TDR0 | R/W | | 00000000B |
| 000023H | Serial Status Register 0 | SSR0 | R,R/W | | 00001000B |
| 000024H | Extended Communication Control Register 0 | ECCR0 | R,W, R/W | | 000000XXB |
| 000025H | Extended Status/Control Register 0 | ESCR0 | R/W | | 00000100B |
| 000026H | Baud Rate Generator Register 00 | BGR00 | R/W | | 00000000B |
| 000027H | Baud Rate Generator Register 01 | BGR01 | R/W | | 00000000B |
| 000028H | Serial Mode Register 1 | SMR1 | W,R/W | UART1 | 00000000B |
| 000029H | Serial Control Register 1 | SCR1 | W,R/W | | 00000000B |
| 00002AH | Reception/Transmission Data Register 1 | RDR1/TDR1 | R/W | | 00000000B |
| 00002BH | Serial Status Register 1 | SSR1 | R,R/W | | 00001000B |
| 00002CH | Extended Communication Control Register 1 | ECCR1 | R,W, R/W | | 000000XXB |
| 00002DH | Extended Status/Control Register 1 | ESCR1 | R/W | | 00000100B |
| 00002EH | Baud Rate Generator Register 10 | BGR10 | R/W | | 00000000B |
| 00002FH | Baud Rate Generator Register 11 | BGR11 | R/W | | 00000000B |
| 000030H | PPG 0 Operation Mode Control Register | PPGC0 | W,R/W | 16-bit PPG 0/1 | 0X000XX1B |
| 000031H | PPG 1 Operation Mode Control Register | PPGC1 | W,R/W | | 0X000001B |
| 000032H | PPG 0/PPG 1 Count Clock Select Register | PPG01 | R/W | | 000000X0B |
| 000033H | Reserved | | | | |
| 000034H | PPG 2 Operation Mode Control Register | PPGC2 | W,R/W | 16-bit PPG 2/3 | 0X000XX1B |
| 000035H | PPG 3 Operation Mode Control Register | PPGC3 | W,R/W | | 0X000001B |
| 000036H | PPG 2/PPG 3 Count Clock Select Register | PPG23 | R/W | | 000000X0B |
| 000037H | Reserved | | | | |
| 000038H | PPG 4 Operation Mode Control Register | PPGC4 | W,R/W | 16-bit PPG 4/5 | 0X000XX1B |
| 000039H | PPG 5 Operation Mode Control Register | PPGC5 | W,R/W | | 0X000001B |
| 00003AH | PPG 4/PPG 5 Clock Select Register | PPG45 | R/W | | 000000X0B |
| 00003BH | Address Detect Control Register 1 | PACSR1 | R/W | Address Match Detection 1 | 00000000B |
| 00003CH | PPG 6 Operation Mode Control Register | PPGC6 | W,R/W | 16-bit PPG 6/7 | 0X000XX1B |
| 00003DH | PPG 7 Operation Mode Control Register | PPGC7 | W,R/W | | 0X000001B |
| 00003EH | PPG 6/PPG 7 Count Clock Control Register | PPG67 | R/W | | 000000X0B |
| 00003FH | Reserved | | | | |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000040H | PPG 8 Operation Mode Control Register | PPGC8 | W,R/W | 16-bit PPG 8/9 | 0X000XX1B |
| 000041H | PPG 9 Operation Mode Control Register | PPGC9 | W,R/W | | 0X000001B |
| 000042H | PPG 8/PPG 9 Count Clock Control Register | PPG89 | R/W | | 000000X0B |
| 000043H | Reserved | | | | |
| 000044H | PPG A Operation Mode Control Register | PPGCA | W,R/W | 16-bit PPG A/B | 0X000XX1B |
| 000045H | PPG B Operation Mode Control Register | PPGCB | W,R/W | | 0X000001B |
| 000046H | PPG A/PPG B Count Clock Select Register | PPGAB | R/W | | 000000X0B |
| 000047H | Reserved | | | | |
| 000048H | PPG C Operation Mode Control Register | PPGCC | W,R/W | 16-bit PPG C/D | 0X000XX1B |
| 000049H | PPG D Operation Mode Control Register | PPGCD | W,R/W | | 0X000001B |
| 00004AH | PPG C/PPG D Count Clock Select Register | PPGCD | R/W | | 000000X0B |
| 00004BH | Reserved | | | | |
| 00004CH | PPG E Operation Mode Control Register | PPGCE | W,R/W | 16-bit PPG E/F | 0X000XX1B |
| 00004DH | PPG F Operation Mode Control Register | PPGCF | W,R/W | | 0X000001B |
| 00004EH | PPG E/PPG F Count Clock Select Register | PPGEF | R/W | | 000000X0B |
| 00004FH | Reserved | | | | |
| 000050H | Input Capture Control Status 0/1 | ICS01 | R/W | Input Capture 0/1 | 00000000B |
| 000051H | Input Capture Edge 0/1 | ICE01 | R/W, R | | XXX0X0XXB |
| 000052H | Input Capture Control Status 2/3 | ICS23 | R/W | Input Capture 2/3 | 00000000B |
| 000053H | Input Capture Edge 2/3 | ICE23 | R | | XXXXXXXXB |
| 000054H | Input Capture Control Status 4/5 | ICS45 | R/W | Input Capture 4/5 | 00000000B |
| 000055H | Input Capture Edge 4/5 | ICE45 | R | | XXXXXXXXB |
| 000056H | Input Capture Control Status 6/7 | ICS67 | R/W | Input Capture 6/7 | 00000000B |
| 000057H | Input Capture Edge 6/7 | ICE67 | R/W, R | | XXX000XXB |
| 000058H | Output Compare Control Status 0 | OCS0 | R/W | Output Compare 0/1 | 0000XX00B |
| 000059H | Output Compare Control Status 1 | OCS1 | R/W | | 0XX00000B |
| 00005AH | Output Compare Control Status 2 | OCS2 | R/W | Output Compare 2/3 | 0000XX00B |
| 00005BH | Output Compare Control Status 3 | OCS3 | R/W | | 0XX00000B |
| 00005CH | Output Compare Control Status 4 | OCS4 | R/W | Output Compare 4/5 | 0000XX00B |
| 00005DH | Output Compare Control Status 5 | OCS5 | R/W | | 0XX00000B |
| 00005EH | Output Compare Control Status 6 | OCS6 | R/W | Output Compare 6/7 | 0000XX00B |
| 00005FH | Output Compare Control Status 7 | OCS7 | R/W | | 0XX00000B |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000060H | Timer Control Status 0 | TMCSR0 | R/W | 16-bit Reload Timer 0 | 00000000B |
| 000061H | Timer Control Status 0 | TMCSR0 | R/W | | XXXX0000B |
| 000062H | Timer Control Status 1 | TMCSR1 | R/W | 16-bit Reload Timer 1 | 00000000B |
| 000063H | Timer Control Status 1 | TMCSR1 | R/W | | XXXX0000B |
| 000064H | Timer Control Status 2 | TMCSR2 | R/W | 16-bit Reload Timer 2 | 00000000B |
| 000065H | Timer Control Status 2 | TMCSR2 | R/W | | XXXX0000B |
| 000066H | Timer Control Status 3 | TMCSR3 | R/W | 16-bit Reload Timer 3 | 00000000B |
| 000067H | Timer Control Status 3 | TMCSR3 | R/W | | XXXX0000B |
| 000068H | A/D Control Status 0 | ADCS0 | R/W | A/D Converter | 000XXXX0B |
| 000069H | A/D Control Status 1 | ADCS1 | R/W | | 0000000XB |
| 00006AH | A/D Data 0 | ADCR0 | R | | 00000000B |
| 00006BH | A/D Data 1 | ADCR1 | R | | XXXXXX00B |
| 00006CH | ADC Setting 0 | ADSR0 | R/W | | 00000000B |
| 00006DH | ADC Setting 1 | ADSR1 | R/W | | 00000000B |
| 00006EH | Reserved | | | | |
| 00006FH | ROM Mirror Function Select | ROMM | W | ROM Mirror | XXXXXXX1B |
| 000070H to 00008FH | Reserved for CAN Controller 0/1. Refer to "■ CAN CONTROLLERS" | | | | |
| 000090H to 00009AH | Reserved | | | | |
| 00009BH | DMA Descriptor Channel Specified Register | DCSR | R/W | DMA | 00000000B |
| 00009CH | DMA Status L Register | DSRL | R/W | | 00000000B |
| 00009DH | DMA Status H Register | DSRH | R/W | | 00000000B |
| 00009EH | Address Detect Control Register 0 | PACSR0 | R/W | Address Match Detection 0 | 00000000B |
| 00009FH | Delayed Interrupt Trigger/Release Register | DIRR | R/W | Delayed Interrupt | XXXXXXX0B |
| 0000A0H | Low-power Mode Control Register | LPMCR | W,R/W | Low Power Control Circuit | 00011000B |
| 0000A1H | Clock Selection Register | CKSCR | R,R/W | Low Power Control Circuit | 11111100B |
| 0000A2H, 0000A3H | Reserved | | | | |
| 0000A4H | DMA Stop Status Register | DSSR | R/W | DMA | 00000000B |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000A5H | Automatic Ready Function Select Register | ARSR | W | External Memory Access | 0011XX00B |
| 0000A6H | External Address Output Control Register | HACR | W | | 00000000B |
| 0000A7H | Bus Control Signal Selection Register | ECSR | W | | 0000000XB |
| 0000A8H | Watchdog Control Register | WDTC | R,W | Watchdog Timer | XXXXX111B |
| 0000A9H | Time Base Timer Control Register | TBTC | W,R/W | Time Base Timer | 1XX00100B |
| 0000AAH | Watch Timer Control Register | WTC | R,R/W | Watch Timer | 1X001000B |
| 0000ABH | Reserved | | | | |
| 0000ACH | DMA Enable L Register | DERL | R/W | DMA | 00000000B |
| 0000ADH | DMA Enable H Register | DERH | R/W | | 00000000B |
| 0000AEH | Flash Control Status Register (Flash memory devices only. Otherwise reserved) | FMCS | R,R/W | Flash Memory | 000X0000B |
| 0000AFH | Reserved | | | | |
| 0000B0H | Interrupt Control Register 00 | ICR00 | W,R/W | Interrupt Control | 00000111B |
| 0000B1H | Interrupt Control Register 01 | ICR01 | W,R/W | | 00000111B |
| 0000B2H | Interrupt Control Register 02 | ICR02 | W,R/W | | 00000111B |
| 0000B3H | Interrupt Control Register 03 | ICR03 | W,R/W | | 00000111B |
| 0000B4H | Interrupt Control Register 04 | ICR04 | W,R/W | | 00000111B |
| 0000B5H | Interrupt Control Register 05 | ICR05 | W,R/W | | 00000111B |
| 0000B6H | Interrupt Control Register 06 | ICR06 | W,R/W | | 00000111B |
| 0000B7H | Interrupt Control Register 07 | ICR07 | W,R/W | | 00000111B |
| 0000B8H | Interrupt Control Register 08 | ICR08 | W,R/W | | 00000111B |
| 0000B9H | Interrupt Control Register 09 | ICR09 | W,R/W | | 00000111B |
| 0000BAH | Interrupt Control Register 10 | ICR10 | W,R/W | | 00000111B |
| 0000BBH | Interrupt Control Register 11 | ICR11 | W,R/W | | 00000111B |
| 0000BCH | Interrupt Control Register 12 | ICR12 | W,R/W | | 00000111B |
| 0000BDH | Interrupt Control Register 13 | ICR13 | W,R/W | | 00000111B |
| 0000BEH | Interrupt Control Register 14 | ICR14 | W,R/W | | 00000111B |
| 0000BFH | Interrupt Control Register 15 | ICR15 | W,R/W | | 00000111B |
| 0000C0H | D/A Converter Data 0 | DAT0 | R/W | D/A Converter | XXXXXXXXB |
| 0000C1H | D/A Converter Data 1 | DAT1 | R/W | | XXXXXXXXB |
| 0000C2H | D/A Control 0 | DACR0 | R/W | | XXXXXXX0B |
| 0000C3H | D/A Control 1 | DACR1 | R/W | | XXXXXXX0B |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000C4H, 0000C5H | Reserved | | | | |
| 0000C6H | External Interrupt Enable 0 | ENIR0 | R/W | External Interrupt 0 | 00000000B |
| 0000C7H | External Interrupt Source 0 | EIRR0 | R/W | | XXXXXXXXB |
| 0000C8H | External Interrupt Level Setting 0 | ELVR0 | R/W | | 00000000B |
| 0000C9H | External Interrupt Level Setting 0 | ELVR0 | R/W | | 00000000B |
| 0000CAH | External Interrupt Enable 1 | ENIR1 | R/W | External Interrupt 1 | 00000000B |
| 0000CBH | External Interrupt Source 1 | EIRR1 | R/W | | XXXXXXXXB |
| 0000CCH | External Interrupt Level Setting 1 | ELVR1 | R/W | | 00000000B |
| 0000CDH | External Interrupt Level Setting 1 | ELVR1 | R/W | | 00000000B |
| 0000CEH | External Interrupt Source Select | EISSR | R/W | | 00000000B |
| 0000CFH | PLL/Sub clock Control Register | PSCCR | W | PLL | XXXX0000B |
| 0000D0H | DMA Buffer Address Pointer L Register | BAPL | R/W | DMA | XXXXXXXXB |
| 0000D1H | DMA Buffer Address Pointer M Register | BAPM | R/W | | XXXXXXXXB |
| 0000D2H | DMA Buffer Address Pointer H Register | BAPH | R/W | | XXXXXXXXB |
| 0000D3H | DMA Control Register | DMACS | R/W | | XXXXXXXXB |
| 0000D4H | I/O Register Address Pointer L Register | IOAL | R/W | | XXXXXXXXB |
| 0000D5H | I/O Register Address Pointer H Register | IOAH | R/W | | XXXXXXXXB |
| 0000D6H | Data Counter L Register | DCTL | R/W | | XXXXXXXXB |
| 0000D7H | Data Counter H Register | DCTH | R/W | | XXXXXXXXB |
| 0000D8H | Serial Mode Register 2 | SMR2 | W,R/W | UART2 | 00000000B |
| 0000D9H | Serial Control Register 2 | SCR2 | W,R/W | | 00000000B |
| 0000DAH | Reception/Transmission Data Register 2 | RDR2/TDR2 | R/W | | 00000000B |
| 0000DBH | Serial Status Register 2 | SSR2 | R,R/W | | 00001000B |
| 0000DCH | Extended Communication Control Register 2 | ECCR2 | R,W, R/W | | 000000XXB |
| 0000DDH | Extended Status Control Register 2 | ESCR2 | R/W | | 00000100B |
| 0000DEH | Baud Rate Generator Register 20 | BGR20 | R/W | | 00000000B |
| 0000DFH | Baud Rate Generator Register 21 | BGR21 | R/W | | 00000000B |
| 0000E0H to 0000EFH | Reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS” | | | | |
| 0000F0H to 0000FFH | External | | | | |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 007900H | Reload Register L0 | PRLL0 | R/W | 16-bit PPG 0/1 | XXXXXXXXB |
| 007901H | Reload Register H0 | PRLH0 | R/W | | XXXXXXXXB |
| 007902H | Reload Register L1 | PRLL1 | R/W | | XXXXXXXXB |
| 007903H | Reload Register H1 | PRLH1 | R/W | | XXXXXXXXB |
| 007904H | Reload Register L2 | PRLL2 | R/W | 16-bit PPG 2/3 | XXXXXXXXB |
| 007905H | Reload Register H2 | PRLH2 | R/W | | XXXXXXXXB |
| 007906H | Reload Register L3 | PRLL3 | R/W | | XXXXXXXXB |
| 007907H | Reload Register H3 | PRLH3 | R/W | | XXXXXXXXB |
| 007908H | Reload Register L4 | PRLL4 | R/W | 16-bit PPG 4/5 | XXXXXXXXB |
| 007909H | Reload Register H4 | PRLH4 | R/W | | XXXXXXXXB |
| 00790AH | Reload Register L5 | PRLL5 | R/W | | XXXXXXXXB |
| 00790BH | Reload Register H5 | PRLH5 | R/W | | XXXXXXXXB |
| 00790CH | Reload Register L6 | PRLL6 | R/W | 16-bit PPG 6/7 | XXXXXXXXB |
| 00790DH | Reload Register H6 | PRLH6 | R/W | | XXXXXXXXB |
| 00790EH | Reload Register L7 | PRLL7 | R/W | | XXXXXXXXB |
| 00790FH | Reload Register H7 | PRLH7 | R/W | | XXXXXXXXB |
| 007910H | Reload Register L8 | PRLL8 | R/W | 16-bit PPG 8/9 | XXXXXXXXB |
| 007911H | Reload Register H8 | PRLH8 | R/W | | XXXXXXXXB |
| 007912H | Reload Register L9 | PRLL9 | R/W | | XXXXXXXXB |
| 007913H | Reload Register H9 | PRLH9 | R/W | | XXXXXXXXB |
| 007914H | Reload Register LA | PRLLA | R/W | 16-bit PPG A/B | XXXXXXXXB |
| 007915H | Reload Register HA | PRLHA | R/W | | XXXXXXXXB |
| 007916H | Reload Register LB | PRLLB | R/W | | XXXXXXXXB |
| 007917H | Reload Register HB | PRLHB | R/W | | XXXXXXXXB |
| 007918H | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | XXXXXXXXB |
| 007919H | Reload Register HC | PRLHC | R/W | | XXXXXXXXB |
| 00791AH | Reload Register LD | PRLLD | R/W | | XXXXXXXXB |
| 00791BH | Reload Register HD | PRLHD | R/W | | XXXXXXXXB |
| 00791CH | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | XXXXXXXXB |
| 00791DH | Reload Register HE | PRLHE | R/W | | XXXXXXXXB |
| 00791EH | Reload Register LF | PRLLF | R/W | | XXXXXXXXB |
| 00791FH | Reload Register HF | PRLHF | R/W | | XXXXXXXXB |
| 007920H | Input Capture 0 | IPCP0 | R | Input Capture 0/1 | XXXXXXXXB |
| 007921H | Input Capture 0 | IPCP0 | R | | XXXXXXXXB |
| 007922H | Input Capture 1 | IPCP1 | R | | XXXXXXXXB |
| 007923H | Input Capture 1 | IPCP1 | R | | XXXXXXXXB |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 007924H | Input Capture 2 | IPCP2 | R | Input Capture 2/3 | XXXXXXXXB |
| 007925H | Input Capture 2 | IPCP2 | R | | XXXXXXXXB |
| 007926H | Input Capture 3 | IPCP3 | R | | XXXXXXXXB |
| 007927H | Input Capture 3 | IPCP3 | R | | XXXXXXXXB |
| 007928H | Input Capture 4 | IPCP4 | R | Input Capture 4/5 | XXXXXXXXB |
| 007929H | Input Capture 4 | IPCP4 | R | | XXXXXXXXB |
| 00792AH | Input Capture 5 | IPCP5 | R | | XXXXXXXXB |
| 00792BH | Input Capture 5 | IPCP5 | R | | XXXXXXXXB |
| 00792CH | Input Capture 6 | IPCP6 | R | Input Capture 6/7 | XXXXXXXXB |
| 00792DH | Input Capture 6 | IPCP6 | R | | XXXXXXXXB |
| 00792EH | Input Capture 7 | IPCP7 | R | | XXXXXXXXB |
| 00792FH | Input Capture 7 | IPCP7 | R | | XXXXXXXXB |
| 007930H | Output Compare 0 | OCCP0 | R/W | Output Compare 0/1 | XXXXXXXXB |
| 007931H | Output Compare 0 | OCCP0 | R/W | | XXXXXXXXB |
| 007932H | Output Compare 1 | OCCP1 | R/W | | XXXXXXXXB |
| 007933H | Output Compare 1 | OCCP1 | R/W | | XXXXXXXXB |
| 007934H | Output Compare 2 | OCCP2 | R/W | Output Compare 2/3 | XXXXXXXXB |
| 007935H | Output Compare 2 | OCCP2 | R/W | | XXXXXXXXB |
| 007936H | Output Compare 3 | OCCP3 | R/W | | XXXXXXXXB |
| 007937H | Output Compare 3 | OCCP3 | R/W | | XXXXXXXXB |
| 007938H | Output Compare 4 | OCCP4 | R/W | Output Compare 4/5 | XXXXXXXXB |
| 007939H | Output Compare 4 | OCCP4 | R/W | | XXXXXXXXB |
| 00793AH | Output Compare 5 | OCCP5 | R/W | | XXXXXXXXB |
| 00793BH | Output Compare 5 | OCCP5 | R/W | | XXXXXXXXB |
| 00793CH | Output Compare 6 | OCCP6 | R/W | Output Compare 6/7 | XXXXXXXXB |
| 00793DH | Output Compare 6 | OCCP6 | R/W | | XXXXXXXXB |
| 00793EH | Output Compare 7 | OCCP7 | R/W | | XXXXXXXXB |
| 00793FH | Output Compare 7 | OCCP7 | R/W | | XXXXXXXXB |
| 007940H | Timer Data 0 | TCDT0 | R/W | Free-run Timer 0 | 00000000B |
| 007941H | Timer Data 0 | TCDT0 | R/W | | 00000000B |
| 007942H | Timer Control Status 0 | TCCSL0 | R/W | | 00000000B |
| 007943H | Timer Control Status 0 | TCCSH0 | R/W | | 0XXXXXXXB |
| 007944H | Timer Data 1 | TCDT1 | R/W | Free-run Timer 1 | 00000000B |
| 007945H | Timer Data 1 | TCDT1 | R/W | | 00000000B |
| 007946H | Timer Control Status 1 | TCCSL1 | R/W | | 00000000B |
| 007947H | Timer Control Status 1 | TCCSH1 | R/W | | 0XXXXXXXB |

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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 007948H | Timer 0/Reload 0 | TMR0/ TMRLR0 | R/W | 16-bit Reload Timer 0 | XXXXXXXXB |
| 007949H | | | R/W | | XXXXXXXXB |
| 00794AH | Timer 1/Reload 1 | TMR1/ TMRLR1 | R/W | 16-bit Reload Timer 1 | XXXXXXXXB |
| 00794BH | | | R/W | | XXXXXXXXB |
| 00794CH | Timer 2/Reload 2 | TMR2/ TMRLR2 | R/W | 16-bit Reload Timer 2 | XXXXXXXXB |
| 00794DH | | | R/W | | XXXXXXXXB |
| 00794EH | Timer 3/Reload 3 | TMR3/ TMRLR3 | R/W | 16-bit Reload Timer 3 | XXXXXXXXB |
| 00794FH | | | R/W | | XXXXXXXXB |
| 007950H | Serial Mode Register 3 | SMR3 | W,R/W | UART3 | 00000000B |
| 007951H | Serial Control Register 3 | SCR3 | W,R/W | | 00000000B |
| 007952H | Reception/Transmission Data Register 3 | RDR3/TDR3 | R/W | | 00000000B |
| 007953H | Serial Status Register 3 | SSR3 | R,R/W | | 00001000B |
| 007954H | Extended Communication Control Register 3 | ECCR3 | R,W, R/W | | 000000XXB |
| 007955H | Extended Status Control Register | ESCR3 | R/W | | 00000100B |
| 007956H | Baud Rate Generator Register 30 | BGR30 | R/W | | 00000000B |
| 007957H | Baud Rate Generator Register 31 | BGR31 | R/W | | 00000000B |
| 007958H | Serial Mode Register 4 | SMR4 | W,R/W | UART4 | 00000000B |
| 007959H | Serial Control Register 4 | SCR4 | W,R/W | | 00000000B |
| 00795AH | Reception/Transmission Data Register 4 | RDR4/TDR4 | R/W | | 00000000B |
| 00795BH | Serial Status Register 4 | SSR4 | R,R/W | | 00001000B |
| 00795CH | Extended Communication Control Register 4 | ECCR4 | R,W, R/W | | 000000XXB |
| 00795DH | Extended Status Control Register | ESCR4 | R/W | | 00000100B |
| 00795EH | Baud Rate Generator Register 40 | BGR40 | R/W | | 00000000B |
| 00795FH | Baud Rate Generator Register 41 | BGR41 | R/W | | 00000000B |
| 007960H to 00796BH | Reserved | | | | |
| 00796CH | Clock Output Enable Register | CLKR | R/W | Clock Monitor | XXXX0000B |
| 00796DH | Reserved | | | | |
| 00796EH | CAN Direct Mode Register | CDMR | R/W | CAN Clock sync | XXXXXXX0B |
| 00796FH | CAN Switch Register | CANSWR | R/W | CAN 0/1 | XXXXXX00B |

*(Continued)*



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| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 007970H | I²C Bus Status Register 0 | IBSR0 | R | I²C Interface 0 | 00000000B |
| 007971H | I²C Bus Control Register 0 | IBCR0 | W,R/W | | 00000000B |
| 007972H | I²C 10-bit Slave Address Register 0 | ITBAL0 | R/W | | 00000000B |
| 007973H | | ITBAH0 | R/W | | 00000000B |
| 007974H | I²C 10-bit Slave Address Mask Register 0 | ITMKL0 | R/W | | 11111111B |
| 007975H | | ITMKH0 | R/W | | 00111111B |
| 007976H | I²C 7-bit Slave Address Register 0 | ISBA0 | R/W | | 00000000B |
| 007977H | I²C 7-bit Slave Address Mask Register 0 | ISMK0 | R/W | | 01111111B |
| 007978H | I²C Data Register 0 | IDAR0 | R/W | | 00000000B |
| 007979H, 00797AH | Reserved | | | | |
| 00797BH | I²C Clock Control Register 0 | ICCR0 | R/W | I²C Interface 0 | 00011111B |
| 00797CH to 00797FH | Reserved | | | | |
| 007980H | I²C Bus Status Register 1 | IBSR1 | R | I²C Interface 1 | 00000000B |
| 007981H | I²C Bus Control Register 1 | IBCR1 | W,R/W | | 00000000B |
| 007982H | I²C 10-bit Slave Address Register 1 | ITBAL1 | R/W | | 00000000B |
| 007983H | | ITBAH1 | R/W | | 00000000B |
| 007984H | I²C 10-bit Slave Address Mask Register 1 | ITMKL1 | R/W | | 11111111B |
| 007985H | | ITMKH1 | R/W | | 00111111B |
| 007986H | I²C 7-bit Slave Address Register 1 | ISBA1 | R/W | | 00000000B |
| 007987H | I²C 7-bit Slave Address Mask Register 1 | ISMK1 | R/W | | 01111111B |
| 007988H | I²C Data Register 1 | IDAR1 | R/W | | 00000000B |
| 007989H, 00798AH | Reserved | | | | |
| 00798BH | I²C Clock Control Register 1 | ICCR1 | R/W | I²C Interface 1 | 00011111B |
| 00798CH to 0079C1H | Reserved | | | | |
| 0079C2H | Clock Modulator Control Register | CMCR | R, R/W | Clock Modulator | 0001X000B |
| 0079C3H to 0079DFH | Reserved | | | | |

*(Continued)*



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*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 0079E0H | Detect Address Setting 0 | PADR0 | R/W | Address Match Detection 0 | XXXXXXXXB |
| 0079E1H | Detect Address Setting 0 | PADR0 | R/W | | XXXXXXXXB |
| 0079E2H | Detect Address Setting 0 | PADR0 | R/W | | XXXXXXXXB |
| 0079E3H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 0079E4H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 0079E5H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 0079E6H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 0079E7H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 0079E8H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 0079E9H to 0079EFH | Reserved | | | | |
| 0079F0H | Detect Address Setting 3 | PADR3 | R/W | Address Match Detection 1 | XXXXXXXXB |
| 0079F1H | Detect Address Setting 3 | PADR3 | R/W | | XXXXXXXXB |
| 0079F2H | Detect Address Setting 3 | PADR3 | R/W | | XXXXXXXXB |
| 0079F3H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 0079F4H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 0079F5H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 0079F6H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 0079F7H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 0079F8H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 0079F9H to 0079FFH | Reserved | | | | |
| 007A00H to 007AFFH | Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS” | | | | |
| 007B00H to 007BFFH | Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS” | | | | |
| 007C00H to 007CFFH | Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS” | | | | |
| 007D00H to 007DFFH | Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS” | | | | |
| 007E00H to 007FFFH | Reserved | | | | |

Notes : • Initial value of “X” represents unknown value.
• Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.



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## ■ CAN CONTROLLERS

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers (1)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $000070_H$ | $000080_H$ | Message Buffer Valid Register | BVALR | R/W | $00000000_B$ $00000000_B$ |
| $000071_H$ | $000081_H$ | | | | |
| $000072_H$ | $000082_H$ | Transmit Request Register | TREQR | R/W | $00000000_B$ $00000000_B$ |
| $000073_H$ | $000083_H$ | | | | |
| $000074_H$ | $000084_H$ | Transmit Cancel Register | TCANR | W | $00000000_B$ $00000000_B$ |
| $000075_H$ | $000085_H$ | | | | |
| $000076_H$ | $000086_H$ | Transmission Complete Register | TCR | R/W | $00000000_B$ $00000000_B$ |
| $000077_H$ | $000087_H$ | | | | |
| $000078_H$ | $000088_H$ | Receive Complete Register | RCR | R/W | $00000000_B$ $00000000_B$ |
| $000079_H$ | $000089_H$ | | | | |
| $00007A_H$ | $00008A_H$ | Remote Request Receiving Register | RRTRR | R/W | $00000000_B$ $00000000_B$ |
| $00007B_H$ | $00008B_H$ | | | | |
| $00007C_H$ | $00008C_H$ | Receive Overrun Register | ROVRR | R/W | $00000000_B$ $00000000_B$ |
| $00007D_H$ | $00008D_H$ | | | | |
| $00007E_H$ | $00008E_H$ | Reception Interrupt Enable Register | RIER | R/W | $00000000_B$ $00000000_B$ |
| $00007F_H$ | $00008F_H$ | | | | |



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**List of Control Registers (2)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007B00H | 007D00H | Control Status Register | CSR | R/W, W<br>R/W, R | 0XXXX0X1B<br>00XX000B |
| 007B01H | 007D01H | | | | |
| 007B02H | 007D02H | Last Event Indicator Register | LEIR | R/W | 000X0000B<br>XXXXXXXXB |
| 007B03H | 007D03H | | | | |
| 007B04H | 007D04H | Receive And Transmit Error Counter | RTEC | R | 00000000B<br>00000000B |
| 007B05H | 007D05H | | | | |
| 007B06H | 007D06H | Bit Timing Register | BTR | R/W | 11111111B<br>X1111111B |
| 007B07H | 007D07H | | | | |
| 007B08H | 007D08H | IDE Register | IDER | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007B09H | 007D09H | | | | |
| 007B0AH | 007D0AH | Transmit RTR Register | TRTRR | R/W | 00000000B<br>00000000B |
| 007B0BH | 007D0BH | | | | |
| 007B0CH | 007D0CH | Remote Frame Receive Waiting Register | RFWTR | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007B0DH | 007D0DH | | | | |
| 007B0EH | 007D0EH | Transmit Interrupt Enable Register | TIER | R/W | 00000000B<br>00000000B |
| 007B0FH | 007D0FH | | | | |
| 007B10H | 007D10H | Acceptance Mask Select Register | AMSR | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007B11H | 007D11H | | | | |
| 007B12H | 007D12H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007B13H | 007D13H | | | | |
| 007B14H | 007D14H | Acceptance Mask Register 0 | AMR0 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007B15H | 007D15H | | | | |
| 007B16H | 007D16H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007B17H | 007D17H | | | | |
| 007B18H | 007D18H | Acceptance Mask Register 1 | AMR1 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007B19H | 007D19H | | | | |
| 007B1AH | 007D1AH | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007B1BH | 007D1BH | | | | |



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**List of Message Buffers (ID Registers) (1)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007A00H to 007A1FH | 007C00H to 007C1FH | General-Purpose RAM | — | R/W | XXXXXXXXB to XXXXXXXXB |
| 007A20H | 007C20H | ID Register 0 | IDR0 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A21H | 007C21H | | | | |
| 007A22H | 007C22H | | | | XXXXXXXXB XXXXXXXXB |
| 007A23H | 007C23H | | | | |
| 007A24H | 007C24H | ID Register 1 | IDR1 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A25H | 007C25H | | | | |
| 007A26H | 007C26H | | | | XXXXXXXXB XXXXXXXXB |
| 007A27H | 007C27H | | | | |
| 007A28H | 007C28H | ID Register 2 | IDR2 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A29H | 007C29H | | | | |
| 007A2AH | 007C2AH | | | | XXXXXXXXB XXXXXXXXB |
| 007A2BH | 007C2BH | | | | |
| 007A2CH | 007C2CH | ID Register 3 | IDR3 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A2DH | 007C2DH | | | | |
| 007A2EH | 007C2EH | | | | XXXXXXXXB XXXXXXXXB |
| 007A2FH | 007C2FH | | | | |
| 007A30H | 007C30H | ID Register 4 | IDR4 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A31H | 007C31H | | | | |
| 007A32H | 007C32H | | | | XXXXXXXXB XXXXXXXXB |
| 007A33H | 007C33H | | | | |
| 007A34H | 007C34H | ID Register 5 | IDR5 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A35H | 007C35H | | | | |
| 007A36H | 007C36H | | | | XXXXXXXXB XXXXXXXXB |
| 007A37H | 007C37H | | | | |
| 007A38H | 007C38H | ID Register 6 | IDR6 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A39H | 007C39H | | | | |
| 007A3AH | 007C3AH | | | | XXXXXXXXB XXXXXXXXB |
| 007A3BH | 007C3BH | | | | |
| 007A3CH | 007C3CH | ID Register 7 | IDR7 | R/W | XXXXXXXXB XXXXXXXXB |
| 007A3DH | 007C3DH | | | | |
| 007A3EH | 007C3EH | | | | XXXXXXXXB XXXXXXXXB |
| 007A3FH | 007C3FH | | | | |



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**List of Message Buffers (ID Registers) (2)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007A40H | 007C40H | ID Register 8 | IDR8 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A41H | 007C41H | | | | |
| 007A42H | 007C42H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A43H | 007C43H | | | | |
| 007A44H | 007C44H | ID Register 9 | IDR9 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A45H | 007C45H | | | | |
| 007A46H | 007C46H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A47H | 007C47H | | | | |
| 007A48H | 007C48H | ID Register 10 | IDR10 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A49H | 007C49H | | | | |
| 007A4AH | 007C4AH | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A4BH | 007C4BH | | | | |
| 007A4CH | 007C4CH | ID Register 11 | IDR11 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A4DH | 007C4DH | | | | |
| 007A4EH | 007C4EH | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A4FH | 007C4FH | | | | |
| 007A50H | 007C50H | ID Register 12 | IDR12 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A51H | 007C51H | | | | |
| 007A52H | 007C52H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A53H | 007C53H | | | | |
| 007A54H | 007C54H | ID Register 13 | IDR13 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A55H | 007C55H | | | | |
| 007A56H | 007C56H | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A57H | 007C57H | | | | |
| 007A58H | 007C58H | ID Register 14 | IDR14 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A59H | 007C59H | | | | |
| 007A5AH | 007C5AH | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A5BH | 007C5BH | | | | |
| 007A5CH | 007C5CH | ID Register 15 | IDR15 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007A5DH | 007C5DH | | | | |
| 007A5EH | 007C5EH | | | | XXXXXXXXB<br>XXXXXXXXB |
| 007A5FH | 007C5FH | | | | |



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**List of Message Buffers (DLC Registers and Data Registers) (1)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007A60H | 007C60H | DLC Register 0 | DLCR0 | R/W | XXXXXXXXB |
| 007A61H | 007C61H | | | | |
| 007A62H | 007C62H | DLC Register 1 | DLCR1 | R/W | XXXXXXXXB |
| 007A63H | 007C63H | | | | |
| 007A64H | 007C64H | DLC Register 2 | DLCR2 | R/W | XXXXXXXXB |
| 007A65H | 007C65H | | | | |
| 007A66H | 007C66H | DLC Register 3 | DLCR3 | R/W | XXXXXXXXB |
| 007A67H | 007C67H | | | | |
| 007A68H | 007C68H | DLC Register 4 | DLCR4 | R/W | XXXXXXXXB |
| 007A69H | 007C69H | | | | |
| 007A6AH | 007C6AH | DLC Register 5 | DLCR5 | R/W | XXXXXXXXB |
| 007A6BH | 007C6BH | | | | |
| 007A6CH | 007C6CH | DLC Register 6 | DLCR6 | R/W | XXXXXXXXB |
| 007A6DH | 007C6DH | | | | |
| 007A6EH | 007C6EH | DLC Register 7 | DLCR7 | R/W | XXXXXXXXB |
| 007A6FH | 007C6FH | | | | |
| 007A70H | 007C70H | DLC Register 8 | DLCR8 | R/W | XXXXXXXXB |
| 007A71H | 007C71H | | | | |
| 007A72H | 007C72H | DLC Register 9 | DLCR9 | R/W | XXXXXXXXB |
| 007A73H | 007C73H | | | | |
| 007A74H | 007C74H | DLC Register 10 | DLCR10 | R/W | XXXXXXXXB |
| 007A75H | 007C75H | | | | |
| 007A76H | 007C76H | DLC Register 11 | DLCR11 | R/W | XXXXXXXXB |
| 007A77H | 007C77H | | | | |
| 007A78H | 007C78H | DLC Register 12 | DLCR12 | R/W | XXXXXXXXB |
| 007A79H | 007C79H | | | | |
| 007A7AH | 007C7AH | DLC Register 13 | DLCR13 | R/W | XXXXXXXXB |
| 007A7BH | 007C7BH | | | | |
| 007A7CH | 007C7CH | DLC Register 14 | DLCR14 | R/W | XXXXXXXXB |
| 007A7DH | 007C7DH | | | | |
| 007A7EH | 007C7EH | DLC Register 15 | DLCR15 | R/W | XXXXXXXXB |
| 007A7FH | 007C7FH | | | | |



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**List of Message Buffers (DLC Registers and Data Registers) (2)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007A80H to 007A87H | 007C80H to 007C87H | Data Register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007A88H to 007A8FH | 007C88H to 007C8FH | Data Register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007A90H to 007A97H | 007C90H to 007C97H | Data Register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007A98H to 007A9FH | 007C98H to 007C9FH | Data Register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AA0H to 007AA7H | 007CA0H to 007CA7H | Data Register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AA8H to 007AAFH | 007CA8H to 007CAFH | Data Register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AB0H to 007AB7H | 007CB0H to 007CB7H | Data Register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AB8H to 007ABFH | 007CB8H to 007CBFH | Data Register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AC0H to 007AC7H | 007CC0H to 007CC7H | Data Register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AC8H to 007ACFH | 007CC8H to 007CCFH | Data Register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AD0H to 007AD7H | 007CD0H to 007CD7H | Data Register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AD8H to 007ADFH | 007CD8H to 007CDFH | Data Register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AE0H to 007AE7H | 007CE0H to 007CE7H | Data Register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AE8H to 007AEFH | 007CE8H to 007CEFH | Data Register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |



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**List of Message Buffers (DLC Registers and Data Registers) (3)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 007AF0H to 007AF7H | 007CF0H to 007CF7H | Data Register 14 (8 bytes) | DTR14 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007AF8H to 007AFFH | 007CF8H to 007CFFH | Data Register 15 (8 bytes) | DTR15 | R/W | XXXXXXXXB to XXXXXXXXB |



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## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

| Interrupt cause | EI²OS Support | DMA channel number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| Reset | N | — | #08 | FFFFDC$_H$ | — | — |
| INT9 instruction | N | — | #09 | FFFFD8$_H$ | — | — |
| Exception | N | — | #10 | FFFFD4$_H$ | — | — |
| CAN 0 RX | N | — | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ |
| CAN 0 TX/NS | N | — | #12 | FFFFCC$_H$ | | |
| CAN 1 RX / Input Capture 6 | Y1 | — | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ |
| CAN 1 TX/NS / Input Capture 7 | Y1 | — | #14 | FFFFC4$_H$ | | |
| CAN 2 RX / I²C0 | N | — | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ |
| CAN 2 TX/NS | N | — | #16 | FFFFBC$_H$ | | |
| 16-bit Reload Timer 0 | Y1 | 0 | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ |
| 16-bit Reload Timer 1 | Y1 | 1 | #18 | FFFFB4$_H$ | | |
| 16-bit Reload Timer 2 | Y1 | 2 | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ |
| 16-bit Reload Timer 3 | Y1 | — | #20 | FFFFAC$_H$ | | |
| PPG 0/1/4/5 | N | — | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ |
| PPG 2/3/6/7 | N | — | #22 | FFFFA4$_H$ | | |
| PPG 8/9/C/D | N | — | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ |
| PPG A/B/E/F | N | — | #24 | FFFF9C$_H$ | | |
| Time Base Timer | N | — | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ |
| External Interrupt 0 to 3, 8 to 11 | Y1 | 3 | #26 | FFFF94$_H$ | | |
| Watch Timer | N | — | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ |
| External Interrupt 4 to 7, 12 to 15 | Y1 | 4 | #28 | FFFF8C$_H$ | | |
| A/D Converter | Y1 | 5 | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ |
| Free-run Timer 0 / Free-run Timer 1 | N | — | #30 | FFFF84$_H$ | | |
| Input Capture 4/5 / I²C1 | Y1 | 6 | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ |
| Output Compare 0/1/4/5 | Y1 | 7 | #32 | FFFF7C$_H$ | | |
| Input Capture 0 to 3 | Y1 | 8 | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ |
| Output Compare 2/3/6/7 | Y1 | 9 | #34 | FFFF74$_H$ | | |
| UART 0 RX | Y2 | 10 | #35 | FFFF70$_H$ | ICR12 | 0000BC$_H$ |
| UART 0 TX | Y1 | 11 | #36 | FFFF6C$_H$ | | |
| UART 1 RX / UART 3 RX | Y2 | 12 | #37 | FFFF68$_H$ | ICR13 | 0000BD$_H$ |
| UART 1 TX / UART 3 TX | Y1 | 13 | #38 | FFFF64$_H$ | | |

*(Continued)*



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*(Continued)*

| Interrupt cause | EI²OS Support | DMA channel number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| UART 2 RX / UART 4 RX | Y2 | 14 | #39 | FFFF60H | ICR14 | 0000BEH |
| UART 2 TX / UART 4 TX | Y1 | 15 | #40 | FFFF5CH | | |
| Flash Memory | N | — | #41 | FFFF58H | ICR15 | 0000BFH |
| Delayed Interrupt | N | — | #42 | FFFF54H | | |

Y1 : Usable
Y2 : Usable, with EI²OS stop function
N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.



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## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC} = AV_{CC}$*2 |
| | AVRH, AVRL | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Maximum Clamp Current | $I_{CLAMP}$ | –4.0 | +4.0 | mA | *5 |
| Total Maximum Clamp Current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 40 | mA | *5 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *4, *6 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *4, *7 |
| “L” level maximum overall output current | $\Sigma I_{OL}$ | — | 100 | mA | *4 |
| “L” level average overall output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *4, *8 |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | *4, *6 |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | *4, *7 |
| “H” level maximum overall output current | $\Sigma I_{OH}$ | — | –100 | mA | *4 |
| “H” level average overall output current | $\Sigma I_{OHAV}$ | — | –50 | mA | *4, *8 |
| Power consumption | $P_D$ | — | 450 | mW | |
| Operating temperature | $T_A$ | –40 | +105 | °C | |
| Storage temperature | $T_{STG}$ | –55 | +150 | °C | |

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set $AV_{CC}$ and $V_{CC}$ to the same voltage. Make sure that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

*3: $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3 V. $V_I$ should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5:
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.

*(Continued)*

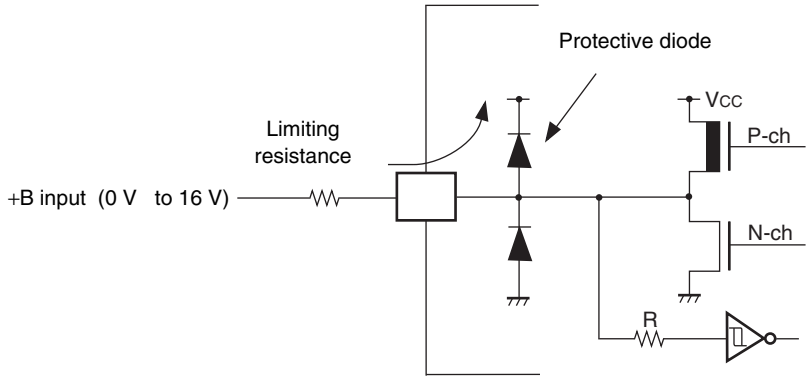


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*(Continued)*

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

- Input/output equivalent circuits




*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



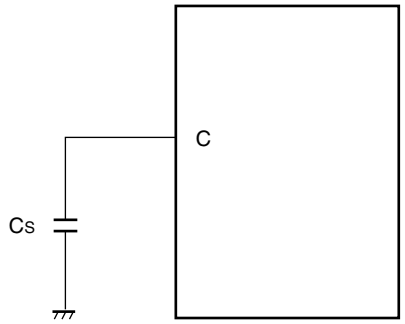
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## 2. Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.0 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.5 | 5.0 | 5.5 | V | Under normal operation, when not using the A/D converter and not Flash programming. |
| | | 4.5 | 5.0 | 5.5 | V | When External bus is used. |
| | | 3.0 | — | 5.5 | V | Maintains RAM data in stop mode |
| Smoothing capacitor | $C_S$ | 0.1 | — | 1.0 | µF | Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor. |
| Operating temperature | $T_A$ | −40 | — | +105 | °C | |

C Pin Connection Diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



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## 3. DC Characteristics

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input H voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{IHS}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85) |
| | $V_{IHA}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if Automotive input levels are selected |
| | $V_{IHT}$ | — | — | 2.0 | — | $V_{CC}$ + 0.3 | V | Port inputs if TTL input levels are selected |
| | $V_{IHS}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | P12, P50, P82, P85 inputs if CMOS input levels are selected |
| | $V_{IHI}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected |
| | $V_{IHR}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{IHM}$ | — | — | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | MD input pin |
| Input L voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85) |
| | $V_{ILA}$ | — | — | $V_{SS}$ – 0.3 | — | 0.5 $V_{CC}$ | V | Port inputs if Automotive input levels are selected |
| | $V_{ILT}$ | — | — | $V_{SS}$ – 0.3 | — | 0.8 | V | Port inputs if TTL input levels are selected |
| | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | P12, P50, P82, P85 inputs if CMOS input levels are selected |
| | $V_{ILI}$ | — | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected |
| | $V_{ILR}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{ILM}$ | — | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | MD input pin |
| Output H voltage | $V_{OH}$ | Normal outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output H voltage | $V_{OHI}$ | $I^2C$ current outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = –3.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output L voltage | $V_{OL}$ | Normal outputs | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| Output L voltage | $V_{OLI}$ | $I^2C$ current outputs | $V_{CC}$ = 4.5 V, $I_{OL}$ = 3.0 mA | — | — | 0.4 | V | |

*(Continued)*



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*(Continued)*

($T_A$ = −40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leak current | $I_{IL}$ | — | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | −1 | — | +1 | µA | |
| Pull-up resistance | $R_{UP}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |
| Pull-down resistance | $R_{DOWN}$ | MD2 | — | 25 | 50 | 100 | kΩ | Except Flash memory devices |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At normal operation. | — | 55 | 70 | mA | |
| | | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory. | — | 70 | 85 | mA | Flash memory devices |
| | | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory. | — | 75 | 90 | mA | Flash memory devices |
| | $I_{CCS}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, In Sleep mode. | — | 25 | 35 | mA | |
| | $I_{CTS}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode | — | 0.3 | 0.8 | mA | |
| | $I_{CTSPLL6}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz | — | 4 | 7 | mA | |
| | $I_{CCL}$ | | $V_{CC}$ = 5.0 V Internal frequency : 8 kHz, In sub operation $T_A$ = +25°C | — | 70 | 140 | µA | |
| | $I_{CCLS}$ | | $V_{CC}$ = 5.0 V Internal frequency : 8 kHz, In sub sleep $T_A$ = +25°C | — | 20 | 50 | µA | |
| | $I_{CCT}$ | | $V_{CC}$ = 5.0 V Internal frequency : 8 kHz, In watch mode $T_A$ = +25°C | — | 10 | 35 | µA | |
| | $I_{CCH}$ | | $V_{CC}$ = 5.0 V, In Stop mode, $T_A$ = +25°C | — | 7 | 25 | µA | |
| Input capacitance | $C_{IN}$ | Other than C, $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, $V_{CC}$, $V_{SS}$ | — | — | 5 | 15 | pF | |

* : The power supply current is measured with an external clock.



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## 4. AC Characteristics

### (1) Clock Timing

($T_A$ = −40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

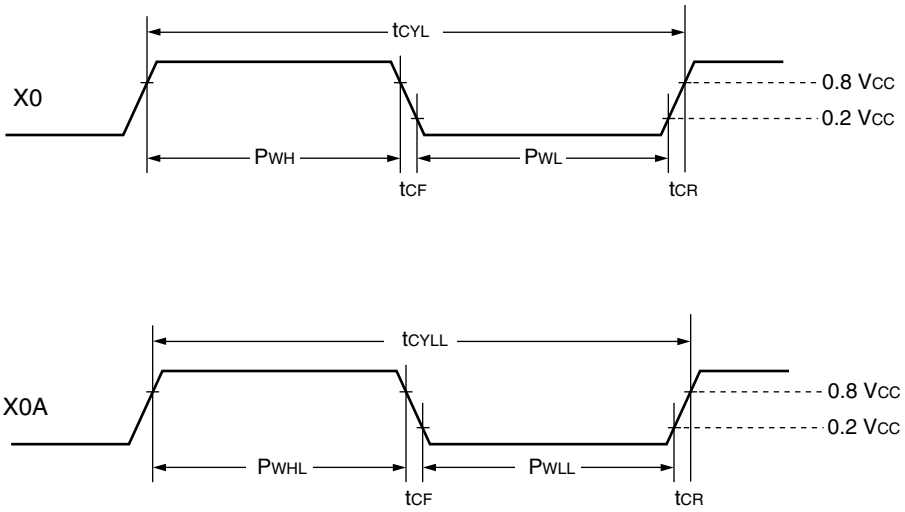
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | When using an oscillation circuit |
| | | | 4 | — | 16 | MHz | PLL multiplied by 1<br>When using an oscillation circuit |
| | | | 4 | — | 12 | MHz | PLL multiplied by 2<br>When using an oscillation circuit |
| | | | 4 | — | 8 | MHz | PLL multiplied by 3<br>When using an oscillation circuit |
| | | | 4 | — | 6 | MHz | PLL multiplied by 4<br>When using an oscillation circuit |
| | | | — | — | 4 | MHz | PLL multiplied by 6<br>When using an oscillation circuit |
| | | | 3 | — | 24 | MHz | When using an external clock* |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | 100 | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | 62.5 | — | 333 | ns | When using an oscillation circuit |
| | | X0, X1 | 41.67 | — | 333 | ns | When using an external clock |
| | $t_{CYLL}$ | X0A, X1A | 10 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30% to 70%. |
| | $P_{WHL}$, $P_{WLL}$ | X0A | 5 | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | — | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.



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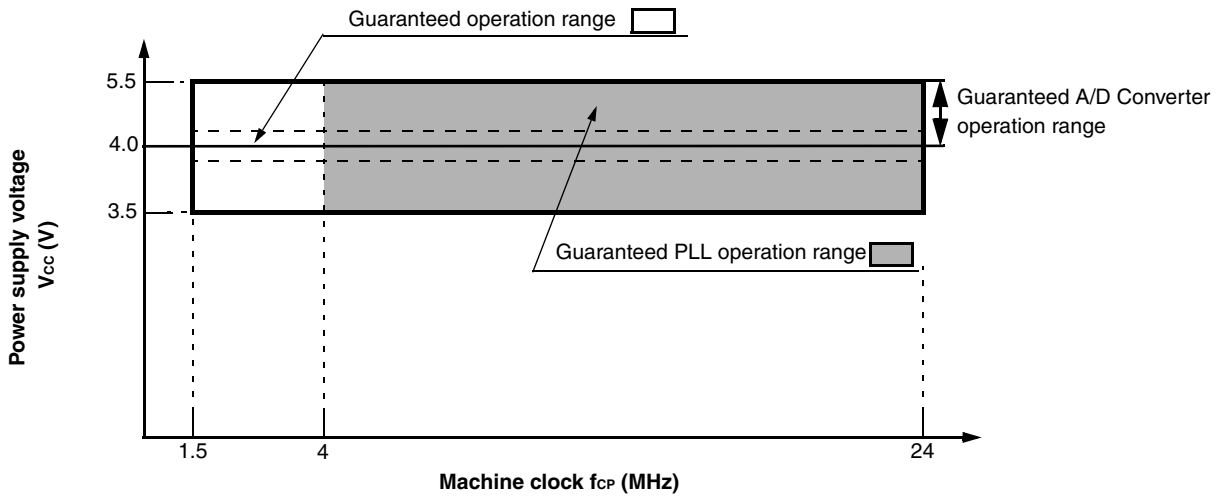
Clock Timing



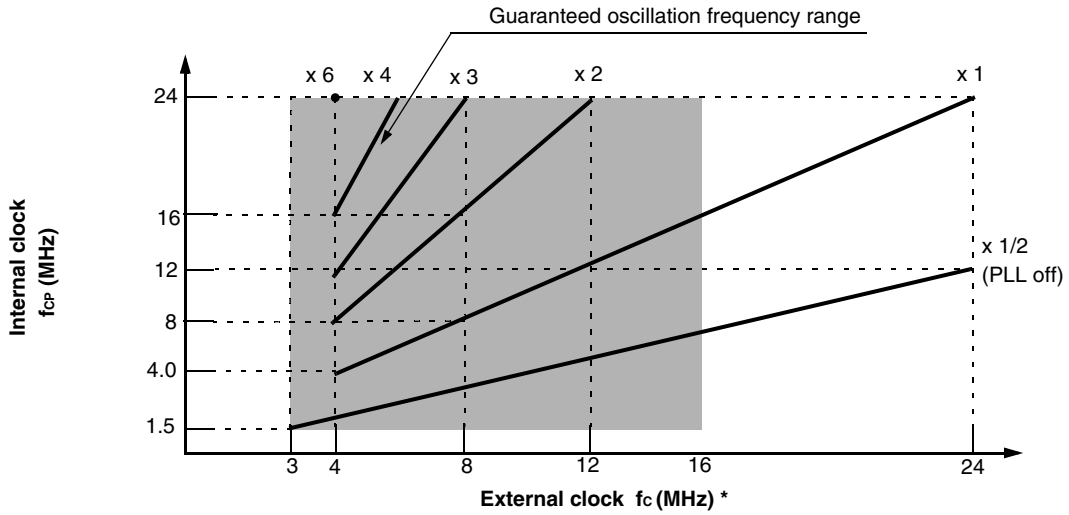



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Guaranteed PLL operation range




**Guaranteed operation range of MB90340E series**




* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz



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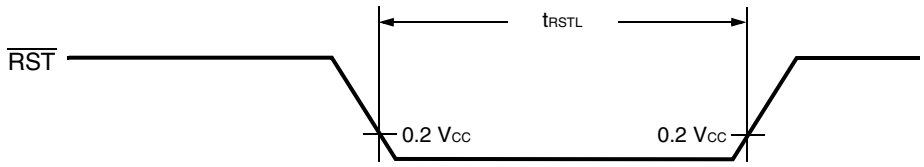
### (2) Reset Standby Input

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

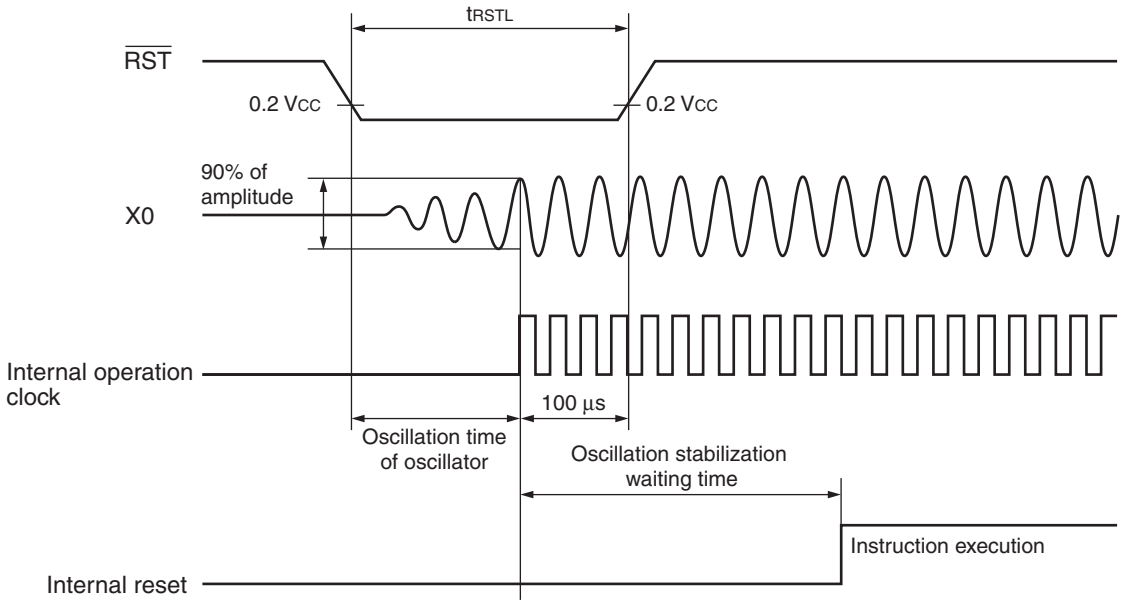
| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500 | — | ns | Under normal operation |
| | | | Oscillation time of oscillator* + 100 µs | — | µs | In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode |
| | | | 100 | — | µs | In Time Timer mode |

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

• **Under normal operation:**




• **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



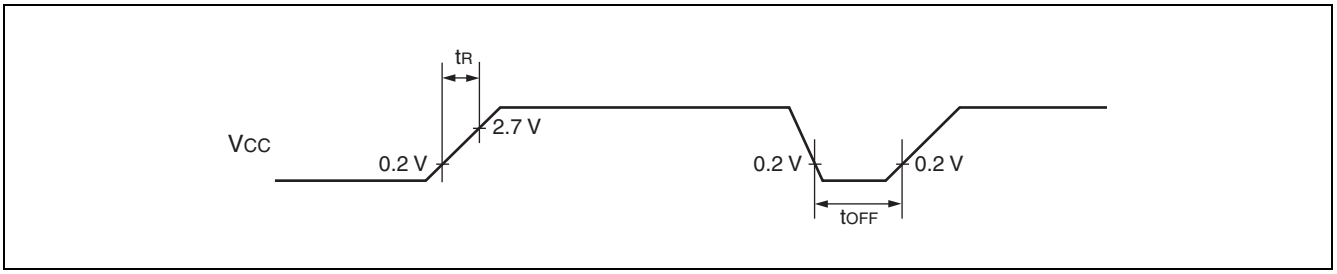



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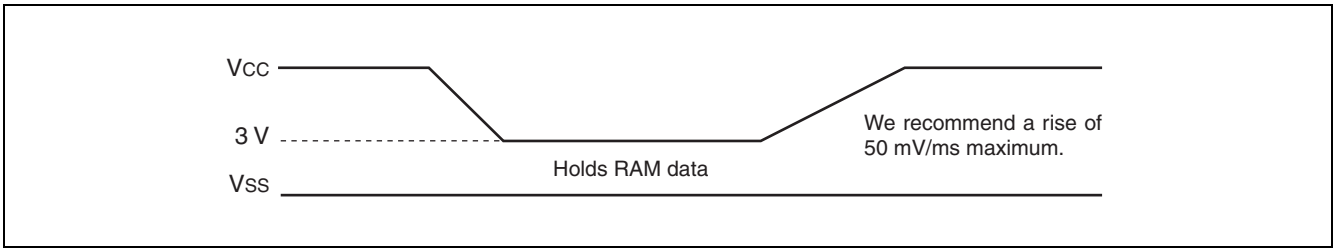
### (3) Power On Reset

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power on rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power off time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Waiting time until power-on |



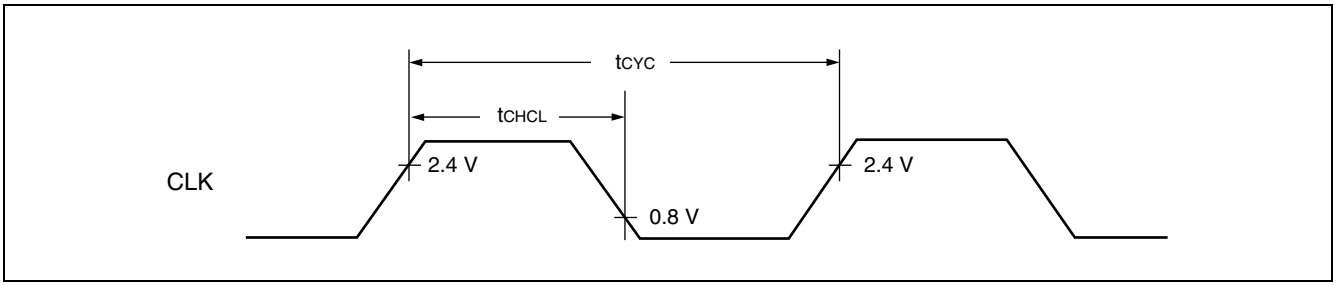

Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.




### (4) Clock Output Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP}$ ≤ 24 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | CLK | — | 62.5 | — | ns | $f_{CP}$ = 16 MHz |
| | | | | 41.67 | — | ns | $f_{CP}$ = 24 MHz |
| CLK ↑ → CLK ↓ | $t_{CHCL}$ | CLK | — | 20 | — | ns | $f_{CP}$ = 16 MHz |
| | | | | 13 | — | ns | $f_{CP}$ = 24 MHz |



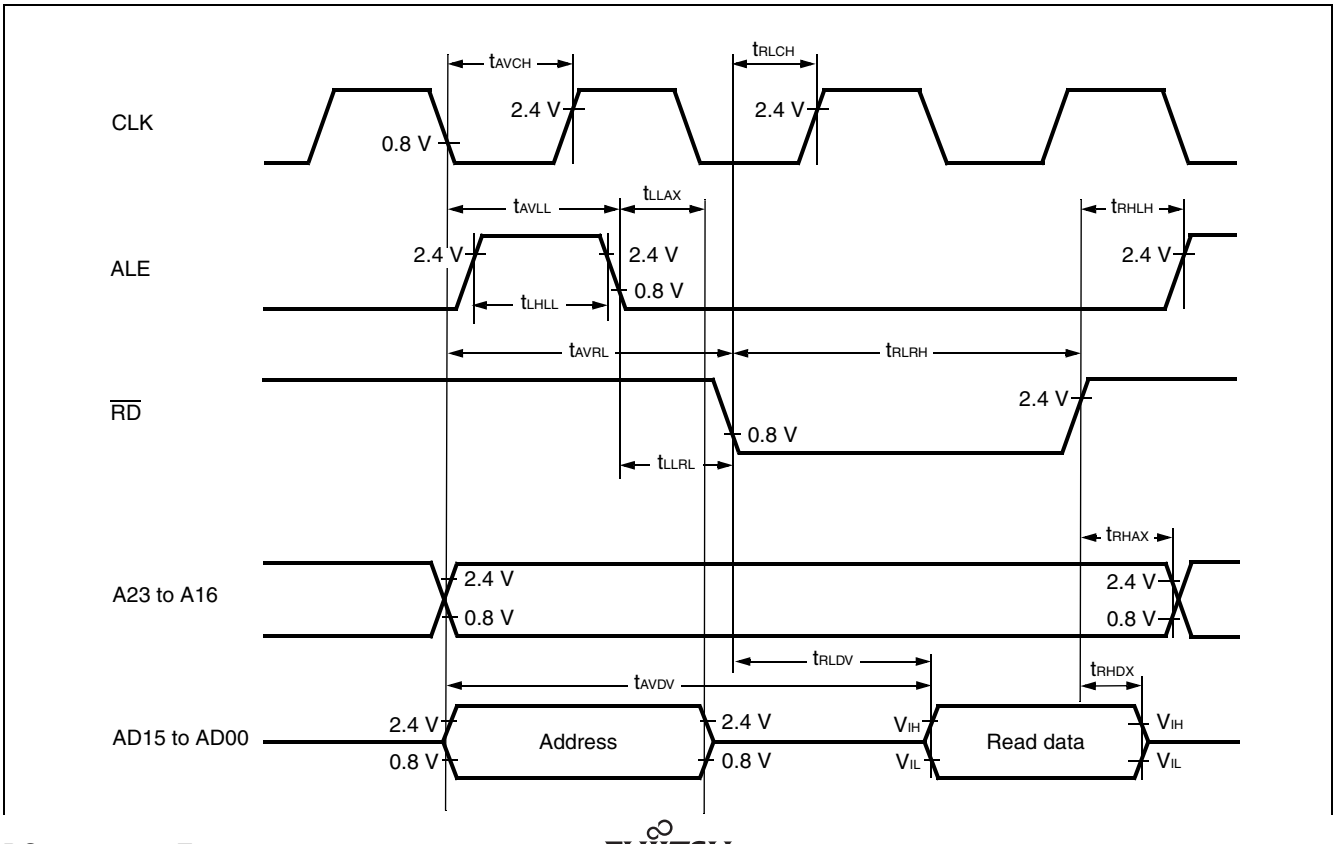



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### (5) Bus Timing (Read)

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP} \leq$ 24 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| ALE pulse width | $t_{LHLL}$ | ALE | — | $t_{CP}/2 - 10$ | — | ns |
| Valid address → ALE ↓ time | $t_{AVLL}$ | ALE, A23 to A16, AD15 to AD00 | | $t_{CP}/2 - 20$ | — | ns |
| ALE ↓ → Address valid time | $t_{LLAX}$ | ALE, AD15 to AD00 | | $t_{CP}/2 - 15$ | — | ns |
| Valid address → $\overline{RD}$ ↓ time | $t_{AVRL}$ | A23 to A16, AD15 to AD00, $\overline{RD}$ | | $t_{CP} - 15$ | — | ns |
| Valid address → Valid data input | $t_{AVDV}$ | A23 to A16, AD15 to AD00 | | — | $5\ t_{CP}/2 - 60$ | ns |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | | $3\ t_{CP}/2 - 20$ | — | ns |
| $\overline{RD}$ ↓ → Valid data input | $t_{RLDV}$ | $\overline{RD}$, AD15 to AD00 | | — | $3\ t_{CP}/2 - 50$ | ns |
| $\overline{RD}$ ↑ → Data hold time | $t_{RHDX}$ | $\overline{RD}$, AD15 to AD00 | | 0 | — | ns |
| $\overline{RD}$ ↑ → ALE ↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | | $t_{CP}/2 - 15$ | — | ns |
| $\overline{RD}$ ↑ → Address valid time | $t_{RHAX}$ | $\overline{RD}$, A23 to A16 | | $t_{CP}/2 - 10$ | — | ns |
| Valid address → CLK ↑ time | $t_{AVCH}$ | A23 to A16, AD15 to AD00, CLK | | $t_{CP}/2 - 16$ | — | ns |
| $\overline{RD}$ ↓ → CLK ↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $t_{CP}/2 - 15$ | — | ns |
| ALE ↓ → $\overline{RD}$ ↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | | $t_{CP}/2 - 15$ | — | ns |



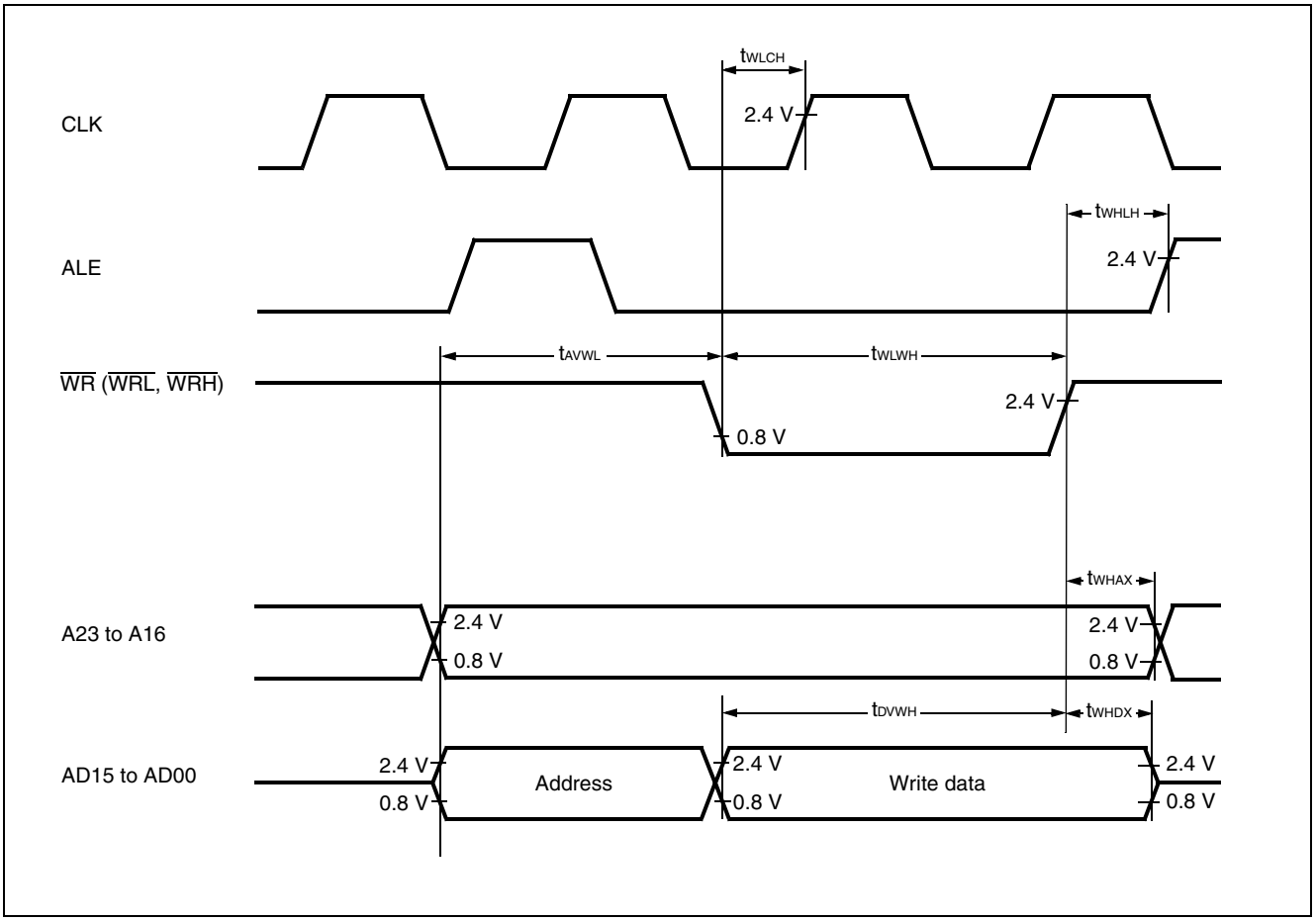



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### (6) Bus Timing (Write)

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP}$ ≤ 24 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Valid address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 to A16, AD15 to AD00, $\overline{WR}$ | — | $t_{CP}$–15 | — | ns |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns |
| Valid data output → $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD15 to AD00, $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns |
| $\overline{WR}$ ↑ → Data hold time | $t_{WHDX}$ | AD15 to AD00, $\overline{WR}$ | | 15 | — | ns |
| $\overline{WR}$ ↑ → Address valid time | $t_{WHAX}$ | A23 to A16, $\overline{WR}$ | | $t_{CP}$/2 – 10 | — | ns |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | | $t_{CP}$/2 – 15 | — | ns |
| $\overline{WR}$ ↓ → CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | | $t_{CP}$/2 – 15 | — | ns |





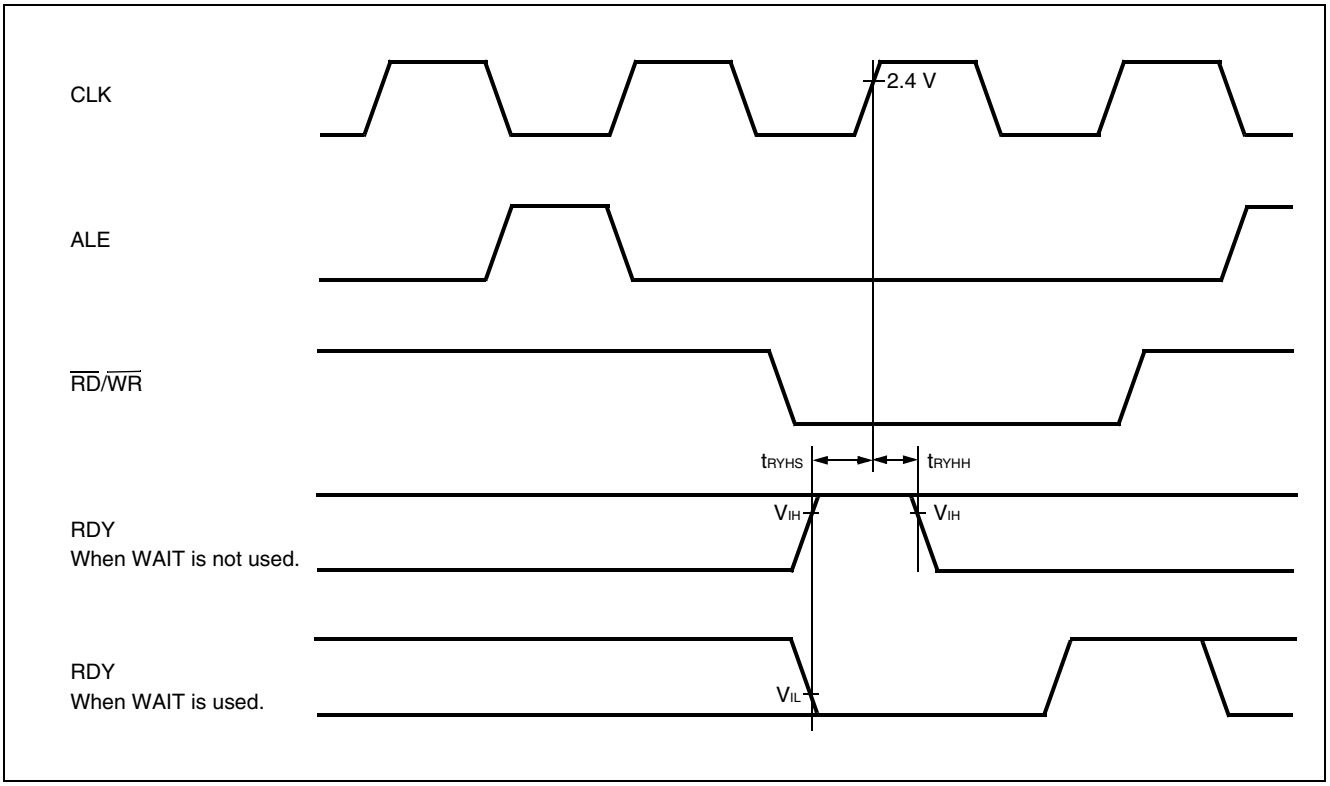

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### (7) Ready Input Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP}$ ≤ 24 MHz)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | $f_{CP}$ = 16 MHz |
| | | | | 32 | — | ns | $f_{CP}$ = 24 MHz |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note : If the RDY setup time is insufficient, use the auto-ready function.





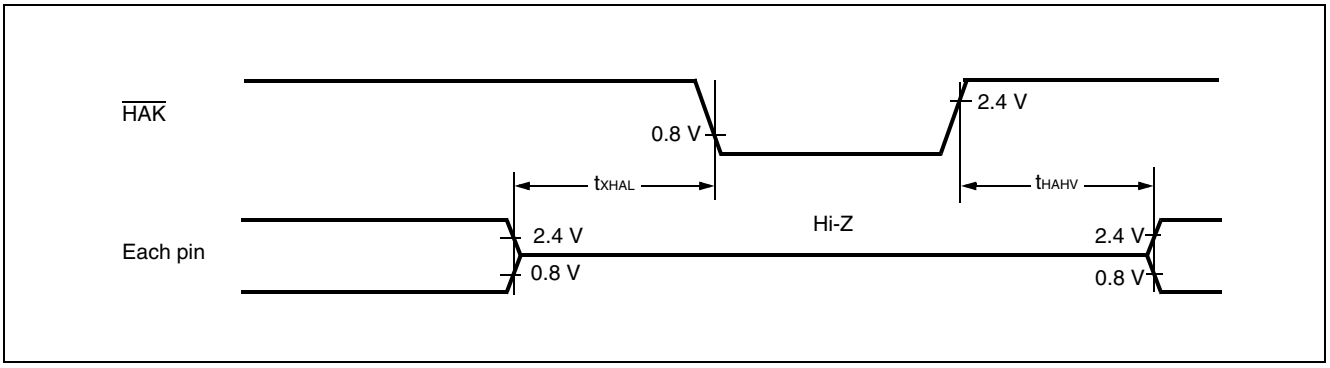

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### (8) Hold Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP}$ ≤ 24 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Pin floating → $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | $t_{CP}$ | ns |
| $\overline{HAK}$ ↑ time → Pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | | $t_{CP}$ | 2 $t_{CP}$ | ns |

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.






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### (9) LIN-UART0/1/2/3

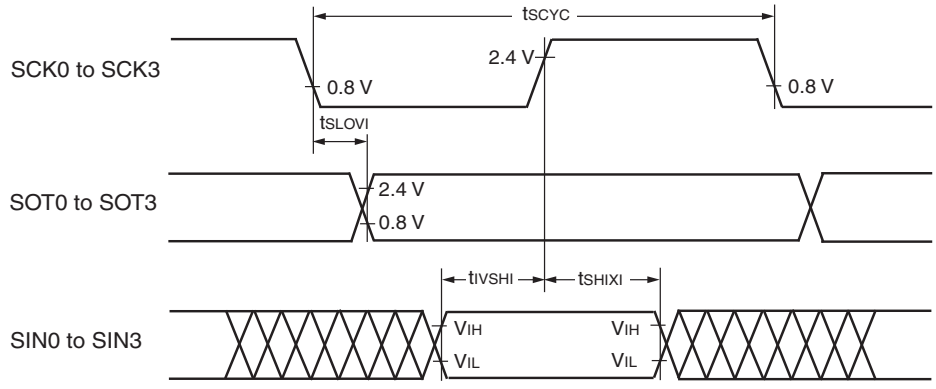
- **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SHSL}$ | SCK0 to SCK3 | External shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 3 $t_{CP}$ - $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SLSH}$ | SCK0 to SCK3 | | $t_{CP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | SCK0, SCK1, SIN0 to SIN3 | | $t_{CP}$ + 30 | — | ns |
| SCK fall time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK0 to SCK3 | | — | 10 | ns |

Notes :
- AC characteristic in CLK synchronized mode.
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

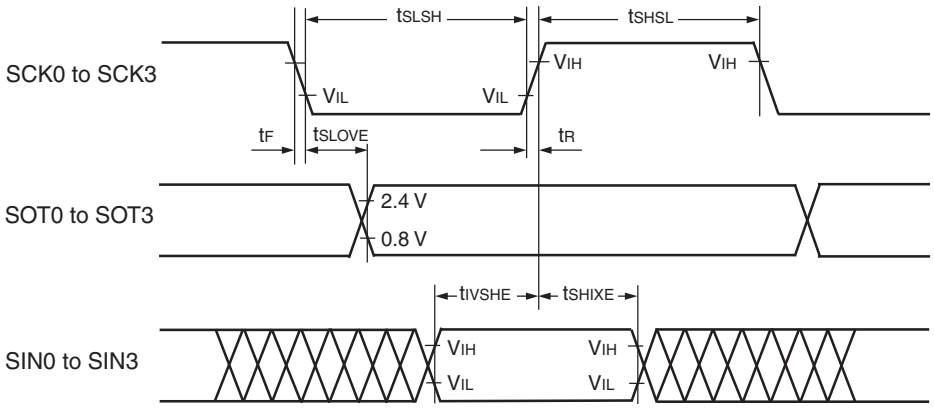
- Internal Shift Clock Mode






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• External Shift Clock Mode




• **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0**

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS}$ = 0 V)

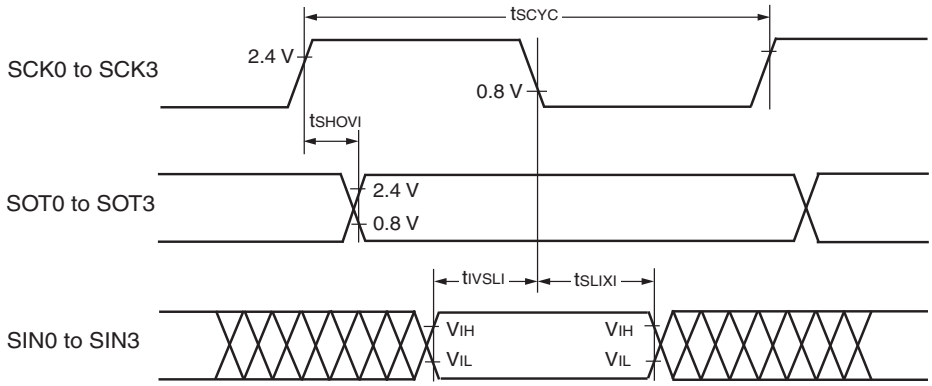
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0 to SCK3 | External shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 3 $t_{CP}$ - $t_R$ | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK0 to SCK3 | | $t_{CP}$ + 10 | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXE}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 30 | — | ns |
| SCK fall time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK0 to SCK3 | | — | 10 | ns |

Notes : • $C_L$ is load capacity value of pins when testing.
• $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

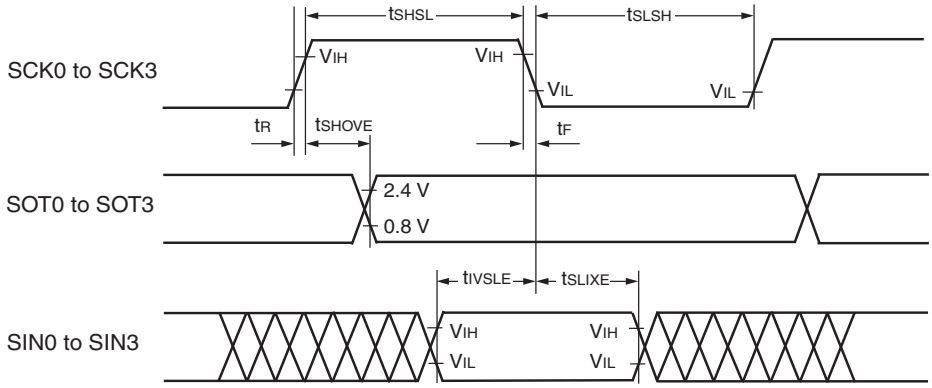


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• Internal Shift Clock Mode




• External Shift Clock Mode





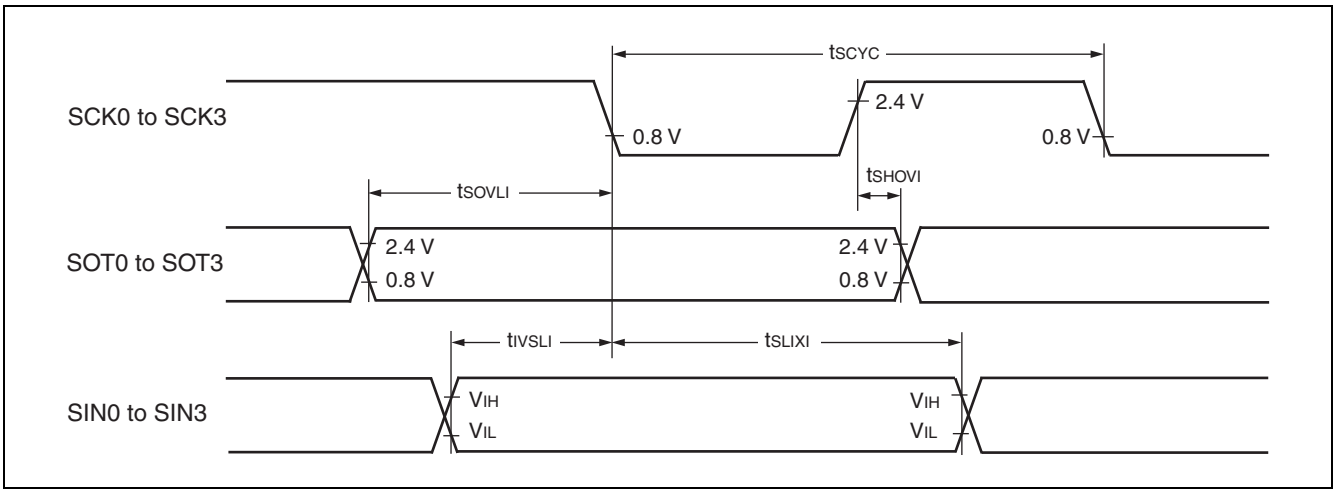

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- **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes : • $C_L$ is load capacity value of pins when testing.
• $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.





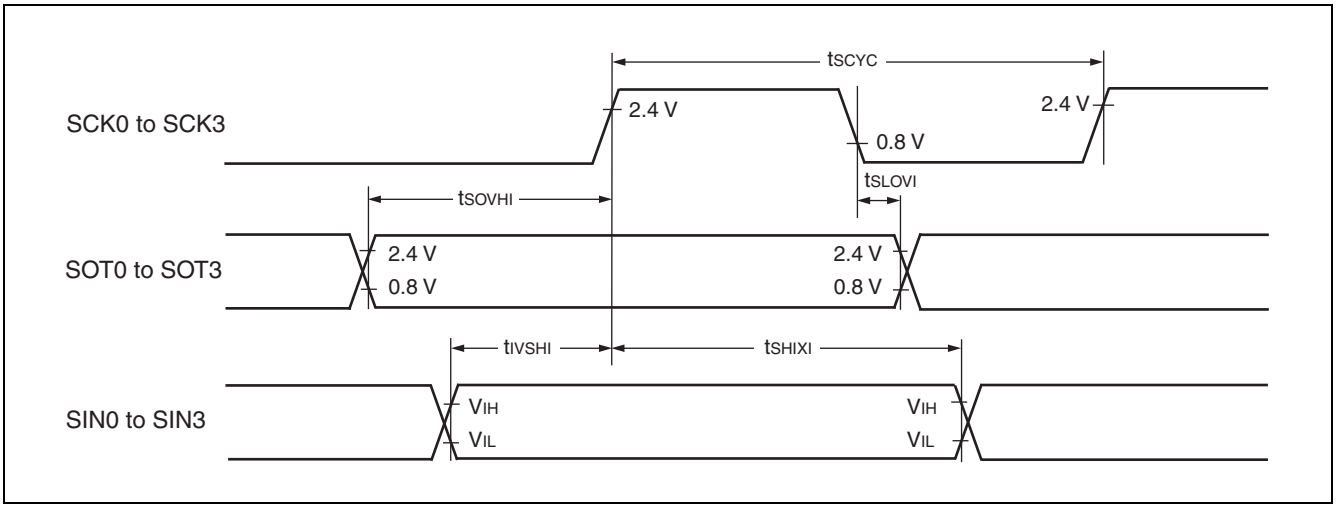

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- **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1**

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes : • $C_L$ is load capacity value of pins when testing.
• $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



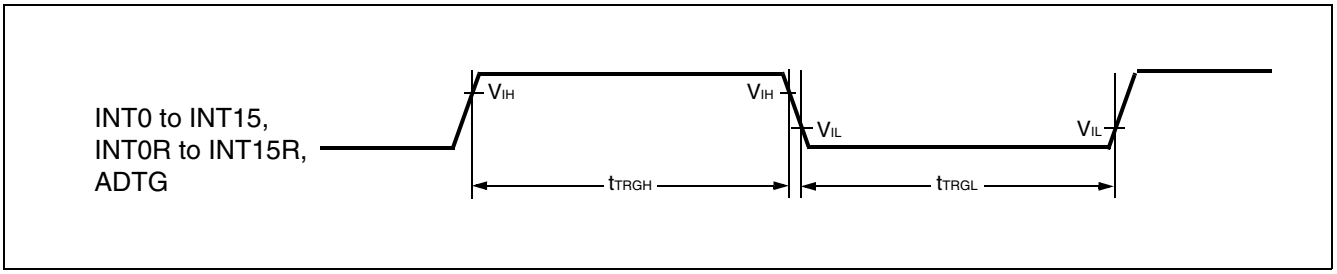



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### (10) Trigger Input Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT15,<br>INT0R to INT15R,<br>ADTG | — | 5 $t_{CP}$ | — | ns |



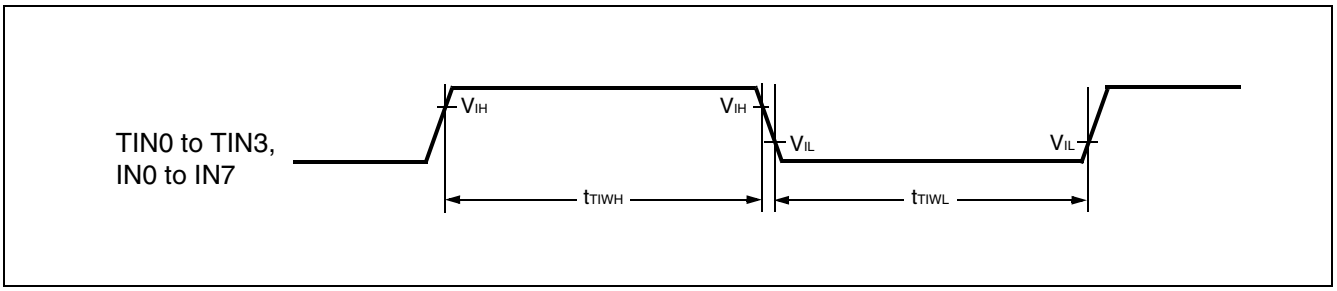



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### (11) Timer Related Resource Input Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

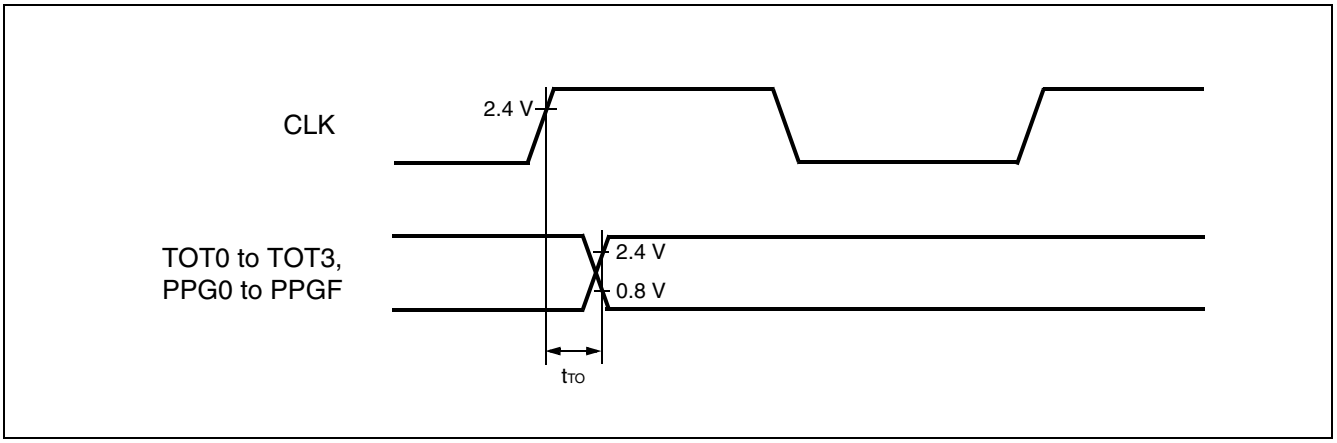
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN0 to TIN3,<br>IN0 to IN7 | — | 4 $t_{CP}$ | — | ns |




### (12) Timer Related Resource Output Timing

($T_A$ = –40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| CLK ↑ → $T_{OUT}$ change time | $t_{TO}$ | TOT0 to TOT3,<br>PPG0 to PPGF | — | 30 | — | ns |






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### (13) I²C Timing

($T_A$ = –40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V)

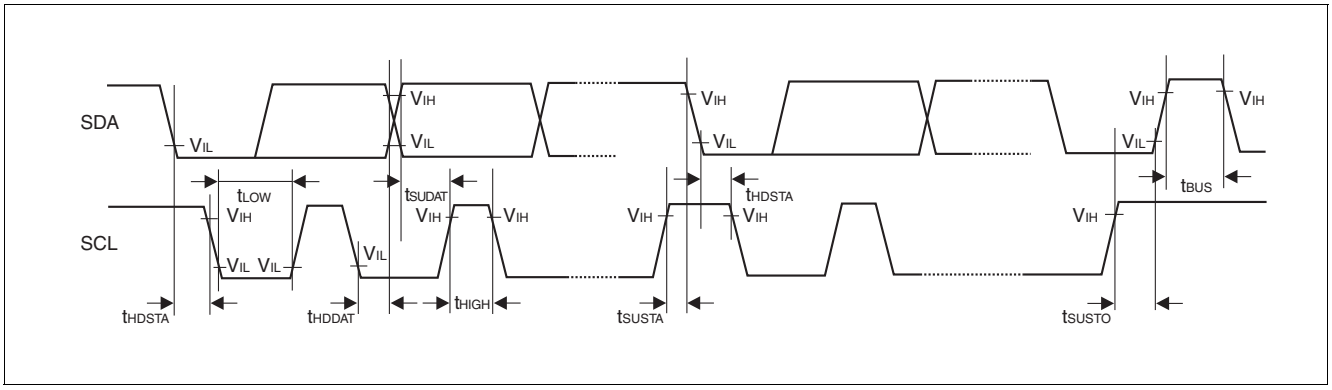
| Parameter | Symbol | Condition | Standard-mode | | Fast-mode*1 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | R = 1.7 kΩ, C = 50 pF*2 | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition SDA↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | — | 0.6 | — | µs |
| "L" width of the SCL clock | $t_{LOW}$ | | 4.7 | — | 1.3 | — | µs |
| "H" width of the SCL clock | $t_{HIGH}$ | | 4.0 | — | 0.6 | — | µs |
| Set-up time (repeated) START condition SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*3 | 0 | 0.9*4 | µs |
| Data set-up time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | — | 100 | — | ns |
| Set-up time for STOP condition SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | — | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{BUS}$ | | 4.7 | — | 1.3 | — | µs |

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum $t_{HDDAT}$ meets the requirement that it does not extend the "L" width ($t_{LOW}$) of the SCL signal.

*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.






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## 5. A/D Converter

($T_A$ = –40 °C to +105 °C, 3.0 V ≤ AVRH – AVRL, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | ±3.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential nonlinearity error | — | — | — | — | ±1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | AN0 to AN23 | AVRL – 1.5 × LSB | AVRL + 0.5 × LSB | AVRL + 2.5 × LSB | V | |
| Full scale reading voltage | $V_{FST}$ | AN0 to AN23 | AVRH – 3.5 × LSB | AVRH – 1.5 × LSB | AVRH + 0.5 × LSB | V | |
| Compare time | — | — | 1.0 | — | 16500 | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 2.0 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Sampling time | — | — | 0.5 | — | ∞ | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 1.2 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Analog port input current | $I_{AIN}$ | AN0 to AN23 | –0.3 | — | +0.3 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN23 | AVRL | — | AVRH | V | |
| Reference voltage range | — | AVRH | AVRL + 2.7 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH – 2.7 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 3.5 | 7.5 | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage current | $I_R$ | AVRH | — | 600 | 900 | µA | |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN23 | — | — | 4 | LSB | |

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) .

Note: The accuracy gets worse as |AVRH – AVRL| becomes smaller.

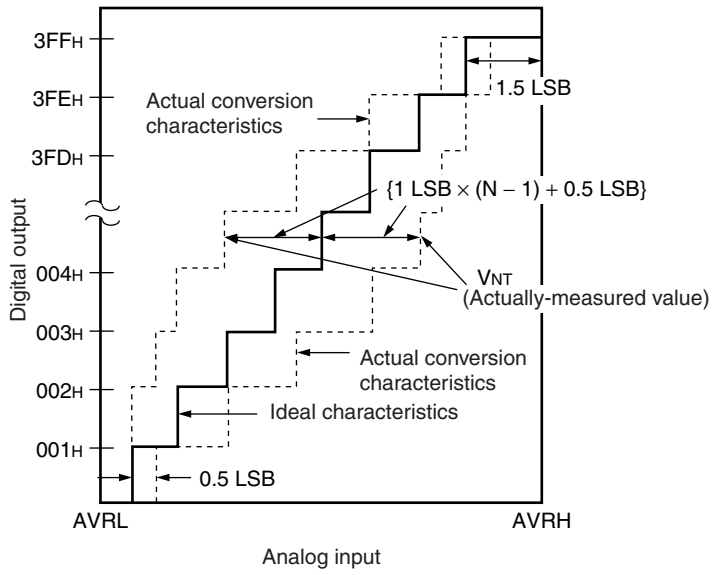


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## 6. Definition of A/D Converter Terms

| | | |
|---|---|---|
| Resolution | : | Analog variation that is recognized by the A/D converter. |
| Non linearity error | : | The deviation between the actual conversion characteristics and a line that joins the zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) to the full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ) . |
| Differential linearity error | : | Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value. |
| Total error | : | Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error. |

Total error




$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

$V_{OT}$ (Ideal value) = AVRL + 0.5 LSB [V]

$V_{FST}$ (Ideal value) = AVRH – 1.5 LSB [V]

$V_{NT}$ : A voltage at which the digital output transitions from $(N - 1)_H$ to $N_H$.

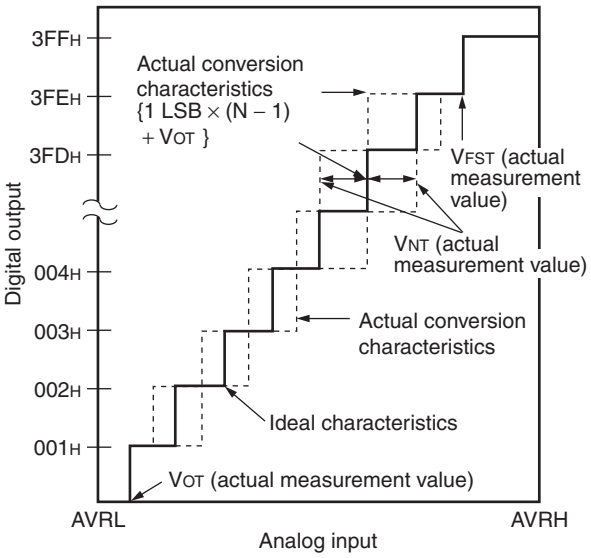
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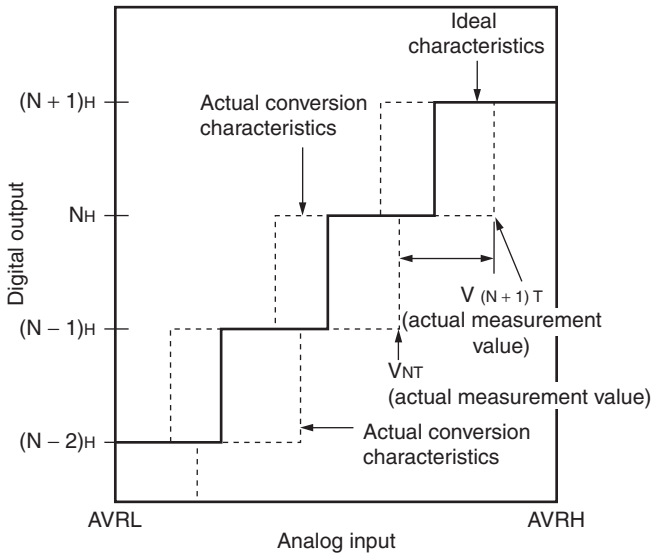
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*(Continued)*

Non linearity error




Differential linearity error




$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : Value of the digital output from the A/D converter
$V_{OT}$ : Voltage at which digital output transits from “$000_H$” to “$001_H$.”
$V_{FST}$ : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”



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## 7. Notes on A/D Converter Section

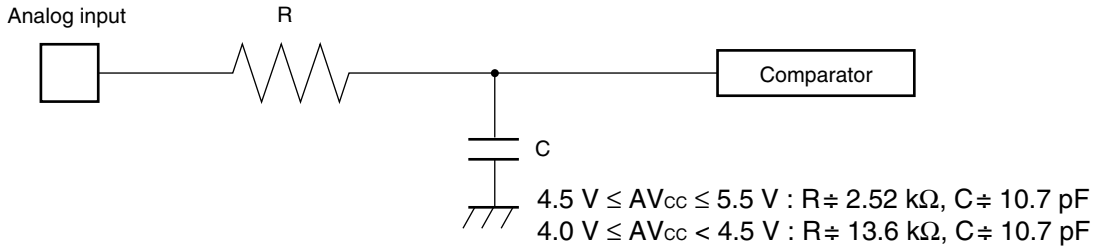
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ $AV_{CC}$ ≤ 5.5 V, sampling period = 0.5 µs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model




Note : Use the values in the figure only as a guideline.



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## 8. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = +25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes programming prior to erasure |
| Chip erase time | | — | 9 | — | s | Excludes programming prior to erasure |
| Word (16-bit width) programming time | | — | 16 | 3600 | µs | Except for the over head time of the system |
| Program/Erase cycle | — | 10000 | — | — | cycle | |
| Flash Data Retention Time | Average<br>$T_A$ = +85 °C | 20 | — | — | year | * |

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .



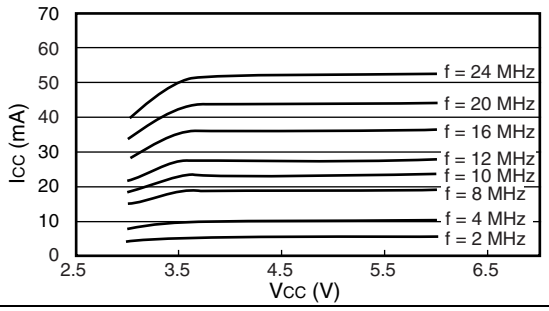
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## ■ EXAMPLE CHARACTERISTICS

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

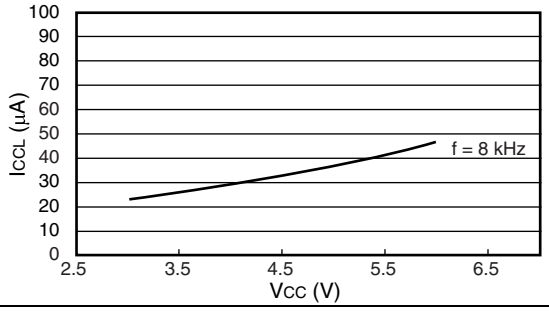
$I_{CC}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



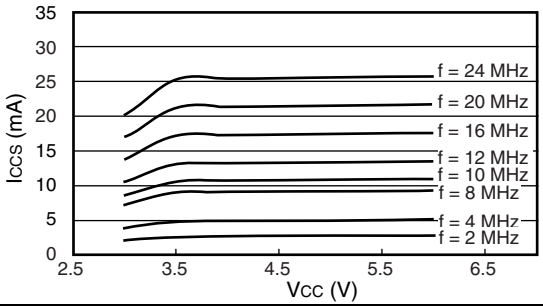

$I_{CCL}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



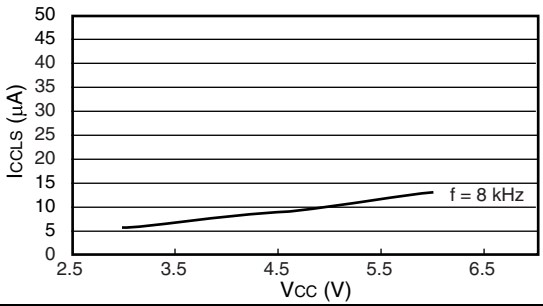

$I_{CCS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



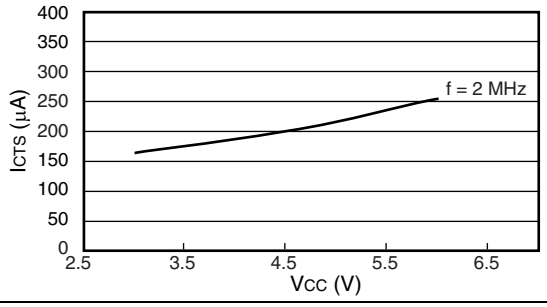

$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



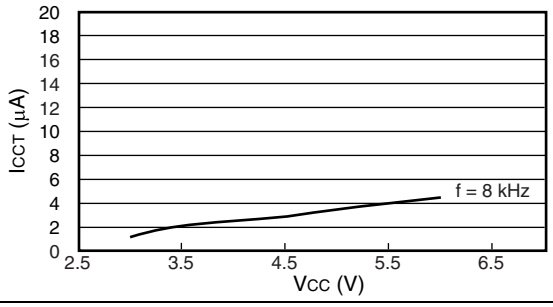

$I_{CTS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



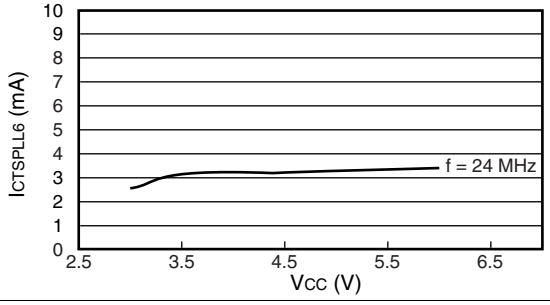

$I_{CCT}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



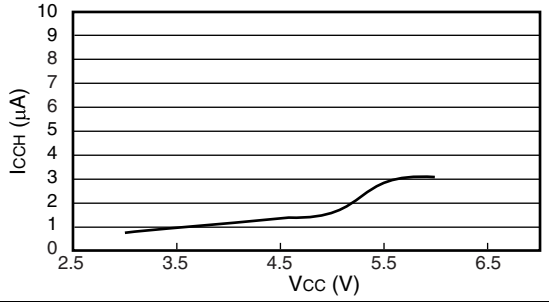

$I_{CTSPLL6}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH}$ – $V_{CC}$

$T_A$ = +25 °C, stopped



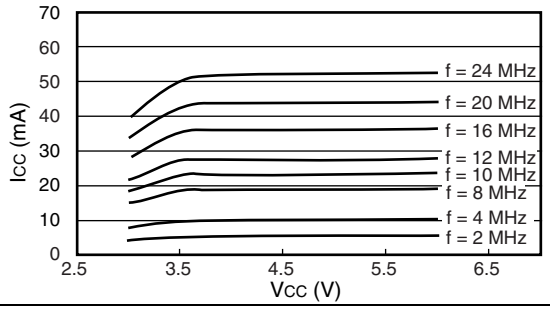



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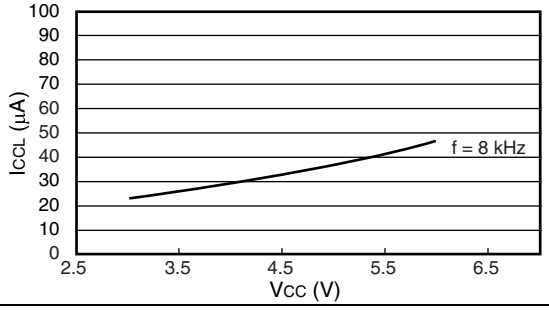
$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



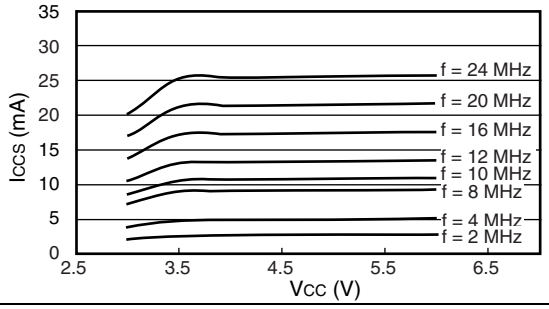

$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



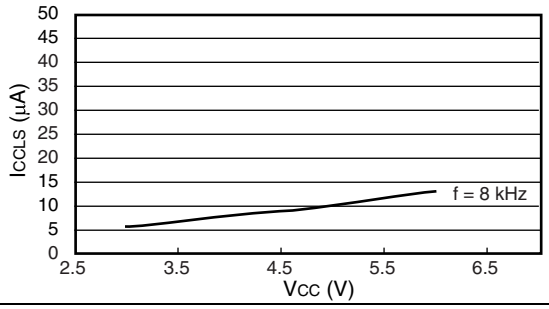

$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



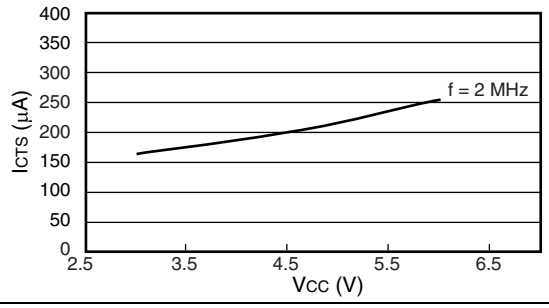

$I_{CCLS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



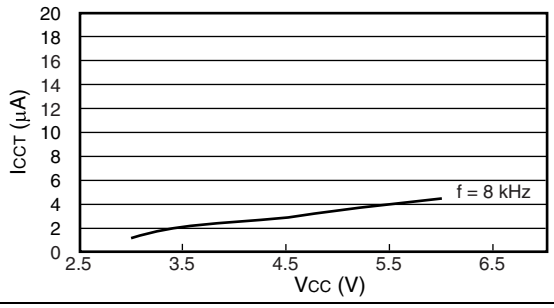

$I_{CTS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



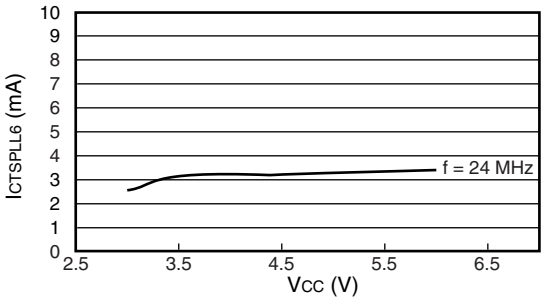

$I_{CCT} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



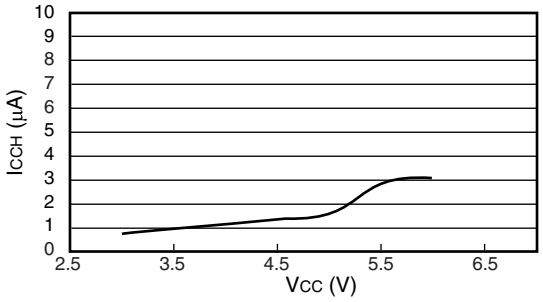

$I_{CTSPLL6} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH} - V_{CC}$

$T_A$ = +25 °C, stopped



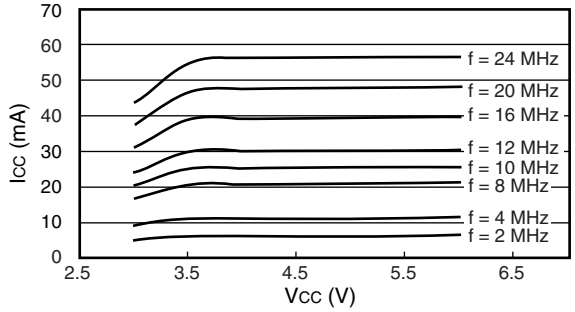



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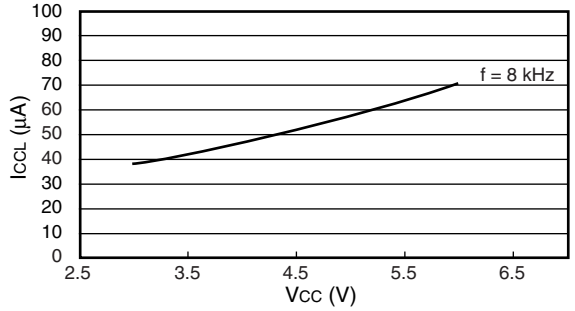
$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



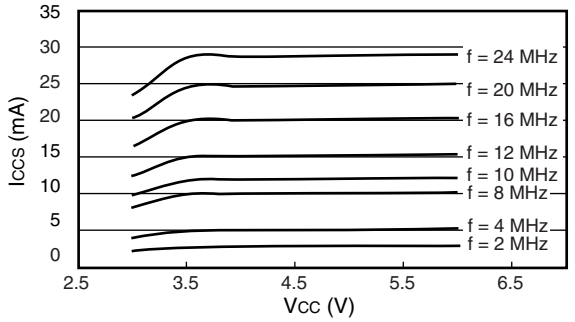

$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



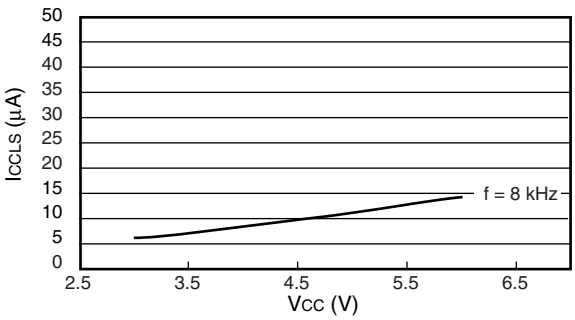

$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



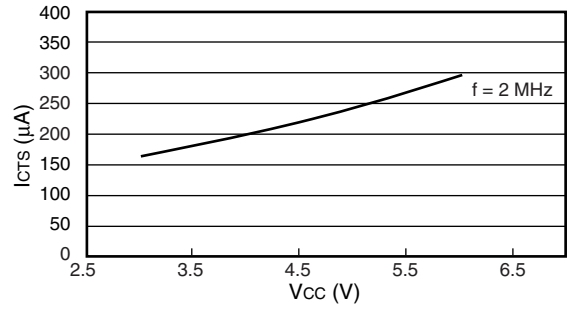

$I_{CCLS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



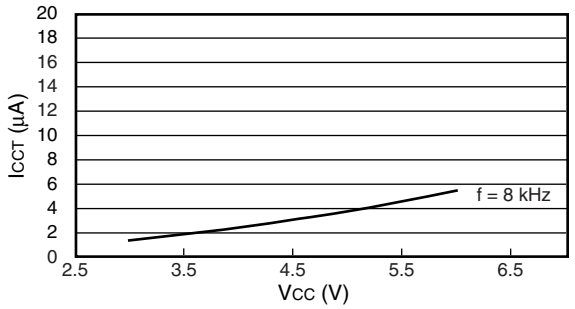

$I_{CTS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



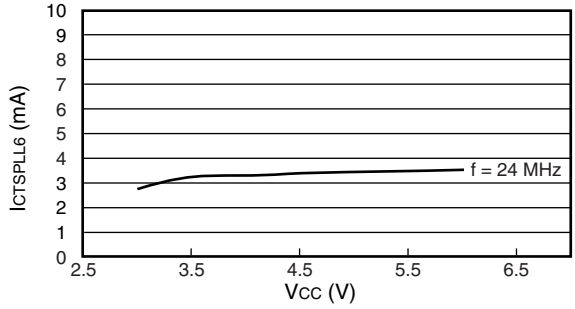

$I_{CCT} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



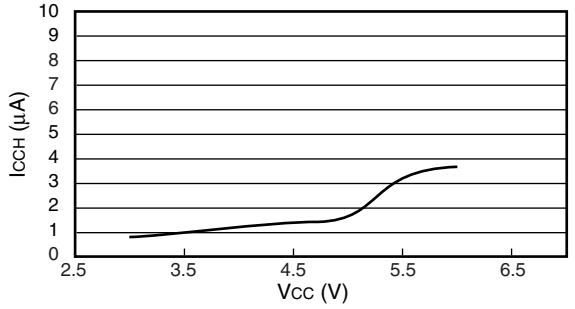

$I_{CTSPLL6} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH} - V_{CC}$

$T_A$ = +25 °C, stopped



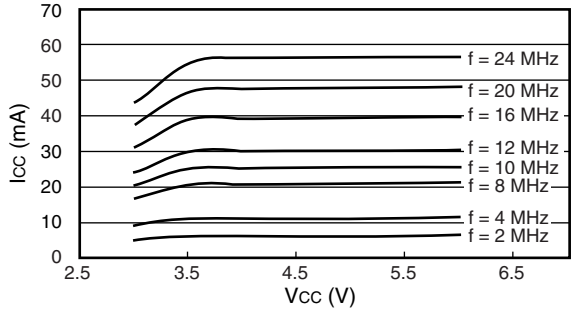



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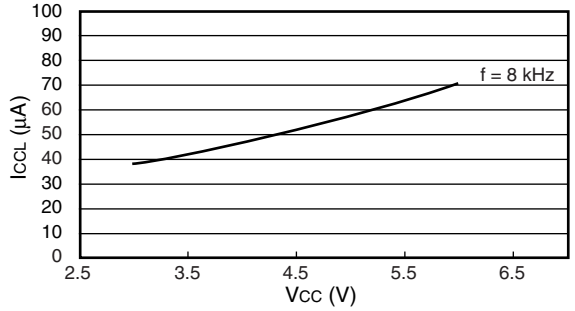
$I_{CC}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



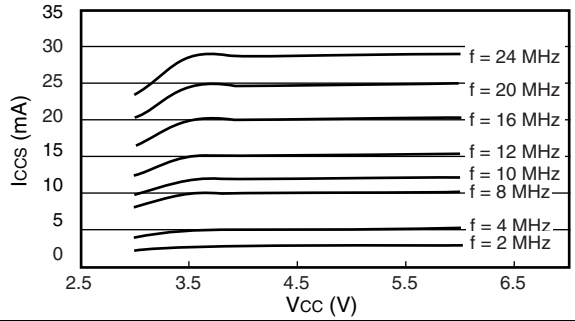

$I_{CCL}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



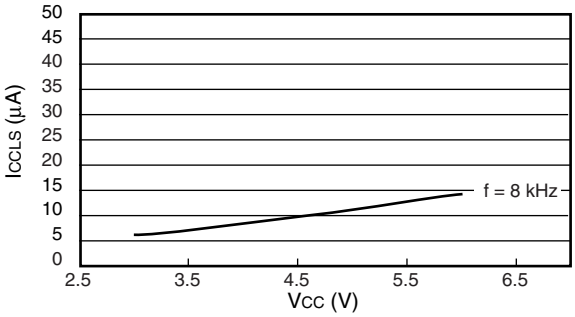

$I_{CCS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



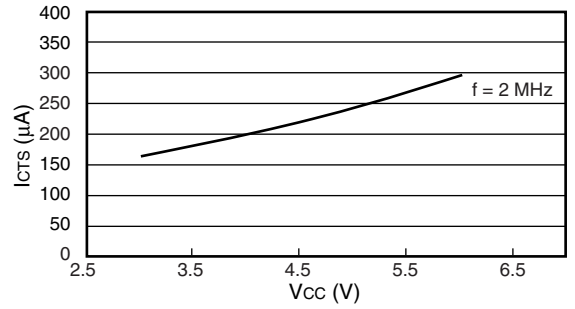

$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



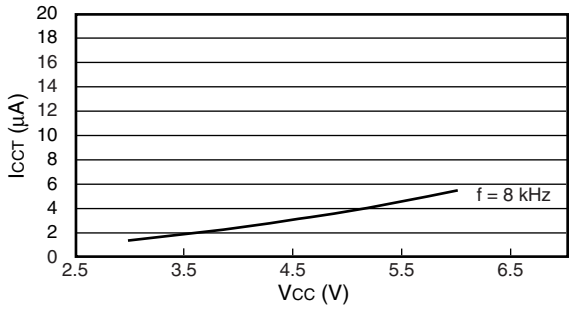

$I_{CTS}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



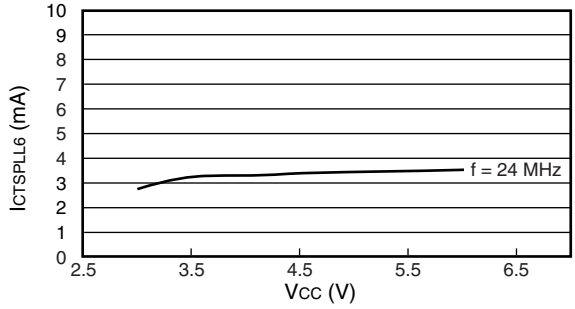

$I_{CCT}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



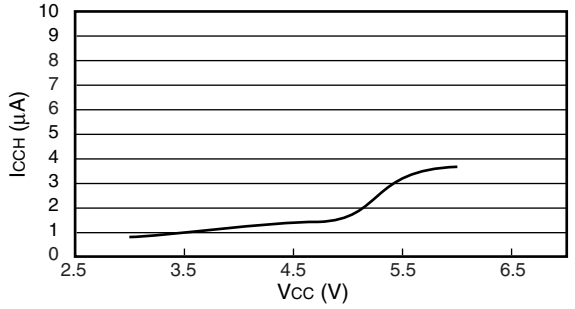

$I_{CTSPLL6}$ – $V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH}$ – $V_{CC}$

$T_A$ = +25 °C, stopped



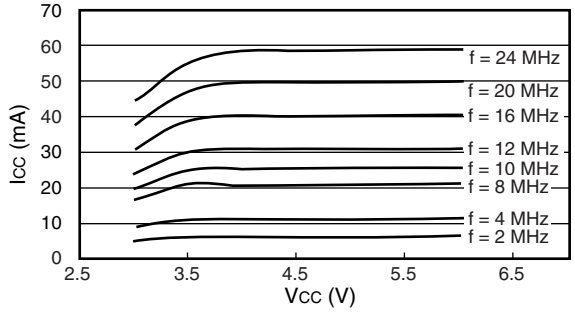



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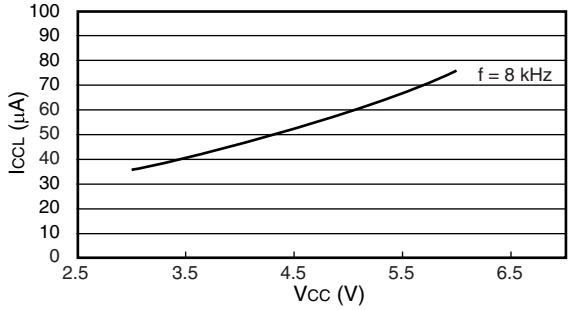
$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



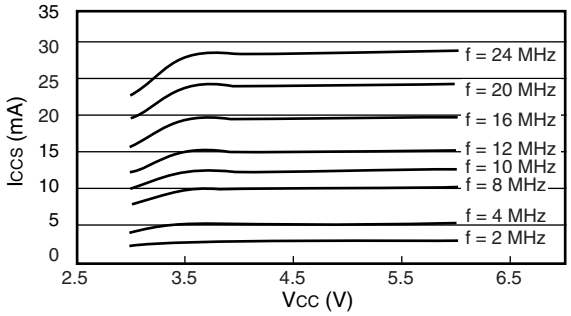

$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



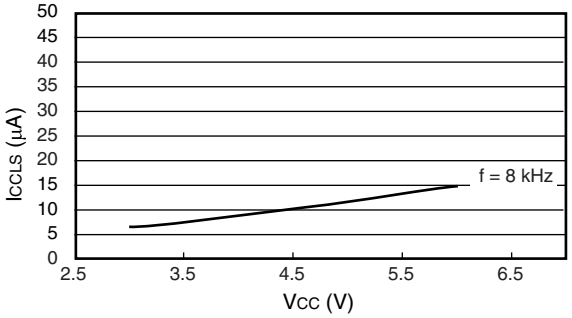

$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



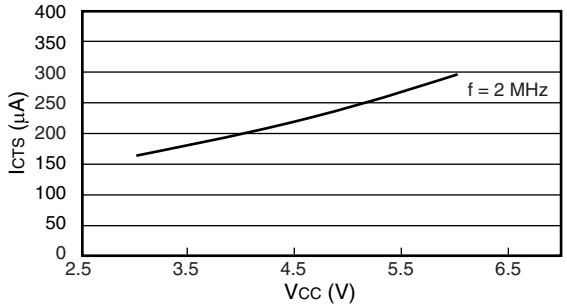

$I_{CCLS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



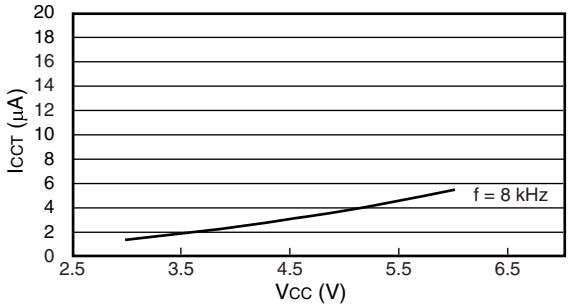

$I_{CTS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



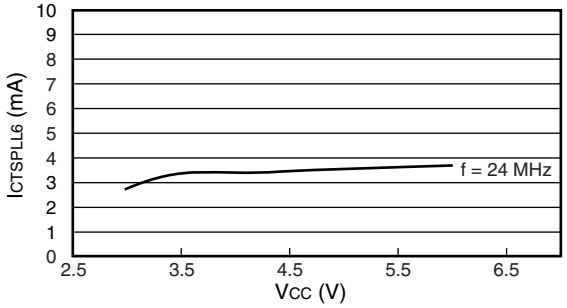

$I_{CCT} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



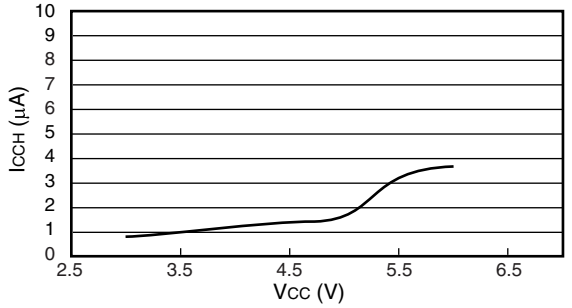

$I_{CTSPLL6} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH} - V_{CC}$

$T_A$ = +25 °C, stopped



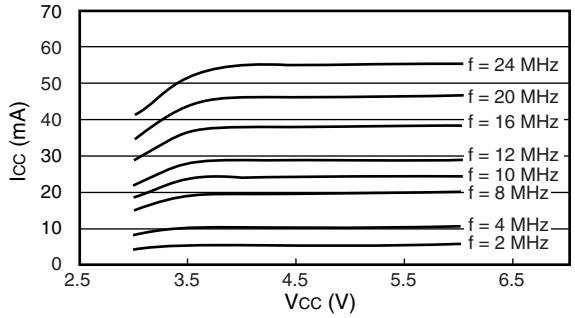



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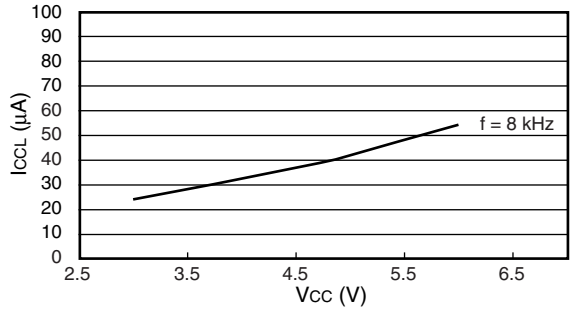
$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



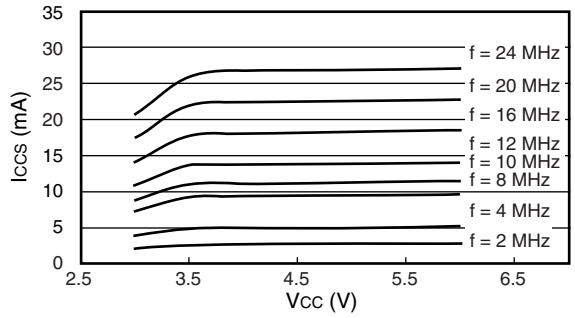

$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



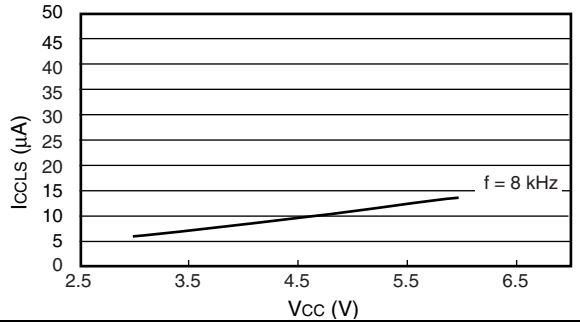

$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



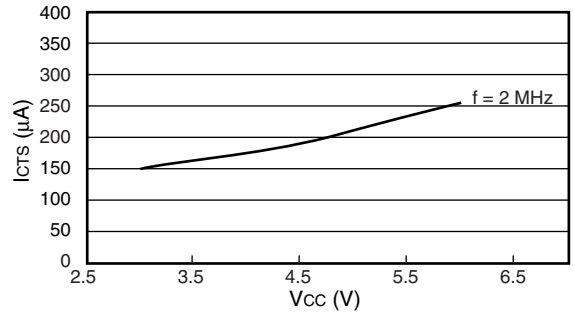

$I_{CCLS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



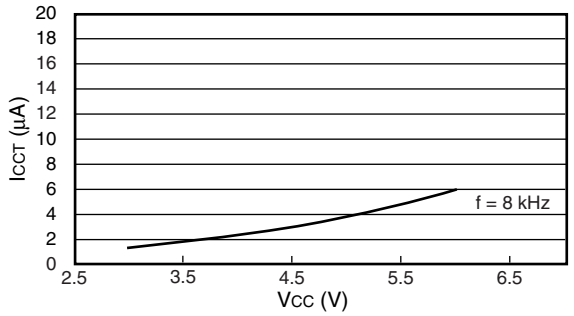

$I_{CTS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



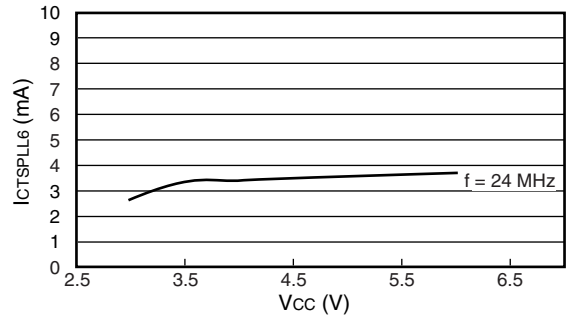

$I_{CCT} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



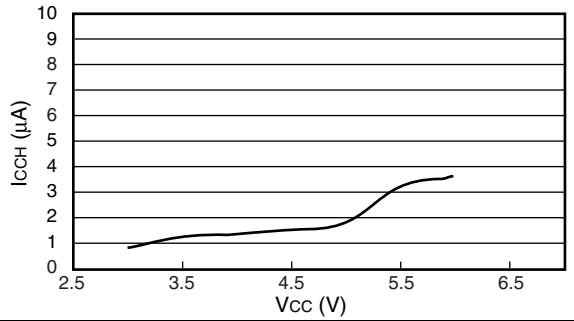

$I_{CTSPLL6} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH} - V_{CC}$

$T_A$ = +25 °C, stopped



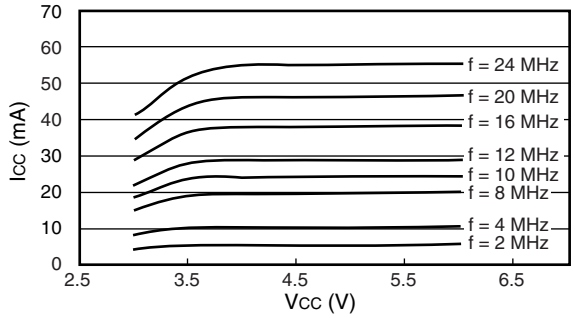



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- MB90347E, MB90347ES, MB90347CE, MB90347CES

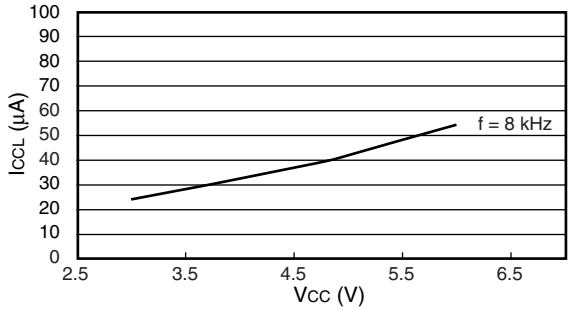
$I_{CC} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



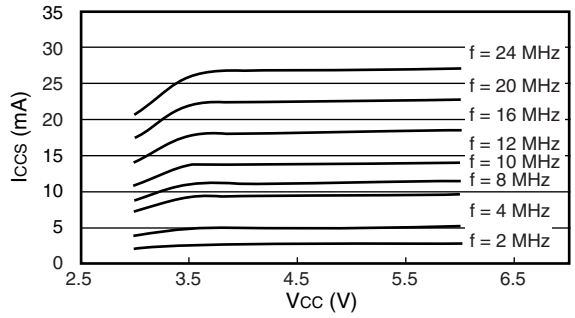

$I_{CCL} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



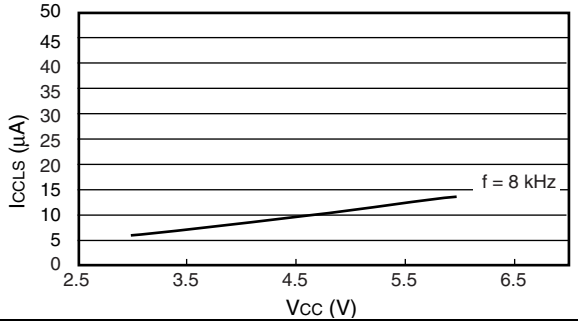

$I_{CCS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



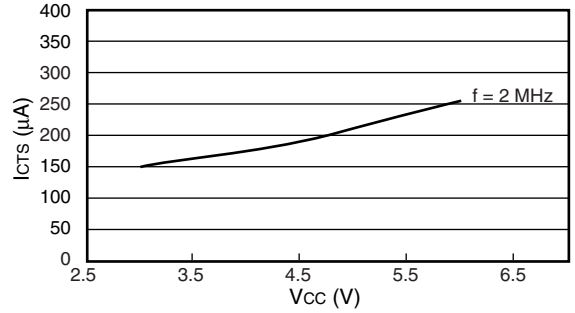

$I_{CCLS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



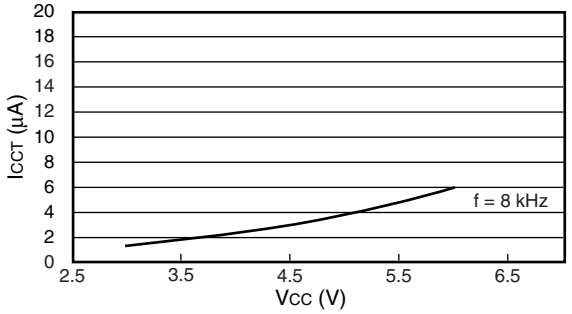

$I_{CTS} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



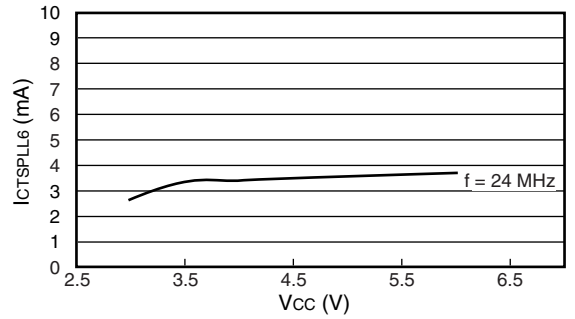

$I_{CCT} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency



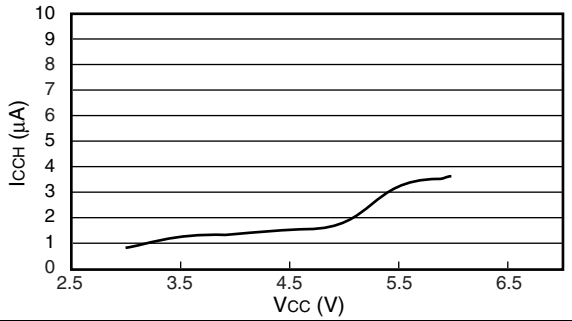

$I_{CTSPLL6} - V_{CC}$

$T_A$ = +25 °C, external clock operation
f = Internal operation frequency




$I_{CCH} - V_{CC}$

$T_A$ = +25 °C, stopped



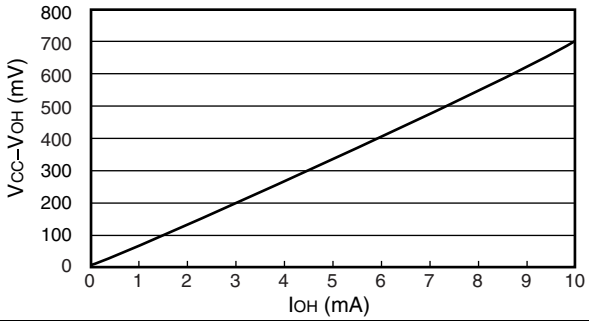



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• I/O characteristics

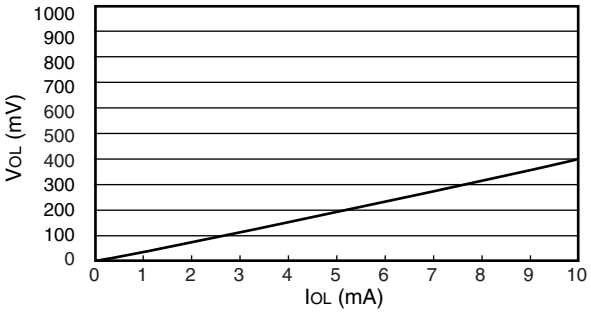
$(V_{CC}-V_{OH})$ – $I_{OH}$

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V



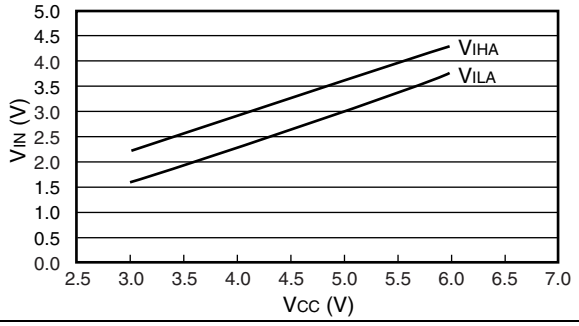

$V_{OL}$ – $I_{OL}$

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V




Automotive $V_{IN}$ – $V_{CC}$

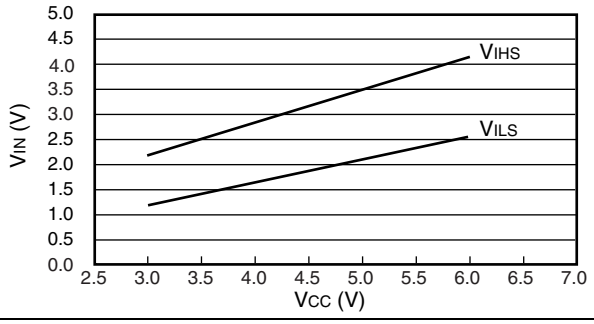
$T_A$ = +25 °C




CMOS $V_{IN}$ – $V_{CC}$

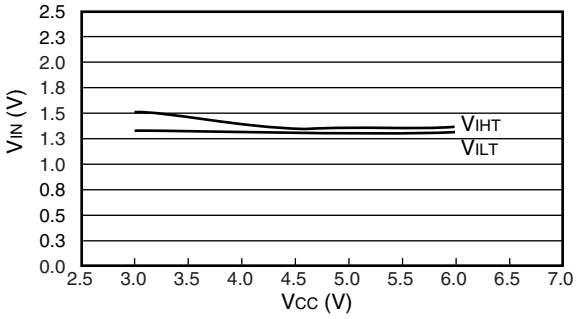
Other than UART-SIN pin and I²C pin

$T_A$ = +25 °C




TTL $V_{IN}$ – $V_{CC}$

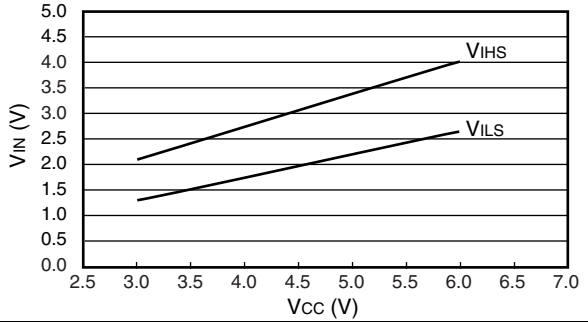
$T_A$ = +25 °C




CMOS $V_{IN}$ – $V_{CC}$

UART-SIN pin, I²C pin

$T_A$ = +25 °C






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## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F342EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F342ESPF | | |
| MB90F342CEPF | | |
| MB90F342CESPF | | |
| MB90F342EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F342ESPMC | | |
| MB90F342CEPMC | | |
| MB90F342CESPMC | | |
| MB90F345EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F345ESPF | | |
| MB90F345CEPF | | |
| MB90F345CESPF | | |
| MB90F345EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F345ESPMC | | |
| MB90F345CEPMC | | |
| MB90F345CESPMC | | |
| MB90F346EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F346ESPF | | |
| MB90F346CEPF | | |
| MB90F346CESPF | | |
| MB90F346EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F346ESPMC | | |
| MB90F346CEPMC | | |
| MB90F346CESPMC | | |

*(Continued)*



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| Part number | Package | Remarks |
|---|---|---|
| MB90F347EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F347ESPF | | |
| MB90F347CEPF | | |
| MB90F347CESPF | | |
| MB90F347EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F347ESPMC | | |
| MB90F347CEPMC | | |
| MB90F347CESPMC | | |
| MB90F349EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F349ESPF | | |
| MB90F349CEPF | | |
| MB90F349CESPF | | |
| MB90F349EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F349ESPMC | | |
| MB90F349CEPMC | | |
| MB90F349CESPMC | | |
| MB90341EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90341ESPF | | |
| MB90341CEPF | | |
| MB90341CESPF | | |
| MB90341EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90341ESPMC | | |
| MB90341CEPMC | | |
| MB90341CESPMC | | |
| MB90342EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90342ESPF | | |
| MB90342CEPF | | |
| MB90342CESPF | | |
| MB90342EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90342ESPMC | | |
| MB90342CEPMC | | |
| MB90342CESPMC | | |

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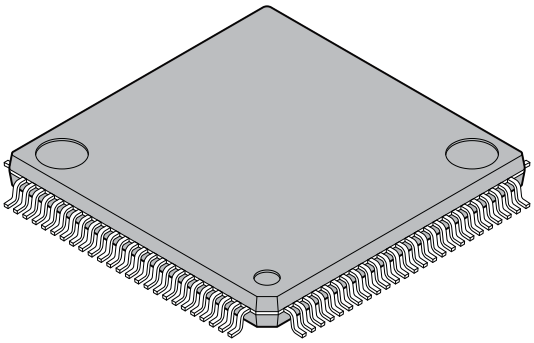
*(Continued)*

| Part number | Package | Remarks |
|---|---|---|
| MB90346EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90346ESPF | | |
| MB90346CEPF | | |
| MB90346CESPF | | |
| MB90346EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90346ESPMC | | |
| MB90346CEPMC | | |
| MB90346CESPMC | | |
| MB90347EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90347ESPF | | |
| MB90347CEPF | | |
| MB90347CESPF | | |
| MB90347EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90347ESPMC | | |
| MB90347CEPMC | | |
| MB90347CESPMC | | |
| MB90348EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90348ESPF | | |
| MB90348CEPF | | |
| MB90348CESPF | | |
| MB90348EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90348ESPMC | | |
| MB90348CEPMC | | |
| MB90348CESPMC | | |
| MB90349EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90349ESPF | | |
| MB90349CEPF | | |
| MB90349CESPF | | |
| MB90349EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90349ESPMC | | |
| MB90349CEPMC | | |
| MB90349CESPMC | | |
| MB90V340E-101CR | 299-pin ceramic PGA (PGA-299C-A01) | For evaluation |
| MB90V340E-102CR | | |



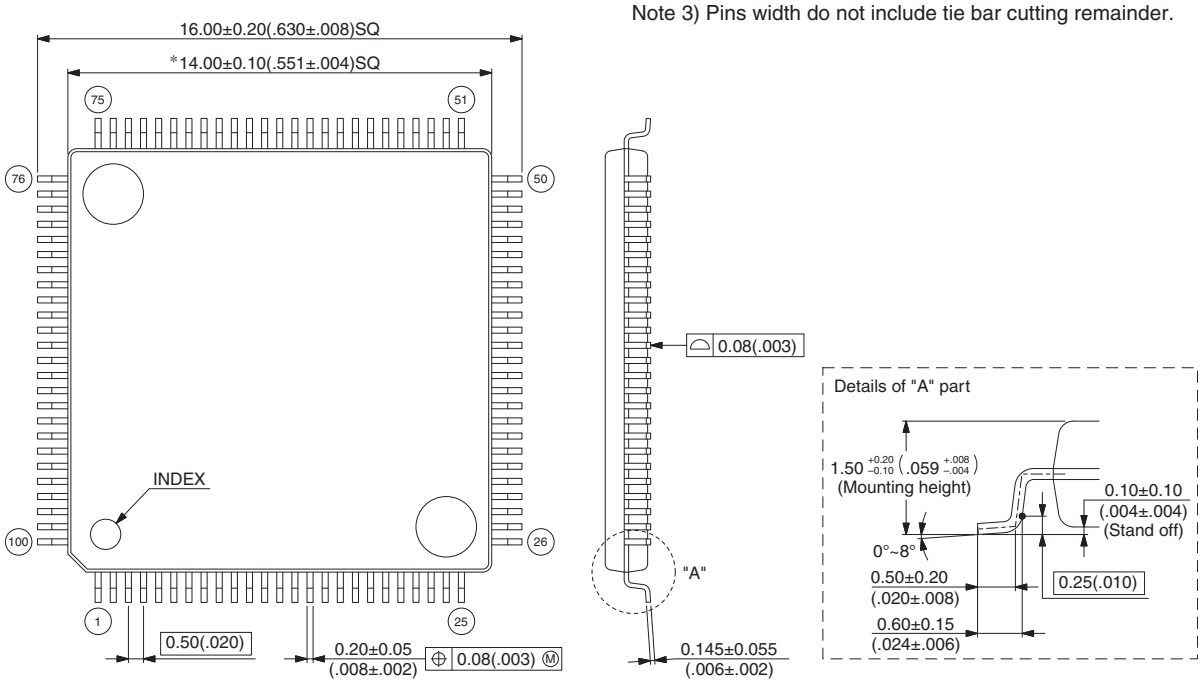
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## ■ PACKAGE DIMENSIONS

| 100-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 14.0 mm × 14.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm Max |
| | Weight | 0.65 g |
| (FPT-100P-M20) | Code (Reference) | P-LFQFP100-14×14-0.50 |

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.




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Dimensions in mm (inches).
Note: The values in parentheses are reference values

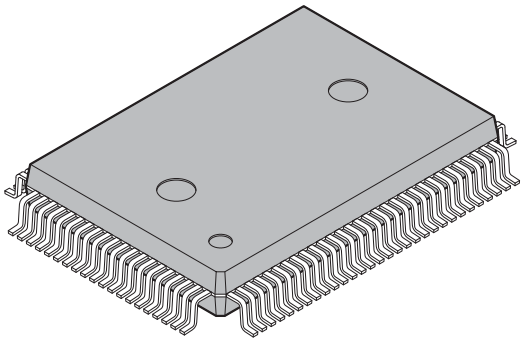
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

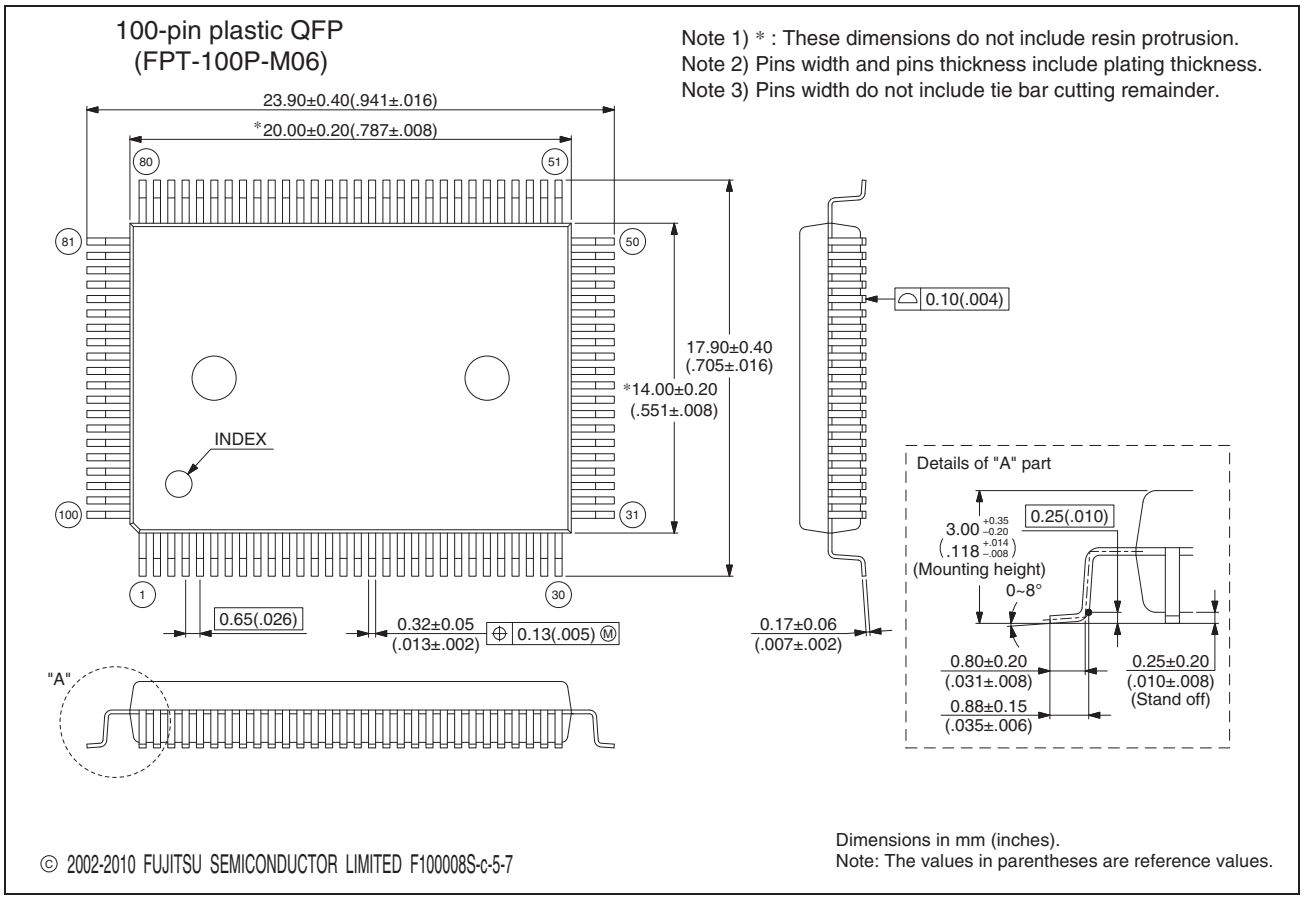
*(Continued)*



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*(Continued)*

| 100-pin plastic QFP | | |
|---|---|---|
|  (FPT-100P-M06) | Lead pitch | 0.65 mm |
| | Package width × package length | 14.00 × 20.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 3.35 mm MAX |
| | Code (Reference) | P-QFP100-14×20-0.65 |
| | | |




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## ■ MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| — | — | Deleted the part numbers;<br>MB90F343E(S), MB90F343CE(S) |
| 51 | ■ ELECTRICAL CHARACTERISTICS<br>1. Absolute Maximum Ratings | Added “*6” in remark for “L" level maximum output current and “H” level maximum output current.<br>Added “*7” in remark for “L" level average output current and “H” level average output current.<br>Added “*8” in remark for “L"level average overall output current and “H” level average overall output current. |
| 52 | | Added as follows.<br>“*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.”<br>“*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.”<br>“*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.” |

The vertical lines marked in the left side of the page show the changes.



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